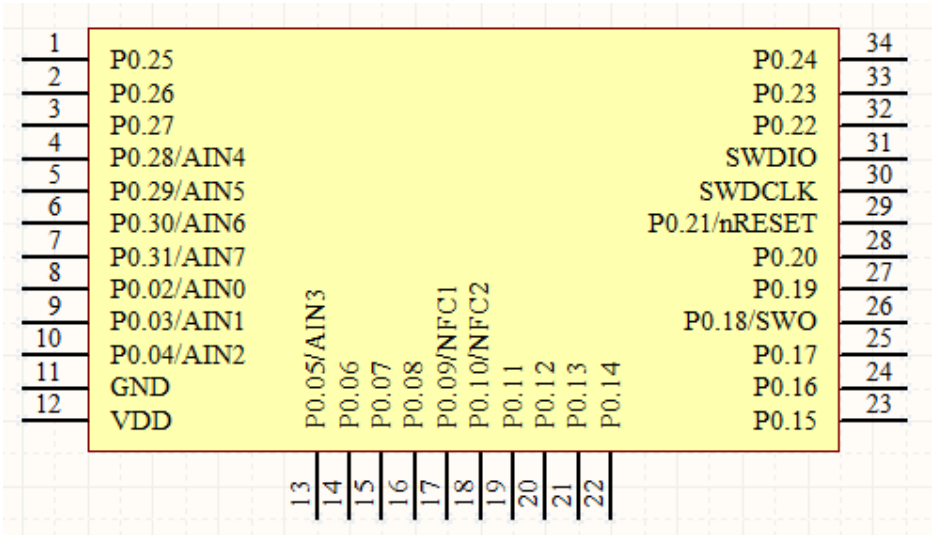
Instruction for BLE Bluetooth module

Product Name: BLUETOOTH MODULE

Model: MLBT001

1, Schematic diagram



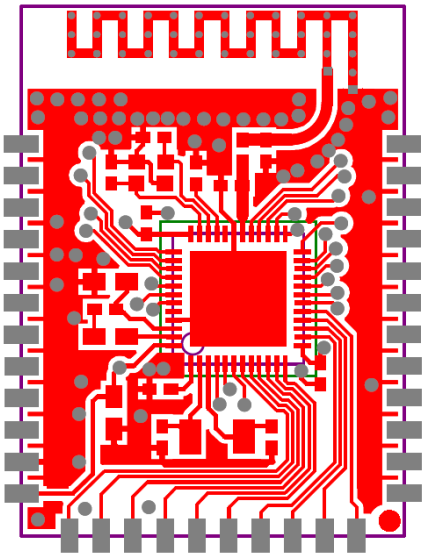
pin assignments

Pin	Name	Type	Description
1	P0.25	Digital I/O	General purpose I/O
2	P0.26	Digital I/O	General purpose I/O
3	P0.27	Digital I/O	General purpose I/O
4	P0.28	Digital I/O	General purpose I/O
	AIN4	Analog input	SAADC/COMP/LPCOMP input
5	P0.29	Digital I/O	General purpose I/O
	AIN5	Analog input	SAADC/COMP/LPCOMP input
6	P0.30	Digital I/O	General purpose I/O
	AIN6	Analog input	SAADC/COMP/LPCOMP input
7	P0.31	Digital I/O	General purpose I/O pin
	AIN7	Analog input	SAADC/COMP/LPCOMP input
8	P0.02	Digital I/O	General purpose I/O
	AIN0	Analog input	SAADC/COMP/LPCOMP input
9	P0.03	Digital I/O	General purpose I/O
	AIN1	Analog input	SAADC/COMP/LPCOMP input
10	P0.04	Digital I/O	General purpose I/O
	AIN2	Analog input	SAADC/COMP/LPCOMP input
11	GND	Power	Ground (Radio supply)
12	VDD	Power	Power supply
13	P0.05	Digital I/O	General purpose I/O
	AIN3	Analog input	SAADC/COMP/LPCOMP input

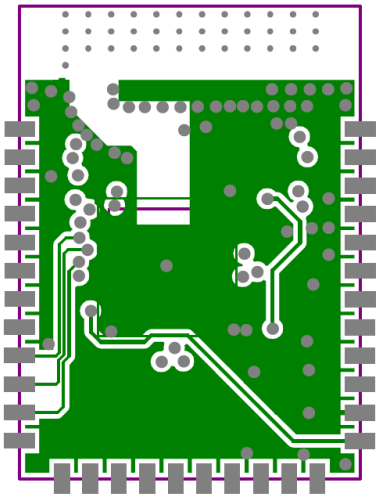
14	P0.06	Digital I/O	General purpose I/O
15	P0.07	Digital I/O	General purpose I/O
16	P0.08	Digital I/O	General purpose I/O
17	NFC1	NFC input	NFC antenna connection
	P0.09	Digital I/O	General purpose I/O
18	NFC2	NFC input	NFC antenna connection
	P0.10	Digital I/O	General purpose I/O
19	P0.11	Digital I/O	General purpose I/O
20	P0.12	Digital I/O	General purpose I/O
21	P0.13	Digital I/O	General purpose I/O
22	P0.14	Digital I/O	General purpose I/O
	TRACEDATA[3]		Trace port output
23	P0.15	Digital I/O	General purpose I/O
	TRACEDATA[2]		Trace port output
24	P0.16	Digital I/O	General purpose I/O
	TRACEDATA[1]		Trace port output
25	P0.17	Digital I/O	General purpose I/O
26	P0.18	Digital I/O	General purpose I/O
	TRACEDATA[0] / SWO		Single wire output Trace port output
27	P0.19	Digital I/O	General purpose I/O
28	P0.20	Digital I/O	General purpose I/O
	TRACECLK		Trace port clock output
29	P0.21	Digital I/O	General purpose I/O
	nRESET		Configurable as pin reset
30	SWDCLK	Digital input	Serial wire debug clock input for debugand programming
31	SWDIO	Digital I/O	Serial wire debug I/O for debug andprogramming
32	P0.22	Digital I/O	General purpose I/O
33	P0.23	Digital I/O	General purpose I/O
34	P0.24	Digital I/O	General purpose I/O

2, PCB diagram

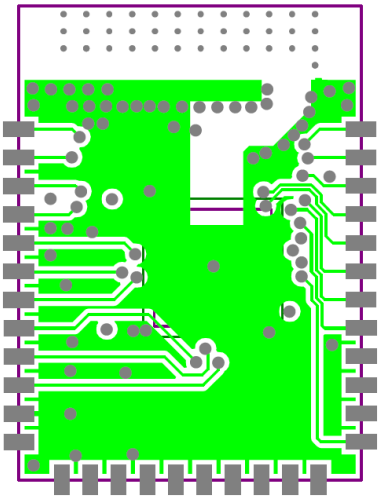
Top layer



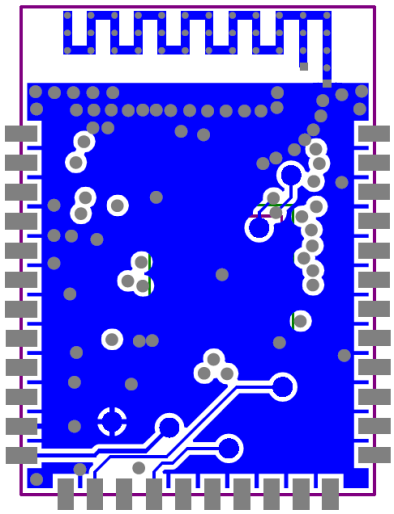
M1 layer



M2 layer



Bottom layer



3, Parameters

Interface means: Stamp half hole

Antenna type: Onboard

Dimension: 25*18*2.8mm

BT version: Version 5.0and above

Frequency：2.402GHz to 2.480GHz

Modulation system: GFSK

Antenna gain: 0dbm

Communication distance: 100m

Welding manner: SMT

Working temperature: -20 – 80℃

Sensitivity under low power consumption: -93 dbm Data transfer rate:250kbps,1MBPS, 2MBPS

Transmitting power under power saving mode:-30dbm Peak current: When receiving:13

When transmitting: 10.5ma

RSSI(DPI 1DB) : When receiving

ARM CORTEX-M0

Serial Wire Debug

Supports non-parallel multi-protocol operations

Be compatible with NRF24L

Storage

Inside flash: 256kb/128kb

16kb ram

Flexible power management

Working voltage: 1.8-3.6v

Using 16MHZ RC: 2.5us wake-up

Turn off mode: 0.4ua@3v

Turn off and keep one storage area RAM: 0.5ua@3v

Running mode & all modules are free: 2.3ua@3v

8/9/10 bit adc – with 8 Configurable channels

31 GPIO

One 32 bit and two 16 bit timers with counting mode.

SPI CO

2-line cardinal extremity (compatible with I2C)

UART (CTS/RTS)

PPI

QDEC

Hardware encryption

RTC

4、Instruction

GPIO:

Access and control for all I/O on one port.

- Input/output direction
- Output drive strength
- Internal pull and pull-down resistance
- High or low level trigger arousal
- Raise interrupt
- All pins can be used by PPI's task/event system； The maximum number of pins that can be connected via PPI is determined by GPIOTE.
- It can be configured as a serial interface or an orthogonal demodulation signal port.

Hardware reset：

Users can use external reset, and GPIO P0.21 pins can be used as external hardware reset pins. To make P0.21 as an external reset pin. The UICR register PSELRESET[0] and PSELRESET[1] must be set to the same value, which is 0x7FFFFF1. When P0.21 is set to reset pins, it will automatically enable internal pull-up.

Module HW debugging and online programming interface:

This module supports two line serial debugging (SWD) interface. It provides a flexible and powerful non-intrusive code modulation mechanism that supports breakpoints, single-step execution, and code command tracking.

Pin	Online programming interface
SWDIO	Serial debugging programming port data.
SWDCLK	Serial debugging programming mouth clock.

J-Link Lite product fully supports the debugging and online programming of this module. For more details, please check at www.segger.com.

End Product Labeling

This transmitter module is authorized only for use in devices.

The final end product must be labeled in a visible area with the following: "Contains FCC ID: 2AOA9MLBT001"

Restrictions：

■Modules are not designed for life support applications. If use or sell in this field, customers need to agree and bear the risk themselves.

■Do not responsible for user's product or App.

■We have carefully checked this manual, but there is no guarantee that the manual is completely free of errors and omissions.

FCC CAUTION:

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) this device may not cause harmful interference, and

(2) this device must accept any interference received, including interference that may cause undesired operation.

Note:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

Reorient or relocate the receiving antenna.

Increase the separation between the equipment and receiver.

Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

Consult the dealer or an experienced radio/TV technician for help.

Please take attention that changes or modification not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. FCC RF EXPOSURE STATEMENT:

The device has been evaluated to meet general RF exposure requirement, The device can be used in portable exposure conduction without restriction.

Electrostatic sensitive device.

Pay attention to the protection measures


ATTENTION
OBSERVE PRECAUTION FOR HANDLING
ELECTROSTATIC SENSITIVE DEVICE
HBM (Human Body Model): Class 2