nRF9160 Hardware Design Guidelines

nWP-037

White Paper

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NORDIC® SEMICONDUCTOR

Contents

Revision history

Date	Description
2022-09-27	• Added External flash memory requirements on page 28 • Editorial changes
September 2020	First release

1 Introduction

This document provides guidelines for the hardware design and integration of nRF9160. These guidelines will help to ensure the best electrical, mechanical, and thermal performance of nRF9160. The guidelines are intended for Nordic Semiconductor's customers, especially system integrators and hardware engineers.

2 Related documentation

In addition to the information in this document, you may need to consult other documents.

Information related to the integration of nRF9160 is provided in the following documents:

- nRF9160 Product Specification
- nWP033 - nRF9160 Antenna and RF Interface Guidelines
- nWP034 - nRF9160 Hardware Verification Guidelines
- nRF91 AT Commands Reference Guide

3 Design overview

This section provides an overview of the operating conditions of nRF9160 and a pinout with a description of each pin. Recommended baseline schematics are also provided illustrating a good starting point for the integration of nRF9160.

3.1 Operating conditions

This section describes the operating conditions that impact the performance and behavior of nRF9160.

3.1.1 Temperature range

The optimal operating case temperature (Tc) of nRF9160 ranges from –30°C to 65°C, achieving the best RF performance including output power transmission and receiver sensitivity.

nRF9160 remains 3GPP compliant in case temperatures that range from –40°C to 85°C. Case temperature is typically the main cause for degradation in RF performance and current consumption, but other factors, such as supply voltage and signaling parameters, may contribute to it as well.

Case temperature is affected by the ambient temperature combined with nRF9160's internal thermal dissipation originating from the LTE modem and application processor's activity.

3.1.1.1 Thermal protection

nRF9160 has a built-in thermal protection mechanism to prevent RF *Power Amplifier (PA)* from breaking and the LTE modem from operating beyond the specified temperature range.

When the internal temperature sensor in nRF9160 measures a case temperature of approximately 90°C, the LTE modem and *Global Positioning System (GPS)* receiver are deactivated to minimize the internal generation of heat and to protect RF PA. When the sensor measures a temperature that is lower than approximately 90°C, the LTE modem is reactivated. Using the application processor is not limited by the thermal protection mechanism.

For more information on thermal protection, see Internal temperature %XTEMP in nRF91 AT Commands Reference Guide.

3.1.2 Voltage range

The operational voltage of nRF9160 ranges from 3.0 V to 5.5 V. The modem transceiver requires a minimum voltage of 3.3 V to fulfill RF performance in the environmental conditions described in nRF9160 Product Specification.

The RF performance and environmental specification described in nRF9160 Product Specification exceed the equivalent requirements in the 3GPP specification. Therefore, nRF9160 is 3GPP compliant with supply voltage down to 3.1 V.

Note: Minimum voltage includes all voltage drops, ripple, and spikes.

3.1.3 Physical characteristics

The physical dimensions of nRF9160 are 16.0 x 10.5 x 1.0 mm. It has a plastic compound mold and integrated metallization to suppress internal radiated emissions and protect against external radio interference.

3.1.4 Supported cellular bands

A list of certified cellular bands can be found in nRF9160 certifications.

3.2 Pinout

This section describes the physical pin mapping and functions of the pins in nRF9160.

3.2.1 Pin assignments

The nRF9160 pinout has 127 pins.

The pin assignment of nRF9160 is shown in the following figure:

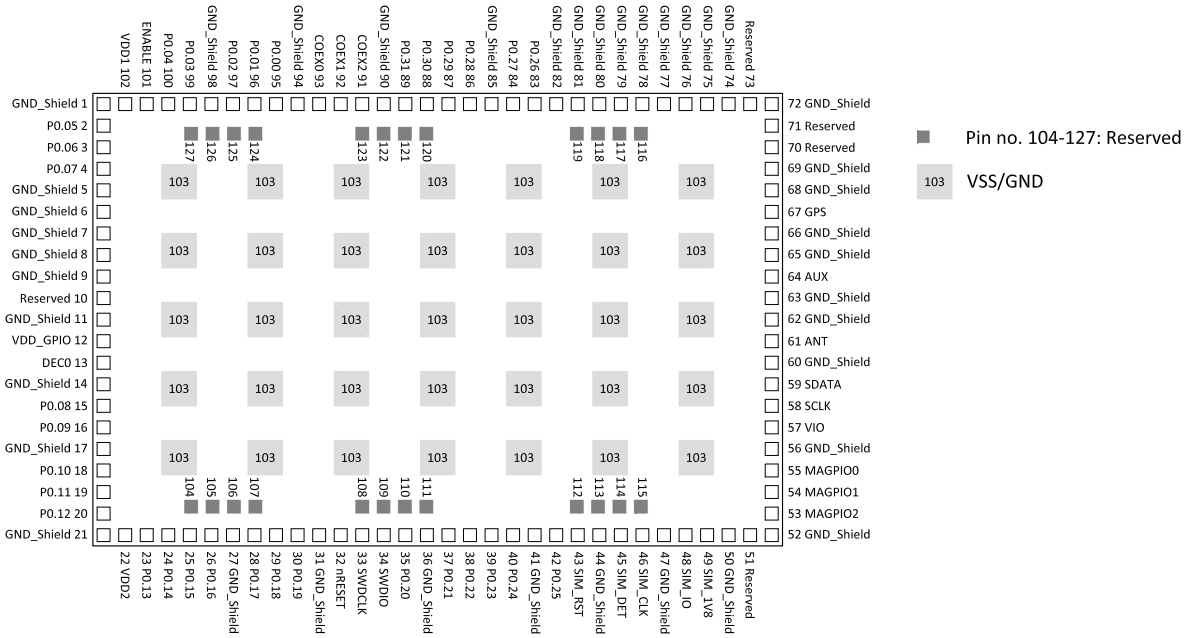

Figure 1: nRF9160 pin assignment

For more information, see nRF9160 Product Specification.

3.2.2 Pin description

Each nRF9160 pin has specified functions and design recommendations. The detailed design recommendations are provided in Hardware integration on page 15.

The following table describes the functions of the nRF9160 pins.

Pin no	Pin name	Function	Description
1	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
2	P0.05	*General-Purpose Input/Output (GPIO)*	Digital I/O, **VDD_GPIO** level.
3	P0.06		
4	P0.07		
5–9	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
10	Reserved		Connect thermally and mechanically to the application board, but leave electrically unconnected.
11	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
12	VDD_GPIO		GPIO power supply input and logic level for GPIOs.
13	DEC0		nRF9160-internal supply capacitor connection.
14	GND_Shield		Microshield ground. Connect to **VSS** (pin 103) and application board ground.
15	P0.08	GPIO	Digital I/O, **VDD_GPIO** level.
16	P0.09		
17	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
18	P0.10	GPIO	Digital I/O, **VDD_GPIO** level.
19	P0.11		
20	P0.12		
21	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
22	VDD2		nRF9160's *PA* PMU supply input. Must be at the same voltage level as **VDD1** (pin 102) supply for the *System on Chip (SoC)*.
23	P0.13	GPIO	Digital I/O and analog input, **VDD_GPIO** level.
24	P0.14		
25	P0.15		
26	P0.16		
27	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
28	P0.17	GPIO	Digital I/O and analog input, **VDD_GPIO** level.
29	P0.18		
30	P0.19		
31	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.

Pin no	Pin name	Function	Description
32	nRESET	System reset	SoC reset.
33	SWDCLK	*Serial Wire Debug (SWD)*	SWD and programming clock input.
34	SWDIO		SWD and programming interface.
35	P0.20	GPIO	Digital I/O and analog input, **VDD_GPIO** level.
36	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
37	P0.21	GPIO	Digital I/O and trace buffer clock, **VDD_GPIO** level.
38	P0.22		Digital I/O, **VDD_GPIO** level.
39	P0.23		
40	P0.24		
41	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
42	P0.25	GPIO	Digital I/O, **VDD_GPIO** level.
43	SIM_RST	*Subscriber Identity Module (SIM)*	SIM reset.
44	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
45	SIM_DET	SIM	SIM detect (currently not a supported feature).
46	SIM_CLK		SIM clock.
47	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
48	SIM_IO	SIM	SIM data.
49	SIM_1V8		SIM card's 1.8 V power supply output.
50	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
51	Reserved	Reserved	Connect thermally and mechanically to the application board but leave electrically unconnected.
52	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
53	MAGPIO2	GPIO	Digital I/O. Controllable by application processor and LTE modem, fixed 1.8 V.
54	MAGPIO1		
55	MAGPIO0		
56	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
57	VIO	RFFE ctrl	Digital I/O. *MIPI RF Front-End Control Interface (RFFE)* VIO compatible, fixed 1.8 V.
58	SCLK		Digital I/O. RFFE CLK compatible, fixed 1.8 V.

Pin no	Pin name	Function	Description
59	SDATA		Digital I/O. RFFE DATA compatible, fixed 1.8 V.
60	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
61	ANT	RF	Cellular antenna port, 50 Ω.
62	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
63	GND_Shield		
64	AUX	RF	Loopback port for cellular antenna. A matching network external to the module is recommended.
65	GND_Shield	Power	Microshield ground, connect to **VSS** (pin 103) and application board ground.
66	GND_Shield		
67	GPS	RF	*GPS* receiver antenna port, 50 Ω.
68	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
69	GND_Shield		
70	Reserved	Reserved	Connect thermally and mechanically to the application board but leave electrically unconnected.
71	Reserved		
72	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
73	Reserved	Reserved	Connect thermally or mechanically to the application board but leave electrically unconnected.
74–82	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
83	P0.26	GPIO	Digital I/O, **VDD_GPIO** level.
84	P0.27		
85	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
86	P0.28	GPIO	Digital I/O, **VDD_GPIO** level.
87	P0.29		
88	P0.30		
89	P0.31		
90	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
91	COEX2	GPIO	Controlled by modem.
92	COEX1		
93	COEX0		
94	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.

Pin no	Pin name	Function	Description
95	P0.00	GPIO	Digital I/O, **VDD_GPIO** level.
96	P0.01		
97	P0.02		
98	GND_Shield	Power	Microshield ground. Connect to **VSS** (pin 103) and application board ground.
99	P0.03	GPIO	Digital I/O, **VDD_GPIO** level.
100	P0.04		Digital I/O, **VDD_GPIO** level.
101	ENABLE	Control	< 0.4 V disable, > 0.8 x **VDD1** enable.
102	VDD1	Power	nRF9160 SoC PMU supply input. Must be at the same voltage level as **VDD2**'s (pin 22) supply for PA.
103	VSS		nRF9160 ground plane. Ensure the connection to the application board ground is solid for good electrical, thermal, and mechanical robustness performance.
104–127	Reserved	Reserved	Connect thermally and mechanically to the application board but leave electrically unconnected.

Table 1: Pin assignments

3.3 Schematic design

The schematic design should start from the most important nRF9160 interfaces which are the supplies and radio frequency interfaces. The *SIM* and control interfaces should also be prioritized, as they may require special application components, for example, for *Electrostatic Discharge (ESD)* protection.

The following figure shows recommendations that can be used as the basis of the application's schematic design.

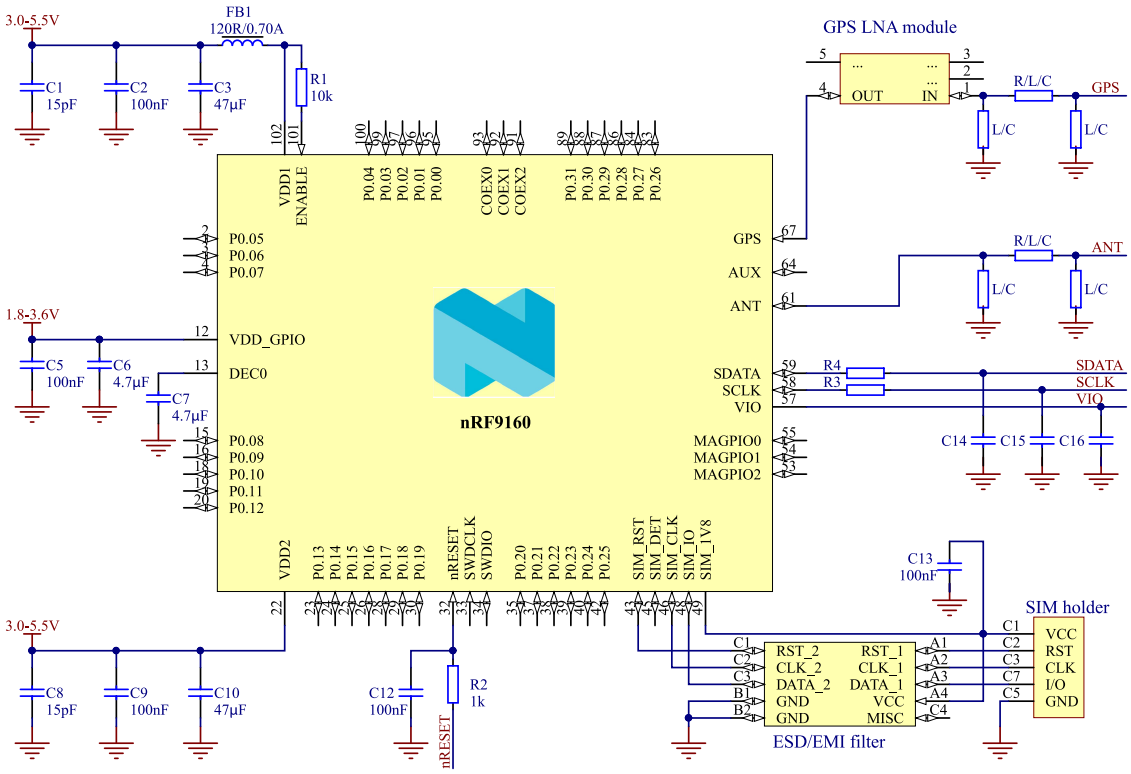

Figure 2: nRF9160 application design recommendations

The following table provides information on recommended components:

Reference	Description	Quality	Example part number
C1	CAP, 15 pF, 25 V, C0G, 0201	X5R, 10 V or better	GJM0335C1E150JB01
C2	CAP, 100 nF, 10 V, X5R, 0201		GRM033R61A104KE15
C3	CAP, 47 uF, 10 V, X5R, 0805		GRM21BR61A476ME15
C5	CAP, 100 nF, 10 V, X5R, 0201		GRM033R61A104KE15
C6	CAP, 4.7uF, 10V, X5R, 0402		GRM155R61A475MEAA
C7			
C8	CAP, 15 pF, 25V, C0G, 0201		GJM0335C1E150JB01
C9	CAP, 100 nF, 10 V, X5R, 0201		GRM033R61A104KE15
C10	CAP, 47 uF, 10 V, X5R, 0805		GRM21BR61A476ME15
C12	CAP, 100 nF, 10 V, X5R, 0201		GRM033R61A104KE15
C13			
C14[1]	Optional. Not recommended to be assembled by default.		GJM0335C1E100JB01
C15[1]			
C16[2]			GRM033R61A104KE15
R/L/C	Antenna matching	High-Q components, for example, Murata LQW15AN series inductors and GJM1555C1 series capacitors	
L/C			
R1	10 kΩ resistor	NA	RC0201FR-0710KL
R2	Resistor in the range of 1 kΩ		RC0201FR-071KL
R3			
R4			

Table 2: nRF9160 application component recommendations

[1]CAP, ≤10 pF, 5%, 25 V, C0G, 0201

[2]CAP, 100 nF, 10 V, X5R, 0201

For recommended matching component values and topology, see the datasheets of the LTE and *GPS* antennas. For more information on the antenna design and interface, see nWP033 - nRF9160 Antenna and RF Interface Guidelines.

4 Hardware integration

This section provides design recommendations and layout guidelines for each nRF9160 pin for a successful integration of nRF9160.

4.1 VSS

VSS (pin 103) is the main electrical ground connection between nRF9160 and the application board. It is also the main thermal dissipation path from nRF9160 and the main mechanical connection.

The connection between **VSS** and the application board must be electrically, thermally, and mechanically strong. It is recommended that the application board *Printed Circuit Board (PCB)*'s ground planes around nRF9160 are as intact and as solid as possible. Use as many ground vias as possible between the top metal layer of the application board and the inner ground layers connected to nRF9160's **VSS** pins. Typically, metal filled vias provide the best thermal conductivity.

4.2 GND_Shield

The following ground pins are dedicated for the embedded microshield: 1, 5–9, 11, 14, 17, 21, 27, 31, 36, 41, 44, 47, 50, 52, 56, 60, 62, 63, 65, 66, 68, 69, 72, 74–82, 85, 90, 94, and 98.

Connect **GND_Shield** electrically strongly to **VSS** (pin 103) and on the application board to the same ground planes as **VSS**.

4.3 ENABLE

ENABLE (pin 101) is a high-impedance control pin for the nRF9160-internal PMU.

It is used to enable and disable nRF9160. Logic high (> 0.8 x VDD1) enables nRF9160. The start delay is in the range of a few milliseconds from pulling the **ENABLE** pin high. Logic low (< 0.4 V) disables nRF9160 and brings it into extremely low current consumption.

In products where nRF9160 is always enabled, the **ENABLE** pin can be connected to **VDD1** (pin 102) on the application board with a series resistor. The series resistor minimizes digital noise coupling between the **VDD1** and **ENABLE** pins. It is recommended to add a decoupling capacitor to the **ENABLE** pin. If **ENABLE** is connected to **VDD1**, a shared capacitor can be used for the **ENABLE** and **VDD1** pins if the **VDD1** decoupling capacitor is located close to the **VDD1** and **ENABLE** pins.

4.3.1 PCB layout design

When designing the *PCB* layout, pin-specific recommendations should be followed.

The **ENABLE** pin has the following recommendations:

- Place **R1** close to the **ENABLE** pin.
- If **ENABLE** is directly connected to **VDD1**, it can use a shared decoupling capacitor with **VDD1** if **VDD1**'s decoupling capacitors and **ENABLE** are located close to each other.
- If **ENABLE** is not directly connected to **VDD1**, a dedicated decoupling capacitor is recommended to be added to the **ENABLE** pin.
- Because **ENABLE** can carry noise from internal and external regulators and the power source, it is not recommended to be routed parallel to sensitive routings, such as RF.

- Avoid routing the Enable signal unshielded on the top and bottom metal layers of the PCB. This risks radiated noise that can deteriorate radiated *GPS* and LTE sensitivity.

4.4 VDD1 and VDD2

Power supply design is one of the main factors in achieving good RF performance, low current consumption, and reliable behavior of a product over its life time in various conditions. **VDD1** (pin 102) and **VDD2** (pin 22) are the main power supply inputs for nRF9160 and form the combined VDD.

VDD1 is connected to the DC converter input of the nRF9160-internal PMU that supplies the *SoC*. **VDD2** is connected to the DC converter input of the nRF9160-internal PMU that supplies the RF *PA*. The operational voltage of **VDD1** and **VDD2** ranges from 3.0 V to 5.5 V. To comply with the RF performance specifications in Electrical specification in nRF9160 Product Specification, the inbuilt LTE modem transceiver is not recommended to be used below 3.3 V, even though nRF9160 can operate down to 3.0 V.

To ensure the operation described in nRF9160 Product Specification, prevent voltage drops, ripple, and spurious below 3.3 V in VDD. Voltage drop is most likely to occur during LTE transmit. This is due to peaks of up to 500 mA/3.3 V happening during **VDD2** current consumption. VDD must not drop below 3.0 V during any nRF9160 operation. To minimize supply voltage ripple and suppress EMI coupling to/from nRF9160, it is recommended to place low ESR capacitors close to the **VDD1** and **VDD2** pins. Supply capacitors of low ESR (<0.1 Ω) are recommended.

To improve power delivery, voltage ripple, and EMI performance, it is recommended to have at least one low ESR supply capacitor **C3** in **VDD1** and **C10** in **VDD2**. Placing ferrite bead FB1 at VDD1 is highly recommended. To further improve filtering for high-frequency components, you can optionally add **C2** and **C1** to **VDD1** or **C9** and **C8** to **VDD2**. The electrical values for **C2** and **C9** may vary depending on the application, but for **C1**, the recommended range is from 1 nF to 470 nF, and for **C8**, it is from 10 pF to 100 pF.

For **VDD_GPIO**, the minimum recommendation is low ESR supply capacitor **C6**. Filtering for high-frequency components can be improved by adding **C5** in the range of 1 nF to 470 nF.

To improve the supply network's EMI performance, a series three terminal filter capacitor can be added close to the battery. For example, Murata NFM15PC can be used. The filter capacitor attenuates unwanted noise generated at wide frequency range approximately from 10 MHz to 3 GHz.

Note: **VDD1** and **VDD2** must be connected to the same supply voltage.

4.4.1 PCB layout design

When designing the *PCB* layout, pin-specific recommendations should be followed.

The **VDD1** and **VDD2** pins have the following recommendations:

- Place low DCR (<0.1 Ω) ferrite bead **FB1** closest to the **VDD1** pin to suppress noise from nRF9160.
- Place capacitors **C4** (**C11**) and **C3** (**C10**) close to the VDD pins for improved power delivery.
- Place capacitors **C1** (**C8**) and **C2** (**C9**) close to the VDD pins to filter high-frequency signal components, especially if the product integrates an internal LTE or *GPS* antenna.
- Connect capacitors to the same ground plane as nRF9160 (pin 103) using low impedance ground connections.
- Use wide enough tracks (DCR <0.1 Ω) for VDD routing to minimize voltage drops and unwanted power consumption coming from routing losses under high current conditions.
- Avoid supply routings close or adjacent to sensitive routings, such as RF.
- Use shielded PCB layers for routings whenever possible to minimize radiated noise.
- Use plenty of ground vias along supply routings to minimize unwanted voltage differences in the application PCB's metal layers.

- A series solder bridge is recommended in the **VDD** routing for current consumption measurements or other diagnostic purposes.

Note: Short low impedance ground connections are mandatory for all supply capacitors.

4.4.2 VDD current consumption

During operation, nRF9160 current consumption depends significantly on the LTE network, end product's antenna design, temperature, battery voltage, and the intensity of the LTE uplink data transmit. Although the typical current consumption of nRF9160 can be very low, the power supply and system must be designed to meet the demands of the potential worst-case level of current consumption.

The worst-case level of current consumption depends, among other things, on the following:

- The temperature range for which the end product is certified.
- The cut-off voltage of the end product's power supply.
- The antenna impedance mismatch behavior when the end product is placed on a metal surface or covered by the user's hand.

The current consumption figures related to hardware design are given in Modem current consumption in nRF9160 Product Specification:

- Radio resource control (RRC) current consumption figures equal to average current consumption over radio frame (10 ms) with up and downlink data transmission in nominal operating conditions.
- Peak current consumption figures in nominal operating conditions equal to average current consumption during uplink transmission in nominal operating conditions.
- Peak current consumption figures in extreme operating conditions equal to average current consumption during uplink transmission in extreme operating conditions. This means Tc >65°C and antenna mismatch of VSWR3:1. In the design of the end product's supply, this is the most stringent target to comply with.

4.4.3 LTE-M and LTE-NB

HD-FDD LTE-M and HD-FDD LTE-NB have different uplink ratios over radio frame and maximum continuous uplink durations. Both systems are based on a 10 ms radio frame consisting of 10 subframes (SF), 1 ms each.

In normal network signaling conditions without uplink repetitions, the number of continuous uplink and downlink subframes may differ noticeably between the systems. In HD-FDD LTE-M, the maximum uplink ratio can be 3 SF/10 SF (33%), whereas in HD-FDD LTE-NB it can be 8 SF/10 SF (80%). This means that in HD-FDD LTE-NB, the uplink can be transmitting approximately three times longer per radio frame than in HD-FDD LTE-M.

However, with uplink repetitions, both systems share the same uplink ratio of 86%. Power consumption at high output power levels for HD-FDD LTE-M is approximately 15% higher than HD-FF LTE-NB. Power supply design requirements are the most rigid for LTE-M.

Note: The end product's power supply and thermal design must comply with the worst-case consumption level. This prevents nRF9160 from occasionally resetting which generates extra current consumption. It also helps reduce overhead in the LTE network connection. Too much overhead could cause the network operator to block the end product from the network.

4.5 VDD_GPIO

VDD_GPIO (pin 12) is the supply for application *GPIO*s P0.00–P0.31 and the COEX interface (pins 91–93) that is provided externally.

The operating voltage of **VDD_GPIO** ranges from 1.8 to 3.6 V and is independent of the **VDD** supply. The GPIOs have software-configurable drive modes. In standard drive mode, pin sink and source currents are approximately 0.5 mA. In high drive mode, pin currents are 3 to 5 mA. The standard drive mode is operational over the voltage range of 1.8 to 3.6 V. High drive mode is operational over the voltage range of 1.8 to 3.6 V, but 5 mA drive current requires **VDD_GPIO** voltage of ≥ 2.7 V.

Standard drive is recommended because lower current results in better EMI performance and interoperability with other application board peripherals. With standard drive, the end product's performance regarding items, such as LTE radiated spurious emissions and LTE receiver radiated sensitivity, is typically somewhat better than with high drive.

Unlike the current consumption of VDD, **VDD_GPIO**'s current consumption is mostly controlled by the end product design. This is because **VDD_GPIO** supplies the application GPIOs which are controlled by the application software provided by the integrator. If the GPIOs are not significantly stressed in the device, **VDD_GPIO** can have a simple power supply strategy. However, if the end product has high momentary current draw from the GPIOs, **VDD_GPIO**'s capability must be designed to comply with it. In the worst case, the momentary concurrent current consumption of all GPIOs should not peak higher than approximately 100 mA. Regardless of the **VDD_GPIO**'s supply capability, it is not recommended to have long periods of high concurrent consumption because it increases the risk of reducing the device's lifetime.

Recommended **VDD_GPIO** decoupling capacitors are shown in Table 2: nRF9160 application component recommendations on page 14.

The following restrictions apply to the **VDD_GPIO** pin:

- **VDD_GPIO** should be applied after **VDD** has been supplied.
- **VDD_GPIO** should be removed before removing **VDD**.
- If **VDD** is supplied and **VDD_GPIO** is grounded, extra current consumption can be generated on **VDD**.
- If the **ENABLE** pin is low, **VDD_GPIO** should also be low.

4.5.1 PCB layout design

When designing the *PCB* layout, pin-specific recommendations should be followed.

The **VDD_GPIO** pin has the following recommendations:

- Place capacitors **C5** and **C6** close to the **VDD_GPIO** pin for good power delivery.
- Use a track that is wide enough (DCR <0.1 Ω) for **VDD_GPIO** routing to minimize voltage drops and unwanted power consumption due to routing losses under high current conditions.
- Connect capacitors to the same ground plane as nRF9160 (pin 103) using low impedance ground connections.
- Avoid supply routings close or adjacent to sensitive routings, such as RF.
- Use shielded PCB layers for routings whenever possible to minimize radiated noise.
- Use plenty of ground vias along supply routings to minimize unwanted voltage differences in the application PCB's metal layers.
- A series solder bridge is recommended in the **VDD** routing for current consumption measurements or other diagnostic purposes.

4.6 GPIOs P0.00–P0.31

The application *GPIO* pins (2–4, 15, 16, 18–20, 23–26, 28–30, 35, 37–40, 42, 83, 84, 86–89, 95–97, 99, and 100) are used for interfacing and communicating with application peripherals like sensors, *Integrated Circuit (IC)*s, external memories, buttons, and LEDs.

GPIOs are powered from **VDD_GPIO**. They have the same voltage level as **VDD_GPIO** and any unwanted noise or spurious that **VDD_GPIO** may contain. Therefore, it is important to have proper noise filtering in

VDD_GPIO (pin 12). It is also important for each individual GPIO pin to meet the filtering requirements specified for the peripherals connected to them. To avoid digital noise generated by the GPIOs, fast transients should be avoided. It is recommended to use the slowest possible rise times that the peripherals connected to the GPIOs allow.

To reduce transient currents, series resistors or ferrite beads can be used on the GPIO lines. For GPIOs, resistors in the range of 100 Ω to 1 kΩ can be considered as they are low current digital controls. Optimal resistor values depend mainly on the connected peripheral drive currents and communication speed or other application-level requirements. In addition to the series resistor, bypass capacitors in the range of a few pF can be considered. They may help to reduce RF coupling to the GPIO lines. Unused GPIOs can be left electrically unconnected, but it is recommended to solder them to the application board for improved thermal and mechanical performance.

Note: Additional capacitance increases GPIO loading and noise originated from GPIO toggling.

Note: It is not recommended to use high voltage, high drive GPIO outputs with high frequency and high capacitance loads unless specifically needed, because it may increase the noise level and affect the performance of the *GPS* and LTE radio receivers.

4.6.1 Features

The *GPIO*s have user-configurable features.

The features are provided in the following list:

- Configurable output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high- or low-level triggers on all pins
- Trigger interrupt on state changes on any pin
- All pins can be used by the *Programmable Peripheral Interconnect (PPI)* task/event system
- One or more GPIO output can be controlled through PPI and *GPIOTE* channels
- All pins can be individually mapped to interface blocks for layout's flexibility
- GPIO state changes captured on SENSE signal can be stored by LATCH register
- Support for secure and non-secure attributes for pins in conjunction with the system protection unit

For more information on GPIO feature support, see GPIO - General purpose input/output in nRF9160 Product Specification.

4.6.2 PCB layout design

When designing the *PCB* layout, pin-specific recommendations should be followed.

The *GPIO* pins have the following recommendations:

- Place filtering series resistors close to the respective GPIO pins.
- Place capacitors close to the origin of noise and ground them to same ground plane as **VSS** on nRF9160.
- Avoid parallel routing of GPIOs close to sensitive RF routings due to the risk of noise decoupling from GPIO to RF routing.
- Avoid parallel routings of GPIOs close to supply or RF routings due to the risk of noise decoupling from other routings to the GPIO routings.
- Use shielded PCB layers for GPIO routings whenever possible to minimize radiated noise.
- Follow the instructions in the peripheral datasheets.

4.7 DEC0

DEC0 (pin 13) is an nRF9160-internal power management unit (PMU) output pin for an external decoupling capacitor.

An external capacitor improves the stability of the internal supply. The voltage level of **DEC0** is approximately 2.2 V. The recommended capacitor value is provided in Table 2: nRF9160 application component recommendations on page 14.

In the *PCB* layout, place **C7** close to the **DEC0** pin and connect the ground capacitor to the same ground plane as nRF9160 **VSS** (pin 103).

4.8 nRESET

nRESET (pin 32) is a dedicated *SoC* reset pin. A SoC reset is generated when the **nRESET** pin is pulled low and released. To ensure that the reset is issued correctly, the reset pin should be held low for a few microseconds.

The **nRESET** pin has a 13 kΩ internal pull-up resistor that is always on and connected to the nRF9160 internal voltage of 2.2 V. The **nRESET** pin can be connected to an external controller or mechanical switch that is controlled by the user. It is recommended to add a bypass capacitor and series resistor in the range of 1 kΩ to the **nRESET** routing close to the **nRESET** pin. For more information on pin reset, see Reset in nRF9160 Product Specification.

Note:

- External pull-up is not allowed in the **nRESET** pin.
- External filtering components affect the minimum pulse length.

4.9 SWD

The *SWD* interface provides a non-intrusive mechanism for debugging and tracing nRF9160. It can also be used for programming the firmware and accessing registers.

The SWD interface consists of **SWDCLK** (pin 33) and **SWDIO** (pin 34). The **SWDCLK** pin provides clock signal, and **SWDIO** provides data. The **SWDIO** pin has an internal pull-up resistor whereas the **SWDCLK** pin has an internal pull-down resistor. The SWD interface's logic high level originates from the **DEC0** level, which is approximately 2.2 V. For more information on the SWD interface, see Debug and trace in nRF9160 Product Specification and nWP034 - nRF9160 Hardware Verification Guidelines.

4.10 UICC

The *Universal Integrated Circuit Card (UICC)* interface is also known as the *Universal Subscriber Identity Module (USIM)* or *SIM* interface. It consists of **SIM_RST** (pin 43), **SIM_DET** (pin 45), **SIM_CLK** (pin 46), **SIM_IO** (pin 48), and **SIM_1V8** (pin 49).

nRF9160 supports UICC Class C interface with 1.8 V nominal voltage as described in *ETSI TS102 221*. If needed, support for higher supply voltage classes must be built with external components, including an external power supply and level shifters towards the UICC interface of the LTE modem.

The LTE modem controls the following physical interfaces towards the UICC and implements the transport protocol over the ISO/IEC 7816-3 interface:

- **SIM_1V8** (power supply): Output from LTE modem
- **SIM_CLK** (clock signal): Output from LTE modem
- **SIM_RST** (reset signal): Output from LTE modem
- **SIM_I/O** (input/output serial data): Bi-directional
- **SIM_DET** (reserved for card detection, not in use)

4.10.1 Features

If the device has a user-accessible slot for a *UICC* card, *ESD* sensitivity should be considered. The nRF9160-internal ESD protection is intended for a 1.5 kV *Human Body Model (HBM)* level. External ESD/EMI filtering is recommended between the UICC card slot and nRF9160.

Several ESD/EMI filtering options are available. A commonly used option is a dedicated integrated component, such as STM EMIF03-SIM02M8, TI TPD3F303, or OnSemi CM1402. Typically, an integrated ESD filter consists of lowpass filters and ESD diodes in a small SMD package. Another option is discrete ESD protection which takes more space on the *PCB*, but can be more flexible for certain applications and a lower-cost solution.

Discrete ESD protection can consist of the following components:

- Bypass capacitors in the range of ≤ 22 pF to **SIM_RST**, **SIM_DET**, **SIM_CLK**, **SIM_IO**, and **SIM_1V8**.
  - A separate supply capacitor ranging from 100 nF to 220 nF connected to **SIM_1V8** can be considered.
- Low capacitance type ESD diodes to **SIM_RST**, **SIM_DET**, **SIM_CLK**, **SIM_IO**, and **SIM_1V8**.
  - Multichannel ESD diodes are commonly used and recommended.
  - Some multichannel diode components incorporate EMI filtering. This type is recommended if the product integrates an LTE antenna, or an external antenna is located close to the *SIM* holder.

The electrical specifications for all UICC signals that should be verified in product design and in the prototyping phase are defined in *ETSI TS 102 221*, chapter Electrical specifications of the UICC. For more information, see nWP034 - nRF9160 Hardware Verification Guidelines.

4.10.2 PCB layout design

When designing the *PCB* layout, interface-specific recommendations should be followed.

The *UICC* interface has the following recommendations:

- If the product integrates a *GPS* or LTE antenna, avoid placing the *SIM* holder close to the antenna due to the risk of digital noise coupling from the SIM application to the antenna.
- Place the UICC application as close to nRF9160 as possible to minimize the routing length. Long routing reduces signal integrity in the UICC interface and increases the risk of radiated noise.
- Use the same application board ground plane for the UICC application and nRF9160's **VSS** to guarantee low impedance ground connection between nRF9160 and the UICC application.
- Avoid routing the UICC interface close or adjacent to sensitive RF routings, such as GPS or ANT.
- Place the *ESD* and EMI components or discrete components as close as possible to the UICC application's pins **SIM_RST**, **SIM_CLK**, **SIM_IO**, and **SIM_1V8** to optimize their performance.
- Consider test points in **SIM_RST**, **SIM_CLK**, and **SIM_IO** for debugging purposes.

4.11 MAGPIO

The MAGPIO interface consists of digital 1.8 V I/O pins 53–55 that can be controlled by the LTE modem and nRF9160 application processor.

When controlled by the LTE modem, MAGPIO timing is aligned with the LTE protocol, which enables LTE protocol synchronous control for nRF9160-external components, such as the antenna tuner. For more information, see LTE modem RF control external interface in nRF9160 Product Specification.

4.12 MIPI RF front-end

MIPI RFFE is a dedicated RF front-end component control interface.

It consists of **VIO** (pin 57), **SCLK** (pin 58), and **SDATA** (pin 59). **VIO** is a 1.8 V supply for the MIPI controller, **SCLK** is the clock for the controller, and **SDATA** is for the control data. The RFFE interface is aligned with the LTE protocol, which enables LTE protocol synchronous control for nRF9160-external components, such as an antenna tuner.

nRF9160 supports RFFE v1.1 with the following exceptions:

- **SCLK** is fixed rate 19.2 MHz.
- Only one RFFE component is supported at a time.
- The **VIO** voltage may be high at any time when nRF9160 is active, not only when external RFFE components are used.
- The capacitive load of **SCLK** and **SDATA** must not exceed 15 pF on the application board.

For noise filtering and diagnostic purposes, it is recommended to add series resistors to **SCLK** (**R3**) and **SDATA** (**R4**). In addition to the series resistor, bypass capacitors (**C14**, **C15**, and **C16**) in the range of few pF can be considered. They may help to reduce RF coupling to the RFFE lines. Additional capacitance increases the RFFE load and potentially deteriorates signal integrity. By default, it is not recommended to assemble capacitors **C14**, **C15**, and **C16**.

Note: **VIO** should be assumed to be high when the LTE modem is active. Therefore, an external RFFE component should not have excessive current leakage at **VIO** in any conditions. Typically, **VIO** consumption or leakage in RFFE components is very low, but it is recommended to be verified from the component datasheet. External RFFE components must withstand a situation where **VIO** is high, but **VDD** low. Typically, this is acceptable, but some RFFE components may be more sensitive than others.

CAUTION: The combined load of *PCB* routing, input load of the RFFE component controller, and parasitic load from the application shall not exceed 15 pF at nRF9160's **SCLK** or **SDATA** pins. Typically, this load equals narrow transmission line length of ≤ 10 cm on the application board, but depends on the actual PCB design.

4.12.1 PCB layout design

When designing the *PCB* layout, interface-specific recommendations should be followed.

The *MIPI RFFE* interface has the following recommendations:

- Parasitic capacitance in routing must not exceed 15 pF at **SCLK** or **SDATA**.
- If additional filtering is needed, place capacitors **C14**, **C15**, and **C16** close to the component RFFE is connected to where the noise originates from, for example, the antenna tuner.
- Avoid adjacent routings of **SCLK** and **SDATA** to noisy routings, such as RF or supply.
- Use shielded PCB layers for RFFE routings whenever possible to minimize radiated coupling.
- Follow the instructions of the RFFE peripheral datasheets.

4.13 ANT

ANT (pin 61) is a 50 Ω single-end interface for the LTE antenna for cellular bands. To ensure good performance, antenna impedance and the characteristic impedance of the transmission line connecting the antenna to the **ANT** pin must be 50 Ω. Impedance mismatch leads to performance deterioration.

The length of the transmission line from the antenna to the **ANT** pin should be kept as short as possible to minimize loss, because loss deteriorates the transmitted and received power in nRF9160 and leads to drawbacks in power consumption and network coverage. A maximum of 0.5 dB loss in the transmission line is acceptable.

nRF9160 includes an *ESD* circuit on the **ANT** pin. The ESD circuit is intended for 1.5 kV *HBM* level, but additional ESD protection is recommended, especially if there are active components, such as switches or antenna tuners, in the antenna path. For the ESD requirements, see the component datasheets.

The **ANT** pin is *DC* grounded. A matching network of a minimum of three components is typically needed close to the antenna. The component values and matching topology depend on the antenna application and antenna path impedance and need to be optimized individually for each design. For more information on the antenna interface, see nWP033 - nRF9160 Antenna and RF Interface Guidelines.

4.13.1 PCB layout design

When designing the *PCB* layout, pin-specific recommendations should be followed.

The **ANT** pin has the following recommendations:

- To ensure good, radiated performance, begin the design by locating the LTE antenna on the PCB.
- Ensure preliminary antenna performance on a chosen PCB location, for example, by simulation.
- When multiple antennas, for example, LTE, *GPS*, and *Bluetooth*® Low Energy are present, minimize antenna crosstalk.
- Antenna transmission line impedance should be 50 Ω. Take this into account when selecting the PCB stack-up.
- Avoid excessive capacitance in routing by opening ground layers under component pads. For example, if the routing is on the top PCB layer, open the ground plane under the **ANT** pad on the next metal layer.
- When opening ground planes, avoid exposing noisy routings under the **ANT** pad.
- Avoid long routing because it causes excessive insertion loss which deteriorates RF performance which cannot be reversed.
- Ensure continuous reference ground plane above, below, or both of the **ANT** routing.
- Consider adding a test connector to the antenna path for production test and diagnostic purposes. Ensure that the test connector or solution does not deteriorate the impedance of the transmission line.

4.14 AUX

AUX (pin 64) is a 50 Ω single-end auxiliary port that can be used to loop back the signal that is fed into the **ANT** pin. **AUX** can be used when two radios share an antenna. For example, when using a combined *GPS* and LTE antenna, an internal RF switch in nRF9160 provides the needed isolation between the GPS and LTE paths.

AUX can be configured in software so that when the GPS receiver is on, **AUX** is connected to the **ANT** inside the *System in Package (SiP)*. This enables the routing of the GPS signal from the shared LTE and GPS antenna to **AUX** and through a recommended external *Low-Noise Amplifier (LNA)* to the GPS input. To minimize mismatch losses, using external matching components between **AUX** and LNA is recommended. For more information on the antenna interface, see nWP033 - nRF9160 Antenna and RF Interface

Guidelines. For more information on configuring the **AUX** firmware, see nRF91 AT Commands Reference Guide.

4.14.1 PCB layout design

When designing the *PCB* layout, pin-specific recommendations should be followed.

The **AUX** pin has the following recommendations:

- Antenna transmission line impedance should be 50 Ω. Take this into account when selecting the PCB stack-up.
- Avoid excessive capacitance in routing by opening ground layers under component pads. For example, if the routing is on the top PCB layer, open the ground plane under the **AUX** pad on the next metal layer.
- When opening ground planes, avoid exposing noisy routings under the **AUX** pad.
- Avoid long routing because it causes excessive insertion loss which deteriorates RF performance which cannot be reversed.
- Ensure continuous reference ground plane above, below, or both of the **AUX** routing.

4.15 GPS

GPS (pin 67) is a 50 Ω single-end interface for the *GPS* antenna.

To ensure good GPS reception performance, antenna impedance and the characteristic impedance of the transmission line connecting the antenna to the **GPS** pin must be 50 Ω. Impedance mismatch leads to reduced performance.

Loss deteriorates the received power and GPS reception of nRF9160. To minimize loss, the length of the transmission line from the antenna to the **GPS** pin should be kept as short as possible. A maximum of 0.5 dB transmission line loss is acceptable. If an external GPS *LNA* is used, and it is located close to the GPS antenna, the routing impedance and length recommendations may be waivered.

nRF9160 includes an *ESD* circuit on the **GPS** pin. The ESD circuit is intended for 1.5 kV *HBM* level, but additional ESD protection is recommended. The **GPS** pin is *DC* grounded. For more information on the antenna interface, see nWP033 - nRF9160 Antenna and RF Interface Guidelines.

> **Note:** Using the GPS receiver without an external LNA and *Band-Pass Filter (BPF)* is not recommended.

4.15.1 PCB layout design

When designing the *PCB* layout, pin-specific recommendations should be followed.

The **GPS** pin has the following recommendations:

- To ensure good, radiated performance, begin the design by locating the *GPS* antenna on the PCB.
- Ensure preliminary antenna performance on a chosen PCB location, for example, by simulation.
- When multiple antennas, for example, LTE, GPS, and Bluetooth Low Energy are present, minimize antenna crosstalk.
- Antenna transmission line impedance should be 50 Ω. Take this into account when selecting the PCB stack-up.
- Avoid excessive capacitance in routing by opening ground layers under component pads. For example, if the routing is on the top PCB layer, open the ground plane under the **GPS** pad on the next metal layer.
- When opening ground planes, avoid exposing noisy routings under the **GPS** pad.

- Avoid long routing because it causes excessive insertion loss which deteriorates RF performance which cannot be reversed.
- Ensure continuous reference ground plane above, below, or both of the **GPS** routing.
- Consider adding a test connector to the antenna path for production test and diagnostic purposes. Ensure that the test connector or solution does not deteriorate the impedance of the transmission line.

4.16 COEX

The COEX interface consists of pins 91–93. It is dedicated for RF interference avoidance towards a companion radio device, such as an external positioning device or Bluetooth Low Energy device.

The COEX interface is powered from **VDD_GPIO**. To control the COEX interface, the LTE modem must be active. When the LTE modem is not active, the COEX interface floats. Therefore, it is mandatory to use external pull-down resistors in the size range of 100 kΩ in the COEX interface.

The COEX pins have the following functionalities:

- **COEX0** (pin 93)
  - Can be configured for external *GPS LNA* control (high state) during GPS receive the same way as the **%XMAGPIO** command with the exception that **%XMAGPIO** controls only one pin. For more information, see MAGPIO configuration %XMAGPIO in nRF91 AT Commands Reference Guide.
- **COEX1** (pin 92)
  - Can be used during GPS receive to deliver GPS one pulse per second (1PPS) time mark pulse.

    Note: Supported in a future release of the modem firmware.
- **COEX2** (pin 91)
  - Can be used as an indicator of LTE or GPS RF activity from the modem to an external device. When **COEX2** is high, the LTE or GPS RF is active, and when it is low, the LTE or GPS RF is inactive.
  - Can be used as a “BLE nGrant”. This means that Bluetooth Low Energy should not transmit when **COEX2** is high and Bluetooth Low Energy can transmit when **COEX2** is low.
  - Can be used with **%XRFTEST** AT commands. For more information, see Production test features in nRF91 AT Commands Reference Guide.

4.16.1 Features

The **COEX** pins are powered from **VDD_GPIO** (pin 12). They have the same voltage level as **VDD_GPIO** and any unwanted noise or spurious that **VDD_GPIO** may contain. Therefore, proper noise filtering in **VDD_GPIO** is important. It is also important for each individual **COEX** pin to meet the filtering requirements specified for the peripherals connected to them.

To reduce transient currents, series resistors or ferrite beads can be used in the **COEX** lines. For low current, digital control type of **COEX** routings, resistor values in the range of 100 Ω to 1 kΩ can be considered. However, the optimal resistor values depend mainly on the connected peripheral drive currents and communication speed required by the peripherals.

In addition to the series resistor, bypass capacitors in the range of few pF can be considered. They may help to reduce RF coupling to the **COEX** lines. Unused **COEX** pins can be left unconnected electrically, but it is recommended to connect them to the application board for improved thermal and mechanical performance. For more information on the COEX interface configurations, see nRF9160 Product Specification.

Note: Additional capacitance increases **COEX** loading and noise originated from **COEX** toggling.

4.16.2 PCB layout design

When designing the *PCB* layout, interface-specific recommendations should be followed.

The COEX interface has the following recommendations:

- Place filtering series resistors close to the respective **COEX** pins.
- Place capacitors close to the origin of noise.
- Ground capacitors to the same ground plane as **VSS** (pin 103).
- Avoid routing **COEX** close to sensitive routings due to the risk of noise decoupling from **COEX**.
- Avoid routing **COEX** close to supply or RF routings due to the risk of noise decoupling to **COEX**.
- Use shielded PCB layers for *GPIO* routings whenever possible to minimize radiated noise.
- Follow the instructions in the peripheral datasheets.

4.17 Reserved

Pins 10, 51, 70, 71, 73, and 104–127 are reserved for Nordic's internal diagnostic purposes.

It is recommended to connect the **Reserved** pins to the application board mechanically and thermally, but to keep them electrically unconnected. To facilitate a simpler or more economical stencil design, **Reserved** pins 104–127 can be left electrically, mechanically, and thermally unconnected with no stencil openings for them.

5 Hardware design

The design of an end product is often driven by small form factor and attractive appearance. However, to achieve a product with solid performance, several design factors must be considered.

Some of those design factors conflict with the small form factor target. Typically, this means a compromise in the design that may affect the performance or appearance of the end product.

When a preliminary schematic of the device is ready, designing the *PCB* can begin. Layout design is typically iterative and involves trade-offs. The first hardware design rarely ends up being the mass-produced version. To minimize the number of hardware design rounds, cost, and time, the selected essential design factors that have a major impact on the end product's RF performance are discussed here.

5.1 Component placement

It is recommended to categorize and prioritize connections between nRF9160 and application components according to how critical they are.

For nRF9160's performance, RF routings are the most critical due to the mandatory impedance control and noticeable impact that they have on the user experience. Power supply routings are also important because insufficient power supply design causes nRF9160 to work improperly. In addition, the *SIM* and *MIPI RFFE* interfaces are sensitive and should be prioritized in the layout work.

It is also recommended to categorize application components according to which ones can be adjacent to one another on the *PCB*. For example, sensitive antennas and noisy DC converters or LEDs should never be adjacent to each other on a PCB. Two antennas, such as *GPS* and LTE, should never be adjacent to each other on a PCB because of the risk of mutual load effect between two nearby radiators. The load effect can noticeably deteriorate antenna efficiency and radiation pattern and have a major impact on the overall performance of the end product.

Some components, such as the LTE antenna and SIM holder, should be close to nRF9160 to minimize the negative impact of a long PCB routing, but not near each other. These components should not be too far from nRF9160, but their mutual distance should be maximized. It is recommended to place these components on the opposite sides of the PCB if possible.

Based on connections and component categorization, layout and component placement mockup can be started. Start the layout work from the most critical routings. Aim to have at least one dedicated PCB metal layer as a common ground plane for the entire PCB, keeping it as intact as possible. This metal layer also acts as the main thermal dissipation power relief path for nRF9160 and other active components on the application board.

A small form factor PCB sets constraints for component placement, especially for the antenna and its ground layer. Optimal placement for antennas is important and helps guarantee radiated performance and a good user experience for the end product. Therefore, it is recommended to estimate with 3D simulation tools the impact of different antenna locations and grounding on the PCB. Antenna design and simulation services are provided by various design houses globally.

Antenna vendors often provide design and measurement services, but typically they are meant only for their own products. If the end product includes antennas from more than one vendor, it is important to make sure that all antennas are verified to perform as expected simultaneously on a small form factor PCB or in the end product.

5.2 External flash memory requirements

If you want to perform a full modem firmware upgrade, an external flash memory with a minimum of 4 MB free space is required.

You can find more information on updating modem firmware at the following links:

- DFU target full modem update
- HTTP full modem update sample
- nRF9160 modem firmware

5.3 Antennas

If a small form factor device integrates antennas with noticeable performance requirements, for example, *GPS* or LTE, the antenna related design should be prioritized.

The key requirement in antenna design is that all antennas fulfill their performance targets in the actual use cases of the end product. The efficiency target for the LTE and GPS antennas should be a minimum of 50%. For the best possible GPS performance, the recommended efficiency is a minimum of 75%.

5.3.1 Troubleshooting

This section describes typical performance related issues in the end product's antenna design and ways to reduce them.

The placement of the antenna on the *PCB* and ground plane prevents from achieving good enough antenna radiation performance.

Follow the antenna vendors recommendations for placing the antenna on the PCB and ground plane.

Verify the antenna radiation pattern and efficiency in an anechoic chamber to match the datasheet.

RF path routing loss between antenna and nRF9160 is too high.

Verify 50 Ω impedance-controlled routing between the antenna and nRF9160.

Target less than 0.5 dB for resistive loss between the antenna and nRF9160.

> **Note:** *GPS* is recommended to be used with an external *LNA*. This means that resistive routing loss between the GPS LNA and nRF9160 is not highly critical. However, it is highly critical to avoid noise coupling from adjacent routings or components to GPS signal routing between the GPS antenna and nRF9160.

Mechanics, casing, battery, or wires deteriorate antenna performance.

Co-design the mechanics to match the PCB and antenna design.

Sharing a small PCB between several antennas, for example, GPS and LTE, causes mutual loading between the antennas.

Verify that the antennas do not cause mutual loading, for example, with passive antenna measurements in an anechoic chamber. Terminating an unused antenna, for example the LTE antenna during GPS, may have a noticeable impact on the mutual loading effect between the antennas. To minimize the load effect, the LTE antenna can be terminated through the **AUX** port (pin 64) to 50 Ω load during GPS.

Active components on the PCB cause wideband noise coupling to the antennas.

Verify that during reception, especially GPS, active components on the PCB do not radiate noise to the GPS antenna. For example, DC converters and LEDs are typical sources of radiating wideband noise. The RSSI scan testing method can be used. For more information, see nWP034 - nRF9160 Hardware Verification Guidelines.

The orientation of the end product in a typical use case is less than optimal for the antenna radiation pattern.

Consider in the design phase what the orientation of the end product is going to be in a typical use case.

Consider in the design phase the type of the GPS antenna, for example, omnidirectional or linear and directive or *Right Hand Circular Polarization (RHCP)*.

Nearby objects deteriorate antenna performance.

Instruct the end user to use the device in the manner it is designed for. For example, inform the user not to expect the best possible radio performance when the device is used inside a building, on a metal surface, or on their body.

GPS signal environment is more challenging than assumed in the design phase.

Instruct the end user to use the device in the manner it is designed for. The GPS signal type must be line-of-sight (LOS), which is rarely available in places like city centers with tall buildings nearby. The issue is even more severe in the polar regions because the GPS system is designed to perform the best in the equatorial regions.

5.4 nRF9160 module

The main principle in placing the nRF9160 module is to optimize the highest priority routings as described in Component placement on page 27.

Other important aspects are to achieve good thermal and mechanical contact to the application board and to avoid placing nRF9160 close to noisy components on the application board, such as DC converters or LEDs.

5.5 Thermal design

Good thermal design on the application board is essential for maximizing the performance and battery life of nRF9160. Poor thermal design causes nRF9160's built-in thermal protection to more easily trigger, preventing nRF9160 from transmitting and receiving LTE and *GPS* data.

The maximum power consumption and operating temperature of nRF9160 and the JEDEC standardized thermal coefficients are shown in the following table.

Parameter	Value
Power consumption (maximum heat power dissipation)	1480 mW
Maximum operating temperature	85°C
RthetaJA (Module-to-Ambient)	23°C/W
RThetaJB (Module-to-Board)	6°C/W
RThetaJC (Module-to-Case)	1°C/W
Maximum allowed Tc (Module case temperature)	85°C
Maximum Allowed Tj (Worst case of module components)	85°C

Table 3: Thermal characteristics of nRF9160

Note: Thermal resistance (JA, JB, and JC) is measured in still air conditions with the module mounted on 72 mm x 46 mm x 1.2mm 6-layer *PCB* with high copper coverage on all metal layers.

5.6 PCB stack-up

Choosing the *PCB* stack-up should be aligned with the end product's PCB requirements.

For nRF9160, the following targets should be considered:

- Dedicate one metal layer that is as intact as possible for the common ground layer.
- Consider the need for 50 Ω RF routings. Sometimes to achieve 50 Ω routing requires the adjacent metal layer to be opened which increases the risk of exposing RF routing to noisy routings.
- Avoid crossing 50 Ω RF routings on the application board. If it cannot be avoided, ensure that their ground planes remain continuous.
- Avoid using through vias in RF routings if they cause a parallel stub to the routing or are not 50 Ω.
- Consider good thermal design and aim to use metal filled vias due to their better thermal conductivity especially close to nRF9160.

Glossary

Band-Pass Filter (BPF)

An electronic device or circuit that passes frequencies within a certain range and rejects frequencies outside that range.

DC

Direct Current

Device Firmware Update (DFU)

A mechanism for upgrading the firmware of a device.

Electrostatic Discharge (ESD)

A sudden discharge of electric current between two electrically charged objects.

Global Positioning System (GPS)

A satellite-based radio navigation system that provides its users with accurate location and time information over the globe.

General-Purpose Input/Output (GPIO)

A digital signal pin that can be used as input, output, or both. It is uncommitted and can be controlled by the user at runtime.

GPIOTE

General-Purpose Input/Output Tasks and Events

Human Body Model (HBM)

Simulates a charged person discharging to ground through a circuit.

Integrated Circuit (IC)

A semiconductor chip consisting of fabricated transistors, resistors, and capacitors.

Low-Noise Amplifier (LNA)

In a radio receiving system, an electronic amplifier that amplifies a very low-power signal without significantly degrading its signal-to-noise ratio.

MIPI RF Front-End Control Interface (RFFE)

A dedicated control interface for the RF front-end subsystem. *MIPI Alliance*

Power Amplifier (PA)

A device used to increase the transmit power level of a radio signal.

Printed Circuit Board (PCB)

A board that connects electronic components.

Programmable Peripheral Interconnect (PPI)

Enables peripherals to interact autonomously with each other using tasks and events independent of the CPU.

Right Hand Circular Polarization (RHCP)

Circular polarization in which the electric field vector rotates in a right-hand sense with respect to the direction of propagation.

Serial Wire Debug (SWD)

A standard two-wire interface for programming and debugging Arm® CPUs.

Subscriber Identity Module (SIM)

A card used in *User Equipment (UE)* containing data for subscriber identification.

System in Package (SiP)

Several integrated circuits, often from different technologies, enclosed in a single module that performs as a system or subsystem.

System on Chip (SoC)

A microchip that integrates all the necessary electronic circuits and components of a computer or other electronic systems on a single integrated circuit.

Universal Integrated Circuit Card (UICC)

A new generation *SIM* used in *UE* for ensuring the integrity and security of personal data.

Universal Subscriber Identity Module (USIM)

A card used in *UE* containing data for subscriber identification.

User Equipment (UE)

Any device used by an end-user to communicate. The UE consists of the Mobile Equipment (ME) and the Universal Integrated Circuit Card (UICC).

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