Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	Acce	Field	Value ID	Value	Description
A	R	ERASEALLSTATUS			Status register for the ERASEALL operation
			Ready	0	ERASEALL is ready
			Busy	1	ERASEALL is busy (on-going)

9.2.5.4 APPROTECT.STATUS

Address offset: 0x00C

Status register for access port protection

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	Acce	Field	Value ID	Value	Description
A	R	APPROTECT			Status bit for access port protection
			Enabled	0	APPROTECT is enabled
			Disabled	1	APPROTECT is disabled
B	R	SECUREAPPROTECT			Status bit for secure access port protection
			Enabled	0	SECUREAPPROTECT is enabled
			Disabled	1	SECUREAPPROTECT is disabled

9.2.5.5 ERASEPROTECT.STATUS

Address offset: 0x018

Status register for UICR ERASEPROTECT configuration

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	Acce	Field	Value ID	Value	Description
A	R	PALL			ERASEALL status
			Enabled	0	ERASEALL protection is enabled
			Disabled	1	ERASELL protection is not enabled and device can be erased

9.2.5.6 ERASEPROTECT.DISABLE

Address offset: 0x01C

Unlock ERASEPROTECT and perform ERASEALL

This register can only be written once per reset

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	Acce	Field	Value ID	Value	Description
A	RW1	KEY			Initiate secure erase even though ERASEPROTECT is enabled if KEY fields match

9.2.5.7 MAILBOX.TXDATA

Address offset: 0x020

Data sent from the debugger to the CPU

Writing to this register will automatically set field DataPending in register TXSTATUS

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	Acce	Field	Value ID	Value	Description
A	RW	Data			Data sent from debugger

9.2.5.8 MAILBOX.TXSTATUS

Address offset: 0x024

Status to indicate if data sent from the debugger to the CPU has been read

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	Acce	Field	Value ID	Value	Description
A	R	Status			Status of register DATA
			NoDataPending	0	No data pending in register TXDATA
			DataPending	1	Data pending in register TXDATA

9.2.5.9 MAILBOX.RXDATA

Address offset: 0x028

Data sent from the CPU to the debugger

Reading from this register will automatically set field NoDataPending in register RXSTATUS

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	Acce	Field	Value ID	Value	Description
A	R	Data			Data sent from CPU

9.2.5.10 MAILBOX.RXSTATUS

Address offset: 0x02C

Status to indicate if data sent from the CPU to the debugger has been read

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	Acce	Field	Value ID	Value	Description
A	R	Status			Status of register DATA
			NoDataPending	0	No data pending in register RXDATA
			DataPending	1	Data pending in register RXDATA

9.2.5.11 IDR

Address offset: 0x0FC

CTRL-AP Identification Register, IDR

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				E E E E D D D D C C C C C C C B B B B A A A A A A A A
Reset 0x12880000				**0 0 0 1 0 0 1 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	Acce	Field	Value ID	Value	Description
A	R	APID			AP Identification
B	R	CLASS			Access Port (AP) class
			NotDefined	0x0	No defined class
			MEMAP	0x8	Memory Access Port
C	R	JEP106ID			JEDEC JEP106 identity code
D	R	JEP106CONT			JEDEC JEP106 continuation code
E	R	REVISION			Revision

9.2.6 Registers

Base address	Peripheral	Instance	Secure mapping	DMA security	Description	Configuration
0x50006000	CTRLAPPERI	CTRL_AP_PERI	S	NA	CTRL-AP-PERI	

Table 100: Instances

Register	Offset	Security	Description
MAILBOX.RXDATA	0x400		Data sent from the debugger to the CPU
MAILBOX.RXSTATUS	0x404		Status to indicate if data sent from the debugger to the CPU has been read
MAILBOX.TXDATA	0x480		Data sent from the CPU to the debugger
MAILBOX.TXSTATUS	0x484		Status to indicate if data sent from the CPU to the debugger status has been read
ERASEPROTECT.LOCK	0x500		Lock ERASEALL mechanism
ERASEPROTECT.DISABLE	0x504		Unlock ERASEPROTECT and perform ERASEALL

Table 101: Register overview

9.2.6.1 MAILBOX.RXDATA

Address offset: 0x400

Data sent from the debugger to the CPU

Reading from this register will automatically set field NoDataPending in register RXSTATUS

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	Acce	Field	Value ID	Value	Description
A	R	RXDATA			Data received from debugger

9.2.6.2 MAILBOX.RXSTATUS

Address offset: 0x404

Status to indicate if data sent from the debugger to the CPU has been read

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	Acce	Field	Value ID	Value	Description
A	R	RXSTATUS			Status of data in register RXDATA
			NoDataPending	0	No data pending in register RXDATA
			DataPending	1	Data pending in register RXDATA

9.2.6.3 MAILBOX.TXDATA

Address offset: 0x480

Data sent from the CPU to the debugger

Writing to this register will automatically set field DataPending in register TXSTATUS

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	Acce	Field	Value ID	Value	Description
A	RW	TXDATA			Data sent to debugger

9.2.6.4 MAILBOX.TXSTATUS

Address offset: 0x484

Status to indicate if data sent from the CPU to the debugger status has been read

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	Acce	Field	Value ID	Value	Description
A	R	TXSTATUS			Status of data in register TXDATA
			NoDataPending	0	No data pending in register TXDATA
			DataPending	1	Data pending in register TXDATA

9.2.6.5 ERASEPROTECT.LOCK

Address offset: 0x500

Lock ERASEALL mechanism

This register can only be written once per reset

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	Acce	Field	Value ID	Value	Description
A	RW1	ERASEPROTECTLOCK			Enable or disable the ERASEALL mechanism
			Unlocked	0	ERASEALL can be issued
			Locked	1	ERASEALL is locked

9.2.6.6 ERASEPROTECT.DISABLE

Address offset: 0x504

Unlock ERASEPROTECT and perform ERASEALL

This register can only be written once per reset

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	Acce	Field	Value ID	Value	Description
A	RW	KEY			Initiate secure erase even though ERASEPROTECT is enabled if KEY fields match

9.3 TAD - Trace and debug control

Configuration interface for trace and debug

9.3.1 Registers

Base address	Peripheral	Instance	Secure mapping	DMA security	Description	Configuration
0xE0080000	TAD	TAD	S	NA	Trace and debug control	

Table 102: Instances

Register	Offset	Security	Description
ENABLE	0x500		Enable debug domain and aquire selected GPIOs
PSEL.TRACECLK	0x504		Pin number configuration for TRACECLK
PSEL.TRACEDATA0	0x508		Pin number configuration for TRACEDATA[0]
PSEL.TRACEDATA1	0x50C		Pin number configuration for TRACEDATA[1]
PSEL.TRACEDATA2	0x510		Pin number configuration for TRACEDATA[2]
PSEL.TRACEDATA3	0x514		Pin number configuration for TRACEDATA[3]
TRACEPORTSPEED	0x518		Clocking options for the Trace Port debug interface

Table 103: Register overview

9.3.1.1 ENABLE

Address offset: 0x500

Enable debug domain and aquire selected GPIOs

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID	A
Reset 0x00000000	**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**

ID	Acce	Field	Value ID	Value	Description
A	RW	ENABLE			
			DISABLED	0	Disable debug domain and release selected GPIOs
			ENABLED	1	Enable debug domain and aquire selected GPIOs

9.3.1.2 PSEL.TRACECLK

Address offset: 0x504

Pin number configuration for TRACECLK

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID			B A A A A A
Reset 0xFFFFFFFF			**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**

ID	Acce	Field	Value ID	Value	Description
A	RW	PIN		[0..31]	Pin number
B	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

9.3.1.3 PSEL.TRACEDATA0

Address offset: 0x508

Pin number configuration for TRACEDATA[0]

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID			B A A A A A
Reset 0xFFFFFFFF			**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**

ID	Acce	Field	Value ID	Value	Description
A	RW	PIN		[0..31]	Pin number
B	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

9.3.1.4 PSEL.TRACEDATA1

Address offset: 0x50C

Pin number configuration for TRACEDATA[1]

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID			B A A A A A
Reset 0xFFFFFFFF			**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**

ID	Acce	Field	Value ID	Value	Description
A	RW	PIN		[0..31]	Pin number
B	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

9.3.1.5 PSEL.TRACEDATA2

Address offset: 0x510

Pin number configuration for TRACEDATA[2]

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID			B A A A A A
Reset 0xFFFFFFFF			**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**

ID	Acce	Field	Value ID	Value	Description
A	RW	PIN		[0..31]	Pin number
B	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

9.3.1.6 PSEL.TRACEDATA3

Address offset: 0x514

Pin number configuration for TRACEDATA[3]

Bit number					31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID					B A A A A A
Reset 0xFFFFFFFF					**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
ID	Acce	Field	Value ID	Value	Description
A	RW	PIN		[0..31]	Pin number
B	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

9.3.1.7 TRACEPORTSPEED

Address offset: 0x518

Clocking options for the Trace Port debug interface

This register is a retained register. Reset behavior is the same as debug components.

Bit number					31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID					A A
Reset 0x00000000					**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	Acce	Field	Value ID	Value	Description
A	RW	TRACEPORTSPEED			Speed of Trace Port clock. Note that the TRACECLK pin will output this clock divided by two.
			32MHz	0	32 MHz Trace Port clock (TRACECLK = 16 MHz)
			16MHz	1	16 MHz Trace Port clock (TRACECLK = 8 MHz)
			8MHz	2	8 MHz Trace Port clock (TRACECLK = 4 MHz)
			4MHz	3	4 MHz Trace Port clock (TRACECLK = 2 MHz)

10 Hardware and layout

10.1 Pin assignments

This section describes the pin assignment and the pin functions.

This device provides flexibility when it comes to routing and configuration of the GPIO pins. However, some pins have recommendations for how the pin should be configured or what it should be used for. See LGA pin assignments on page 379 for more information about this.

10.1.1 Pin assignments

The pin assignment table and figure describe the assignments for this variant of the chip.

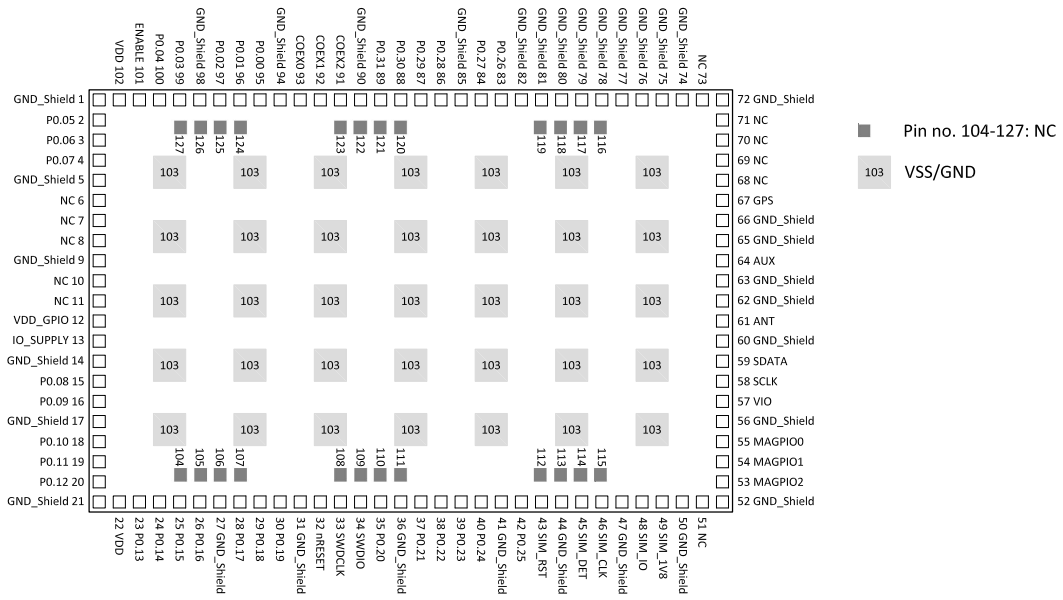

Figure 111: LGA pin assignments, top view

Pin no	Pin name	Function	Description
1	GND_Shield	Power	Ground
2	P0.05	Digital I/O (SoC)	General purpose I/O
3	P0.06	Digital I/O (SoC)	General purpose I/O
4	P0.07	Digital I/O (SoC)	General purpose I/O
5	GND_Shield	Power	Ground
6	NC		Not connected/reserved for Nordic use
7	NC		Not connected/reserved for Nordic use
8	NC		Not connected/reserved for Nordic use
9	GND_Shield	Power	Ground
10	NC		Not connected/reserved for Nordic use
11	NC		Not connected/reserved for Nordic use
12	VDD_GPIO	Power	GPIO power supply input and logic level
13	IO_SUPPLY	Power	Reserved for Nordic use
14	GND_Shield	Power	Ground
15	P0.08	Digital I/O (SoC)	General purpose I/O
16	P0.09	Digital I/O (SoC)	General purpose I/O

Pin no	Pin name	Function	Description
17	GND_Shield	Power	Ground
18	P0.10	Digital I/O (SoC)	General purpose I/O
19	P0.11	Digital I/O (SoC)	General purpose I/O
20	P0.12	Digital I/O (SoC)	General purpose I/O
21	GND_Shield	Power	Ground
22	VDD	Power	Supply voltage input
23	P0.13	Digital I/O (SoC)	General purpose I/O.
	AIN0	Analog input	Analog input.
24	P0.14	Digital I/O (SoC)	General purpose I/O.
	AIN1	Analog input	Analog input.
25	P0.15	Digital I/O (SoC)	General purpose I/O.
	AIN2	Analog input	Analog input.
26	P0.16	Digital I/O (SoC)	General purpose I/O.
	AIN3	Analog input	Analog input.
27	GND_Shield	Power	Ground
28	P0.17	Digital I/O (SoC)	General purpose I/O.
	AIN4	Analog input	Analog input.
29	P0.18	Digital I/O (SoC)	General purpose I/O.
	AIN5	Analog input	Analog input.
30	P0.19	Digital I/O (SoC)	General purpose I/O.
	AIN6	Analog input	Analog input.
31	GND_Shield	Power	Ground
32	nRESET	Digital I/O (SoC)	System reset
33	SWDCLK	Digital input	Serial wire debug clock input for debug and programming
34	SWDIO	Digital I/O	Serial wire debug I/O for debug and programming
35	P0.20	Digital I/O (SoC)	General purpose I/O.
	AIN7	Analog input	Analog input.
36	GND_Shield	Power	Ground
37	P0.21	Digital I/O (SoC)	General purpose I/O.
	TRACECLK	Trace clock	Trace buffer clock (optional).
38	P0.22	Digital I/O (SoC)	General purpose I/O.
	TRACEDATA0	Trace data	Trace buffer TRACEDATA[0] (optional).
39	P0.23	Digital I/O (SoC)	General purpose I/O.
	TRACEDATA1	Trace data	Trace buffer TRACEDATA[1] (optional).
40	P0.24	Digital I/O (SoC)	General purpose I/O.
	TRACEDATA2	Trace data	Trace buffer TRACEDATA[2] (optional).
41	GND_Shield	Power	Ground
42	P0.25	Digital I/O (SoC)	General purpose I/O.
	TRACEDATA3	Trace data	Trace buffer TRACEDATA[3] (optional).
43	SIM_RST	Digital I/O (SoC)	SIM reset
44	GND_Shield	Power	Ground
45	SIM_DET	Digital I/O (SoC)	SIM detect
46	SIM_CLK	Digital I/O (SoC)	SIM clock
47	GND_Shield	Power	Ground
48	SIM_IO	Digital I/O (SoC)	SIM data
49	SIM_1V8	Power	SIM 1.8 V power supply output
50	GND_Shield	Power	Ground
51	NC		Not connected/reserved for Nordic use
52	GND_Shield	Power	Ground

Pin no	Pin name	Function	Description
53	MAGPIO2	Digital I/O (SoC)	Reserved for Nordic use
54	MAGPIO1	Digital I/O (SoC)	Reserved for Nordic use
55	MAGPIO0	Digital I/O (SoC)	Reserved for Nordic use
56	GND_Shield	Power	Ground
57	VIO	Power	Reserved for Nordic use
58	SCLK	Digital I/O (SoC)	Reserved for Nordic use
59	SDATA	Digital I/O (SoC)	Reserved for Nordic use
60	GND_Shield	Power	Ground
61	ANT	RF	Single-ended radio antenna connection
62	GND_Shield	Power	Ground
63	GND_Shield	Power	Ground
64	AUX	RF	ANT output port
65	GND_Shield	Power	Ground
66	GND_Shield	Power	Ground
67	GPS	RF	GPS receiver input
68	NC		Not connected/reserved for Nordic use
69	NC		Not connected/reserved for Nordic use
70	NC		Not connected/reserved for Nordic use
71	NC		Not connected/reserved for Nordic use
72	GND_Shield	Power	Ground
73	NC		Not connected/reserved for Nordic use
74	GND_Shield	Power	Ground
75	GND_Shield	Power	Ground
76	GND_Shield	Power	Ground
77	GND_Shield	Power	Ground
78	GND_Shield	Power	Ground
79	GND_Shield	Power	Ground
80	GND_Shield	Power	Ground
81	GND_Shield	Power	Ground
82	GND_Shield	Power	Ground
83	P0.26	Digital I/O (SoC)	General purpose I/O
84	P0.27	Digital I/O (SoC)	General purpose I/O
85	GND_Shield	Power	Ground
86	P0.28	Digital I/O (SoC)	General purpose I/O
87	P0.29	Digital I/O (SoC)	General purpose I/O
88	P0.30	Digital I/O (SoC)	General purpose I/O
89	P0.31	Digital I/O (SoC)	General purpose I/O
90	GND_Shield	Power	Ground
91	COEX2	Digital I/O (SoC)	Coexistence interface
92	COEX1	Digital I/O (SoC)	Coexistence interface
93	COEX0	Digital I/O (SoC)	Coexistence interface
94	GND_Shield	Power	Ground
95	P0.00	Digital I/O (SoC)	General purpose I/O
96	P0.01	Digital I/O (SoC)	General purpose I/O
97	P0.02	Digital I/O (SoC)	General purpose I/O
98	GND_Shield	Power	Ground
99	P0.03	Digital I/O (SoC)	General purpose I/O
100	P0.04	Digital I/O (SoC)	General purpose I/O
101	ENABLE		Enable for the SiP internal regulator for the nRF91 SoC. **Note:** The nRF91 will not start until this pin is enabled.
102	VDD	Power	Supply voltage

Pin no	Pin name	Function	Description
103	VSS	Power	Ground
104-127	NC		Not connected/reserved for Nordic use (do not connect)

Table 104: LGA pin assignments

10.2 Mechanical specifications

The mechanical specifications for the packages show the dimensions in millimeters.

10.2.1 16.00 x 10.50 mm package

Dimensions in millimeters for the nRF9160 LGA 16.00 x 10.50 mm package.

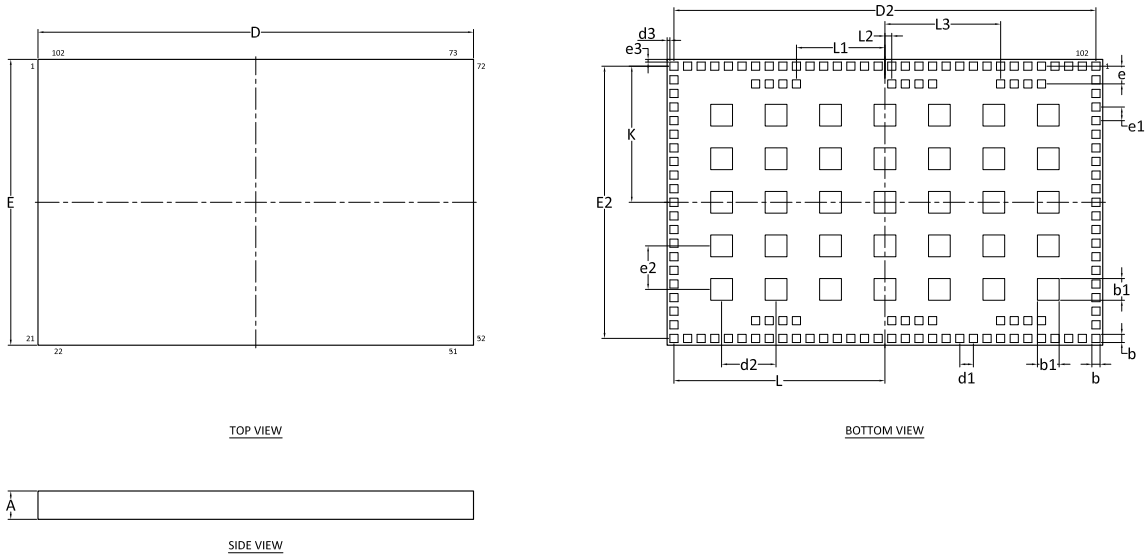

Figure 112: LGA 16.00 x 10.50 mm package

	A	b	b1	D	E	e	d1	e1	D2	E2	d2	e2	d3	e3	K	L	L1	L2	L3
Min.	0.98			15.90	10.40														
Nom.	1.04	0.30	0.80	16.00	10.50	0.65	0.50	0.50	15.50	10.00	2.00	1.60	0.10	0.10	5.00	7.75	3.25	0.25	4.25
Max.	1.10			16.10	10.60														

Table 105: LGA dimensions in millimeters

10.3 Reference circuitry

To ensure good RF performance when designing PCBs, it is highly recommended to use the PCB layouts and component values provided by Nordic Semiconductor.

Documentation for the different package reference circuits, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from www.nordicsemi.com.

10.3.1 Schematic

The bill of material (BOM) is TBD.

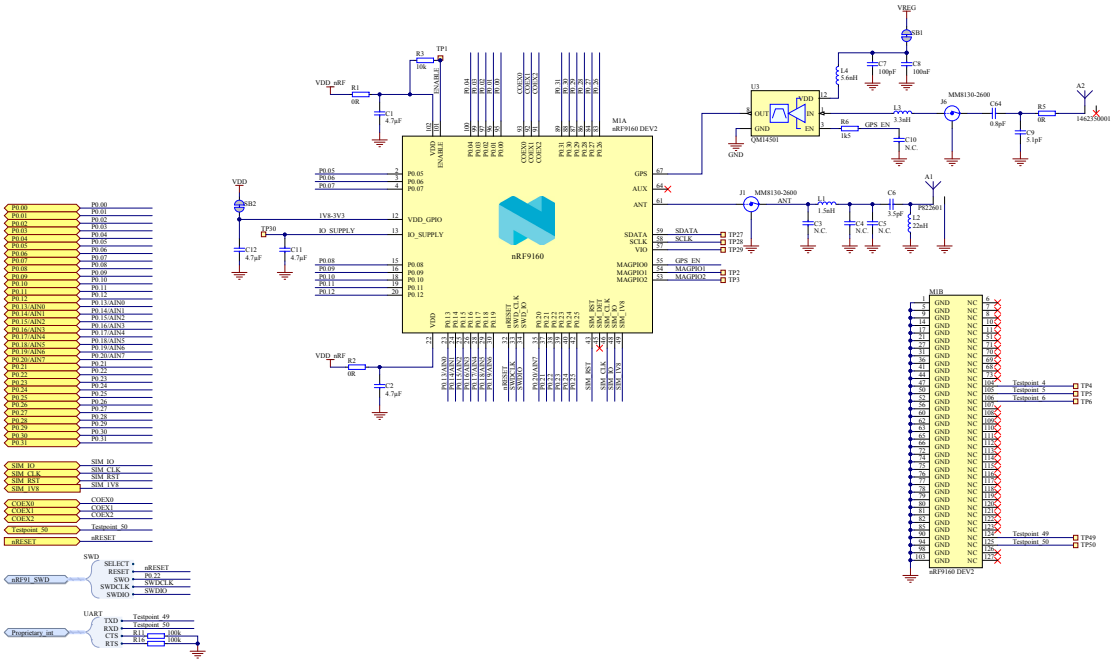

Figure 113: Schematic, with antenna details

10.3.2 PCB layout example

The PCB layout shown below is a part of an example reference layout for the LGA package, showing antenna details.

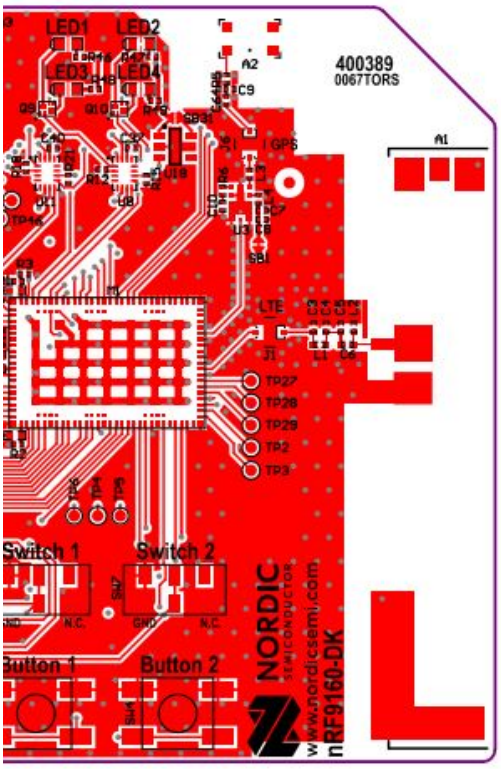

Figure 114: Top layer

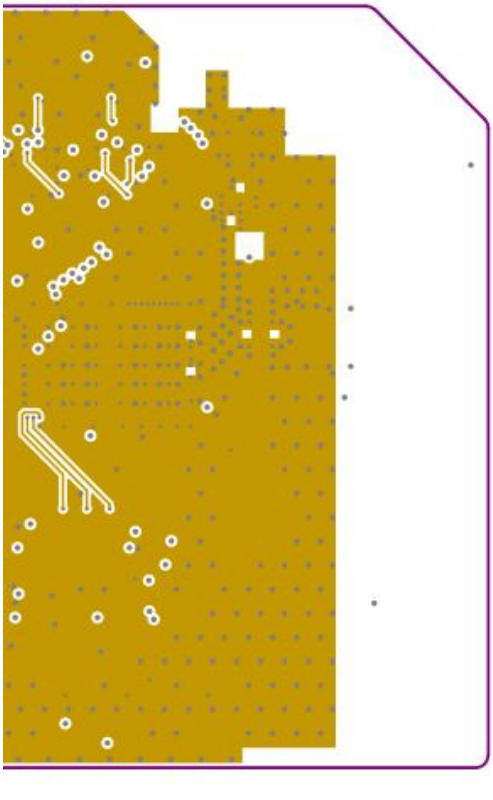

Figure 115: Mid layer 1

10.3.3 PCB laminate specification

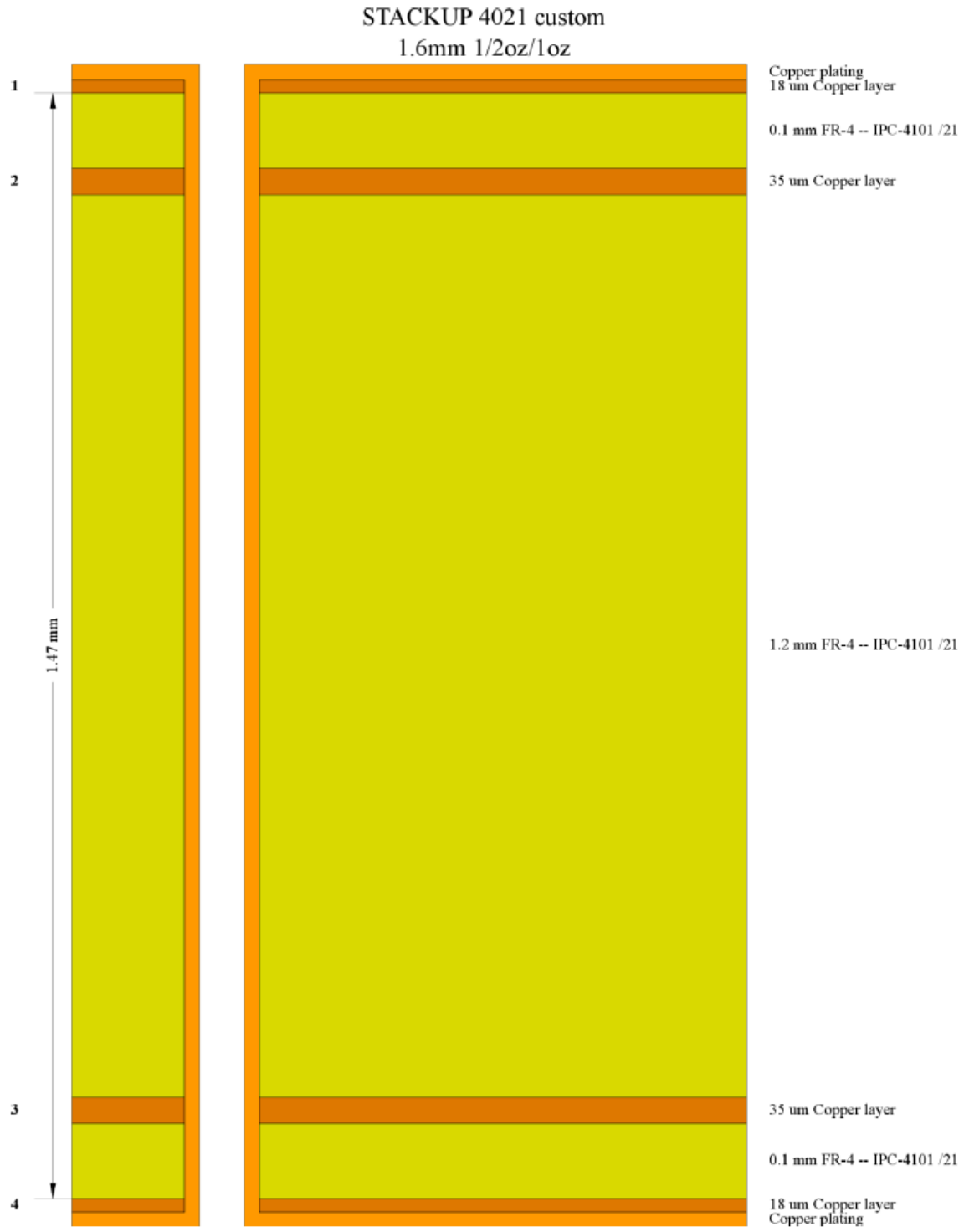

Figure 116: Elprint's 4 layer 4001 stackup

11 Recommended operating conditions

The operating conditions are the physical parameters that the chip can operate within.

Symbol	Parameter	Notes	Min.	Nom.	Max.	Units
VDD	Battery input voltage	Including voltage drop, ripple and spikes. RF 3GPP compliancy requires 3.3 V.	3.0	3.8	5.5	V
VDD_GPIO	GPIO input voltage		1.7		3.6	V
$GPIO_H$	GPIO high level voltage				VDD_GPIO	V
$MAGPIO_H$	MAGPIO high level voltage			1.8	1.8	V
$t_{R\_VDD\_GPIO}$	VDD_GPIO rise time (0 V to 1.7 V)	IO_SUPPLY should be ramped up before or in parallel with VDD_GPIO			60	ms
TA	Operating temperature		-40	25	85	°C

Table 106: Recommended operating conditions

Note: There can be excessive leakage at VDD and/or VDD_GPIO if any of these supply voltages is outside its range given in Recommended operating conditions on page 386.

11.1 VDD_GPIO considerations

VDD_GPIO is the supply to the general purpose I/O.

The following restrictions should be taken into considerations:

- VDD_GPIO should be applied after VDD has been supplied
- VDD_GPIO should be removed before removing VDD
- If VDD is supplied and VDD_GPIO is grounded, an extra current consumption can be generated on VDD

12 Absolute maximum ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

	Note	Min.	Max.	Unit
Supply voltages				
VDD		-0.3	5.5	V
VDD_GPIO		-0.3	3.9	V
VSS			0	V
I/O pin voltage				
$V_{I/O}$, VDD_GPIO ≤ 3.6 V		-0.3	VDD_GPIO + 0.3	V
$V_{I/O}$, VDD_GPIO > 3.6 V		-0.3	3.9	V
Radio				
RF input level			10	dBm
Environmental (LGA package)				
Storage temperature		-40	125	°C
MSL	Moisture Sensitivity Level		2	
ESD HBM	Human Body Model		2	kV
ESD CDM	Charged Device Model		500	V
Flash memory				
Endurance		10 000		Write/erase cycles
Retention		10 years at 85°C		

Table 107: Absolute maximum ratings

13 Ordering information

This chapter contains information on IC marking, ordering codes, and container sizes.

13.1 IC marking

The nRF9160 IC package is marked like described below.

N	9	1	6	0	
<P	P>	<V	V>	<H>	<P>
<Y	Y>	<W	W>	<L	L>

Figure 117: Package marking

13.2 Box labels

Here are the box labels used for the nRF9160.

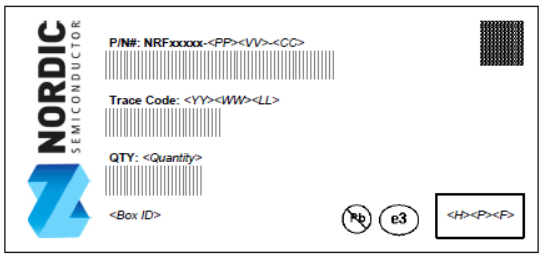

Figure 118: Inner box label

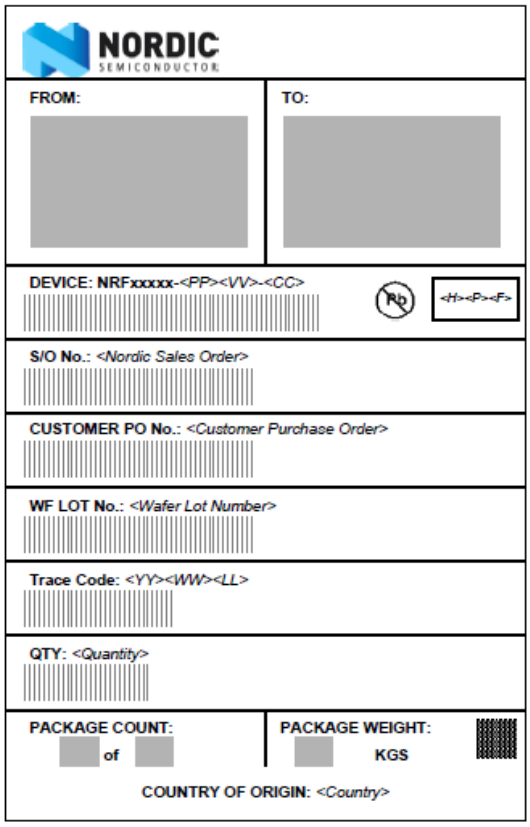

Figure 119: Outer box label

13.3 Order code

Here are the nRF9160 order codes and definitions.

n	R	F	9	1	6	0	-	<P	P>	<V	V>	-	<C	C>

Figure 120: Order code

Abbreviation	Definition and implemented codes
N91/nRF91	nRF91 Series product
60	Part code
<PP>	Package variant code
<VV>	Function variant code
<H><P><F>	Build code H - Hardware version code P - Production configuration code (production site, etc.) F - Firmware version code (only visible on shipping container label)
<YY><WW><LL>	Tracking code YY - Year code WW - Assembly week number LL - Wafer lot code
<CC>	Container code

Table 108: Abbreviations

13.4 Code ranges and values

Defined here are the nRF9160 code ranges and values.

<PP>	Package	Size (mm)	Pin/Ball count	Pitch (mm)

Table 109: Package variant codes

<VV>	Flash (kB)	RAM (kB)

Table 110: Function variant codes

<H>	Description
[A . . Z]	Hardware version/revision identifier (incremental)

Table 111: Hardware version codes

<P>	Description
[0 . . 9]	Production device identifier (incremental)
[A . . Z]	Engineering device identifier (incremental)

Table 112: Production configuration codes

<F>	Description
[A . . N, P . . Z]	Version of preprogrammed firmware
[0]	Delivered without preprogrammed firmware

Table 113: Production version codes

<YY>	Description
[15 . . 99]	Production year: 2015 to 2099

Table 114: Year codes

<WW>	Description
[1 . . 52]	Week of production

Table 115: Week codes

<LL>	Description
[AA . . ZZ]	Wafer production lot identifier

Table 116: Lot codes

<CC>	Description
R7	7" Reel
R	13" Reel
T	Tray

Table 117: Container codes

13.5 Product options

Defined here are the nRF9160 product options.

Order code	Minimum ordering quantity (MOQ)	Comment
nRF9160-SICA-R	2500	LTE-M/NB-IoT/GPS product
nRF9160-SIAA-R	2500	LTE-M only product
nRF9160-SIBA-R	2500	NB-IoT only product

Table 118: nRF9160 order codes

Order code	Description
nRF9160-DK	

Table 119: Development tools order code

14 FCC/ISED regulatory notices

Modification statement

Nordic Semiconductor has not approved any changes or modifications to this device by the user. Any changes or modifications could void the user's authority to operate the equipment.

Nordic Semiconductor n'approuve aucune modification apportée à l'appareil par l'utilisateur, quelle qu'en soit la nature. Tout changement ou modification peuvent annuler le droit d'utilisation de l'appareil par l'utilisateur.

Interference statement

This device complies with Part 15 of the FCC Rules and Industry Canada's licence-exempt RSS standards. Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Wireless notice

This equipment complies with FCC and ISED radiation exposure limits set forth for an uncontrolled environment. The antenna should be installed and operated with minimum distance of 20 cm between the radiator and your body. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Cet appareil est conforme aux limites d'exposition aux rayonnements de l'ISDE pour un environnement non contrôlé. L'antenne doit être installée de façon à garder une distance minimale de 20 centimètres entre la source de rayonnements et votre corps. L'émetteur ne doit pas être colocalisé ni fonctionner conjointement avec à autre antenne ou autre émetteur.

Permitted antenna

This radio transmitter has been approved by FCC and ISED to operate with the antenna types listed below with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Type	Band	Max gain
SMD	Band 4	6 dBi
	Band 13	6.9 dBi

Le présent émetteur radio a été approuvé par ISDE pour fonctionner avec les types d'antenne énumérés ci dessous et ayant un gain admissible maximal. Les types d'antenne non inclus dans cette liste, et dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

Type	Bande	Gain maximal
CMS	Bande 4	6 dBi
	Bande 13	6.9 dBi

FCC Class B digital device notice

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

CAN ICES-3 (B)/NMB-3 (B)

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de classe B est conforme à la norme canadienne ICES-003.

Labeling requirements for the host device

The host device shall be properly labelled to identify the modules within the host device. The certification label of the module shall be clearly visible at all times when installed in the host device, otherwise the host device must be labelled to display the FCC ID and IC of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as follows:

Contains FCC ID: 2ANPO00NRF9160
Contains IC: 24529-NRF9160

L'équipement hôte doit être correctement étiqueté pour identifier les modules dans l'équipement. L'étiquette de certification du module doit être clairement visible en tout temps lorsqu'il est installé dans l'hôte, l'équipement hôte doit être étiqueté pour afficher le FCC ID et IC du module, précédé des mots "Contient le module émetteur", ou le mot "Contient", ou un libellé similaire exprimant la même signification, comme suit:

Contient FCC ID: 2ANPO00NRF9160
Contient IC: 24529-NRF9160

15 Legal notices

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Nordic Semiconductor ASA reserves the right to make corrections, enhancements, and other changes to this document without notice.

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Nordic Semiconductor ASA products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury.

Nordic Semiconductor ASA customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nordic Semiconductor ASA for any damages resulting from such improper use or sale.

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Nordic Semiconductor products meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substances (RoHS) and the requirements of the REACH regulation (EC 1907/2006) on Registration, Evaluation, Authorization and Restriction of Chemicals.

The SVHC (Substances of Very High Concern) candidate list is continually being updated. Complete hazardous substance reports, material composition reports and latest version of Nordic Semiconductor's REACH statement can be found on our website http://www.nordicsemi.com.

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