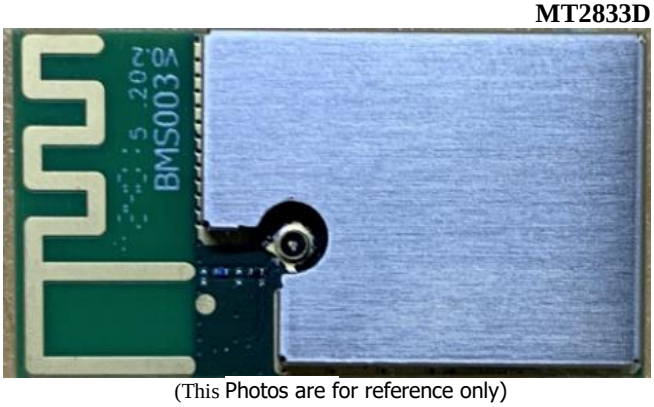
BMS003 BT5.3 LE Audio Module

Bluetooth Qualifie

MT2833D



(This Photos are for reference only)

Features

• Supports Bluetooth 5.3 dual-mode (BDR/EDR/ BLE) specifications
• ARM® Cortex®-M33 with Floating Point Unit (FPU) and Memory Protection Unit (MPU)
Maximum speed: 260MHz
• Cadence® HiFi5® Audio Engine DSP coprocessor with Neural Network Extension
Maximum speed: 520MHz
• low latency 1MB system RAM (SYSRAM) with maximum speed 260MHz
• USB 2.0 device
• Support maximum three I2C Master mode 400kbps Up to 3.4Mbps
• Support maximum three I3C Master mode up to 12Mbps
• Support maximum three UART interface Up to 3Mbps
• Support maximum three SPI master interface, Clock up to 52MHz
• EMMC4.41/SDIO v2.0, up to 52MHz, 1-bit/4-bit mode eMMC4.41,
• Stand-alone module with on-board PWB antenna and Bluetooth stack
• Supports high resolution up to 24-bit, 192 kHz audio data format
• Supports14 PWM channels
• Supports12-bit AUXADC channels
• Supports maximum four I2S interface
• Supports SPDIF receiver
• Supports to connect max three hosts with HFP/A2DP profiles simultaneously
• Supports smart phone applications by Bluetooth SPP or BLE link
• Supports firmware field upgrade by USB/OTA
• Supports four microphones
• Compact surface mount module:28.28 * 15.60 * 4.0 mm
• LGA package 122pin, Flatness is less than 0.05mm
• RoHS compliant
• Ideal for portable battery operated devices
• Internal battery regulator circuitry DSP Audio Processing
• Support for single SCO or Esco link with CVSD/mSBC coding.

Peripherals

• Integrated 1.8V and 3V configurable switching regulator and low-dropout (LDO) regulator
• Built-in ADC for battery monitoring and voltage sense
• Built-in ADC for charger thermal protection
• Built-in under voltage protection (UVP)
• An AUX-In port for external audio input
• Multiple I/O pins for control and status

HCI Interface

• High-speed HCI-UART interface (supports up to 3M bps)

RF/Analog

• Frequency spectrum: 2.402 GHz to 2.480 GHz
• Receive sensitivity: -97 dBm (2 Mbps EDR)
• Crystal : 26MHZ ±20PPM@-20℃~+70℃
• AVG Output Power：
8±2dBm (BDR) , 6±2dBm (EDR)
4±2dBm (BLE1M/2M)
• Antenna gain：2.7dBi(Peak)

Audio Codec

• SBC,AAC, LDAC
• 24-bit digital-to-analog converter (DAC) with 105dB SNR
• 24-bit analog-to-digital converter (ADC) with 95dB SNR
• Supports up to 24-bit, 192 kHz I2S digital audio

MAC/Baseband Processor

• Supports Bluetooth 5.3 dual-mode
• BDR/EDR transport for audio, voice, and SPP data exchange
• BLE transport for proprietary transparent service and Apple Notification Center Service (ANCS) data exchange

Operating Condition

• Operating voltage: 3.2V to 4.6V
• Operating temperature: -20 ℃ to +70 ℃

Description

The BMS003 LE Audio module is made in China, a fully qualified Bluetooth 5.3 dual-mode (BDR/EDR/BLE) module for designers to add wireless audio and voice applications to their products. The BMS003 products is a Bluetooth module that provides a complete wireless solution with Bluetooth stack, integrated PWB antenna, and worldwide radio certifications in a compact surface-mount package.

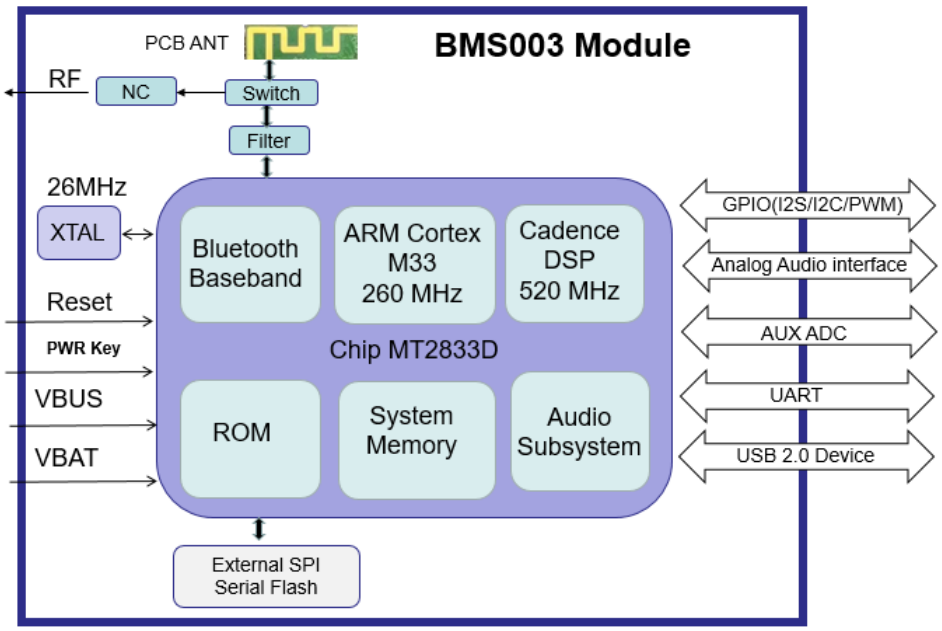
Applications

• Sound bar and Subwoofer (FW dependent)
• Bluetooth portable speaker phone
• Multi-speaker (FW dependent)
• Bluetooth headset

1. DEVICE OVERVIEW

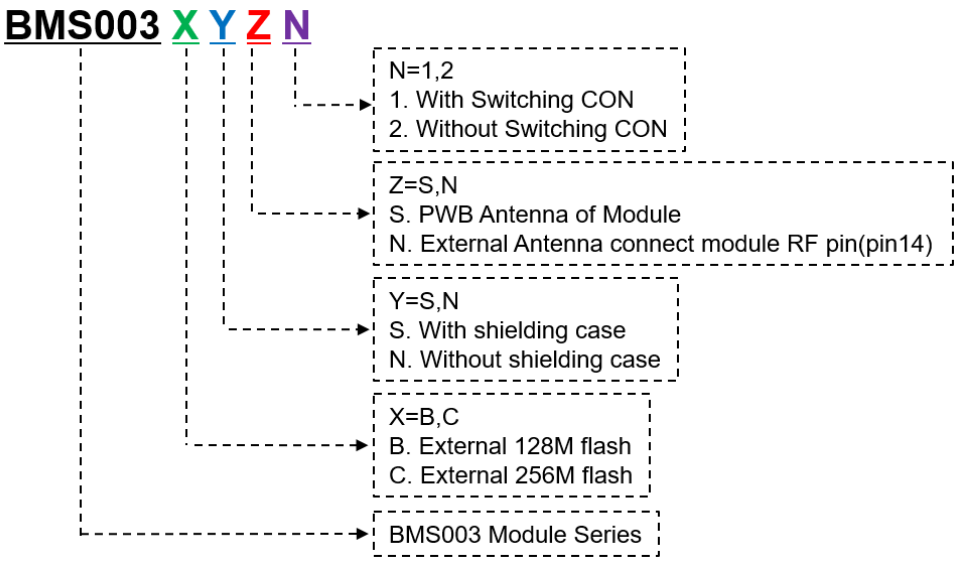
The BMS003 LEAudio modules built around AIROHA MT2833D SoC respectively. Module integrates the Bluetooth 5.3 dual- mode radio transceiver, Power Management Unit (PMU), a crystal and DSP. Users can configure the UI and DSP setting of BMS003 module by use a Windows-based tool.

1.1 Block Diagram



BMS003 module provides a fully compliant Bluetooth system to v5.3 of the specification for data and voice communications. The module and device's firmware is fully compliant with the Bluetooth specification V5.3. BMS003 module integrate a SPI serial flash up to 256Mbit, a master crystal frequency is 26MHz, shielding case (depending on needs) and diversifying interface.

1.2 BMS003 Module series



2. AUDIO CODEC

2.1 Auxiliary ADC Block description

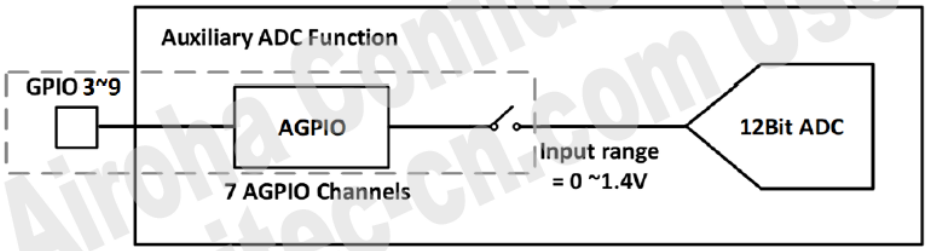


Figure 2.1-1 ADC Block Diagram

The auxiliary ADC includes the following functional blocks:

- Analog multiplexer. Selects signal from one of the seven auxiliary input pins. Real-world messages, such as temperature, are monitored and translated to the voltage domain.
- 12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

2.2 Audio uplink (Analog part)

The block diagram of audio uplink is illustrated below Figure 2.2-1. Audio uplink path is composed of PGA and audio ADC. The uplink front-end to PGA input can be configured as ACC differential and single-ended type. Besides, the ACC type has 10KΩ and 20KΩ input impedance for selection. The PGA gain range of differential mode is the 0~30dB per 6dB step and the ACC type of PGA can provide 3dB and 9dB gain option additionally. There are four input pairs of the uplink path that can be configured as AMIC.

- Four channel PGA and ADC analog MIC input
- VIN2P/N and VIN3P/N can be configured as Line-in mode
- High performance support: 100dB SNR and -90dB THD+N
- Normal performance support: 100dB SNR and -80dB THD+N
- Low-power performance support: 95dB SNR and -88dB THD+N
- Ultra-low power mode support: 90Db SNR and -80dB THD+N
- Analog Gain Rang is 0dB to 30dB of differential mode
- ACC mode input impedance of PGA: 10KΩ or 20KΩ
- VIN2P/N~VIN3P/N configuration: Differential or single-ended input

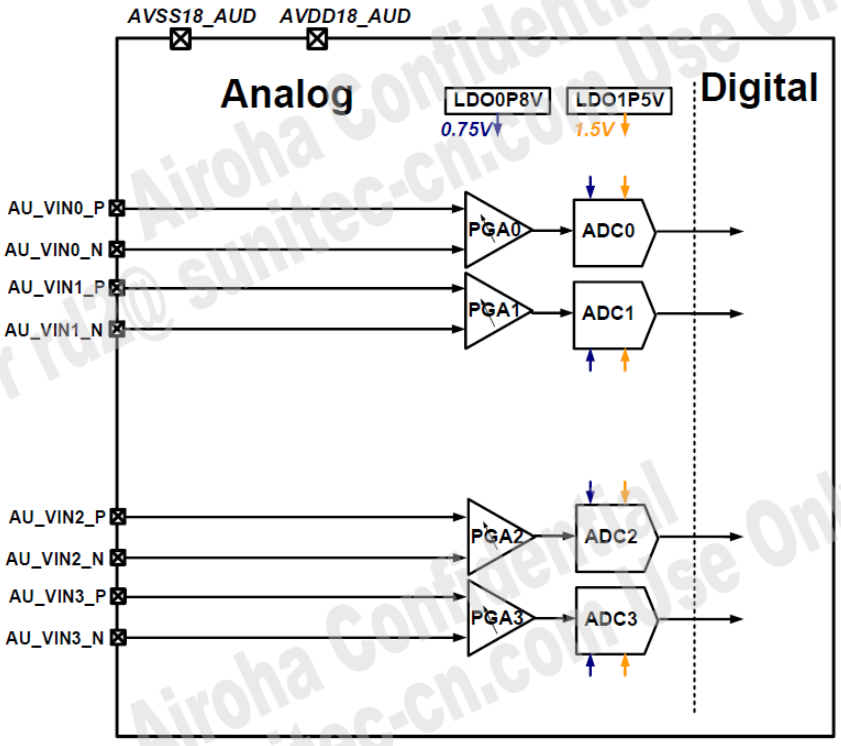


Figure 2.2-1 The Block Diagram of Audio Uplink (Analog part)

2.3 Audio downlink (Analog part)

Low-power MT2833D audio downlink includes stereo DACs and audio Class-G/D amplifiers for audio playback. The amplifiers is implemented with class-D and class-G mode The digital Class-G controller preview the maximum signal level of input digital LCH and RCH signals, and then adjust the power level up or down in advance before the signal is played. The fully differential headphone amplifiers can deliver up to 38mW into 16Ohm load. The class-G gain range of amplifier is -22dB to +8dB, 1dB/step. The class-D gain range of amplifier is -8dB to +4dB, 3dB/step. The VCM Tacker is embedded to generate an adaptive reference voltage for Class-G amplifier. AVDD18_AUD_DRV.The Capless LDOs are embedded in the audio downlink to enhance the power supply rejection ratio(PSRR).

- 38mW Stereo HP driver diff. output into 16Ohm
- High-performance mode support: -95dB THD and 110dB(A) SNR for HP output path
- Low-power music playback with Class-G Operation
- Ultra Low-power music playback with Class-D Operation
- Click-and-pop noise suppression of Class-G amplifiers <-80dBVpp
- Low output DC offset < 300uV

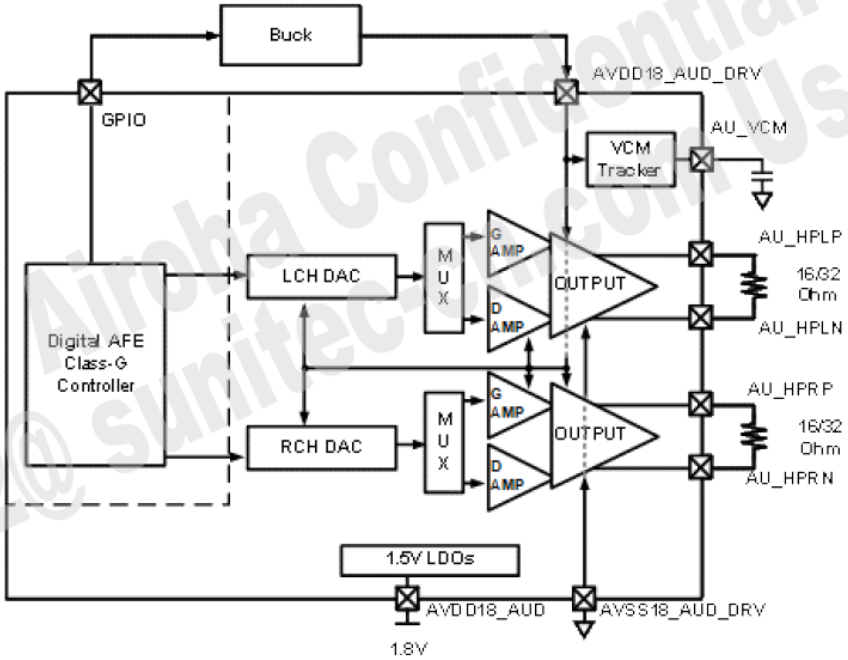


Figure 2.3-1 The Block Diagram of Audio Downlink (Analog part)

The proposed downlink path supports the following features:

- The data precisions in the downlink path are 24-bit data width.
- The supported input sample rates for downlink:
- 8K/11.025K/12K/16K/22.05K/24K/32K/44.1K/48K/96K/192K

2.4 Digital controller for Class-G amplifier

The Class-G amplifier is used for power saving of playback, and it can adjust the HP amplifier power rail according the audio content. The Class-G digital controller detects audio signal amplify and sends a control signal to buck converter through GPIO. When source swing goes high, the digital controller makes the Class-G amplifier change the DAC output from low-voltage to high-voltage state to avoid signal clipping. When source swing goes low, it has a configurable hold time control to prevent the Class-G amplifier from frequently adjusting the voltage. If the signal stays in a low state after a specific hold time, the digital controller sends a request to make the Class-G amplifier change the output from a high-voltage state to a low-voltage state. Otherwise, the output stays in a high-voltage state.

Figure 2.4-1 shows the block diagram of the Class-G digital controller. The audio digital Class-G path includes the following blocks: Preview FIFO, Frame Preview, EN-FSM, Hold Time control and DA signal generator. The EN-FSM module enables each voltage level in Class G. The Class-G input source is from the O_08 and O_09 (the same as downlink), which is defined in the audio interconnection. The output of DA Generator is sent to the analog DAC.

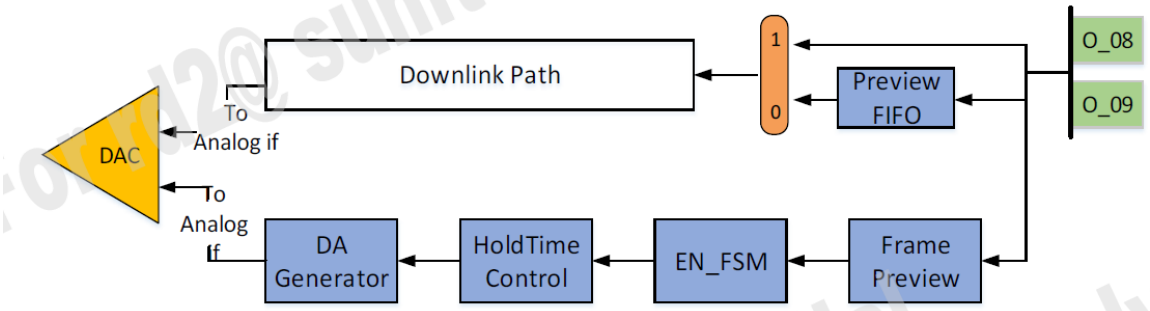


Figure 2.4-1 The Block Diagram of Class-G Amplifier Digital Part

The Class-G digital controller supports the following features:

- Support for the independent selection for Class-G amplifier high-voltage and low-voltage levels.
- Support for programmable high-voltage and low-voltage thresholds in the digital controller.
- Support for a programmable hold time in the digital controller to prevent frequently voltage switching.
- Built-in signal generator hardware for the DA signal request to the Class-G amplifier.

3. Power-on/off sequence

PMIC manages the power-on and power-off of the handset. If the battery voltage is neither in the UVLO state nor in the thermal condition, there are three methods to power on the handset system.

3.1 Pulling PWRKEY (CHIP_EN pull high)

Pushing PWRKEY (pulling the CHIP_EN pin to high level)
Pulling PWRKEY high is a typical method to turn on the handset. The system reset ends at the moment when all default-on regulators are sequentially turned on. After that, the MCU will send the PWRHOLD signal back to PMIC for acknowledgement. To successfully power on the handset, PWRKEY should be kept high until PMIC receives PWRHOLD from the MCU.

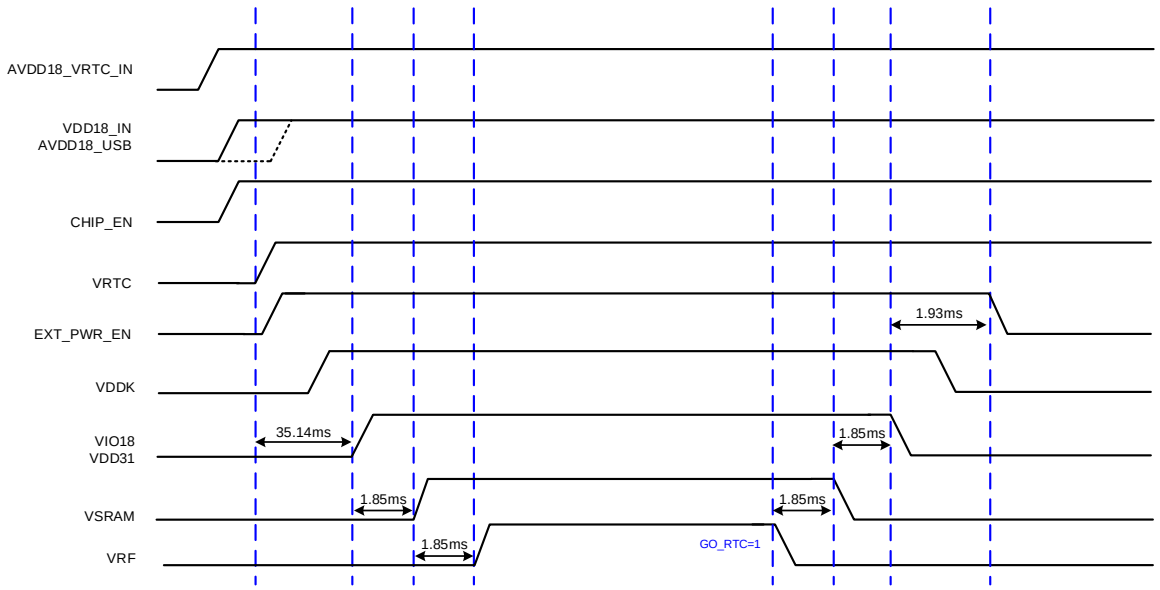


Figure 3.1-1 Power-on/off control sequence by press PWRKEY

Note: Those timings are typical values in regulator timing; timing variation is +/-50%

3.2 Valid charger plug-in

Valid charger plug-in (CHRIN voltage within valid range)
The charger plug-in will also turn on the handset if the charger is valid and VSYS > UVLO, the handset will also be powered on.

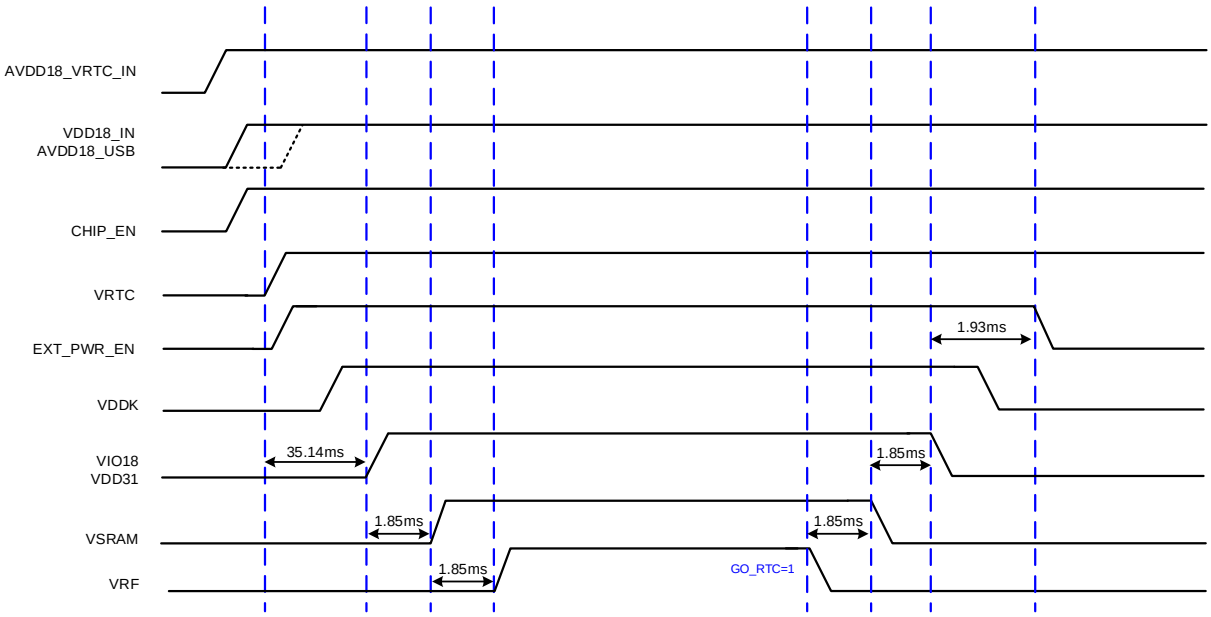


Figure 3.2-1 Power-on/off control sequence by charger plug-in

Note: Those timings are typical values in regulator timing; timing variation is +/-50%

4. Battery charge specification revision 1.2 (BC1.2)

4.1 Feature and description

USB charging port detection:

MT2833D BC1.2 charger detector is used to distinguish the different types of charger. This BC1.2 detector provide a capable method to determine several types of charging port which including Standard Downstream Ports (SDP), Charging Downstream Ports (CDP), Dedicated Charger Ports (DCP), Apple charger, non-standard charger. Typically, BC1.2 detection will execute immediately after the charger is plugged-in for charger input current limit configuration (The current limit setting please refer to the Charger's Datasheet). The BC1.2 detection circuits follow the "Battery Charging Specification Revision 1.2", please refer to this specification for detailed charger detection flow.

4.2 Functional block

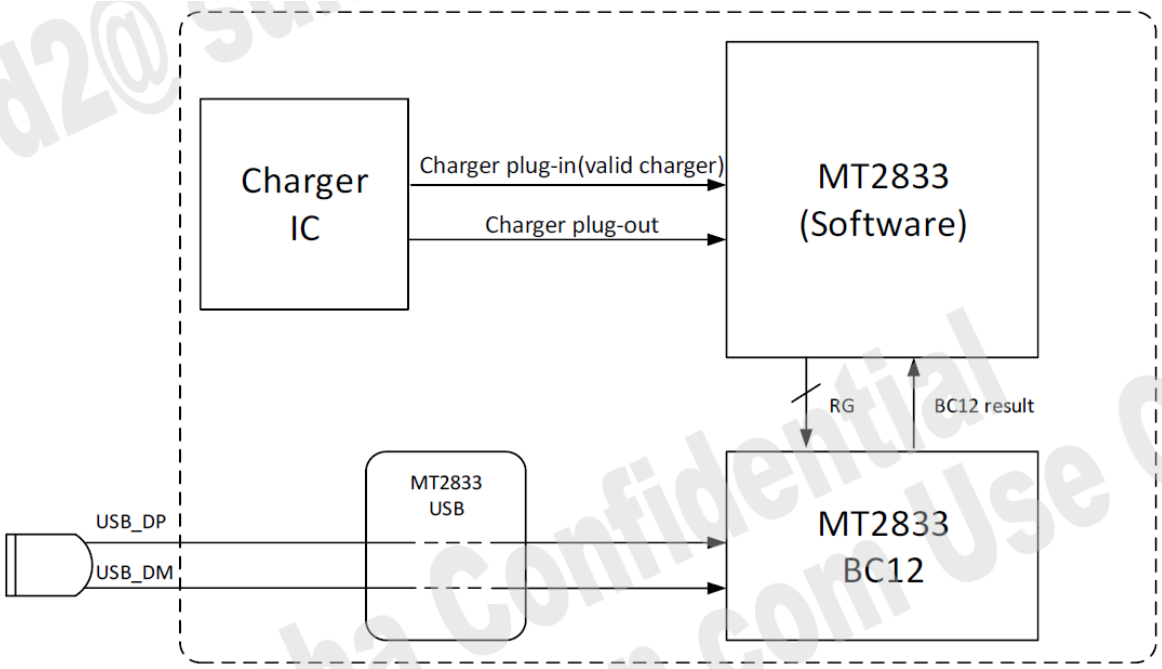


Figure 4.2-1 BC1.2 function block diagram

4.3 Linear Battery Charging

- Input current limit: 1.0A
- Power Path Management for Powering the System and Charging the Battery
- 24V Maximum Rating for VBUS Power
- JEITA Charge Protection
- NTC Thermistor Input
- Supports up to 0.5-A Charge Current with Current Monitoring Output (ISET)
- Programmable fast charging mode

5. Bluetooth RF Subsystem

5.1 Bluetooth description

The MT2833 series Bluetooth (BT) RF subsystem (as shown in ***Figure 5.1-1***) consists of a highly integrated transceiver with tunable on-chip RF band pass filter (BPF) and BT TRX co-matching network.

MT2833 series adopts a low intermediate frequency (LIF) receiver architecture. The receiver, including the on-chip RF BPF and TRX co-matching network, consists of a LNA and single balanced passive mixer, a complex BPF and a pair of 10-bit SAR ADCs.

The direct conversion transmitter consists of a pair of 10-bit current DACs and passive LPFs, an active IQ modulator(IQM) and a Class AB push-pull PA. This PA is capable of transmitting +11dBm power for enhanced data rate(EDR) and +15dBm for basic data rate(BDR).

The Δ-Σ fractional-N RF synthesizer is phase locked to 26MHz reference clock to generate the RF LO frequency. The BBPLL generates sampling clock for ADC and DAC as well as digital clock to BT modem.

MT2833 series implements various automatic calibration schemes to minimize changes in RF performance from chip-to-chip and temperature variations.

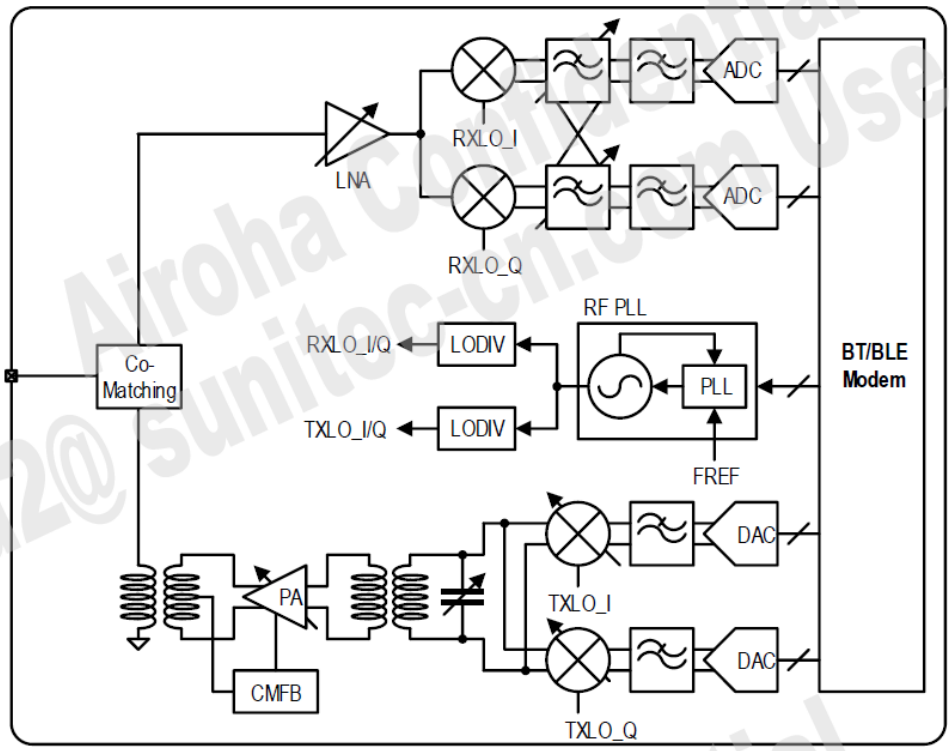


Figure 5.1-1 BC1.2 Bluetooth RF transceiver system

5.2 Functional specifications

Typical RF performances are specified for mid. channel, TA = +25℃, and under recommended operating conditions, unless stated otherwise.

Table 5.2-1 Recommended operating conditions

Description	Condition	Min	Typical	Max	Unit
AVDD_VPA Supply			1.8		V
AVDD_BTRF Supply			0.9		V
AVDD_DCXO Supply			0.9		V

5.3 Basic data rate – Receiver & Transmitter specifications

Items	Rate	Units	Min	Typ	Max
Frequency Range	--	MHZ	2402	--	2480
RF AVG Maximum Output Power	GFSK	dBm	6	8	10
RF Peak Maximum Output Power	GFSK	dBm	--	--	10
RF Maximum Power Control gain step Range	GFSK	dBm	2	4	8
RF Maximum Receiver Sensitivity@ BER＜0.1%	GFSK	dBm	-97	-95	-70
Maximum detectable input power @ BER＜0.1%	GFSK	dBm	-20	-5	-
Crystal Frequency Calibration	--	KHz	-5	0	5
Modulation Characteristics（Delta F1 Avg）	--	KHz	140	157	175
Carrier Frequency Drift	GFSK	KHz	-40	0	40

5.4 Enhanced data rate –Receiver & Transmitter specifications

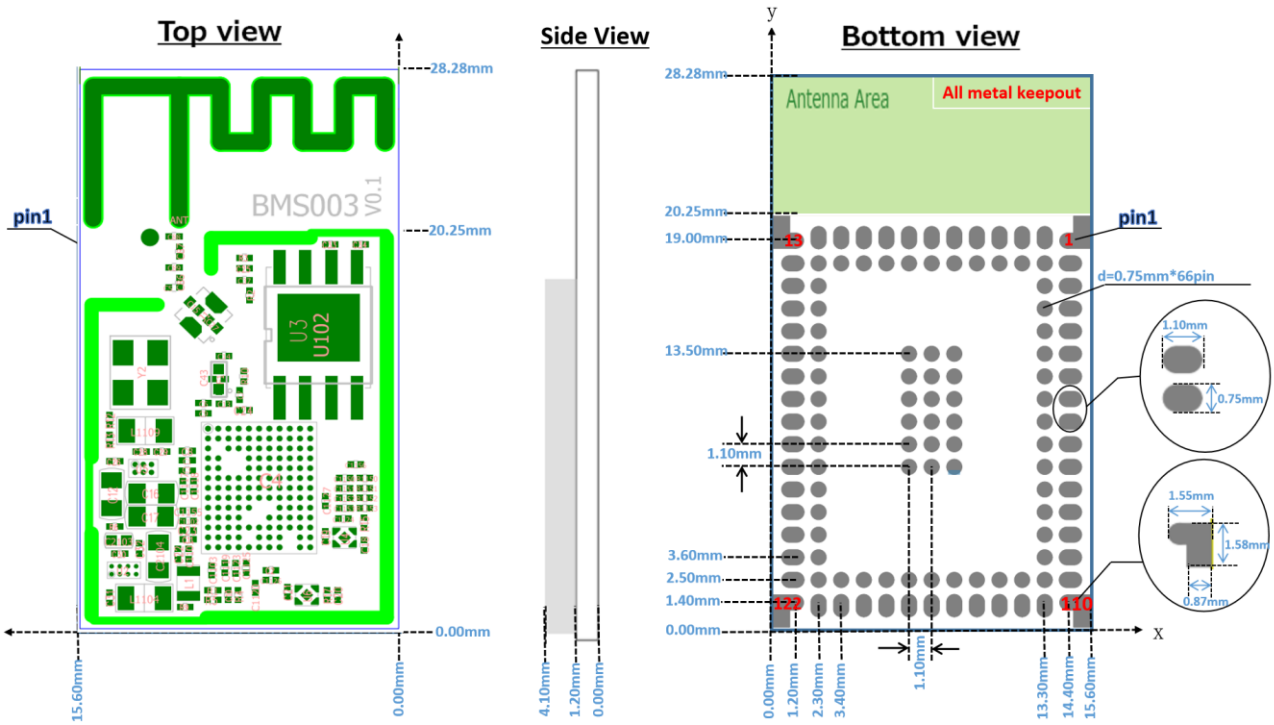
Items	Rate	Units	Min	Typ	Max
Frequency Range	--	MHZ	2402	--	2480
RF AVG Maximum Output Power	π/4 DQPSK	dBm	4	6	8
	8DPSK	dBm	4	6	8
RF Peak Maximum Output Power	π/4 DQPSK	dBm	--	--	10
	8DPSK	dBm	--	--	10
RF Maximum Power Control gain step Range	π/4 DQPSK	dBm	2	4	8
	8DPSK	dBm	2	4	8
RF Maximum Receiver Sensitivity@ BER＜0.01%	π/4 DQPSK	dBm	−97	−95	−70
	8DPSK	dBm	−91	−89	−70
Maximum detectable input power @ BER＜0.01%	π/4 DQPSK	dBm	−20	−5	
	8DPSK	dBm	−20	−5	
Frequency stability ω0	π/4 DQPSK	KHz	−10	4	10
	8DPSK	KHz	−10	4	10
Frequency stability ω1	π/4 DQPSK	KHz	−75	20	75
	8DPSK	KHz	−75	20	75
|ω0+ω1|	π/4 DQPSK	KHz	−75	20	75
	8DPSK	KHz	−75	20	75
Crystal Frequency Calibration	--	KHz	−5	0	5

5.5 Bluetooth LE –Receiver & Transmitter specifications

Items	Rate	Units	Min	Typ	Max
Frequency Range	--	MHZ	2402	--	2480
Maximum Output Power	1M	dBm	2	4	6
	2M	dBm	2	4	6
Maximum Receiver Sensitivity@ PER＜30.8%	1M	dBm	−100	−98	−70
	2M	dBm	−97	−95	−70
Maximum detectable input power @ PER＜30.8%	1M	dBm	−10	−5	−
	2M	dBm	−10	−5	
Crystal Frequency Calibration	--	KHz	−5	0	5
Modulation Characteristics(Delta F1 Avg)	1M	KHz	235	250	265
	2M	KHz	450	500	550
Carrier Frequency Drift	--	KHz	−50	5	50

6. Module Description

6.1 BMS003 module structure



Tolerances:
PWB Thickness: ±0.16mm
Note: PWB Dimensions: X: 15.6mm, Y: 28.28mm and tolerances:±0.5mm

6.2 BMS003 module pin diagram

Pin NO.	13	12	11	10	9	8	7	6	5	4	3	2	1
Pin Name	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
Pin NO.	26	25	24	23	22	21	20	19	18	17	16	15	14
Pin Name	GPIO54	GPIO56	GPIO19	GPIO55	GPIO4	GPIO0	GPIO7	GPIO1	GPIO10	GND	GND	GND	RF
Pin NO.	30	29										28	27
Pin Name	GPIO16	GPIO51										GND	GND
Pin NO.	34	33										32	31
Pin Name	GPIO17	GPIO45										GPIO27	GPIO35
Pin NO.	38	37										36	35
Pin Name	GPIO18	GPIO52										GPIO44	GPIO40
Pin NO.	45	44				43	42	41				40	39
Pin Name	GPIO15	GPIO53				GND	GND	GND				GPIO47	GPIO25
Pin NO.	52	51				50	49	48				47	46
Pin Name	GPIO14	GPIO46				GND	GND	GND				GPIO48	GPIO26
Pin NO.	59	58				57	56	55				54	53
Pin Name	GPIO13	GPIO20				GND	GND	GND				GPIO42	GPIO34
Pin NO.	66	65				64	63	62				61	60
Pin Name	GPIO33	GPIO23				GND	GND	GND				GPIO28	GPIO36
Pin NO.	73	72				71	70	69				68	67
Pin Name	GPIO32	GPIO22				GND	GND	GND				GPIO38	GPIO39
Pin NO.	80	79				78	77	76				75	74
Pin Name	GPIO37	GPIO29				GND	GND	GND				GPIO49	GPI43
Pin NO.	84	83										82	81
Pin Name	AU_VIN3N	GPIO31										GPIO50	GPI41
Pin NO.	88	87										86	85
Pin Name	AU_VIN3P	AU_HPRP										GPIO3	GPIO40
Pin NO.	92	91										90	89
Pin Name	AU_VIN2N	AU_HPRN										GPIO2	DVDD_IO_0
Pin NO.	96	95										94	93
Pin Name	AU_VIN2P	AU_HPLN										GPIO9	VDDK_SEL
Pin NO.	109	108	107	106	105	104	103	102	101	100	99	98	97
Pin Name	AU_VIN1N	AU_HPLP	GPIO24	GPIO21	GPIO11	GPIO12	RTC_GPIO3	RTC_GPIO1	RTC_GPIO0	RTC_GPIO1	GPIO8	GPIO57	AVDD18_VRTC_IN
Pin NO.	122	121	120	119	118	117	116	115	114	113	112	111	110
Pin Name	AU_VIN1P	AU_VINON	AU_VINOP	GPIO5	USB_DM	USB_DP	GPIO6	CHIP_EN	VAUDIO18	VIO18	VDD18_BUCK	VDD31_USB	VBAT

6.3 BMS003 module pin function description and power domain

Pin No.	Pin Type	Pull-Type	Power domain	Pin Name	Description
1	P	-	-	GND	Ground reference
2	P	-	-	GND	Ground reference
3	P	-	-	GND	Ground reference
4	P	-	-	GND	Ground reference
5	P	-	-	GND	Ground reference
6	P	-	-	GND	Ground reference
7	P	-	-	GND	Ground reference
8	P	-	-	GND	Ground reference
9	P	-	-	GND	Ground reference
10	P	-	-	GND	Ground reference
11	P	-	-	GND	Ground reference
12	P	-	-	GND	Ground reference
13	P	-	-	GND	Ground reference
15	P	-	-	GND	Ground reference
16	P	-	-	GND	Ground reference
17	P	-	-	GND	Ground reference
27	P	-		GND	Ground reference
28	P	-		GND	Ground reference
41	P	-	-	GND	Ground reference
42	P	-	-	GND	Ground reference
43	P	-	-	GND	Ground reference
48	P	-	-	GND	Ground reference
49	P	-	-	GND	Ground reference
50	P	-	-	GND	Ground reference
55	P	-	-	GND	Ground reference
56	P	-	-	GND	Ground reference
57	P	-	-	GND	Ground reference
62	P	-	-	GND	Ground reference
63	P	-	-	GND	Ground reference
64	P	-	-	GND	Ground reference
69	P	-	-	GND	Ground reference
70	P	-	-	GND	Ground reference
71	P	-	-	GND	Ground reference
76	P	-	-	GND	Ground reference
77	P	-	-	GND	Ground reference
78	P	-	-	GND	Ground reference
14	AI	-	-	BT_RFIN	Bluetooth 50 ohm transmitter output and receiver input
21	DIO	PD	DVDD_IO_0	GPIO0	General purpose input/output, Pin 0 Alternate Pin Functions: ■ CM33 JTAG ■ I2C(0) ■ CTP
19	DIO	PD	DVDD_IO_0	GPIO1	General purpose input/output, Pin 1 Alternate Pin Functions: ■ CM33 JTAG ■ I2C(0) ■ CTP
90	DIO	PD	DVDD_IO_0	GPIO2	General purpose input/output, Pin 2 Alternate Pin Functions: ■ DSP JTAG ■ I2S master (0) ■ I2S slave (2) ■ CTP
86	DIO	PD	DVDD_IO_0	GPIO3	General purpose input/output, Pin 3 Alternate Pin Functions: ■ DSP JTAG ■ I2S master (0) ■ I2S slave (2) ■ CTP
22	DIO	PD	DVDD_IO_0	GPIO4	General purpose input/output, Pin 4 Alternate Pin Functions:

					■ DSP JTAG ■ I2S master (0) ■ I2S slave (2) ■ AUX_ADC
119	DIO	PD	DVDD_IO_0	GPIO5	General purpose input/output, Pin 5 Alternate Pin Functions: ■ DSP JTAG ■ I2S master (0) ■ DMIC (0) ■ AUX_ADC
116	DIO	PD	DVDD_IO_0	GPIO6	General purpose input/output, Pin 6 Alternate Pin Functions: ■ DSP JTAG ■ DMIC (0) ■ I2S master (0) ■ I2S slave (2) ■ AUX_ADC
20	DIO	PD	DVDD_IO_0	GPIO7	General purpose input/output, Pin 7 Alternate Pin Functions: ■ UART(2) ■ AUXADC
99	DIO	PD	DVDD_IO_0	GPIO8	General purpose input/output, Pin 8 Alternate Pin Functions: ■ UART(2) ■ AUXADC
94	DIO	PD	DVDD_IO_0	GPIO9	General purpose input/output, Pin 9 Alternate Pin Functions: ■ UART(1) ■ PWM ■ AUXADC
18	DIO	PD	DVDD_IO_0	GPIO10	General purpose input/output, Pin 10 Alternate Pin Functions: ■ UART(1) ■ PWM
105	DIO	PD	DVDD_IO_0	GPIO11	General purpose input/output, Pin 11 Alternate Pin Functions: ■ UART(0) ■ PWM
104	DIO	PD	DVDD_IO_0	GPIO12	General purpose input/output, Pin 12 Alternate Pin Functions: ■ UART(0)
59	DIO	Hi-Z	DVDD_IO_1	GPIO13	General purpose input/output, Pin 13 Alternate Pin Functions: ■ UART(1) ■ PWM ■ I2C(0) ■ IRRX
52	DIO	PD	DVDD_IO_1	GPIO14	General purpose input/output, Pin 14 Alternate Pin Functions: ■ UART(1) ■ PWM ■ I2C(0) ■ I2S_master（0）
45	DIO	PD	DVDD_IO_1	GPIO15	General purpose input/output, Pin 15 Alternate Pin Functions: ■ I3C(1) ■ PWM ■ I2C(1) ■ I2S_master（0） ■ I2S_master（1） ■ CLK03
30	DIO	PD	DVDD_IO_1	GPIO16	General purpose input/output, Pin 16 Alternate Pin Functions: ■ I3C(1) ■ I2C(1) ■ I2S_master（0）

					■ I2S_master（1） ■ I2S_slave（1）
34	DIO	PD	DVDD_IO_1	GPIO17	General purpose input/output, Pin 17 Alternate Pin Functions: ■ I3C(1) ■ I3C(0) ■ I2C(2) ■ I2S_master（0） ■ I2S_master（1） ■ I2S_slave（1） ■ CM33_JTAG
38	DIO	PD	DVDD_IO_1	GPIO18	General purpose input/output, Pin 18 Alternate Pin Functions: ■ I3C(1) ■ I3C(0) ■ I2C(2) ■ I2S_master（0） ■ I2S_master（1） ■ I2S_slave（1） ■ CM33_JTAG
24	DIO	HIGH	DVDD_IO_1	GPIO19	General purpose input/output, Pin 19 Alternate Pin Functions: ■ MSDC(0) ■ ESC ■ SPI Slave(0) ■ SPI Master(0) ■ UART(0) ■ CLK01
58	DIO	PD	DVDD_IO_0	GPIO20	General purpose input/output, Pin 20 Alternate Pin Functions: ■ MSDC(0) ■ ESC ■ SPI Slave(0) ■ SPI Master(0) ■ UART(0)
106	DIO	PD	DVDD_IO_0	GPIO21	General purpose input/output, Pin 21 Alternate Pin Functions: ■ MSDC(0) ■ ESC ■ SPI Slave(0) ■ SPI Master(0) ■ UART(0)
72	DIO	PD	DVDD_IO_0	GPIO22	General purpose input/output, Pin 22 Alternate Pin Functions: ■ MSDC(0) ■ ESC ■ SPI Slave(0) ■ SPI Master(0) ■ UART(0)
65	DIO	PD	DVDD_IO_0	GPIO23	General purpose input/output, Pin 23 Alternate Pin Functions: ■ MSDC(0) ■ ESC ■ SPI Slave(0) ■ SPI Master(0)
107	DIO	PD	DVDD_IO_0	GPIO24	General purpose input/output, Pin 24 Alternate Pin Functions: ■ MSDC(0) ■ ESC ■ SPI Slave(0) ■ SPI Master(0) ■ I2S_master（0） ■ I2S_slave（3）
39	DIO	PD	DVDD_IO_0	GPIO25	General purpose input/output, Pin 25 Alternate Pin Functions: ■ MSDC(0)

					■ I2S_master（0） ■ I2S_slave（3） ■ CLK02 ■ SPDIF ■ Pull high to enter USB download mode
46	DIO	PD	DVDD_IO_0	GPIO26	General purpose input/output, Pin 26 Alternate Pin Functions: ■ I2S_master (1) ■ I2S_slave（1）
32	DIO	PD	DVDD_IO_0	GPIO27	General purpose input/output, Pin 27 Alternate Pin Functions: ■ I2S Master(0) ■ I2S Slave(0) ■ SPI Master(1) ■ PWM
61	DIO	PD	DVDD_MC0	GPIO28	General purpose input/output, Pin 28 Alternate Pin Functions: ■ I2S Master(1) ■ I2S Slave(3) ■ SPI Master(1) ■ PWM
79	DIO	PD	DVDD_IO_1	GPIO29	General purpose input/output, Pin 29 Alternate Pin Functions: ■ I2S Master(2) ■ I2S Slave(4) ■ SPI Master(1) ■ PWM ■ SPDIF
35	DIO	PD	DVDD_IO_0	GPIO30	General purpose input/output, Pin 30 Alternate Pin Functions: ■ I2S Master(0) ■ I2S Slave(0) ■ SPI Master(1) ■ PWM
83	DIO	PD	DVDD_IO_0	GPIO31	General purpose input/output, Pin 31 Alternate Pin Functions: ■ I2S Master(2) ■ I2S Slave(1) ■ SPI Master(1) ■ PWM
73	DIO	PD	DVDD_IO_0	GPIO32	General purpose input/output, Pin 32 Alternate Pin Functions: ■ I2S Master(2) ■ I2S Slave(1) ■ SPI Master(1) ■ PWM
66	DIO	PD	DVDD_MC0	GPIO33	General purpose input/output, Pin 33 Alternate Pin Functions: ■ I2S Master(2) ■ I2S Slave(1) ■ SPI Master(1) ■ PWM
53	DIO	PD	DVDD_IO_0	GPIO34	General purpose input/output, Pin 34 Alternate Pin Functions: ■ I2S Master(1) ■ I2S Slave(2) ■ SPI Master(2) ■ PWM ■ DSP JTAG
31	DIO	PD	DVDD_IO_0	GPIO35	General purpose input/output, Pin 35 Alternate Pin Functions: ■ I2S Master(0) ■ I2S Slave(0) ■ SPI Master(2) ■ DSP JTAG

60	DIO	PD	DVDD_IO_0	GPIO36	General purpose input/output, Pin 36 Alternate Pin Functions: ■ I2S Master(1) ■ I2S Slave(3) ■ SPI Master(2) ■ DMIC(0)
80	DIO	PD	DVDD_IO_0	GPIO37	General purpose input/output, Pin 37 Alternate Pin Functions: ■ I2S Master(2) ■ I2S Slave(4) ■ SPI Master(2) ■ DMIC(0) ■ PWM
68	DIO	PD	DVDD_IO_0	GPIO38	General purpose input/output, Pin 38 Alternate Pin Functions: ■ I2S Master(3) ■ I2S Slave(3) ■ SPI Master(2) ■ SPDIF_RX ■ PWM
67	DIO	PD	DVDD_IO_0	GPIO39	General purpose input/output, Pin 39 Alternate Pin Functions: ■ I2S Master(3) ■ I2S Slave(4) ■ SPI Master(2) ■ DMIC(1) ■ PWM
85	DIO	PD	DVDD_IO_0	GPIO40	General purpose input/output, Pin 40 Alternate Pin Functions: ■ I2S Master(3) ■ I2S Slave(4) ■ SPI Master(1) ■ DMIC(1)
81	DIO	PD	DVDD_IO_0	GPIO41	General purpose input/output, Pin 41 Alternate Pin Functions: ■ I2S Master(3) ■ I2S Slave(2) ■ SPI Master(1) ■ DMIC(0) ■ PWM
54	DIO	PD	DVDD_IO_0	GPIO42	General purpose input/output, Pin 42 Alternate Pin Functions: ■ I2S Master(1) ■ I2S Slave(2) ■ SPI Master(1) ■ DMIC(0) ■ PWM
74	DIO	PD	DVDD_IO_0	GPIO43	General purpose input/output, Pin 43 Alternate Pin Functions: ■ I2S Master(3) ■ I2S Slave(2) ■ SPI Master(1) ■ DMIC(1) ■ DSP_JTAG
36	DIO	PD	DVDD_IO_0	GPIO44	General purpose input/output, Pin 44 Alternate Pin Functions: ■ SPI Master(1) ■ CLKO0 ■ DSP_JTAG
33	DIO	PD	DVDD_IO_0	GPIO45	General purpose input/output, Pin 45 Alternate Pin Functions: ■ SPI Master(2) ■ DSP_JTAG
51	DIO	PD	DVDD_IO_0	GPIO46	General purpose input/output, Pin 46 Alternate Pin Functions: ■ SPI Master(2) ■ DSP_JTAG

40	DIO	PD	DVDD_IO_0	GPIO47	General purpose input/output, Pin 47 Alternate Pin Functions: ■ UART(2) ■ I2C(0) ■ I2C(2) ■ I3C(0)
47	DIO	PD	DVDD_IO_0	GPIO48	General purpose input/output, Pin 48 Alternate Pin Functions: ■ UART(2) ■ I2C(0) ■ I2C(2) ■ I3C(0)
75	DIO	PD	DVDD_IO_0	GPIO49	General purpose input/output, Pin 49 Alternate Pin Functions: ■ UART(1) ■ I2C(1) ■ I2C(2) ■ I3C(1)
82	DIO	PD	DVDD_IO_0	GPIO50	General purpose input/output, Pin 50 Alternate Pin Functions: ■ UART(1) ■ I2C(1) ■ I2C(2) ■ I3C(1)
29	DIO	PD	DVDD_IO_0	GPIO51	General purpose input/output, Pin 51 Alternate Pin Functions: ■ CLKO0 ■ SPI Master (2)
37	DIO	PD	DVDD_IO_0	GPIO52	General purpose input/output, Pin 52 Alternate Pin Functions: ■ PWM ■ SPI Master (2)
44	DIO	PD	DVDD_IO_0	GPIO53	General purpose input/output, Pin 53 Alternate Pin Functions: ■ IRRX ■ SPI Master (2)
26	DIO	PD	DVDD_IO_0	GPIO54	General purpose input/output, Pin 54 Alternate Pin Functions: ■ SPI Master (1) ■ SPI Master (2)
23	DIO	PD	DVDD_IO_0	GPIO55	General purpose input/output, Pin 55 Alternate Pin Functions: ■ SPI Master (1) ■ SPI Master (2)
25	DIO	PD	DVDD_IO_0	GPIO56	General purpose input/output, Pin 54 Alternate Pin Functions: ■ SPI Master (1) ■ USB
98	DIO	PD	DVDD_IO_0	GPIO57	General purpose input/output, Pin 54 Alternate Pin Functions: ■ SPI Master (1) ■ USB
101	DIO	Hi-Z	VDIG18	RTC_GPIO0	RTC GPIO0
100	DIO	Hi-Z	VDIG18	RTC_GPIO1	RTC GPIO 1
102	DIO	Hi-Z	VDIG18	RTC_GPIO2	RTC GPIO 2
103	DIO	Hi-Z	VDIG18	RTC_GPIO3	RTC GPIO 3
115	AI	-	VDD18_VRTC_IN	CHIP_EN	PWRKEY Button
108	AO	-	AVDD18_AUD_DRV	AU_HPLP	Headphone L-ch P-side
95	AO	-	AVDD18_AUD_DRV	AU_HPLN	Headphone L-ch N-side
91	AO	-	AVDD18_AUD_DRV	AU_HPRN	Headphone R-ch N-side
87	AO	-	AVDD18_AUD_DRV	AU_HPRP	Headphone R-ch P-side
120	AI	-	-	AU_VIN0_P	Audio input CH0 P-side

121	AI	-	-	AU_VIN0_N	Audio input CH0 N-side
122	AI	-	-	AU_VIN1_P	Audio input CH1 P-side
109	AI	-	-	AU_VIN1_N	Audio input CH1 N-side
96	AI	-	-	AU_VIN2_P	Audio input CH2 P-side
92	AI	-	-	AU_VIN2_N	Audio input CH2 N-side
88	AI	-	-	AU_VIN3_P	Audio input CH3 P-side
84	AI	-	-	AU_VIN3_N	Audio input CH3 N-side
110	P	input	-	VBAT	Battery connection. Connect VBAT to the positive terminal of battery.
97	I	output	VBAT	AVDD18_VRTC_IN	PMU supply
89	P	input	-	DVDD_IO_0	Power input of GPIO group 0
93	P	input	-	VDDK_SEL	VCORE power switch default low
111	P	output	VBAT	VDD31_USB	VLDO33 output voltage
113	P	output	-	VIO18	Buck VIO18, 1V8 power output, max130mA.
114	P	input	-	VAUDIO18	DAC Power supply input.
112	P	output	-	VDD18_BUCK	DC-DC Buck VDD18, 1V8 power output, max500mA
117	AIO	-	VDD31_USB	USB_DP	USB signal DP
118	AIO	-	VDD31_USB	USB_DM	USB signal DN

7. Antenna of BMS003 Module

7.1 Recommended for PWB Antenna design

Around of the PWB Antenna should keep out of metal over 15mm, so that RF have a good performance, show as ***Figure 7.1-1***

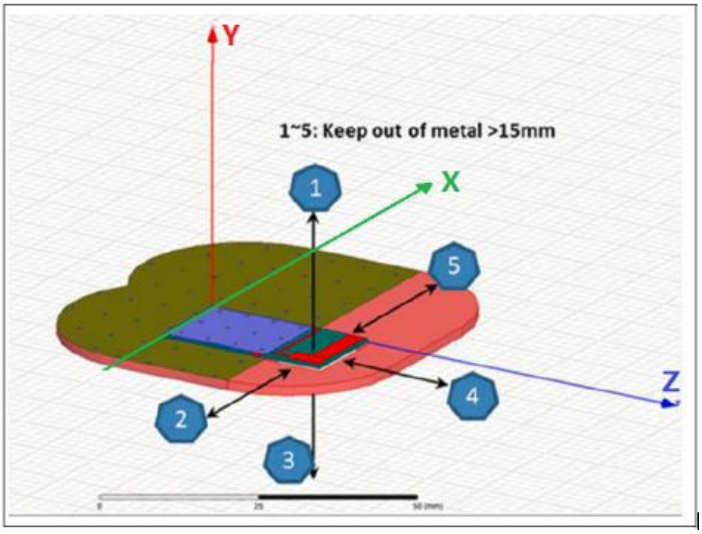


Figure 7.1-1 BMS003 PWB ANT design

7.2 Module Placement Guidelines

For a Bluetooth-enabled product, the antenna placement affects the overall performance of the system. The antenna requires free space to radiate RF signals and it must not be surrounded by the ground plane. Recommend that the areas underneath the antenna on the host PWB must not contain copper on top, inner, or bottom layers, as illustrated in ***Figure 7.2-2***.

A low-impedance ground plane will ensure the best radio performance (best range, lowest noise). The ground plane can be extended beyond the minimum recommendation, as required for the main PWB EMC noise reduction. For the best range performance, keep all external metal at least 15 mm away from the on-board PWB trace antenna.

Figure 7.2-1 illustrate examples of good and poor placement of the BMS003 module on a host board with GND plane.

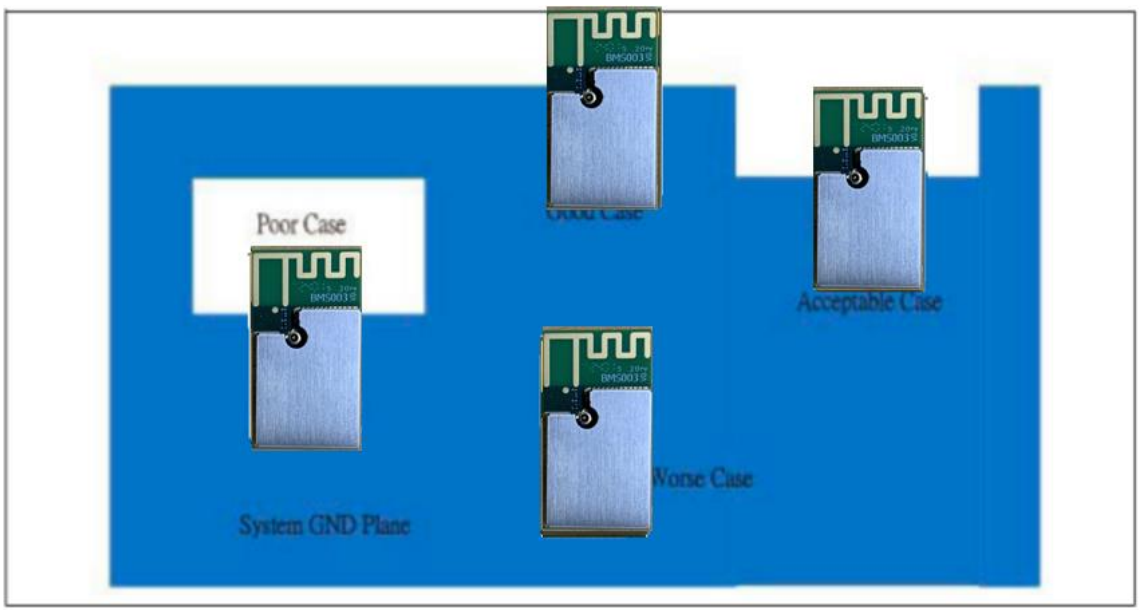


Figure 7.2-1

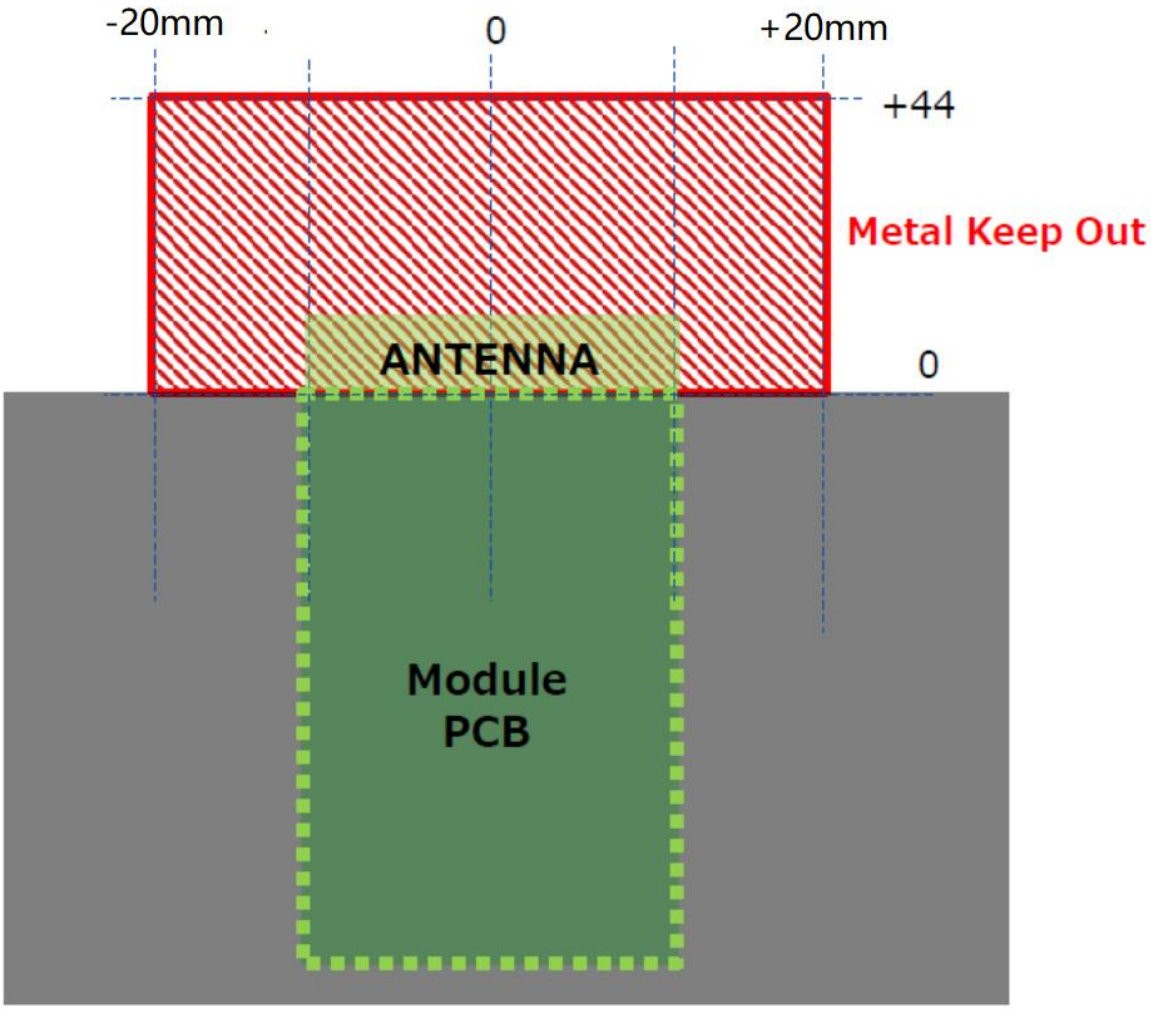


Figure 7.2-2 Recommended PWB footprint of BMS003 module

8. Electrical Characteristics

This section provides an overview of the BMS003 LEAudio module electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the BMS003 module are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification is not implied.

8.1 Module Power Consumption (Vcore =0.8V)

Table 8.1-1 BMS003 power consumption

Module base on Sunitec BMS003 EVB		
Condition：TA = +25℃ , Vcore=0.8V		
Mode	Power Consumption (mA)	
BT Pairing mode	Max.	4.65
	Avg.	3.88
	Min.	2.20
Connected mode	Max.	4.2
	Avg.	3.46
	Min.	3.2
Disconnect mode	Max.	5.0
	Avg.	3.62
	Min.	3.35
Reconnecting mode	Max.	5.2
	Avg.	3.82
	Min.	2.89
BT SBC streaming mode （Play 1KHZ 0dB）	Max.	8.03
	Avg.	7.03
	Min.	5.58
BT SBC streaming mode （Play Silence tone）	Max.	7.95
	Avg.	6.23
	Min.	5.38
AUX in mode	Max.	8.35
	Avg.	6.94
	Min.	6.43
Call active mode	Max.	17.54
	Avg.	13.84
	Min.	10.42

Note:

1. BT Firmware: FW_ER3_speaker_ref_design_20240111_TEST1
2. BT Codec： SBC
3. The current consumption values are measured with the BMS003 EVB as test platform, with BAT_IN = 3.89V. The Distance between the smartphone and BMS003 EVB is 30cm, and the speaker is without loading.

8.2 Module Power Supply

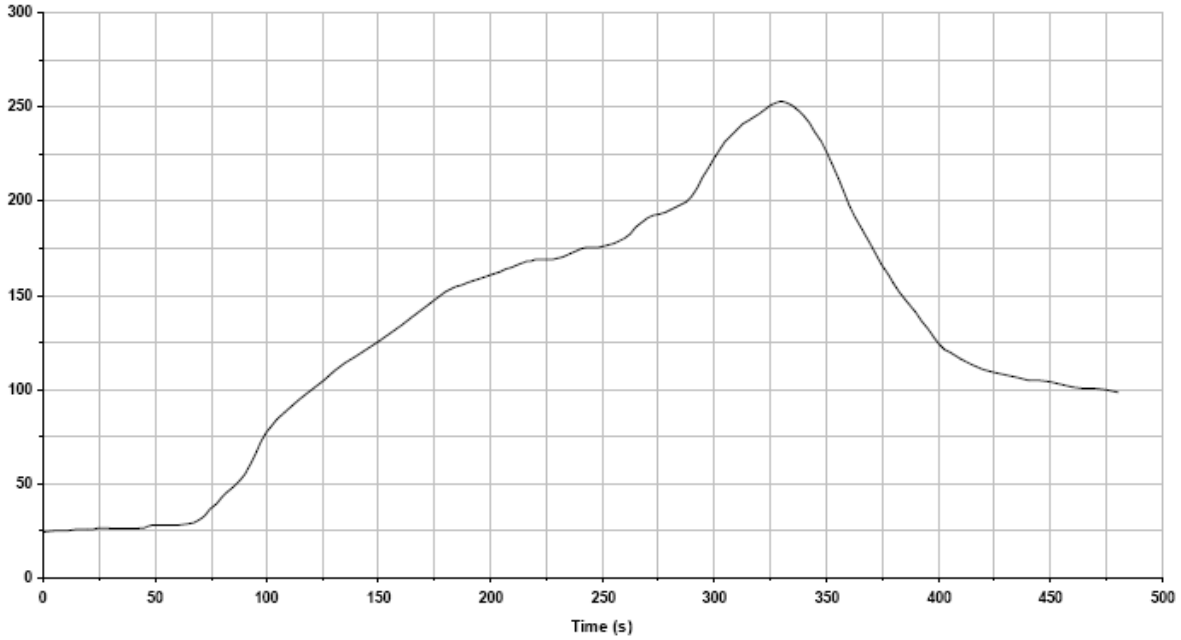
Table 8.2-1 operating conditions

Recommended Operating Conditions	Min	Max
Operating Temperature Range	-20°C	+70°C
Supply Voltage, (VBAT)	+3.0V	+5.0V
VSYS Voltage (VSYS)	+3.0V	+4.8V
Supply Voltage, (VBUS)	+4.1V	+7.2V
Power key（High voltage）	0.7 * AVDD50	--
Power key（Low voltage）	--	0.3 * AVDD50
SYSRSTB （High voltage）	0.7 * VIO	--
SYSRSTB （Low voltage）	--	0.3 * VIO

Table 8.2-2 Absolute Maximum rate conditions

Absolute Maximum rate Conditions	Min	Max
Operating Temperature Range	-55°C	+125°C
Supply Voltage, (VBAT)	-0.5V	+6.0V
VSYS Voltage (VSYS)	-0.5V	+6.0V
Power supply for GPIO group (DVDD_IO_0-1)	+1.62V	+3.63V
Supply Voltage, (VBUS)	-0.5V	+24V
Digital input voltage for IO type（VIN0-VIN3））	-0.5V	+3.63V

9. Recommended Reflow Temperature Profile:

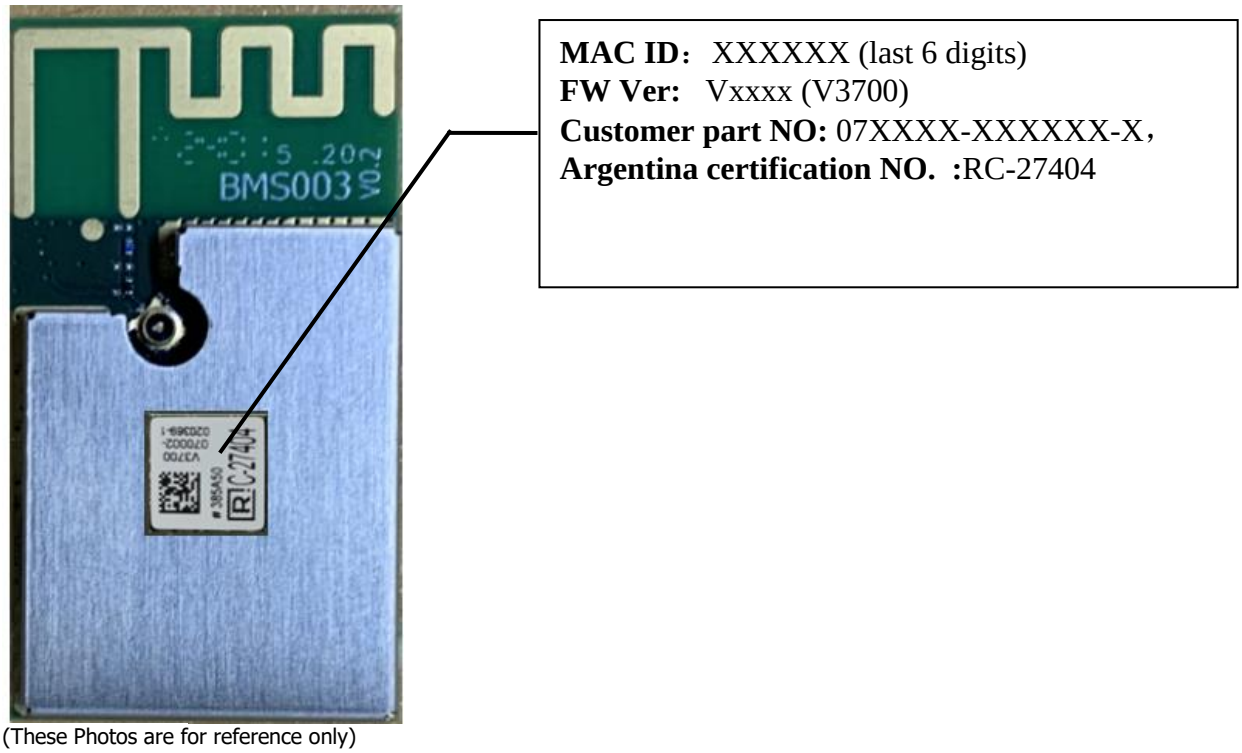


Key features of the profile:

-Initial Ramp=1-2.5℃/sec to 175℃ equilibrium
-Equilibrium time=60 to 90 seconds
-Ramp to Maximum temperature (250℃)=3℃/sec Max
-Time above liquidus temperature (217℃): 70 - 90 seconds
-Device absolute maximum reflow temperature: 250℃
-TAMURA solder paster

10.QR code label information:

Label



MAC ID: XXXXXX (last 6 digits)
FW Ver: Vxxxx (V3700)
Customer part NO: 07XXXX-XXXXXX-X,
Argentina certification NO. :RC-27404

(These Photos are for reference only)

11.Certification

11.1 BQB Certification QDID

・Declaration ID：

・QDID：

11.2 EMC Certification

The BMS003 module has received the regulatory approval for following countries:

No	Country	Certification	STANDARD	Certification ID/No.
1	United States	FCC	FCC Part 15C	
2	Canada	IC	RSS-247	
3	Europe	CE	EN 62368-1:2014 EN 623681:2014/A11:2017	
			EN 50663:2017	
			EN 301 489-1 V2.2.3 EN 301 489-17 V3.2.4 EN 300 328 V2.2.2	
4	Argentina	CNC	Protocolo para Equipos de Espectro Ensanchado por Salto en Frecuencia V13.1; Protocolo para Equipos de Banda Ancha V13.2	
5	Japan	TELEC/JATE	ARIB STD -T66 Version 3.7 MIC Notification NO.88 Appendix NO.43	
6	Malaysia	Malaysia	MCMC MTSFB TC T007:2020	
7	UAE	TRA	TIC-D01-CS01	
8	Peru	Peru	0902-2022-MTC/29.01	

The component does not contain any prohibited substance specified in “SS-00259”.
If using recycled plastic or sheathed wire as customer-classified, it shall be procured from a Sony green partner.

12.Electrostatic discharge（ESD）：HBM≥1000V，CDM≥500V

13.Un-opened reels Shelf life:

The module can be stored for 25±3℃ 30-60%RH for 6 months. After unpacking, the finished patch should be used within 24 hours to avoid welding pad oxidation. Unused materials are returned to sealed packaging in time.

14.Reliability Test:

Test items	Test method
Vibration ReliabilityTest	1.Single module: Vibration frequency: 50Hz Vibration amplitude: 0.5mm Vibration time: 30 minutes 2.After the test, confirm whether the appearance and function are qualified.
Drop Reliability Test	1.Single module weight <10g, drop height 1.0m， marble floor. 2.The top, bottom, left, right, front and rear 6 surfaces fell once each, a total of 6 times. 3.After the test, confirm whether the appearance and function are qualified.
Low Temperature Reliability Test	1.The BMS003 module is installed on the EVB, bluetooth connection is made with the BMS003 module, and the music is continuously played on the phone. 2.The installed EVB was placed in the high-low temperature test chamber at a working temperature of -20℃ degrees for 4 hours. 3.After the completion of the test, the EVB and the module were removed from the high-low temperature test chamber and placed at room temperature for 1 hour,then confirm whether the appearance and function are qualified.
High Temperature Reliability Test	1.The BMS003 module is installed on the EVB, bluetooth connection is made with the BMS003 module, and the music is continuously played on the phone. 2.The installed EVB was placed in the high-low temperature test chamber at a working temperature of 70℃ for 4 hours. 3.After the completion of the test, the EVB and the module were removed from the high-low temperature test chamber and placed at room temperature for 1 hour,then confirm whether the appearance and function are qualified.
Aging Test	1.The BMS003 module is installed on the EVB, bluetooth connection is made with the BMS003 module. 2.Place the installed EVB at room temperature and continue playing music for 48 hours. 3.After the test, confirm whether the appearance and function are qualified.
Vibration Reliability Test	1.The BMS003 module is installed on the EVB， then put the EVB into a protective housing to do test: Vibration frequency: 50Hz Vibration amplitude: 0.5mm Vibration time: 30 minutes 2.After the test, confirm whether the appearance and function are qualified.
Drop Reliability Test	1.The module is installed on the EVB，then put the EVB into a protective housing to do test, the drop test condition as follow： [2019/6/11 SONY] Drop height = 122cm 6-surface, 8-corner, 12-edge line, = total 26times. Please add some weight to the housing to make total weight to be [2021/5/25 SONY] 1）XE-M： 1380g 2）XE-L ： 810g If 1) test was Failed, then please test 2). 2.After the test, confirm whether the appearance and function are qualified.
Weldability	Recommended Reflow Temperature Profile

15.Standard Packing Information

Module packing Box (Max 2100pcs module per box)

42pcs per tray, 10trays per ESD bag, vacuum packing sealed in ESD PE bag.

Maximum modules per ESD bag is 420pcs

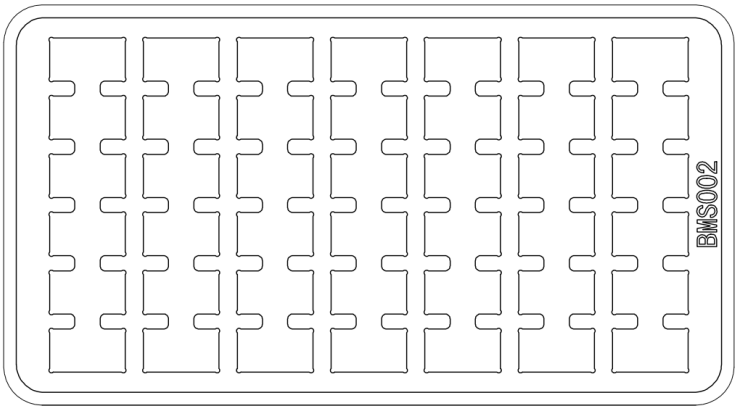
Module packing bag dimension: 290*160*6.5mm

Delivering carton box

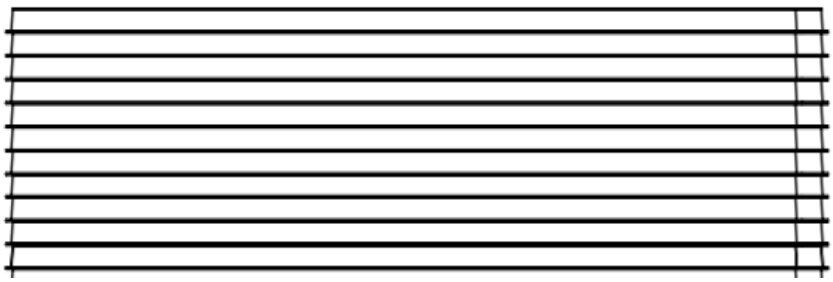
To hold of module carton box for shipment, 6bags per box (Max 2520pcs modules per box)

Delivery Carton Box dimension: 310.0mm x 340.0mm x 340.0mm (W x D x H)

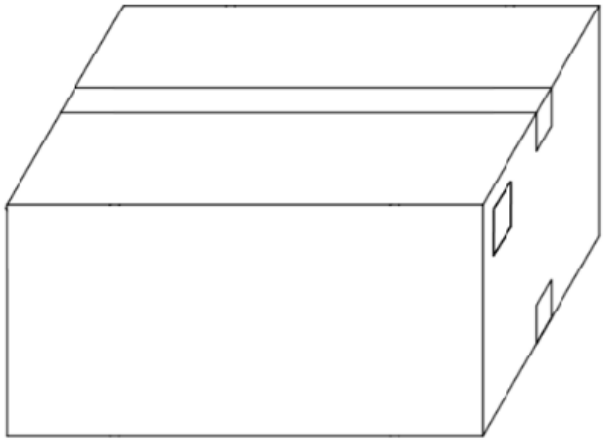
ESD tray dimension: 290*160*6.5mm



（plastic tray size :290mm*160mm*6.5mm，qty :42 pcs/ tray）



（10 trays / package bag）



（carton size： 310mm*340mm*340mm，6 bags / carton , total :2520pcs/carton ）

The actual photo

（plastic tray photo :42 pcs/ tray）

（ESD PE bag dimension）

（Vacuum packing： 10trays per ESD bag)

Carton box (6bags in per carton box)

16.Document History

Revision	Date	History
V1.0	2023-07-17	First release
V1.1	2023-12-27	Updated pin description
V1.2	2024-05-30	Updated shielding case, Antenna gain and ESD
V1.3	2024-06-07	Updated RF performances

Contact Information
SUNITEC ELECTRONICS TECHNOLOGY LIMITED
China Factory:
Building C No.725 , WeiXiangTai Industrial Zone, FuCheng Street ,
LongHua District , ShenZhen ,Guangdong , China
Tel: 86-755-28016180
Fax: 86-755-28016097
E-mail: sales16@sunitec-cn.com or manager@sunitec-cn.com
Http://www.sunitec-cn.com

IC Warning This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions:
(1) This device may not cause interference, and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.
The modular can be installed or integrated in mobile or fix devices only. This modular cannot be installed in any portable device.

For a host manufacture's using a certified modular, if (1) the module's IC number is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the IC number of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module IC: 23011-BMS003" or "Contains IC: 23011-BMS003" must be used.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement Le modular peut être installé ou intégré dans un mobile ou réparer une seule chose Installation dans n’importe quell appareil portable.

Pour un hôte, on utilise un modular, si (1) le numéro de module est non visible Quand on est installé dans le serveur, or (2) si le propriétaire est commercialisé Straightforward commonly used for the access to remove travail so that the number IC en vue Le module est visible;Ensuite, le label permanent a été attribué au module: "Contient le Module IC: 23011-BMS003" " ou "contenu IC: 23011-BMS003" doit be used.

Radiation Exposure Statement
This modular complies with RF radiation exposure limits set forth for an uncontrolled environment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with multi-transmitter product procedures. This modular must be installed and operated with a minimum distance of 20 cm between the radiator and user body.

Déclaration d'exposition aux rayonnements
Ce module est conforme aux limites d'exposition aux rayonnements RF définies pour un environnement non contrôlé. Cet émetteur ne doit pas être co-localisé ou fonctionner en conjonction avec une autre antenne ou émetteur, sauf conformément aux procédures du produit multi-émetteur. Ce modulaire doit être installé et exploité avec une distance minimale de 20 cm entre le radiateur et le corps de l'utilisateur.

FCC Statement

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) this device must accept any interference received, including interference that may cause undesired operation.

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

If the FCC identification number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following: “Contains Transmitter Module FCC ID: 2AMX3BMS003” Or “Contains FCC ID: 2AMX3BMS003”

When the module is installed inside another device, the user manual of the host must contain below warning statements;

1. This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference.

(2) This device must accept any interference received, including interference that may cause undesired operation.

2. Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

The devices must be installed and used in strict accordance with the manufacturer's instructions as described in the user documentation that comes with the product.

Any company of the host device which install this modular with Limited Single modular approval should perform the test of radiated emission and spurious emission according to FCC part 15C : 15.247 and 15.209 requirement, Only if the test result comply with FCC part 15C : 15.247 and 15.209 requirement，then the host can be sold legally.

Requirement per KDB996369 D03

2.2 List of applicable FCC rules

List the FCC rules that are applicable to the modular transmitter. These are the rules that specifically establish the bands of operation, the power, spurious emissions, and operating fundamental frequencies. DO NOT list compliance to unintentional-radiator rules (Part 15 Subpart B) since that is not a condition of a module grant that is extended to a host manufacturer. See also Section 2.10 below concerning the need to notify host manufacturers that further testing is required.3

Explanation: This module meets the requirements of FCC part 15.247.

2.3 Summarize the specific operational use conditions

Describe use conditions that are applicable to the modular transmitter, including for example any limits on antennas, etc. For example, if point-to-point antennas are used that require reduction in power or compensation for cable loss, then this information must be in the instructions. If the use condition limitations extend to professional users,

then instructions must state that this information also extends to the host manufacturer's instruction manual. In addition, certain information may also be needed, such as peak gain per frequency band and minimum gain, specifically for master devices in 5 GHz DFS bands.

Explanation: The EUT has a PCB Antenna, and the antenna use a permanently attached antenna which is not replaceable.

2.4 Limited module procedures

If a modular transmitter is approved as a "limited module," then the module manufacturer is responsible for approving the host environment that the limited module is used with. The manufacturer of a limited module must describe, both in the filing and in the installation instructions, the alternative means that the limited module manufacturer uses to verify that the host meets the necessary requirements to satisfy the module limiting conditions.

A limited module manufacturer has the flexibility to define its alternative method to address the conditions that limit the initial approval, such as: shielding, minimum signaling amplitude, buffered modulation/data inputs, or power supply regulation. The alternative method could include that the limited module manufacturer reviews detailed test data or host designs prior to giving the host manufacturer approval.

This limited module procedure is also applicable for RF exposure evaluation when it is necessary to demonstrate compliance in a specific host. The module manufacturer must state how control of the product into which the modular transmitter will be installed will be maintained such that full compliance of the product is always ensured. For additional hosts other than the specific host originally granted with a limited module, a Class II permissive change is required on the module grant to register the additional host as a specific host also approved with the module.

Explanation: The module is a single module.

2.5 Trace antenna designs

For a modular transmitter with trace antenna designs, see the guidance in Question 11 of KDB Publication 996369 D02 FAQ – Modules for Micro-Strip Antennas and traces. The integration information shall include for the TCB review the integration instructions for the following aspects: layout of trace design, parts list (BOM), antenna, connectors, and isolation requirements.

a) Information that includes permitted variances (e.g., trace boundary limits, thickness,
length, width, shape(s), dielectric constant, and impedance as applicable for each type of antenna);

b) Each design shall be considered a different type (e.g., antenna length in multiple(s) of frequency, the wavelength, and antenna shape (traces in phase) can affect antenna gain and must be considered);

c) The parameters shall be provided in a manner permitting host manufacturers to design the printed circuit (PC) board layout;

d) Appropriate parts by manufacturer and specifications;

e) Test procedures for design verification; and

f) Production test procedures for ensuring compliance.

The module grantee shall provide a notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify the module grantee that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

Explanation: Yes, The module with trace antenna designs, and This manual has been shown the layout of trace design, antenna, connectors, and isolation requirements.

2.6 RF exposure considerations

It is essential for module grantees to clearly and explicitly state the RF exposure conditions that permit a host product manufacturer to use the module. Two types of instructions are required for RF exposure information: (1) to the host product manufacturer, to define the application conditions (mobile, portable – xx cm from a person’s body); and (2) additional text needed for the host product manufacturer to provide to end users in their end-product manuals. If RF exposure statements and use conditions are not provided, then the host product manufacturer is required to take responsibility of the module through a change in FCC ID (new application).

Explanation: This module complies with FCC RF radiation exposure limits set forth for an uncontrolled environment, This equipment should be installed and operated with a minimum distance of 20 centimeters between the radiator and your body." This module is designed to comply with the FCC statement, FCC ID is: 2AMX3BMS003.

2.7 Antennas

A list of antennas included in the application for certification must be provided in the instructions. For modular transmitters approved as limited modules, all applicable professional installer instructions must be included as part of the information to the host product manufacturer. The antenna list shall also identify the antenna types (monopole, PIFA, dipole, etc. (note that for example an “omni-directional antenna” is not considered to be a specific “antenna type”)).

For situations where the host product manufacturer is responsible for an external connector, for example with an RF pin and antenna trace design, the integration instructions shall inform the installer that unique antenna connector must be used on the Part 15 authorized transmitters used in the host product. The module manufacturers shall provide a list of acceptable unique connectors.

Explanation: The EUT has a PCB Antenna, and the antenna use a permanently attached antenna which is unique.

2.8 Label and compliance information

Grantees are responsible for the continued compliance of their modules to the FCC rules. This includes advising host product manufacturers that they need to provide a physical or e-label stating “Contains FCC ID” with their finished product. See Guidelines for Labeling and User Information for RF Devices – KDB Publication 784748.

Explanation: The host system using this module, should have label in a visible area indicated the following texts: “Contains FCC ID: 2AMX3BMS003, Contains IC: 23011-BMS003 ”

2.9 Information on test modes and additional testing requirements5

Additional guidance for testing host products is given in KDB Publication 996369 D04 Module Integration Guide. Test modes should take into consideration different operational conditions for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product. The grantee should provide information on how to configure test modes for host product evaluation for different operational conditions for a stand-alone modular transmitter in a host, versus with multiple, simultaneously transmitting modules or other transmitters in a host.

Grantees can increase the utility of their modular transmitters by providing special means, modes, or instructions that simulates or characterizes a connection by enabling a transmitter. This can greatly simplify a host manufacturer’s determination that a module as installed in a host complies with FCC requirements.

Explanation: Top band can increase the utility of our modular transmitters by providing instructions that simulates or characterizes a connection by enabling a transmitter.

2.10 Additional testing, Part 15 Subpart B disclaimer

The grantee should include a statement that the modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

Explanation: The module without unintentional-radiator digital circuity, so the module does not require an evaluation by FCC Part 15 Subpart B. The host shoule be evaluated by the FCC Subpart B.