

FSC-BT836B

Bluetooth Module Data Sheet

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Release Record

| Version Number | Release Date | Comments |
|----------------|--------------|------------------------|
| Revision 2.0 | 2019-08-17 | First Release |
| Revision 2.1 | 2019-11-16 | Update antenna package |
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1. INTRODUCTION

FSC-BT836B is Feasycom's dual-mode (BR/EDR and LE) Bluetooth 5.0 compliant module. It supports SPP, HID, GATT, ATT, and other profiles. It provides several customizable hardware interfaces such as UART, USB, PCM, I2C, AIO, PIO, etc.

FSC-BT836B incorporates high-performance MCU, Bluetooth controller and chip antenna in a small package so that customers can integrate FSC-BT836B in small products.

FSC-BT836B uses UART as the programming interface, customers can use AT commands to read or write the configuration of the module through UART. FSC-BT836B is powered by Feasycom's Bluetooth stack which could provide more possibilities to the applications of customers. For programming with FSC-BT836B, please refer to the relevant programming user guide.

1.1 Feature

- ◆ Fully qualified Bluetooth 5.0/4.2/4.0/3.0/2.1/2.0/1.2/1.1
- ◆ Postage stamp sized form factor
- ◆ Low power
- ◆ Class 1.5 support(high output power)
- ◆ The default UART Baud rate is 115.2Kbps and can support from 1200bps up to 921.6Kbps
- ◆ UART, I²C ,USB hardware interfaces
- ◆ Support the OTA upgrade
- ◆ Embedded Bluetooth stack profiles support: SPP, HID,GATT, ATT, GAP
- ◆ Support Apple MFi (iAP2), iBeacon

1.2 Application

- ◆ Smart Watch and Bluetooth Bracelet
- ◆ Health & Medical devices
- ◆ Wireless POS
- ◆ Measurement and monitoring systems
- ◆ Industrial sensors and controls
- ◆ Asset tacking

Module picture as below showing



2. GENERAL SPECIFICATION

| General Specification | |
|-------------------------|--|
| Chip Set | RTL8761 |
| Product ID | FSC-BT836B |
| Dimension | 13mm x 26.9mm x 2.4mm |
| Bluetooth Specification | Bluetooth V5.0 (Dual Mode) |
| Power Supply | 3.3 Volt DC |
| Output Power | 10 dBm (Class 1.5) |
| Sensitivity | -94.5dBm@0.1%BER |
| Frequency Band | 2.402GHz -2.480GHz ISM band |
| Modulation | GFSK, $\pi/4$ -DQPSK, 8-DPSK |
| Baseband Crystal OSC | 40MHz |
| Hopping & channels | 1600hops/sec, 1MHz channel space,79 Channels(BT 5.0 to 2MHz channel space) |
| RF Input Impedance | 50 ohms |
| Antenna | Integrated chip antenna |
| Interface | Data: UART (Standard), I ² C Others: PIO, AIO, PWM.USB |
| Profile | SPP, HID, GATT, ATT, GAP |
| Advanced Feature | MFi, Airsync, iBeacon, OTA |

| | |
|---------------|------------------------|
| Temperature | -20°C to +70 °C |
| Humidity | 10%~95% Non-Condensing |
| Environmental | RoHS Compliant |

Table 1

3. PHYSICAL CHARACTERISTIC

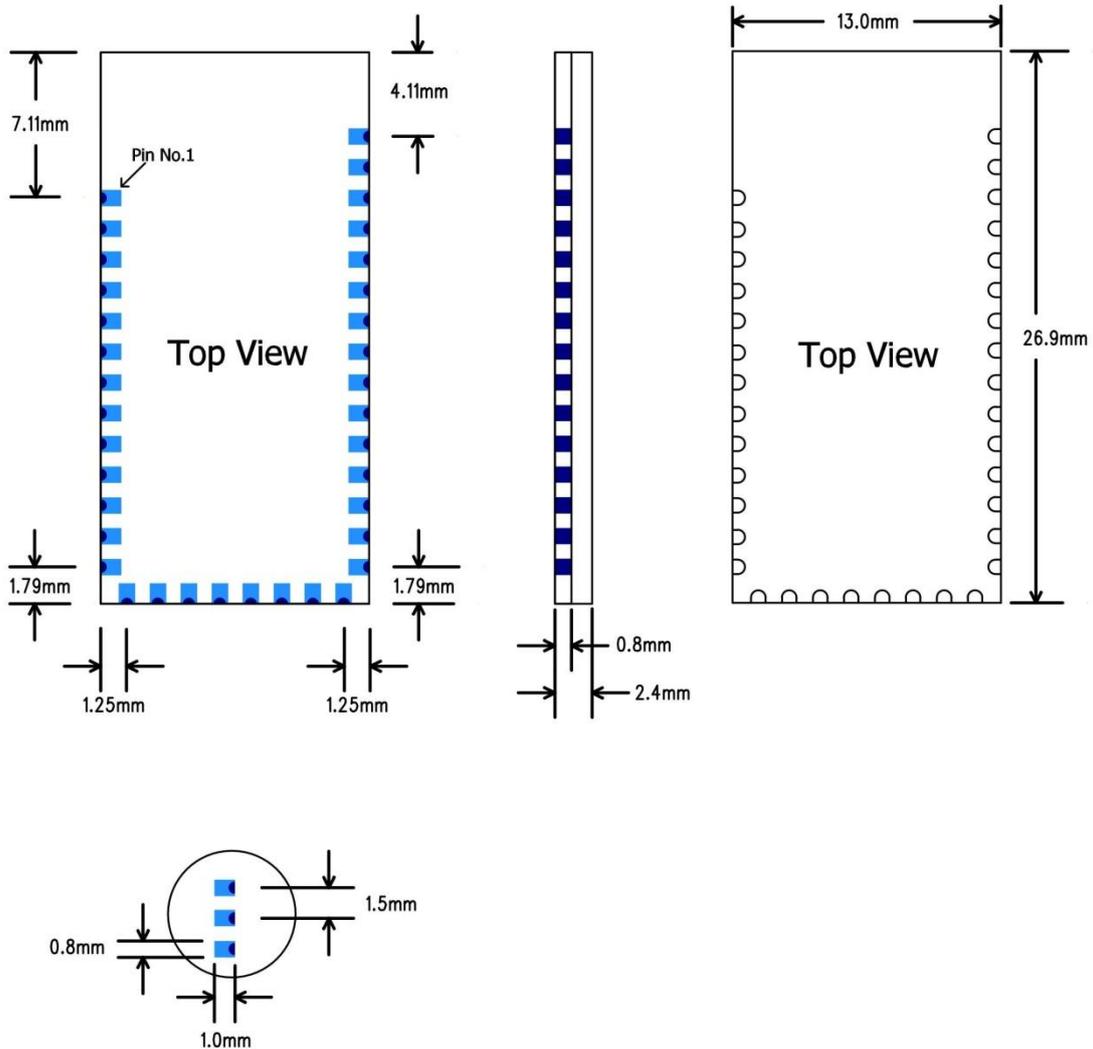


Figure 2

4. PIN DEFINITION DESCRIPTIONS

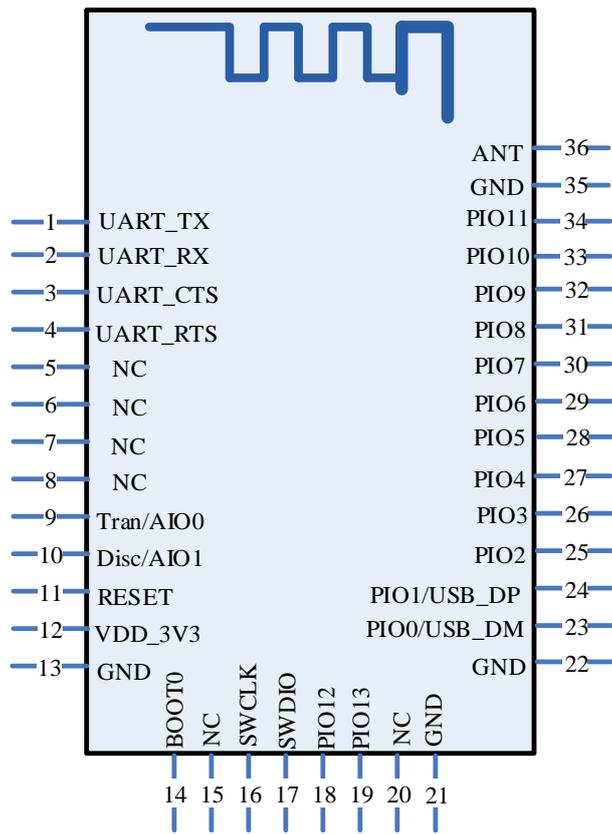


Figure 1: FSC-BT836B PIN Diagram

| Pin NO. | Pin Name | Type | Pin Descriptions |
|---------|----------|-------------|------------------|
| 1 | UART_TX | CMOS output | UART data output |
| 2 | UART_RX | CMOS input | UART data input |

| | | | |
|----|-------------|----------------|---|
| 3 | UART_CTS | CMOS input | UART clear to send active low Alternative Function: Programmable input/output line |
| 4 | UART_RTS | CMOS output | UART request to send active low Alternative Function: Programmable input/output line |
| 5 | NC | | |
| 6 | NC | | |
| 7 | NC | | |
| 8 | NC | | |
| 9 | Tran/AIO0 | I/O | Host MCU change UART transmission mode. (Default) Alternative Function: Analogue programmable I/O line. |
| 10 | Disc/AIO1 | I/O | Host MCU disconnect bluetooth. (Default). Alternative Function: Analogue programmable I/O line. |
| 11 | RESET | CMOS input | Reset if low. Input debounced so must be low for >5ms to cause a reset. |
| 12 | VDD_3V3 | VDD | Power supply voltage 3.3V |
| 13 | GND | VSS | Power Ground |
| 14 | BOOT0 | CMOS input | The default is low. (internal 10K resistance drop) UART DFU Mode, Enabled at startup when set to high level, Disabled by default |
| 15 | NC | NC | NC |
| 16 | SWCLK | Bi-directional | Debugging through the clk line(Default) |
| 17 | SWDIO | Bi-directional | Debugging through the data line(Default) |
| 18 | PIO12 | Bi-directional | Programmable input/output line Alternative Function: UART3 data output |
| 19 | PIO13 | Bi-directional | Programmable input/output line Alternative Function: UART3 data input |
| 20 | NC | NC | NC |
| 21 | GND | VSS | Power Ground |
| 22 | GND | VSS | Power Ground |
| 23 | PIO0/USB_DM | Bi-directional | Programmable input/output line Alternative Function: USB_DM(optional) |
| 24 | PIO1/USB_DP | Bi-directional | Programmable input/output line Alternative Function: USB_DP(optional) |

| | | | |
|----|---------|------------------|---|
| 25 | PIO2 | Bi-directional | Programmable input/output line |
| 26 | PIO3 | Bi-directional | Programmable input/output line |
| 27 | PIO4 | Bi-directional | Programmable input/output line Alternative Function: BT Power Mode, low level in run mode, it will be set to high level when fall asleep. |
| 28 | PIO5 | Bi-directional | Programmable input/output line |
| 29 | PIO6 | Bi-directional | Programmable input/output line Alternative Function: I ² C Serial Clock input/output |
| 30 | PIO7 | Bi-directional | Programmable input/output line Alternative Function: I ² C Serial Data input/output |
| 31 | PIO8 | Bi-directional | Programmable input/output line |
| 32 | PIO9 | Bi-directional | Programmable input/output line Alternative Function: LED(Default) |
| 33 | PIO10 | Bi-directional | Programmable input/output line Alternative Function: BT Status(Default) |
| 34 | PIO11 | Bi-directional | Programmable input/output line |
| 35 | GND | VSS | Power Ground |
| 36 | EXT_ANT | RF signal output | By default, this PIN is an empty feet. This PIN can connect to an external antenna to improve the Bluetooth signal coverage. If you need to use an external antenna, by modifying the module on the 0R resistance to block out the on-board antenna; Or contact Feasycom for modification. |

Table 2

5. Interface Characteristics

5.1 UART Interface

Four signals are used to implement the UART function. When FSC-BT836B is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

The interface consists of four-line connection as described in below:

| Signal name | Driving source | Description |
|-------------|----------------|-------------|
|-------------|----------------|-------------|

| | | |
|----------|-------------------|---|
| UART-TX | FSC-BT836B module | Data from FSC-BT836B module |
| UART-RX | Host | Data from Host |
| UART-RTS | FSC-BT836B module | Request to send output of FSC-BT836B module |
| UART-CTS | Host | Clear to send input of FSC-BT836B module |

Table 3

Possible UART Settings

| Property | Possible Values |
|------------------------|--------------------|
| BCSP-Specific Hardware | Enable or Disable |
| Baudrate | 1200bps to 921Kbps |
| Flow Control | RTS/CTS or None |
| Data bit length | 8bits |
| Parity | None, Odd or Even |
| Number of Stop Bits | 1 or 2 |

Table 4

Default Data Format

| Property | Possible Values |
|---------------------|-----------------|
| Baudrate | 115.2Kbps |
| Flow Control | None |
| Data bit length | 8bit |
| Parity | None |
| Number of Stop Bits | 1 |

Table 5

5.2 SPI /I²S Interface

Up to two SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I²S interfaces supporting four different audio standards can operate as master or slave at half-duplex communication mode. They can be configured to transfer 16

and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, they can output a clock for an external audio component at 256 times the sampling frequency.

5.2.1 SPI characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------------------------|----------------------------------|--|-------------|-------------|------|
| f_{SCK} $1/t_{c(SCK)}$ | SPI clock frequency | Master mode | - | 18 | MHz |
| | | Slave mode | - | 18 | |
| $t_{r(SCK)}$ $t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C = 15 pF | - | 6 | ns |
| $t_{su(NSS)}$ | NSS setup time | Slave mode | 4Tpclk | - | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode | 2Tpclk + 10 | - | |
| $t_{w(SCKH)}$ $t_{w(SCKL)}$ | SCK high and low time | Master mode, $f_{PCLK} = 36$ MHz, presc = 4 | Tpclk/2 - 2 | Tpclk/2 + 1 | |
| $t_{su(MI)}$ $t_{su(SI)}$ | Data input setup time | Master mode | 4 | - | |
| | | Slave mode | 5 | - | |
| $t_{h(MI)}$ $t_{h(SI)}$ | Data input hold time | Master mode | 4 | - | |
| | | Slave mode | 5 | - | |
| $t_{a(SO)}^{(2)}$ | Data output access time | Slave mode, $f_{PCLK} = 20$ MHz | 0 | 3Tpclk | |
| $t_{dis(SO)}^{(3)}$ | Data output disable time | Slave mode | 0 | 18 | |
| $t_{v(SO)}$ | Data output valid time | Slave mode (after enable edge) | - | 22.5 | |
| $t_{v(MO)}$ | Data output valid time | Master mode (after enable edge) | - | 6 | |
| $t_{h(SO)}$ $t_{h(MO)}$ | Data output hold time | Slave mode (after enable edge) | 11.5 | - | |
| | | Master mode (after enable edge) | 2 | - | |
| DuCy(SCK) | SPI slave input clock duty cycle | Slave mode | 25 | 75 | % |

Table 6 SPI characteristics

1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

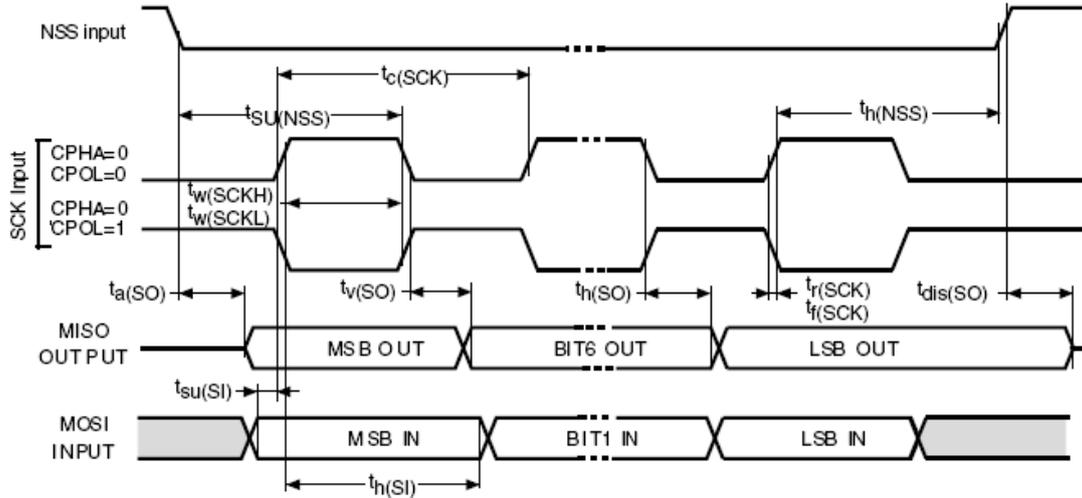
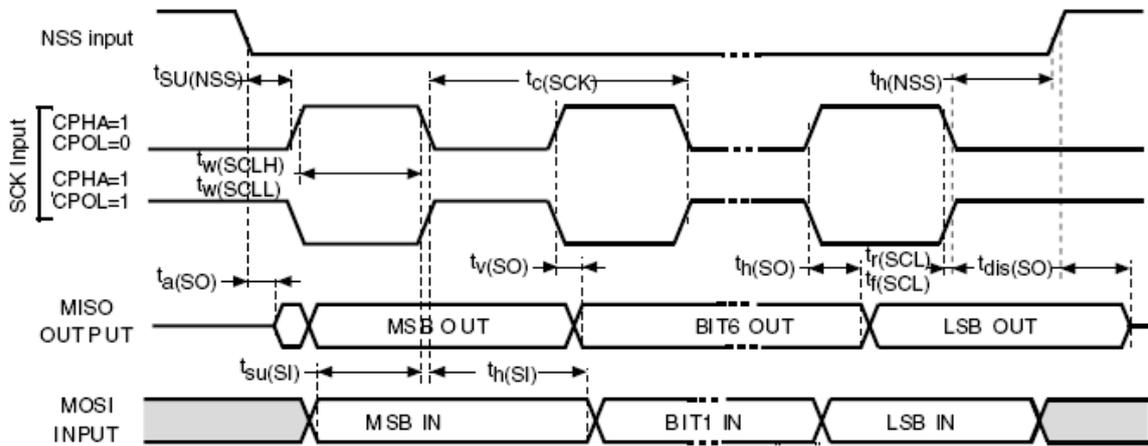
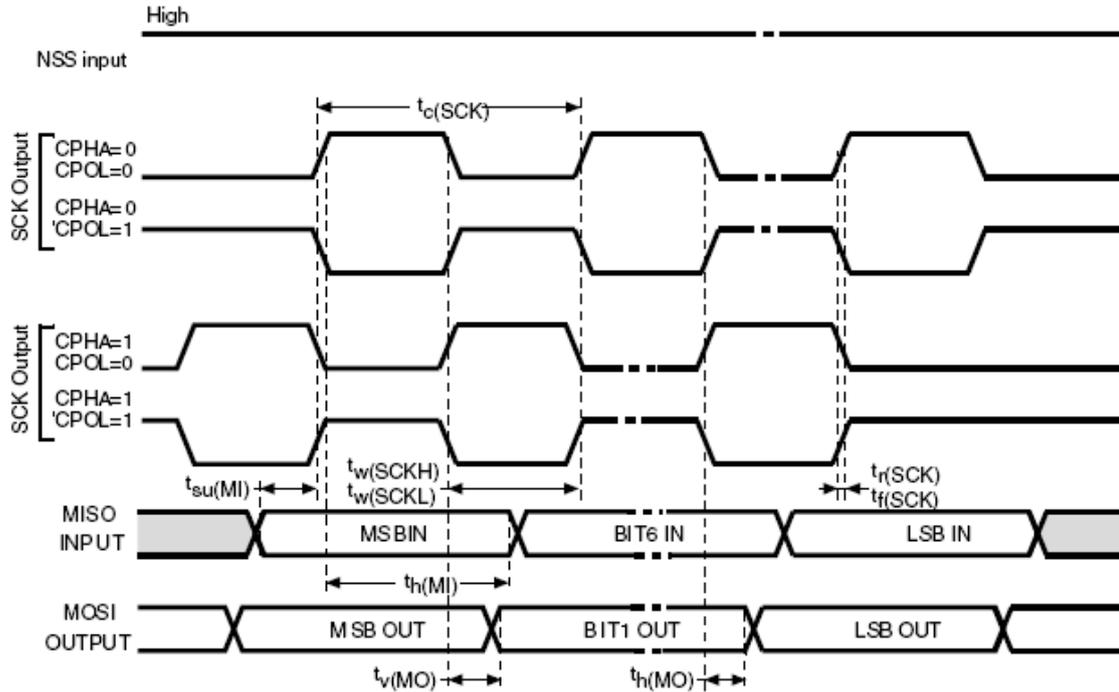


Figure 3: SPI timing diagram - slave mode and CPHA = 0



* 1. Measurement points are done at CMOS levels: 0.3 VDD and 0.7 VDD.

Figure 4: SPI timing diagram - slave mode and CPHA = 1



1.Measurement points are done at CMOS levels: 0.3 VDD and 0.7 VDD

Figure 5: SPI timing diagram - master mode

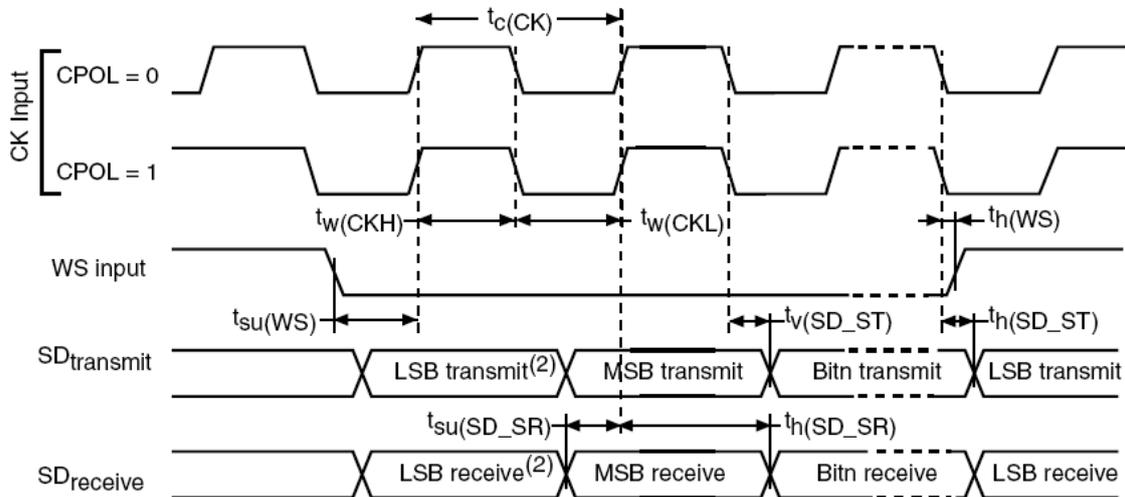
5.2.2 I²S characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-------------------------|---|---|-------|-------|------|
| f_{CK} $1/t_c(CK)$ | I ² S clock frequency | Master mode (data: 16 bits, Audio frequency = 48 kHz) | 1.597 | 1.601 | MHz |
| | | Slave mode | 0 | 6.5 | |
| $t_r(CK)$ | I ² S clock rise time | Capacitive load $C_L = 15$ pF | - | 10 | ns |
| $t_f(CK)$ | I ² S clock fall time | | - | 12 | |
| $t_w(CKH)$ | I ² S clock high time | Master $f_{CLK} = 16$ MHz, audio frequency = 48 kHz | 306 | - | |
| $t_w(CKL)$ | I ² S clock low time | | 312 | - | |
| $t_v(WS)$ | WS valid time | Master mode | 2 | - | |
| $t_h(WS)$ | WS hold time | Master mode | 2 | - | |
| $t_{su}(WS)$ | WS setup time | Slave mode | 7 | - | |
| $t_h(WS)$ | WS hold time | Slave mode | 0 | - | |
| DuCy(SCK) | I ² S slave input clock duty cycle | Slave mode | 25 | 75 | % |

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------------|------------------------|--|-----|-----|------|
| $t_{su(SD_MR)}$ | Data input setup time | Master receiver | 6 | - | ns |
| $t_{su(SD_SR)}$ | Data input setup time | Slave receiver | 2 | - | |
| $t_{h(SD_MR)}^{(2)}$ | Data input hold time | Master receiver | 4 | - | |
| $t_{h(SD_SR)}^{(2)}$ | | Slave receiver | 0.5 | - | |
| $t_{v(SD_ST)}^{(2)}$ | Data output valid time | Slave transmitter (after enable edge) | - | 20 | |
| $t_{h(SD_ST)}$ | Data output hold time | Slave transmitter (after enable edge) | 13 | - | |
| $t_{v(SD_MT)}^{(2)}$ | Data output valid time | Master transmitter (after enable edge) | - | 4 | |
| $t_{h(SD_MT)}$ | Data output hold time | Master transmitter (after enable edge) | 0 | - | |

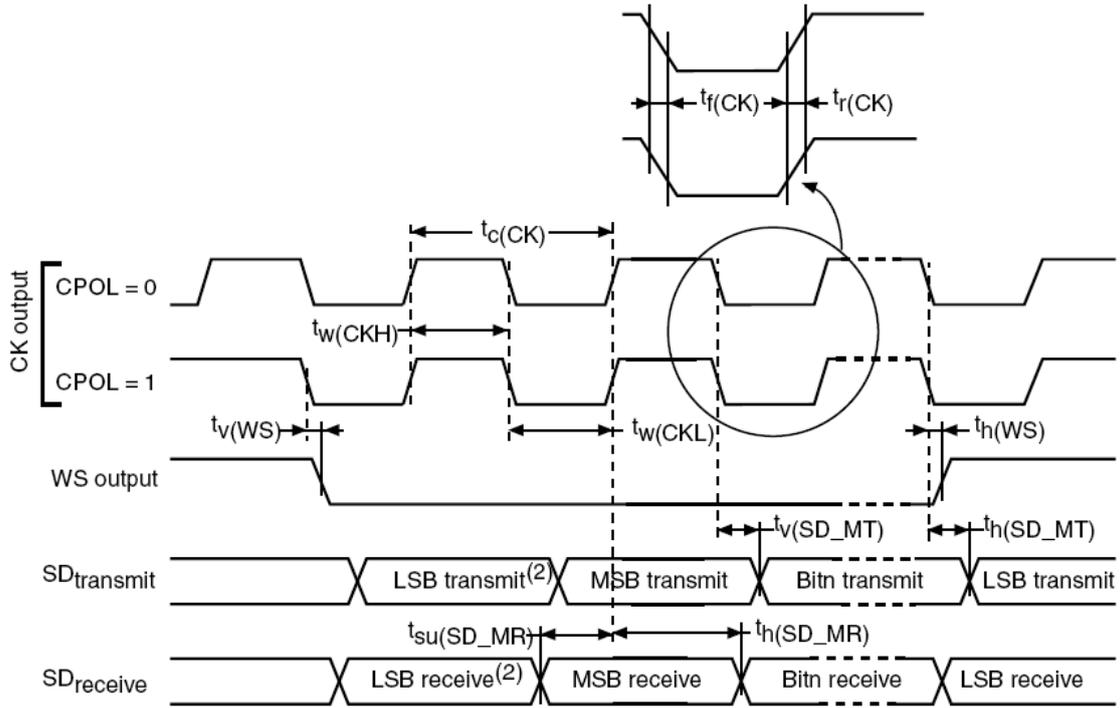
1. Data based on design simulation and/or characterization results, not tested in production.
2. Depends on fPCLK. For example, if fPCLK = 8 MHz, then TPCLK = 1/fPCLK = 125 ns.

Table 7 I²S characteristics



1. Measurement points are done at CMOS levels: $0.3 \times VDDIOx$ and $0.7 \times VDDIOx$.
2. LSB transmit/receive of the previously transmitted byte.
No LSB transmit/receive is sent before the first byte.

Figure 6: I²S slave timing diagram (Philips protocol)



1. Data based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte.
No LSB transmit/receive is sent before the first byte.

Figure 7: I²S master timing diagram (Philips protocol)

5.3 AIO , PIO lines I²C and USB

Up to 19 programmable bidirectional input/output (I/O) can be used.
Two general purpose analogue interface pin can be used.
PIO6 and PIO7 can be used as I²C interface.

Inter-Integrated Circuit Interface (I²C)

The I²C module provides an interface between the MCU and a serial I²C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fastmode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I²C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 4 external pins and 6 internal signals.

Universal serial bus (USB)

The FSC-BT836B embeds a full-speed USB device peripheral compliant with the USB specification version 2.0.

The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 KB and suspend/resume support.

6. RECOMMENDED TEMPERATURE REFLOW PROFILE

The re-flow profiles are illustrated in Figure 4 and Figure 5 below.

- Follow: IPC/JEDEC J-STD-020 C
- Condition:
 - Average ramp-up rate(217°C to peak):1~2°C/sec max.
 - Preheat:150~200C,60~180 seconds
 - Temperature maintained above 217°C:60~150 seconds
 - Time within 5°C of actual peak temperature:20~40 sec.
 - Peak temperature:250+0/-5°C or 260+0/-5°C
 - Ramp-down rate:3°C/sec.max.
 - Time 25°C to peak temperature:8 minutes max
 - Cycle interval: 5 minus

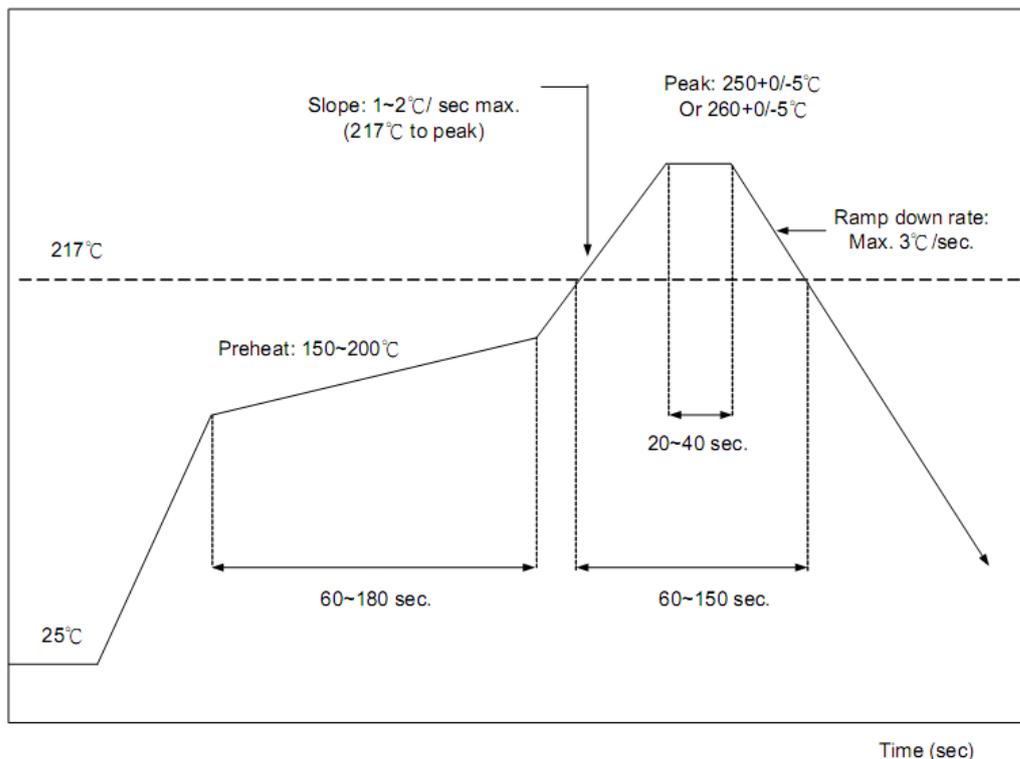


Figure 8: Typical Lead-free Re-flow Solder Profile

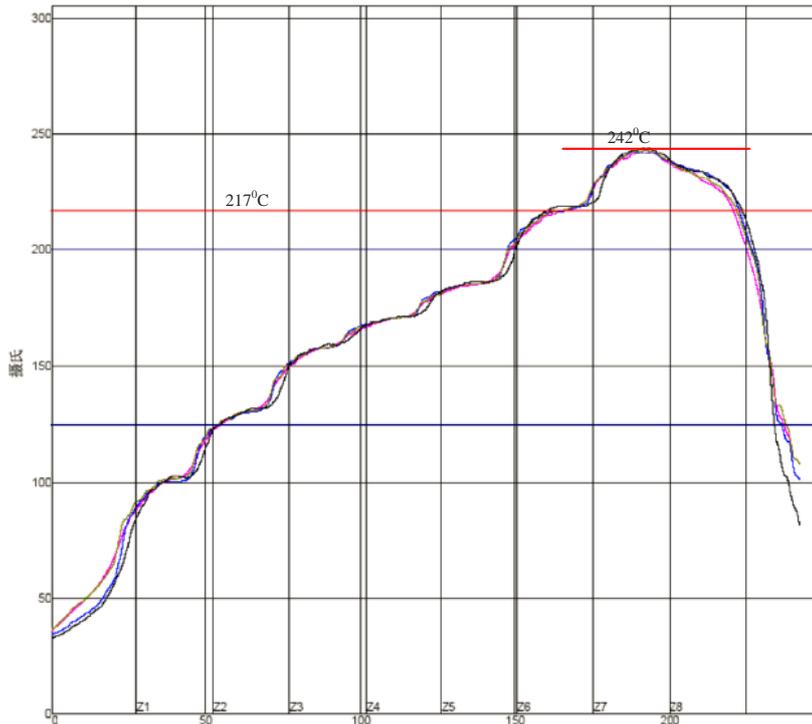


Figure 9: Typical Lead-free Re-flow

The soldering profile depends on various parameters according to the use of different solder and material. The data here is given only for guidance on solder re-flow.

FSC-BT836B will withstand up to two re-flows to a maximum temperature of 245°C.

7. Reliability and Environmental Specification

7.1 Temperature test

Put the module in demo board which uses exit power supply, power on the module and connect to mobile. Then put the demo in the -40°C space for 1 hour and then move to $+85^{\circ}\text{C}$ space within 1 minute, after 1 hour move back to -40°C space within 1 minute. This is 1 cycle. The cycles are 32 times and the units have to pass the testing.

7.2 Vibration Test

The module is being tested without package. The displacement requests 1.5mm and sample is vibrated in three directions(X,Y,Z).Vibration frequency set as 0.5G , a sweep rate of 0.1 octave/min from 5Hz to 100Hz last for 90 minutes each direction. Vibration frequency set as 1.5G, a sweep rate of 0.25 octave/min from 100Hz to 500Hz last for 20 minutes each direction.

7.3 Desquamation test

Use clamp to fix the module, measure the pull of the component in the module, make sure the module`s soldering is good.

7.4 Drop test

Free fall the module (condition built in a wrapper which can defend ESD) from 150cm height to cement ground, each side twice, total twelve times. The appearance will not be damaged and all functions OK.

7.5 Packaging information

After unpacking, the module should be stored in environment as follows:

Temperature: 25°C ± 2°C

Humidity: <60%

No acidity, sulfur or chlorine environment

The module must be used in four days after unpacking.

8. Layout and Soldering Considerations

8.1 Soldering Recommendations

FSC-BT836B is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

8.2 Layout Guidelines

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

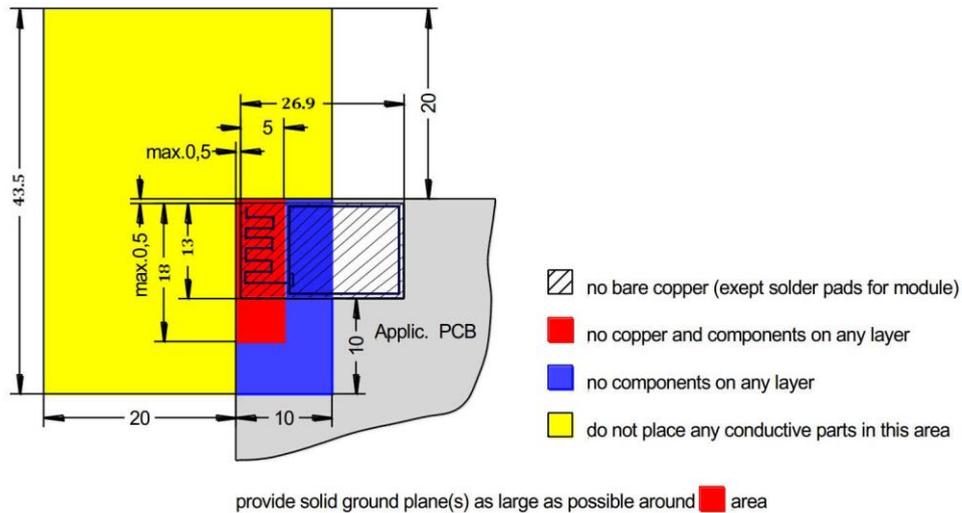


Figure 6: FSC-BT836B Restricted Area

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

FCC Statements

(OEM) Integrator has to assure compliance of the entire end-product incl. the integrated RF Module. For 15 B (§15.107 and if applicable §15.109) compliance, the host manufacturer is required to show compliance with 15 while the module is installed and operating.

Furthermore the module should be transmitting and the evaluation should confirm that the module's intentional emissions (15C) are compliant (fundamental / out-of-band). Finally the integrator has to apply the appropriate equipment authorization (e.g. Verification) for the new host device per definition in §15.101.

Integrator is reminded to assure that these installation instructions will not be made available to the end-user of the final host device.

The final host device, into which this RF Module is integrated" has to be labeled with an auxiliary label stating the FCC ID of the RF Module, such as "Contains FCC ID:2AMWOFSC-BT836B

"This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:

(1) this device may not cause harmful interference, and
(2) this device must accept any interference received, including interference that may cause undesired operation."

"Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment."

the Integrator will be responsible to satisfy SAR/ RF Exposure requirements, when the module is integrated into the host device.