FSC-BT1036C

Bluetooth 5.2 Dual Mode Module Datasheet

Version 1.2

Revision History

Version	Data	Notes	
1.0	2022/03/12	Initial Version	Marsh
1.1	2022/06/21	Updade Schematic and Picture	Marsh
1.2	2023/01/14	Updata Reset Time	Marsh

Contact Us

Shenzhen Feasycom Co.,LTD

Email: sales@feasycom.com

Address: Rm 508, Building A, Fenghuang Zhigu, No.50, Tiezai Road,
Xixiang ,Baoan District,Shenzhen,518100,China.
Tel: 86-755-27924639,86-755-23062695

1. INTRODUCTION

Overview

FSC-BT1036C it is a Bluetooth dual-mode module series. It supports a Bluetooth Low Energy and compliant system for audio and data communication.

FSC-BT1036C integrates an ultra-low-power DSP and application processor with embedded flash memory, a high-performance stereo codec, a power management subsystem, I^2S, LED drivers and ADC I/O in a SOC IC.

By default, FSC-BT1036C module is equipped with powerful and easy-to-use Feasycom firmware. It's easy to use and completely encapsulated. Feasycom firmware enables users to access Bluetooth functionality with simple ASCII commands delivered to the module over serial interface - it's just like a Bluetooth modem.

Therefore, FSC-BT1036C provides an ideal solution for developers who want to integrate Bluetooth wireless technology into their design.

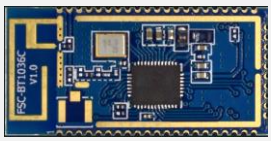
Application

- Bluetooth speakers
- Bluetooth music box
- Wired/wireless stereo headsets/headphones
- Audio transmitter

Features

- Bluetooth 5.2 classic and low energy
- Active noise cancellation
- Voice-activated assistant
- 24 bits audio quality
- 8 kHz to 384 kHz audio sample rate
- Acoustic echo cancellation

1.1 Selection of version

Order Number	Descriptions	Module picture as below showing
FSC-BT1036C	Dimension: 13*26.9*1.8mm（without cover）	

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Wireless Specification	Chip	BT V5.2 Dual-mode
	Frequency	2.402 - 2.480 GHz
	Transmit Power	+10 dBm (Maximum)
	Receive Sensitivity	-93.0 dBm (typ.) BDR=1Mbps
		-94.0 dBm (typ.) BDR=2Mbps
		-86.0 dBm (typ.) EDR=3Mbps
		-97 dBm (typ.) BLE=1Mbps
Host Interface and Peripherals	UART Interface	TX, RX, CTS, RTS
		General Purpose I/O
		Default 115200,N,8,1
		Baudrate support from 1200 to 4000000
	GPIO	14 (maximum – configurable) lines
	I^2C Interface	1 I^2C Master interface with speed up to 400 kbps
	ADC Interface	Analog input voltage range: 0~ 1.8V
		12-bit ADC
	USB Interface	1 full-speed (12Mbps) (***This feature is not enabled***)
Profiles	BR/EDR	SPP (Serial Port Profile) - Up to 600 Kbps
		A2DP/AVRCP/HFP/HSP/HOGP/PBAP/SPP Profiles support
	Bluetooth Low Energy	GATT Client & Peripheral
		Simultaneous BR/EDR and BLE support
Audio		24bit ADC/DAC
FW upgrade		UART
Supply Voltage	Supply	VDD: 3.3V
Power Consumption		Shut down:0.9uA(typ)
		Standby:20uA(typ)
		A2DP/HFP:6mA(typ)
		BLE TX 10dBm:28mA(typ)

Environmental	Operating	-20°C to +85°C
	Storage	-40°C to +85°C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:		Human Body Model: Class 2 2kV (all pins)
		Charged Device Model: Class III 500 V (all pins)

3. HARDWARE SPECIFICATION

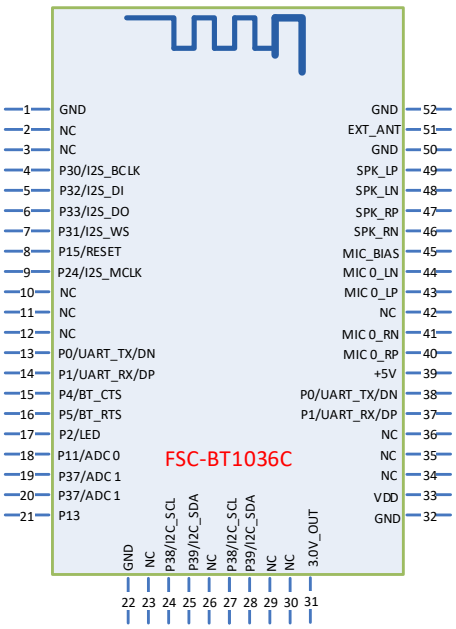


Figure 2: FSC-BT1036C PIN Diagram(Top View)

3.1 PIN Definition Descriptions

Table 2: Pin definition

Pin Name	Pin Number			Type	Descriptions	Notes
	BT1036A	BT1036B	BT1036C			
P0/UART_TX/DN	3	1	13,38	I/O	GPIO0/UART_TX/USB_DN	
P1/UART_RX/DP	4	2	14,37	I/O	GPIO1/UART_RX/USB_DP	
P5/UART_RTS	1	4	16	I/O	GPIO5/UART_RTS/Line in_R	
P4/UART_CTS	2	3	15	I/O	GPIO4/UART_CTS/ Line in_L	
P38/I^{2}C_SCL	6	29	24,27	I/O	GPIO38/I^{2}C_SCL	
P39/I^{2}C_SDA	5	30	25,28	I/O	GPIO39/I^{2}C_SDA	
P37/ADC1	7	28	19,20	I/O	GPIO37/ADC1	
P11/ADC0	22	33,34	18	I/O	GPIO11/ADC0/ STATUS(default)	
P15/RESET	8	11	8	I/O	GPIO15/RESET （Low level for more than 15ms）	
+5V	16	15	39	VDD	+5V input ***(Not used by default)***	
VDD	9	12	33	VDD	Power Supplies （3.3V）	
3.0V_OUT	-	-	31	VDD	3.0V_out(30mA)	

GND	10,11,17,26	13,14,21,22,35	1,22,32,50,52	VSS	GND	
MIC0_RN	-	-	41	Audio	MIC0/Line_IN differential R input, negative	
MIC0_RP	28	18	40	Audio	MIC0/Line_IN differential R input, positive	
MIC0_LN	-	-	44	Audio	MIC0/Line_IN differential L input, negative	
MIC0_LP	29	9,17	43	Audio	MIC0/Line_IN differential L input, positive	
MIC1_RP	-	10	-	Audio	MIC1/Line_IN differential R input, positive	
MIC_BIAS	30	16	45	VDD	MIC Power Supplies	
SPK_L	-	19,23	-	Audio	Line_out, left(16/32 Ω load cannot be connected)	
SPK_R	-	20,24	-	Audio	Line_out,right(16/32 Ω load cannot be connected)	
SPK_LN	32	-	48	Audio	Headphone/speaker differential L output, negative	
SPK_LP	31	-	49	Audio	Headphone/speaker differential L output, positive	
SPK_RN	34	-	46	Audio	Headphone/speaker differential R output, negative	
SPK_RP	33	-	47	Audio	Headphone/speaker differential R output, positive	
P30/I^2S_BCLK	21	5	4	I/O	GPIO30/ I^2S_BCLK	
P32/ I^2S_DI	19	7	5	I/O	GPIO32/ I^2S_DI	
P33/ I^2S_DO	20	6	6	I/O	GPIO33/ I^2S_DO	
P31/ I^2S_WS	18	8	7	I/O	GPIO31/ I^2S_WS	
P24/ I^2S_MCLK	23	31	9	I/O	GPIO24/ I^2S_MCLK	
P2/LED	24	32	17	I/O	GPIO2/LED(default)	
P13	25	25	21	I/O	GPIO13	
EXT_ANT	27	36	51	o	External antenna	
NC	12~15	-	2,3,10~12,23, 26,29,30, 34~36,42		NC	

4. PHYSICAL INTERFACE

4.1 Power Management

4.1.1 Power Supply

- The FSC-BT1036C can be powered directly from a 3.1V to 4.35V external battery via the VDD pin or it can be powered from a 4.75V to 5.5V USB power supply via the +5V pin. The +5V can be also used to charge battery with internal charge control circuit.

4.1.2 Battery Charger

- The default mode for the FSC-BT1036C battery charger is OFF.
- The internal charger circuit can provide up to 220mA of charge current.

4.2 Audio Peripherals

- The FSC-BT1036C comes with a rich set of audio peripherals to enhance the Bluetooth listening experience. The chip includes 24 bits analog-to-digital converter (ADC) and 24 bits digital-to-analog converter (DAC), together with amplifier and bias. **The DAC is capable of driving 16 Ω speakers with up to 30 pF of load capacitance (BT1036B except)**.
- The typical sample rate of ADC and DAC is to 8 kHz、44.1 kHz and 48 kHz, but could be set to any number from 8 kHz to 384 kHz.
- There is also digital microphone interface to support up to 1 digital microphone. The PDM does the 8:1 CIC decimation that the PCM sample rate could be up to 384 kHz when the PDM clock frequency is 3.072 MHz.

4.3 USB interface (*This feature is not enabled*)

- The USB interface supports both host and device mode, with full speed.

4.4 I^2S interface

- The I^2S interface supports both master and slave mode, with sample rate from 7.35 kHz to 384 kHz.
- There is an I^2S DPLL dedicate for I^2S and audio ADC/DAC, that it can output master clock for external device.

4.5 Serial Interfaces

4.5.1 UART Interface

FSC-BT1036C provides one channels of Universal Asynchronous Receiver/Transmitters(UART)(Full-duplex asynchronous communications). The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports ten types of interrupts.

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

This module output is at 3.3V CMOS logic levels (tracks VCC). Level conversion must be added to interface with an RS-232 level compliant interface.

Some serial implementations link CTS and RTS to remove the need for handshaking. We do not recommend linking

CTS and RTS except for testing and prototyping. If these pins are linked and the host sends data when the FSC-BT1036C deasserts its RTS signal, there is significant risk that internal receive buffers will overflow, which could lead to an internal processor crash. This drops the connection and may require a power cycle to reset the module. We recommend that you adhere to the correct CTS/RTS handshaking protocol for proper operation.

Table 3: Possible UART Settings

Parameter	Possible Values	
Baudrate	Minimum	2400 baud (≤2%Error)
	Standard	115200bps(≤1%Error)
	Maximum	4Mbaud(≤1%Error)
Flow control		RTS/CTS, or None
Parity		None, Odd or Even
Number of stop bits		1 /2
Bits per channel		8

When connecting the module to a host, please make sure to follow .

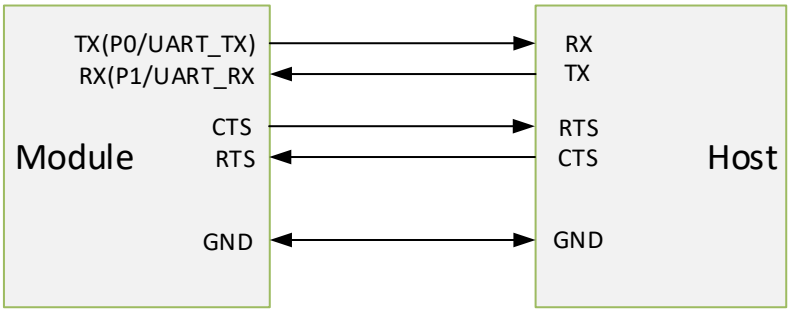


Figure 3: UART Connection

4.5.2 I²C Interface

FSC-BT1036C includes a configurable I²C interface.

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more details about I²C Bus Timing.

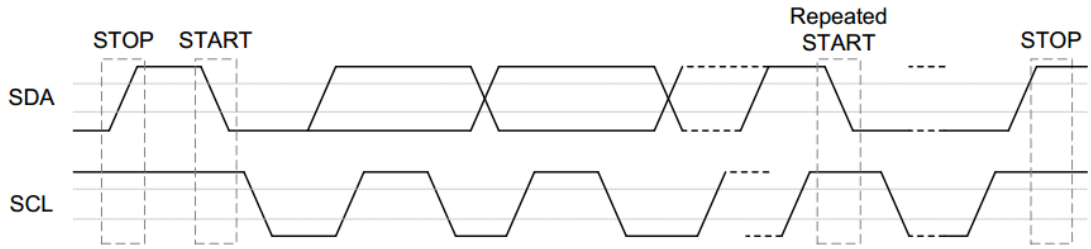


Figure 4: I2C Bus Timing

The device on-chip I^2C logic provides the serial interface that meets the I^2C bus standard mode specification. The I^2C port handles byte transfers autonomously. The I^2C H/W interfaces to the I^2C bus via two pins: SDA and SCL. Pull up resistor is needed for I^2C operation as these are open drain pins. When the I/O pins are used as I^2C port, user must set the pins function to I^2C in advance.

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below. Exceeding these values causes permanent damage.

The average PIO pin output current is defined as the average current value flowing through any one of the corresponding pins for a 100mS period. The total average PIO pin output current is defined as the average current value flowing through all of the corresponding pins for a 100mS period. The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

Table 4: Absolute Maximum Rating

Parameter	Min	Max	Unit
+5V	4.75	5.5	V
VDD	3.1	4.35	V
T_{ST} - Storage Temperature	-40	+85	°C

(a) Standard maximum input voltage is 5.75V, a 6.50V maximum depends on firmware version and implementation of over-temperature protection software, for more information contact Feasycom.
(b) VDD is the VDD_IO supply domain for this I/O. Voltage must not exceed 3.6 V on any I/O.

5.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
+5V	4.75	5	5.5	V
VDD		3.3		V
T_A - Operating Temperature	-20	-	+85	℃

5.3. Battery Charger(*This feature is not enabled*)

Table 6: Battery Charger

Parameter		Min	Type	Max	Unit
Input voltage, +5V		4.75	5.00	5.75	V
Trickle Charge Mode	**Charge Current at trickle mode as percent of fast charge mode)**		10%		
Fast Charge Mode	**Charge current at fast charge mode**	5		220	mA
V_end(Need Calibrated)	VBAT voltage when Charge End		4.2		V

5.4 Audio Characteristics

5.4.1 Analogue to Digital Converter

Table 7: Analogue to Digital Converter (single-ended/differential audio input)

Parameter	Ccnditions	Min	Type	Max	Unit
Resolution	-	-	-	24	Bits
Output Sample Rate, F_{sample}	-	8	-	384	KHz
Input level		-	200		mV_{rms}
SNR		-	100	-	dB

5.4.2 Digital to Analogue Converter

Table 8: Digital to Analogue Converter （differential audio output）

Parameter	Ccnditions			Min	Type	Max	Unit
DAC Diff. Output	With 600ohm loading			-	-	1.0	Vrms
Amplitude	With 16ohm loading			-	-	0.8	Vrms
SNR	f_{in} = 1kHz	F_{sample}	Load		104		dB

6. MSL &ESD Protection

Table 9: MSL and ESD

Parameter	Class	Max Rating
MSL grade(with JEDEC J-STD-020)		MSL 3
Human Body Model Contact Discharge per ANSI/ESDA/JEDEC JS-001	2	2kV(all pins)
Charged Device Model Contact Discharge per JEDEC/EIA JESD22-C101	III	500V (all pins)

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below **Table 10** and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below **Table 10**, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Table 10: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated@ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

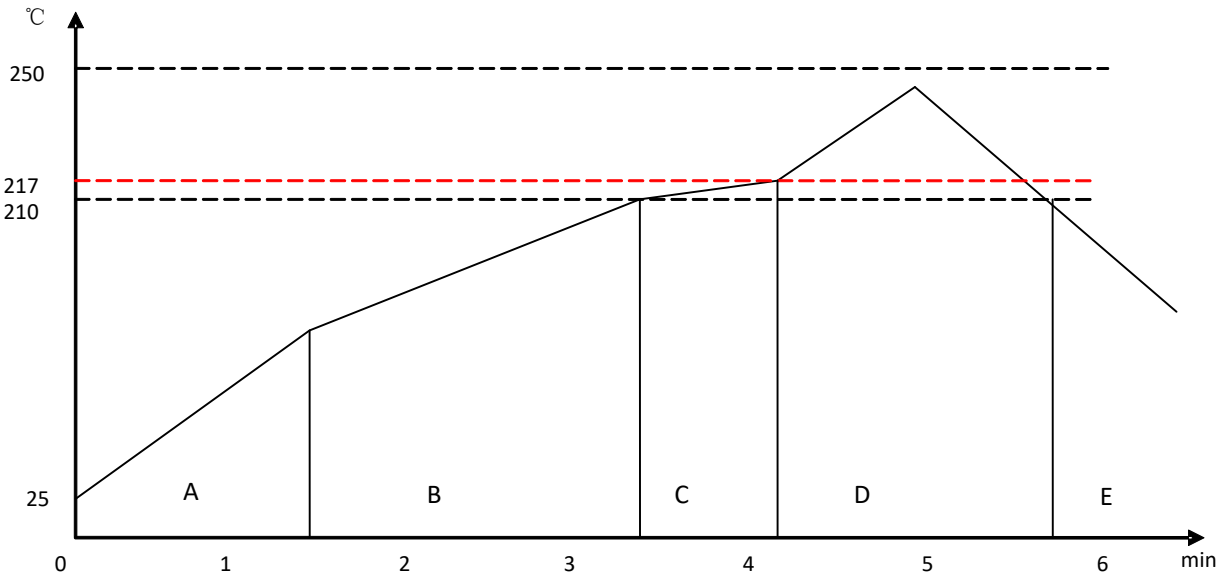


Figure 5: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. PCB layout

- Dimension: 13mm(W) x 26.9mm(L) x 1.8mm(H) Tolerance: ±0.2mm
- Module size: 13mm X 26.9mm Tolerance: ±0.2mm
- Pad size: 1.6mmX0.6mm Tolerance: ±0.2mm
- Pad pitch: 1.0mm Tolerance: ±0.1mm

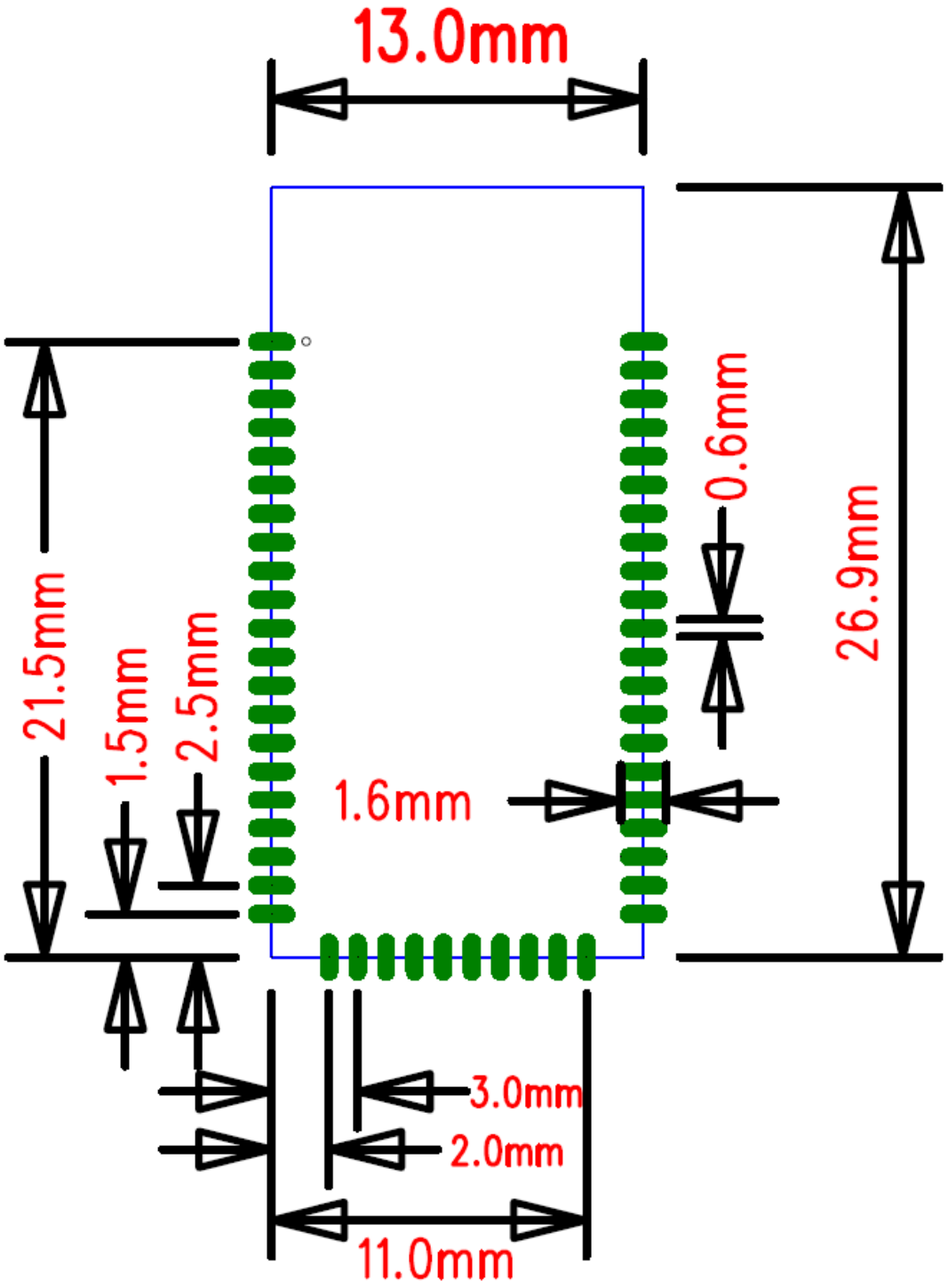


Figure 8: FSC-BT1036C pad

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT1036C is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

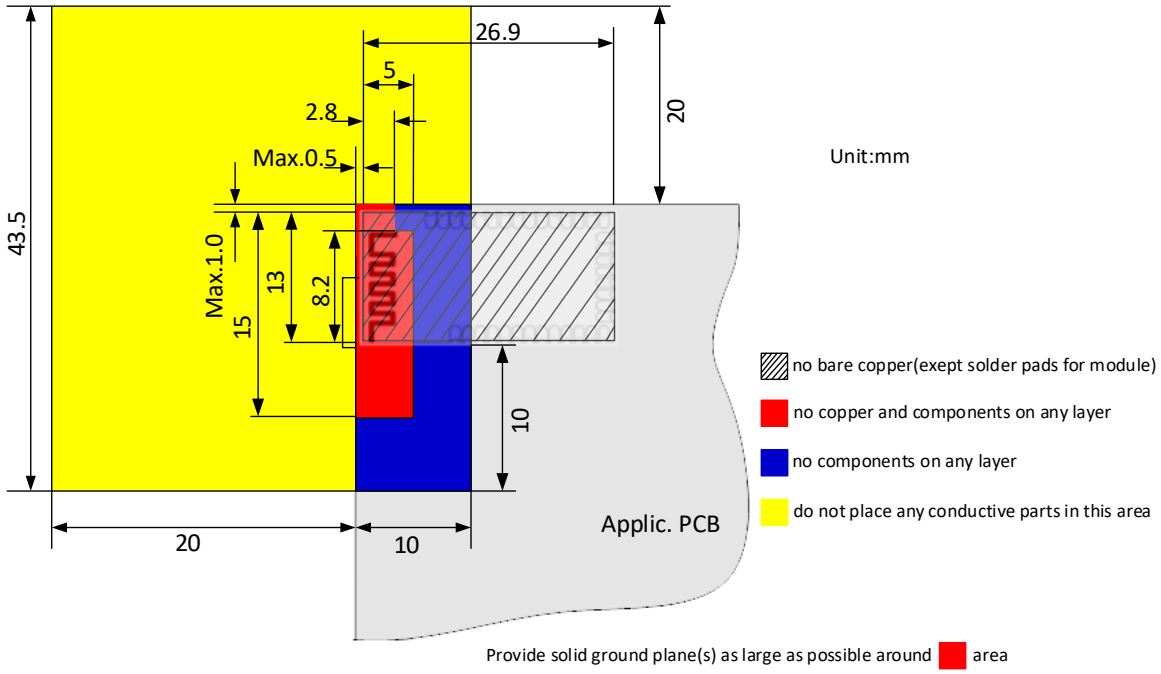


Figure 9: FSC-BT1036C Restricted Area

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in **Figure** below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

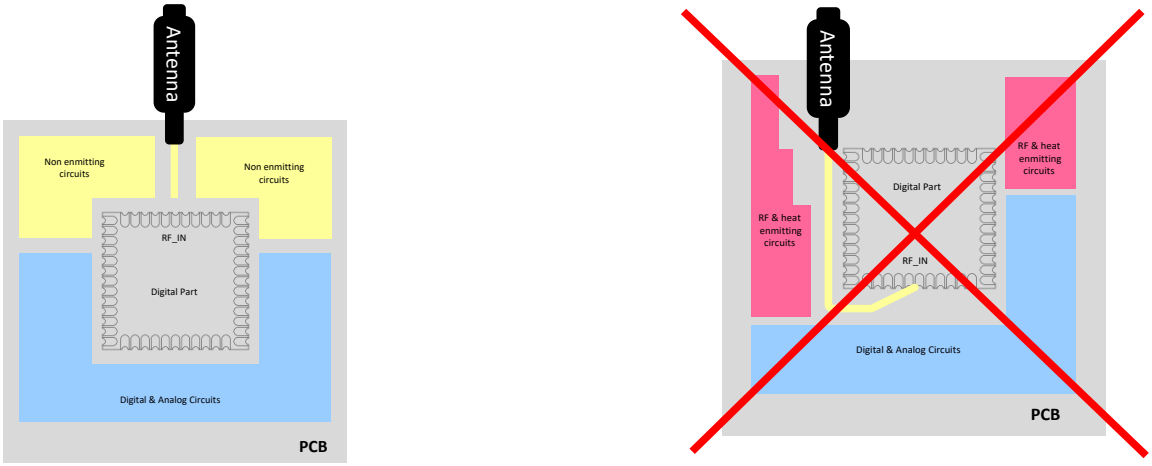


Figure 10: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

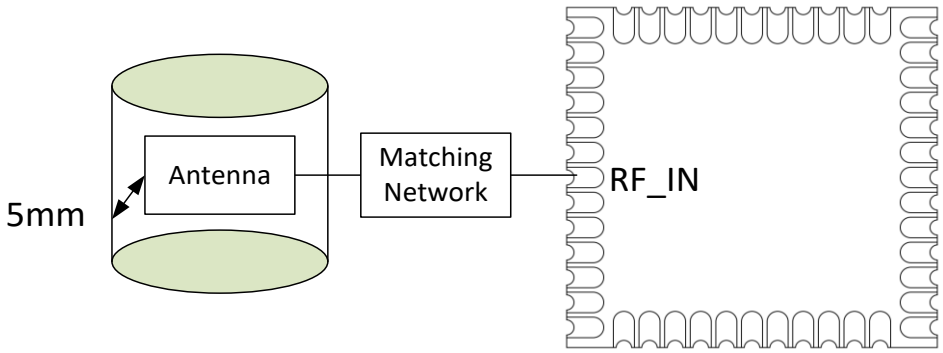


Figure 11: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.

- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

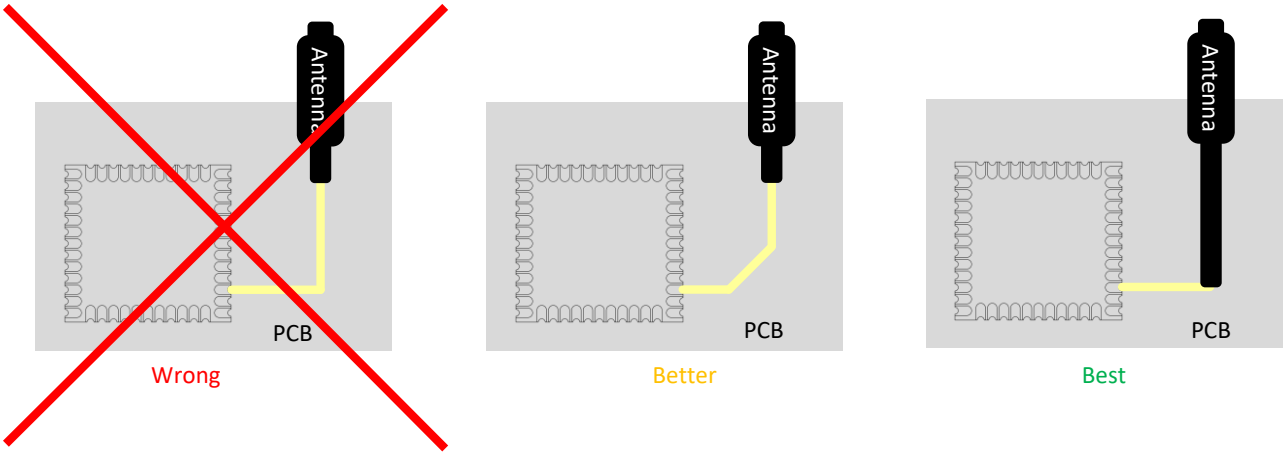


Figure 12: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10. PRODUCT PACKAGING INFORMATIONM(For reference only)

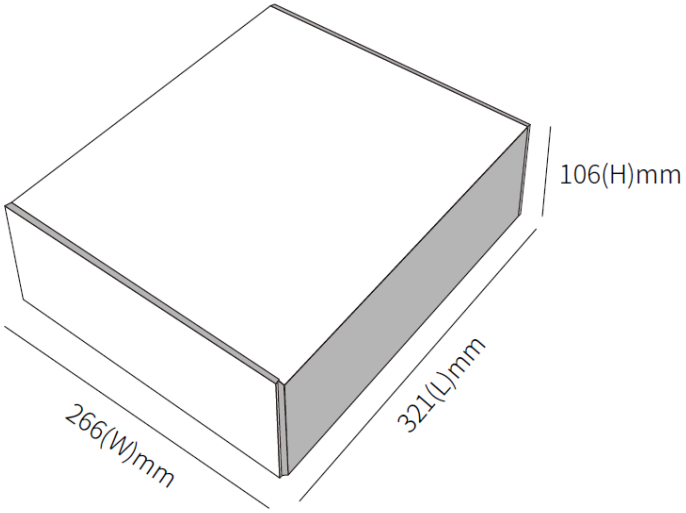
10.1 DefaultPacking

a, Tray vacuumzhi

b, Tray Dimension: 180mm * 195mm

Figure 13: Tray vacuum

10.2 Packing box(Optional)



* If require any other packing, must be confirmed with customer

* Package: 2000PCS Per Carton (Min Carton Package)

Figure 14: Packing Box