SUNRISE Technology

SPECIFICATION

SPEC. NO. : _____ **REV :** 1.0

DATE : 2021.07.22

PRODUCT NAME : AI00240

Bluetooth Low Energy 5.0 Module

	APPROVED	CHECKED	PREPARED	DCC ISSUE
NAME				

INDEX

Bluetooth Low Energy 5.0 Module

Key Features

- Bluetooth 5, 2 Mbps, CSA #2, Advertising Extensions
- 64 MHz ARM® Cortex-M4F processor
- 512 KB Flash + 64 KB RAM
- Software stacks available as downloads
- Supports 1 Mbps and 2 Mbps Bluetooth LE modes
- 100 dB link budget
- Sensitivity of -96 dbm for Bluetooth LE
- Programmable output power +4 dBm to -20 dBm
- RSSI with 1 dB resolution
- Flexible and configurable 32 pin GPIO
- Programmable Peripheral Interface – PPI
- Automatic smart power management
- Full set of digital interfaces including: SPI/2-wire/I²S/UART/PDM/QDEC with EasyDMA
- 12-bit/200 ksps ADC
- 128-bit AES ECB/CCM/AAR co-processor
- Integrated balun with 50 Ω single-ended output
- Ultra low-power 32 kHz crystal and RC oscillators
- Wide supply voltage range (1.7 V to 3.6 V)
- On-chip DC/DC buck converter
- Individual power management for all peripherals
- 2 channels 4 levels Low Voltage Detector

Power Supply

- VDD input is 1.7V to 3.6V

Antenna

- Printed Antenna

Temperature

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

Applications

- IoT
  - Home automation
  - Sensor networks
  - Building automation
- Personal Area Networks
  - Health / fitness sensor and monitor device
  - Medical devices
  - Key-fobs and wrist watches
- Interactive entertainment devices
  - Remote control
  - Gaming controller
- Beacons
- A4WP wireless chargers and devices
- Remote control toys
- Computer peripherals and I/O devices
  - Mouse
  - Keyboard
  - Multi-touch trackpad

1、Interface Description

1-1. PIN Diagram

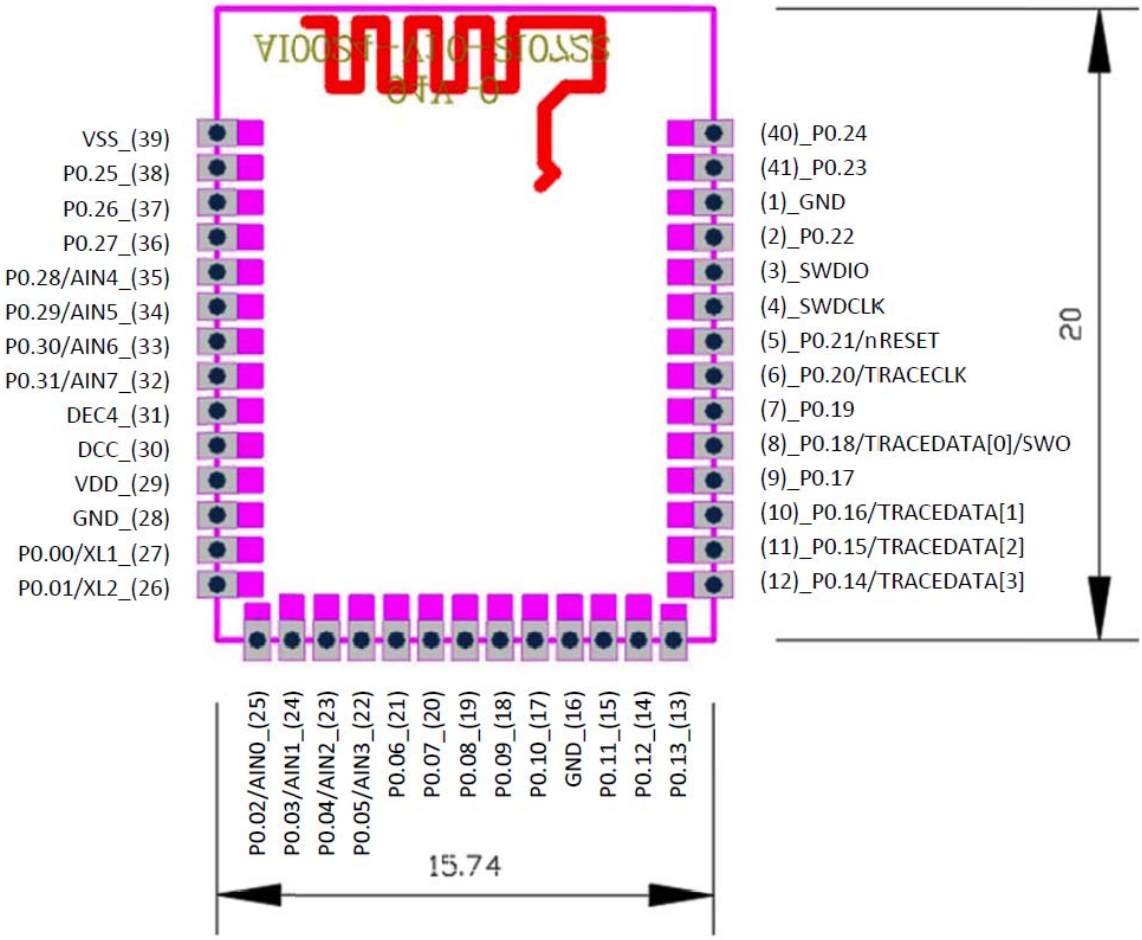


Figure1-1 AI00240 PIN Diagram

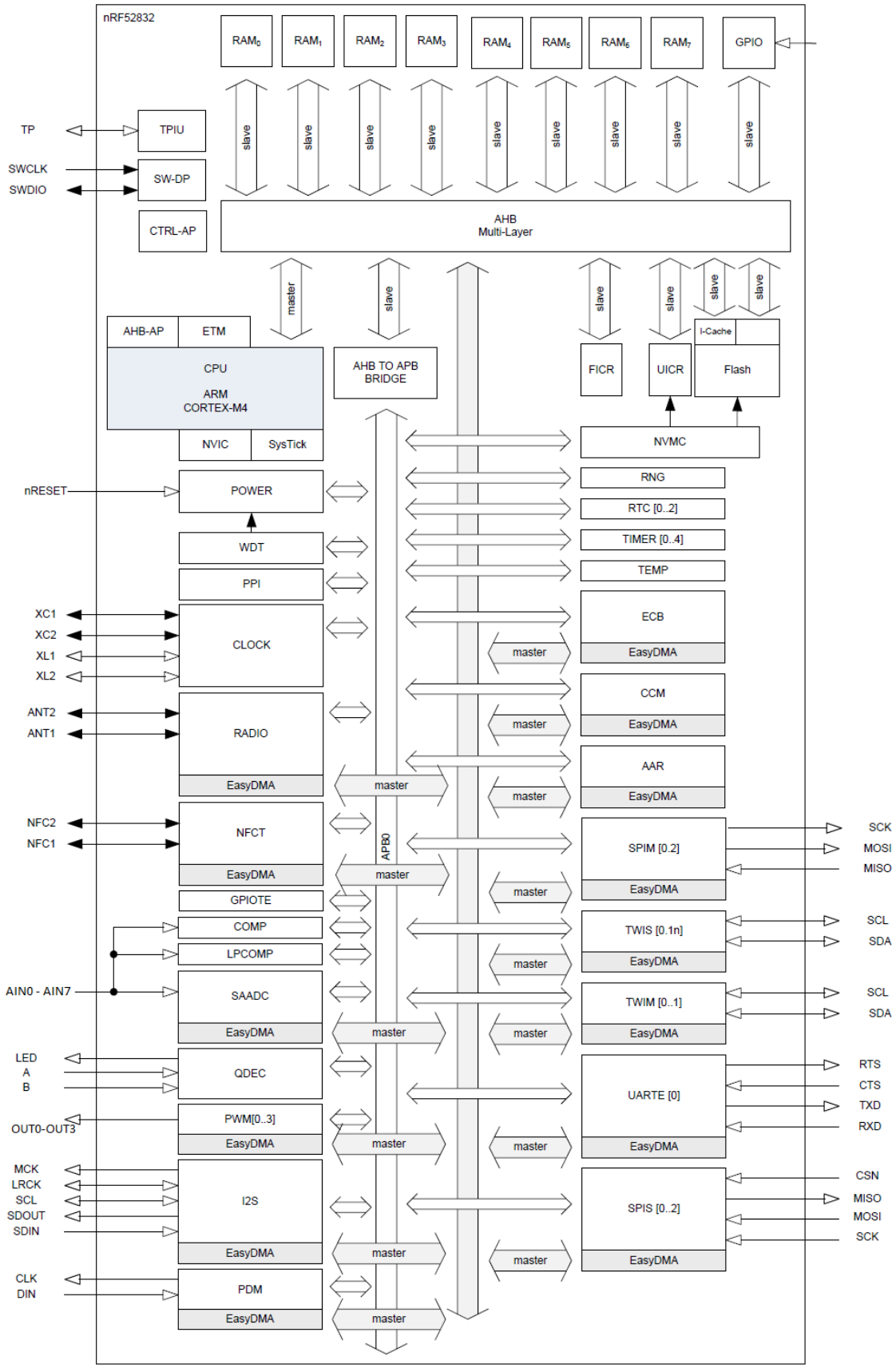
1-2. PIN Description

Table1-3

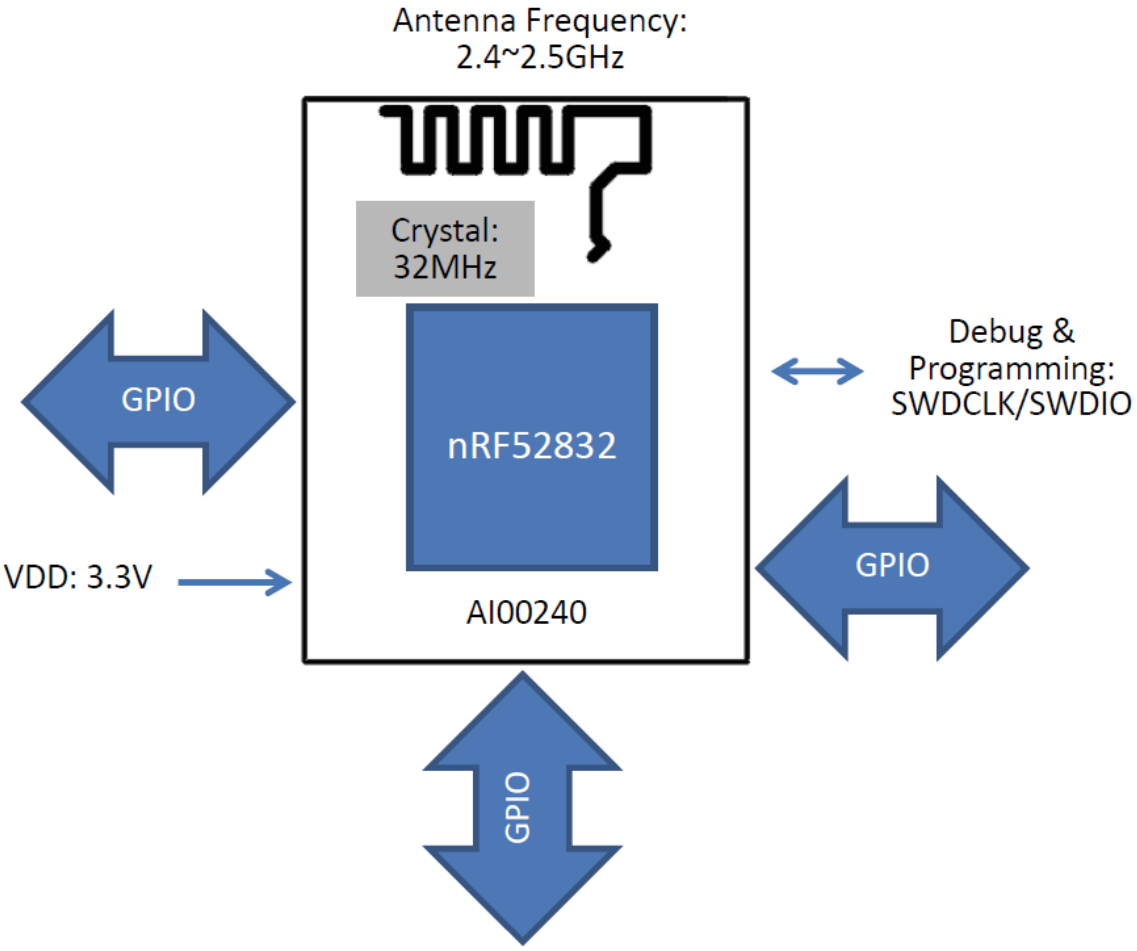
PIN NO.	Name	I/O Type	Function Description	Other Function
1	GND	G	The pad must be connected to a solid ground plane	
2	P0.22	I/O	General-purpose digital I/O	
3	SWDIO	I/O	Serial Wire debug I/O for debug and programming	
4	SWDCLK	I	Serial Wire debug clock input for debug and programming	
5	P0.21	I/O	General-purpose digital I/O	RESET Configurable as system RESET pin
6	P0.20	I/O	General-purpose digital I/O	TraceCLK Trace port clock output
7	P0.19	I/O	General-purpose digital I/O	
8	P0.18	I/O	General-purpose digital I/O	
9	P0.17	I/O	General-purpose digital I/O	TraceData(0) Trace port output
10	P0.16	I/O	General-purpose digital I/O	TraceData(2) Trace port output
11	P0.15	I/O	General-purpose digital I/O	TraceData(1) Trace port output
12	P0.14	I/O	General-purpose digital I/O	TraceData(3) Trace port output
13	P0.13	I/O	General-purpose digital I/O	
14	P0.12	I/O	General-purpose digital I/O	
15	P0.11	I/O	General-purpose digital I/O	
16	GND	G	General-purpose digital I/O	
17	P0.10	I/O	General-purpose digital I/O	
18	P0.09	I/O	General-purpose digital I/O	
19	P0.08	I/O	General-purpose digital I/O	

20	P0.07	I/O	General-purpose digital I/O	
21	P0.06	I/O	General-purpose digital I/O	
22	P0.05	I/O	General-purpose digital I/O	AIN3_Analog input SAADC/COMP/LPCOMP input
23	P0.04	I/O	General-purpose digital I/O	AIN2_Analog input SAADC/COMP/LPCOMP input
24	P0.03	I/O	General-purpose digital I/O	AIN1_Analog input SAADC/COMP/LPCOMP input
25	P0.02	I/O	General-purpose digital I/O	AIN0_Analog input SAADC/COMP/LPCOMP input
26	P0.01	I/O	General-purpose digital I/O	XL2_Analog input Connection to 32.768khz crystal (LFXO)
27	P0.00	I/O	General-purpose digital I/O	XL1_Analog input Connection to 32.768khz crystal (LFXO)
28	GND	G	The pad must be connected to a solid ground plane	
29	VCC	P	Power-supply pin	
30	DCC	P	DC/DC converter output pin	
31	DEC4	P	1V3 regulator supply decoupling. Input from DC/DC converter. Output from 1V3 LDO .	
32	P0.31	I/O	General-purpose digital I/O	AIN7_ Analog input SAADC/COMP/LPCOMP input
33	P0.30	I/O	General-purpose digital I/O	AIN6_ Analog input SAADC/COMP/LPCOMP input
34	P0.29	I/O	General-purpose digital I/O	AIN5_ Analog input General-purpose digital I/O
35	P0.28	I/O	General-purpose digital I/O	AIN4_ Analog input SAADC/COMP/LPCOMP input
36	P0.27	I/O	General-purpose digital I/O	
37	P0.26	I/O	General-purpose digital I/O	
38	P0.25	I/O	General-purpose digital I/O	
39	GND	G	The pad must be connected to a solid ground plane	
40	P0.24	I/O	General-purpose digital I/O	
41	P0.23	I/O	General-purpose digital I/O	

1-3. MCU(nRF52832) Block Diagram



1-4. Module Block Diagram



2、Electrical Specification

Any technical spec shall refer to Nordic's official documents as final reference. Contents below are from "nRF52832 Product Specification v1.4", please click to download full spec.

2-1. Absolute maximum ratings

	Min.	Max.	Unit
Supply voltages			
VDD	-0.3	+3.9	V
VSS		0	V
I/O pin voltage			
VI/O, VDD ≤3.6 V	-0.3	VDD + 0.3 V	V
Environmental QFN48, 6×6 mm package			
Storage temperature	-40	+125	°C
MSL (moisture sensitivity level)		2	
ESD HBM (human body model)		4	kV
ESD CDM (charged device model)		1000	V
Flash memory			
Endurance	10 000		Write/erase cycles
Retention	10 years at 40°C		

2-2. Operation Condition

Symbol	Parameter	Notes	Min.	Nom.	Max.	Units
VDD	Supply voltage, independent of DCDC enable		1.7	3.0	3.6	V
tR_VDD	Supply rise time (0 V to 1.7 V)				60	ms
TA	Operating temperature		-40	25	85	°C

Important: The on-chip power-on reset circuitry may not function properly for rise times longer than the specified maximum.

2-3. General Radio Characteristics

Symbol	Description	Min.	Typ.	Max.	Units
fOP	Operating frequencies	2360		2500	MHz
fPLL,PROG,RES	PLL programming resolution		2		kHz
fPLL,CH,SP	PLL channel spacing		1		MHz
fDELTA,1M	Frequency deviation @ 1 Msps		±170		kHz
fDELTA,BLE,1M	Frequency deviation @ BLE 1Msps		±250		kHz
fDELTA,2M	Frequency deviation @ 2 Msps		±320		kHz
fDELTA,BLE,2M	Frequency deviation @ BLE 2 Msps		±500		kHz
fskSPS	On-the-air data rate	1		2	Msps

2-4. Radio Current Consumption (Transmitter)

Symbol	Description	Min.	Typ.	Max.	Units
ITX,PLUS4Dbm,DCDC	TX only run current (DCDC, 3V) PRF =+4 dBm		7.5		mA
ITX,PLUS4Dbm	TX only run current PRF = +4 dBm		16.6		mA
ITX,0Dbm,DCDC	TX only run current (DCDC, 3V)PRF = 0dBm		5.3		mA
ITX,0Dbm	TX only run current PRF = 0dBm		11.6		mA
ITX,MINUS4Dbm,DCDC	TX only run current DCDC, 3V PRF = -4dBm		4.2		mA
ITX,MINUS4Dbm	TX only run current PRF = -4 dBm		9.3		mA
ITX,MINUS8Dbm,DCDC	TX only run current DCDC, 3V PRF = -8 dBm		3.8		mA
ITX,MINUS8Dbm	TX only run current PRF = -8 dBm		8.4		mA
ITX,MINUS12Dbm,DCDC	TX only run current DCDC, 3V PRF = -12 dBm		3.5		mA
ITX,MINUS12Dbm	TX only run current PRF = -12 dBm		7.7		mA
ITX,MINUS16Dbm,DCDC	TX only run current DCDC, 3V PRF = -16 dBm		3.3		mA
ITX,MINUS16Dbm	TX only run current PRF = -16 dBm		7.3		mA
ITX,MINUS20Dbm,DCDC	TX only run current DCDC, 3V PRF = -20 dBm		3.2		mA
ITX,MINUS20Dbm	TX only run current PRF = -20 dBm		7.0		mA
ITX,MINUS40Dbm,DCDC	TX only run current DCDC, 3V PRF = -40 dBm		2.7		mA
ITX,MINUS40Dbm	TX only run current PRF = -40 dBm		5.9		mA
ISTART,TX,DCDC	TX start-up current DCDC, 3V, PRF = 4 dBm		4.0		mA
ISTART,TX	TX start-up current, PRF = 4 dBm		8.8		mA

2-5. Radio current consumption (Receiver)

Symbol	Description	Min.	Typ.	Max.	Units
IRX,1M,DCDC	RX only run current (DCDC, 3V) 1Msps / 1Msps BLE		5.4		mA
IRX,1M	RX only run current 1Msps / 1Msps BLE		11.7		mA
IRX,2M,DCDC	RX only run current (DCDC, 3V) 2Msps / 2Msps BLE		5.8		mA
IRX,2M	RX only run current 2Msps / 2Msps BLE		12.9		mA
ISTART,RX,DCDC	RX start-up current (DCDC 3V)		3.5		mA
ISTART,RX,LDO	RX start-up current (LDO 3V)		7.5		mA

2-6. Transmitter specification

Symbol	Description	Min.	Typ.	Max.	Units
PRF	Maximum output power		4	6	dBm
PRFC	RF power control range		24		dB
PRFCR	RF power accuracy			±4	dB
PRF1,1	1st Adjacent Channel Transmit Power 1 MHz (1 Msps Nordic proprietary mode)		-25		dBc
PRF2,1	2nd Adjacent Channel Transmit Power 2 MHz (1 Msps Nordic proprietary mode)		-50		dBc

PRF1,2	1st Adjacent Channel Transmit Power 2 MHz (2 Msps Nordic proprietary mode)	-25	dBc
PRF2,2	2nd Adjacent Channel Transmit Power 4 MHz (2 Msps Nordic proprietary mode)	-50	dBc
PRF1,2,BLE	1st Adjacent Channel Transmit Power 2 MHz (2 Msps BLE mode)	-20	dBc
PRF2,2,BLE	2nd Adjacent Channel Transmit Power 4 MHz (2 Msps BLE mode)	-50	dBc

2-7. Receiver operation

Symbol	Description	Min.	Typ.	Max.	Units
PRX,MAX	Maximum received signal strength at < 0.1% BER		0		dBm
PSENS,IT,1M	Sensitivity, 1Msps nRF mode[1]		-93		dBm
PSENS,IT,SP,1M,BLE	Sensitivity, 1Msps BLE ideal transmitter, <=37 bytes BER=1E-3[2]		-96		dBm
PSENS,IT,LP,1M,BLE	Sensitivity, 1Msps BLE ideal transmitter >=128 bytes BER=1E-43[3]		-95		dBm
PSENS,IT,2M	Sensitivity, 2Msps nRF mode[4]		-89		dBm

1 Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR[1…7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3dB.

2 As defined in the Bluetooth Core Specification v4.0 Volume 6: Core System Package (Low Energy Controller Volume)

3 Equivalent BER limit < 10E-04

4 Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR[1…7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3dB.

5

Symbol	Description	Min.	Typ.	Max.	Units
PSENS,IT,SP,2M,BLE	Sensitivity, 2Msps BLE ideal transmitter, Packet length <=37bytes		-93		dBm
PSENS,DT,SP,2M,BLE	Sensitivity, 2Msps BLE dirty transmitter, Packet length <=37bytes		-93		dBm
PSENS,IT,LP,2M,BLE	Sensitivity, 2Msps BLE ideal transmitter >= 128bytes		-92		dBm
PSENS,DT,LP,2M,BLE	Sensitivity, 2Msps BLE dirty transmitter, Packet length >= 128bytes		-92		dBm

2-8. RX selectivity

RX selectivity with equal modulation on interfering signal[1]

Symbol	Description	Min.	Typ.	Max.	Units
C/I1M,co-channel	1Msps mode, Co-Channel interference		9		dB
C/I1M,-1MHz	1 Msps mode, Adjacent (-1 MHz) interference		-2		dB
C/I1M,+1MHz	1 Msps mode, Adjacent (+1 MHz) interference		-10		dB
C/I1M,-2MHz	1 Msps mode, Adjacent (-2 MHz) interference		-19		dB
C/I1M,+2MHz	1 Msps mode, Adjacent (+2 MHz) interference		-42		dB
C/I1M,-3MHz	1 Msps mode, Adjacent (-3 MHz) interference		-38		dB
C/I1M,+3MHz	1 Msps mode, Adjacent (+3 MHz) interference		-48		dB
C/I1M,±6MHz	1 Msps mode, Adjacent (≥6 MHz) interference		-50		dB
C/I1MBLE,co-channel	1 Msps BLE mode, Co-Channel interference		6		dB

C/I1MBLE,-1MHz	1 Msps BLE mode, Adjacent (-1 MHz) interference	-2	dB
C/I1MBLE,+1MHz	1 Msps BLE mode, Adjacent (+1 MHz) interference	-9	dB
C/I1MBLE,-2MHz	1 Msps BLE mode, Adjacent (-2 MHz) interference	-22	dB
C/I1MBLE,+2MHz	1 Msps BLE mode, Adjacent (+2 MHz) interference	-46	dB
C/I1MBLE,>3MHz	1 Msps BLE mode, Adjacent (≥3 MHz) interference	-50	dB
C/I1MBLE,image	Image frequency Interference	-22	dB
C/I1MBLE,image,1M	Adjacent (1 MHz) interference to in-band image frequency	-35	dB
C/I2M,co-channel	2Msps mode, Co-Channel interference	10	dB
C/I2M,-2MHz	2 Msps mode, Adjacent (-2 MHz) interference	6	dB
C/I2M,+2MHz	2 Msps mode, Adjacent (+2 MHz) interference	-14	dB
C/I2M,-4MHz	2 Msps mode, Adjacent (-4 MHz) interference	-20	dB
C/I2M,+4MHz	2 Msps mode, Adjacent (+4 MHz) interference	-44	dB
C/I2M,-6MHz	2 Msps mode, Adjacent (-6 MHz) interference	-42	dB
C/I2M,+6MHz	2 Msps mode, Adjacent (+6 MHz) interference	-47	dB
C/I2M,≥12MHz	2 Msps mode, Adjacent (≥12 MHz) interference	-52	dB
C/I2MBLE,co-channel	2 Msps BLE mode, Co-Channel interference	7	dB
C/I2MBLE,±2MHz	2 Msps BLE mode, Adjacent (±2 MHz) interference	0	dB
C/I2MBLE,±4MHz	2 Msps BLE mode, Adjacent (±4 MHz) interference	-47	dB
C/I2MBLE,≥6MHz	2 Msps BLE mode, Adjacent (≥6 MHz) interference	-49	dB
C/I2MBLE,image	Image frequency Interference	-21	dB
C/I2MBLE,image,	Adjacent (2 MHz) interference to in-band image frequency	-36	dB

[1] Wanted signal level at PIN = -67 dBm. One interferer is used, having equal modulation as the wanted signal. The input power of the interferer where the sensitivity equals BER = 0.1% is presented

2-9. RX intermodulation

RX intermodulation[1]

Symbol	Description	Min.	Typ.	Max.	Units
PIMD,1M	IMD performance, 1 Msps (3 MHz, 4 MHz, and 5 MHz offset)		-33		dBm
PIMD,1M,BLE	IMD performance, BLE 1 Msps (3 MHz, 4 MHz, and 5 MHz offset)		-30		dBm
PIMD,2M	IMD performance, 2 Msps (6 MHz, 8 MHz, and 10 MHz offset)		-33		dBm

[1] Wanted signal level at PIN = -64 dBm. Two interferers with equal input power are used. The interferer closest in frequency is not modulated, the other interferer is modulated equal with the wanted signal. The input power of the interferers where the sensitivity equals BER = 0.1% is presented.

[2]

Symbol	Description	Min.	Typ.	Max.	Units
PIMD,2M,BLE	IMD performance, BLE 2 Msps (6 MHz, 8 MHz, and 10 MHz offset)		-32		dBm

2-10. Radio timing

Symbol	Description	Min.	Typ.	Max.	Units
tTXEN	Time between TXEN task and READY event after		140		us

	channel FREQUENCY configured		
$t_{TXEN,FAST}$	Time between TXEN task and READY event after channel FREQUENCY configured (Fast Mode)	40	us
$t_{TXDISABLE}$	Time between DISABLE task and DISABLED event when the radio was in TX and mode is set to 1Msps	6	us
$t_{TXDISABLE,2M}$	Time between DISABLE task and DISABLED event when the radio was in TX and mode is set to 2Msps	4	us
t_{RXEN}	Time between the RXEN task and READY event after channel FREQUENCY configured in default mode	140	us
$t_{RXEN,FAST}$	Time between the RXEN task and READY event after channel FREQUENCY configured in fast mode	40	us
t_{SWITCH}	The minimum time taken to switch from RX to TX or TX to RX (channel FREQUENCY unchanged)	20	us
$t_{RXDISABLE}$	Time between DISABLE task and DISABLED event when the radio was in RX	0	us
$t_{TXCHAIN}$	TX chain delay	0.6	us
$t_{RXCHAIN}$	RX chain delay	9.4	us
$t_{RXCHAIN,2M}$	RX chain delay in 2Msps mode	5	us

2-11. Received Signal Strength Indicator (RSSI) specifications

Symbol	Description	Min.	Typ.	Max.	Units
$RSSI_{ACC}$	RSSI Accuracy Valid range -90 to -20 dBm		±2		dB
$RSSI_{RESOLUTION}$	RSSI resolution		1		dB
$RSSI_{PERIOD}$	Sample period		0.25		us

2-12. Jitter

Symbol	Description	Min.	Typ.	Max.	Units
$t_{DISABLEDJITTER}$	Jitter on DISABLED event relative to END event when shortcut between END and DISABLE is enabled.		0.25		us
$t_{READYJITTER}$	Jitter on READY event relative to TXEN and RXEN task.		0.25		us

2-13. Delay when disabling the RADIO

Symbol	Description	Min.	Typ.	Max.	Units
$t_{TXDISABLE,1M}$	Disable delay from TX. Delay between DISABLE and DISABLED for MODE = Nrf_1Mbit and MODE = Ble_1Mbit		6		us
$t_{RXDISABLE,1M}$	Disable delay from RX. Delay between DISABLE and DISABLED for MODE = Nrf_1Mbit and MODE = Ble_1Mbit		0		us

2-14. CPU performance

The CPU clock speed is 64 MHz. Current and efficiency data is taken when in System ON and the CPU is executing the CoreMark™ benchmark. It includes power regulator and clock base currents. All other blocks are IDLE.

Symbol	Description	Min.	Typ.	Max.	Units
W_{FLASH}	CPU wait states, running from flash, cache disabled	0		2	
$W_{FLASHCACHE}$	CPU wait states, running from flash, cache enabled	0		3	
W_{RAM}	CPU wait states, running from RAM			0	
$I_{DDFLASHCACHE}$	CPU current, running from flash, cache enabled, LDO		7.4		mA
$I_{DDFLASHCACHEDCDC}$	CPU current, running from flash, cache enabled, DCDC 3V		3.7		mA
$I_{DDFLASH}$	CPU current, running from flash, cache disabled, LDO		8.0		mA
$I_{DDFLASHDCDC}$	CPU current, running from flash, cache disabled, DCDC 3V		3.9		mA
I_{DDRAM}	CPU current, running from RAM, LDO		6.7		mA
$I_{DDRAMDCDC}$	CPU current, running from RAM, DCDC 3V		3.3		mA
$I_{DDFLASH/MHz}$	CPU efficiency, running from flash, cache enabled, LDO		125		µA/ MHz
$I_{DDFLASHDCDC/MHz}$	CPU efficiency, running from flash, cache enabled, DCDC 3V		58		µA/ MHz
CMFLASH	CoreMark5, running from flash, cache enabled		215		Core
CMFLASH/MHz	CoreMark per MHz, running from flash, cache enabled		3.36		Core MHz
CMFLASH/mA	CoreMark per mA, running from flash, cache enabled, DCDC 3V		58		Core mA

3、GPIO — General purpose input/output

The general purpose input/output (GPIO) is organized as one port with up to 32 I/Os (dependent on package) enabling access and control of up to 32 pins through one port. Each GPIO can be accessed individually.
GPIO has the following user-configurable features:

- Up to 32 GPIO
- 8 GPIO with Analog channels for SAADC, COMP or LPCOMP inputs
- Configurable output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on state changes on any pin
- All pins can be used by the PPI task/event system
- One or more GPIO outputs can be controlled through PPI and GPIOTE channels
- All pins can be individually mapped to interface blocks for layout flexibility
- GPIO state changes captured on SENSE signal can be stored by LATCH register

The GPIO Port peripheral implements up to 32 pins, PIN0through PIN31. Each of these pins can be individually configured in the PIN_CNF[n] registers (n=0..31).

The following parameters can be configured through these registers:

- Direction
- Drive strength
- Enabling of pull-up and pull-down resistors
- Pin sensing
- Input buffer disconnect
- Analog input (for selected pins)

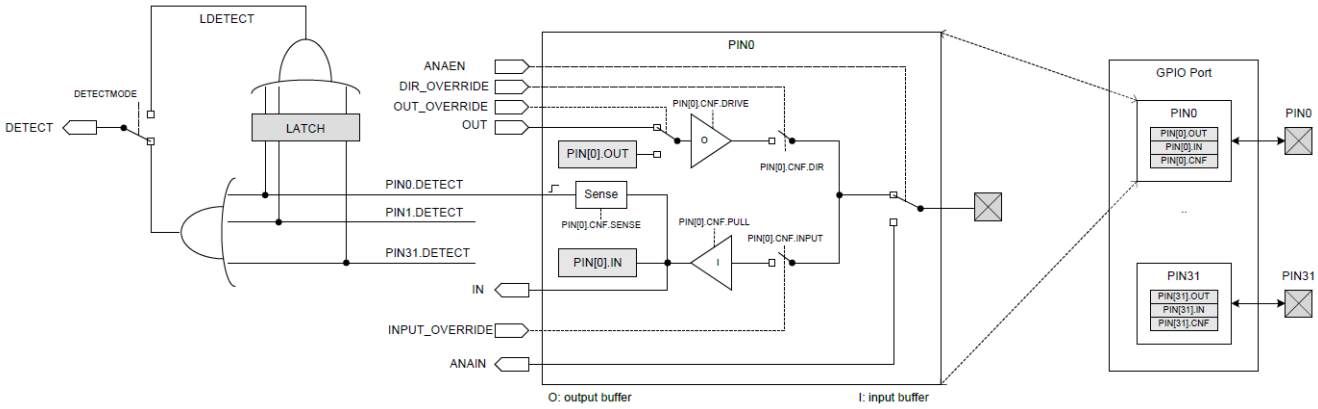


Figure: GPIO Port and the GPIO pin details

GPIO Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage	0.7 x VDD		VDD	V
V_{IL}	Input low voltage	VSS		0.3 x VDD	V
$V_{OH,SD}$	Output high voltage, standard drive, 0.5 mA, VDD ≥1.7	VDD-0.4		VDD	V
$V_{OH,HDH}$	Output high voltage, high drive, 5 mA, VDD >= 2.7 V	VDD-0.4		VDD	V
$V_{OH,HDL}$	Output high voltage, high drive, 3 mA, VDD >= 1.7 V	VDD-0.4		VDD	V
$V_{OL,SD}$	Output low voltage, standard drive, 0.5 mA, VDD ≥1.7	VSS		VSS+0.4	V
$V_{OL,HDH}$	Output low voltage, high drive, 5 mA, VDD >= 2.7 V	VSS		VSS+0.4	V
$V_{OL,HDL}$	Output low voltage, high drive, 3 mA, VDD >= 1.7 V	VSS		VSS+0.4	V
$I_{OL,SD}$	Current at VSS+0.4 V, output set low, standard drive, VDD ≥1.7	1	2	4	mA
$I_{OL,HDH}$	Current at VSS+0.4 V, output set low, high drive, VDD >= 2.7 V	6	10	15	mA
$I_{OL,HDL}$	Current at VSS+0.4 V, output set low, high drive, VDD >= 1.7 V	3			mA
$I_{OH,SD}$	Current at VDD-0.4 V, output set high, standard drive, VDD ≥1.7	1	2	4	mA
$I_{OH,HDH}$	Current at VDD-0.4 V, output set high, high drive, VDD >= 2.7 V	6	9	14	mA
$I_{OH,HDL}$	Current at VDD-0.4 V, output set high, high drive, VDD >= 1.7 V	3			mA
$t_{RF,15pF}$	Rise/fall time, low drive mode, 10-90%, 15 pF load[1]		9		ns
$t_{RF,25pF}$	Rise/fall time, low drive mode, 10-90%, 25 pF load[1]		13		ns
$t_{RF,50pF}$	Rise/fall time, low drive mode, 10-90%, 50 pF load[1]		25		ns
$t_{HRF,15pF}$	Rise/Fall time, high drive mode, 10-90%, 15 pF load[1]		4		ns
$t_{HRF,25pF}$	Rise/Fall time, high drive mode, 10-90%, 25 pF load[1]		5		ns
$t_{HRF,50pF}$	Rise/Fall time, high drive mode, 10-90%, 50 pF load[1]		8		ns
R_{PU}	Pull-up resistance	11	13	16	kΩ
R_{PD}	Pull-down resistance	11	13	16	kΩ
C_{PAD}	Pad capacitance		3		pF
C_{PAD_NFC}	Pad capacitance on NFC pads		4		pF
I_{NFC_LEAK}	Leakage current between NFC pads when driven to different states		2	10	µA

The current drawn from the battery when GPIO is active as an output is calculated as follows: $I_{GPIO}=V_{DD}\ C_{load}\ f$
C_{load} being the load capacitance and “f” is the switching frequency.

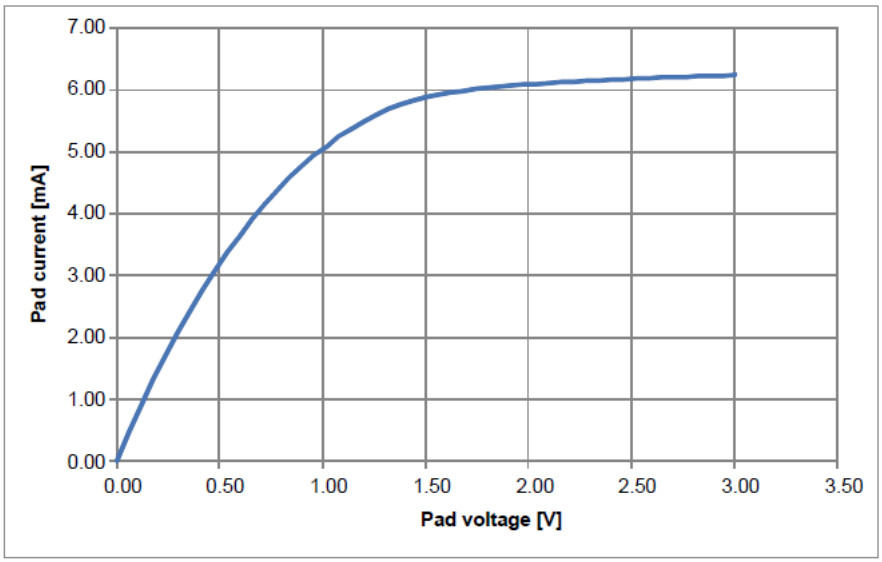


Figure: GPIO drive strength vs Voltage, standard drive, VDD = 3.0 V

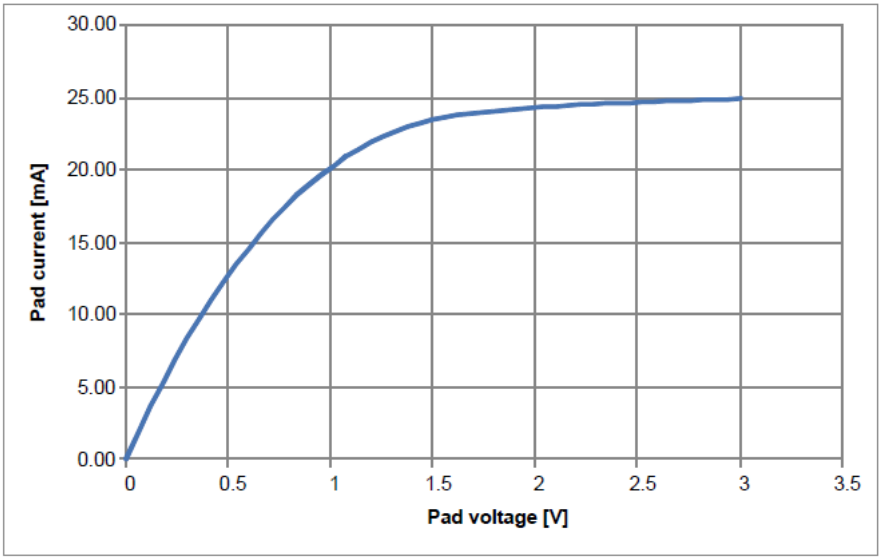


Figure: GPIO drive strength vs Voltage, high drive, VDD = 3.0 V

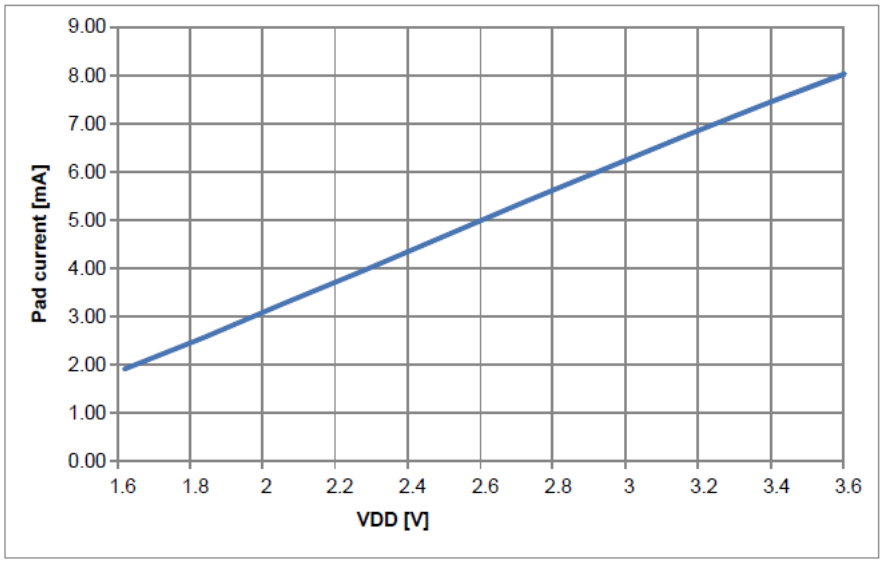


Figure: Max sink current vs Voltage, standard drive

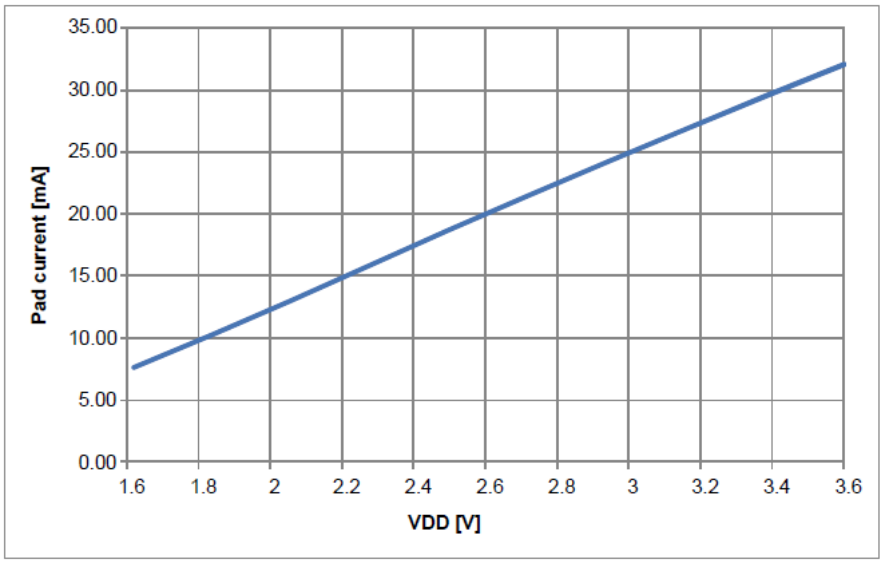


Figure: Max sink current vs Voltage, high drive

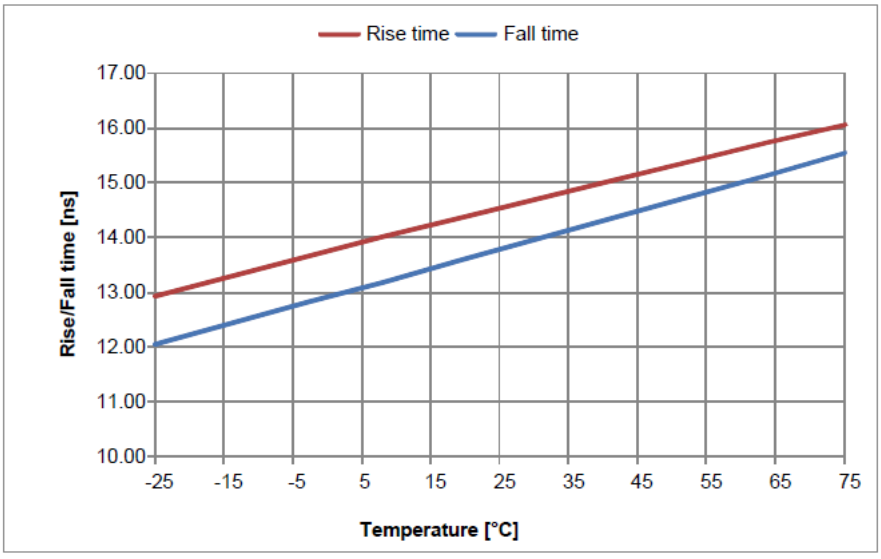


Figure: Rise and fall time vs Temperature, 10%-90%, 25pF load capacitance, VDD = 3.0 V

4、RADIO — 2.4 GHz Radio

The RADIO contains a 2.4 GHz radio receiver and a 2.4 GHz radio transmitter that is compatible with Nordic's proprietary 1 Mbps and 2 Mbps radio modes in addition to 1 Mbps and 2 Mbps *Bluetooth*® low energy mode.

EasyDMA in combination with an automated packet assembler and packet disassembler, and an automated CRC generator and CRC checker, makes it very easy to configure and use the RADIO. See *Figure: RADIO block diagram* on page 205 for details.

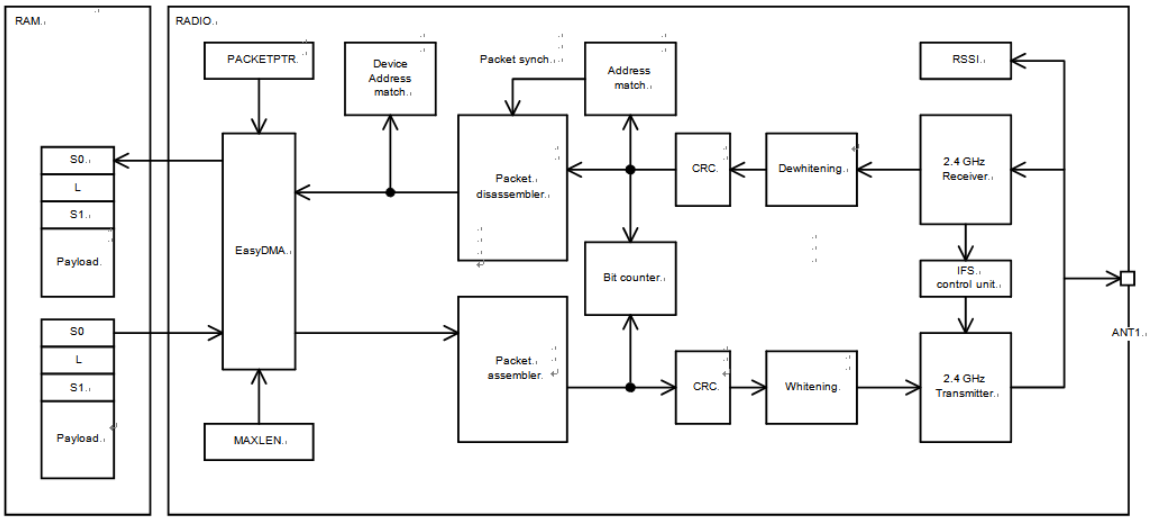


Figure: RADIO block diagram

General Radio Characteristics

Symbol	Description	Min.	Typ.	Max.	Units
f_{OP}	Operating frequencies	2360		2500	MHz
$f_{PLL,PROG,RES}$	PLL programming resolution		2		kHz
$f_{PLL,CH,SP}$	PLL channel spacing		1		MHz
$f_{DELTA,1M}$	Frequency deviation @ 1 Msps		±170		kHz

$f_{DELTA,BLE,1M}$	Frequency deviation @ BLE 1Msps		±250	kHz
$f_{DELTA,2M}$	Frequency deviation @ 2 Msps		±320	kHz
$f_{DELTA,BLE,2M}$	Frequency deviation @ BLE 2 Msps		±500	kHz
f_{skSPS}	On-the-air data rate	1	2	Msps

5、SPI — Serial peripheral interface master

The SPI master provides a simple CPU interface which includes a TXD register for sending data and an RXD register for receiving data. This section is added for legacy support for now.

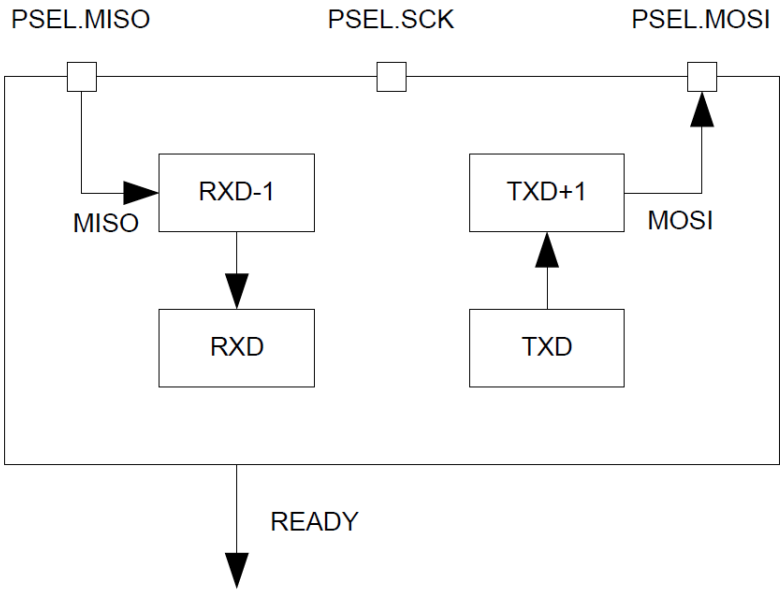


Figure: SPI master

RXD-1 and TXD+1 illustrate the double buffered version of RXD and TXD respectively.

SPI master mode pin configuration

The different signals SCK, MOSI, and MISO associated with the SPI master are mapped to physical pins.

This mapping is according to the configuration specified in the PSELSCK, PSELMOSI,

and PSELMISO registers respectively. If a value of 0xFFFFFFFF is specified in any of these registers, the associated SPI master signal is not connected to any physical pin. The PSELSCK, PSELMOSI, and PSELMISO registers and their configurations are only used as long as the SPI master is enabled, and retained only as long as the device is in ON mode. PSELSCK, PSELMOSI, and PSELMISO must only be configured when the SPI master is disabled.

To secure correct behavior in the SPI, the pins used by the SPI must be configured in the GPIO peripheral as described in *Table: GPIO configuration* on page 514 prior to enabling the SPI. The SCK must always be connected to a pin, and that pin's input buffer must always be connected for the SPI to work. This configuration must be retained in the GPIO for the selected IOs as long as the SPI is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behavior.

GPIO configuration

SPI master signal	SPI master pin	Direction	Output value
SCK	As specified in PSELSCK	Output	Same as CONFIG.CPOL
MOSI	As specified in PSELMOSI	Output	0
MISO	As specified in PSELMISO	Input	Not applicable

SPI master interface

Symbol	Description	Min.	Typ.	Max.
f_{SPI}	Bit rates for SPI[38]	8[39]	Mbps	f_{SPI}
$I_{SPI,2Mbps}$	Run current for SPI, 2 Mbps		50	µA
$I_{SPI,8Mbps}$	Run current for SPI, 8 Mbps		50	µA
$I_{SPI,IDLE}$	Idle current for SPI (STARTed, no CSN activity)	<1		µA
$t_{SPI,START,LP}$	Time from writing TXD register to transmission started, low power mode	$t_{SPI,START,CL}$ + t		µs
$t_{SPI,START,CL}$	Time from writing TXD register to transmission started, constant latency mode	1		µs

6、TWI — I²C compatible two-wire interface

The TWI master is compatible with I²C operating at 100 kHz and 400 kHz.

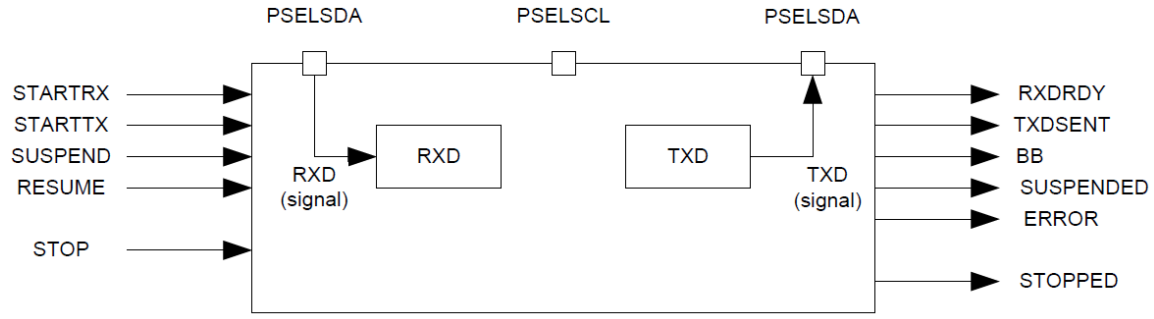


Figure: TWI master's main features

Master mode pin configuration

The different signals SCL and SDA associated with the TWI master are mapped to physical pins according to the configuration specified in the PSELSCL and PSELSDA registers respectively. If a value of 0xFFFFFFFF is specified in any of these registers, the associated TWI master signal is not connected to any physical pin. The PSELSCL and PSELSDA registers and their configurations are only used as long as the TWI master is enabled, and retained only as long as the device is in ON mode. PSELSCL and PSELSDA must only be configured when the TWI is disabled.

To secure correct signal levels on the pins used by the TWI master when the system is in OFF mode, and when the TWI master is disabled, these pins must be configured in the GPIO peripheral as described in *Table: GPIO configuration* on page 522.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behavior.

Table 125: GPIO configuration

TWI master signal	TWI master pin	Direction	Drive strength	Output value
SCL	As specified in PSELSCL	Input	S0D1	Not applicable
SDA	As specified in PSELSDA	Input	S0D1	Not applicable

TWI interface electrical specifications

Symbol	Description	Min.	Typ.	Max.	Units
f_{TWI}	Bit rates for TWI[40]	100		400	kbps
$I_{TWI,100kbps}$	Run current for TWI, 100 kbps		50		µA
$I_{TWI,400kbps}$	Run current for TWI, 400 kbps		50		µA
$t_{TWI,START,LP}$	Time from STARTRX/STARTTX task to transmission started, Low power mode		$t_{TWI,START}$ + t		µs
$t_{TWI,START,CL}$	Time from STARTRX/STARTTX task to transmission started, Constant latency mode		1.5		µs

7、UART — Universal asynchronous receiver/ transmitter

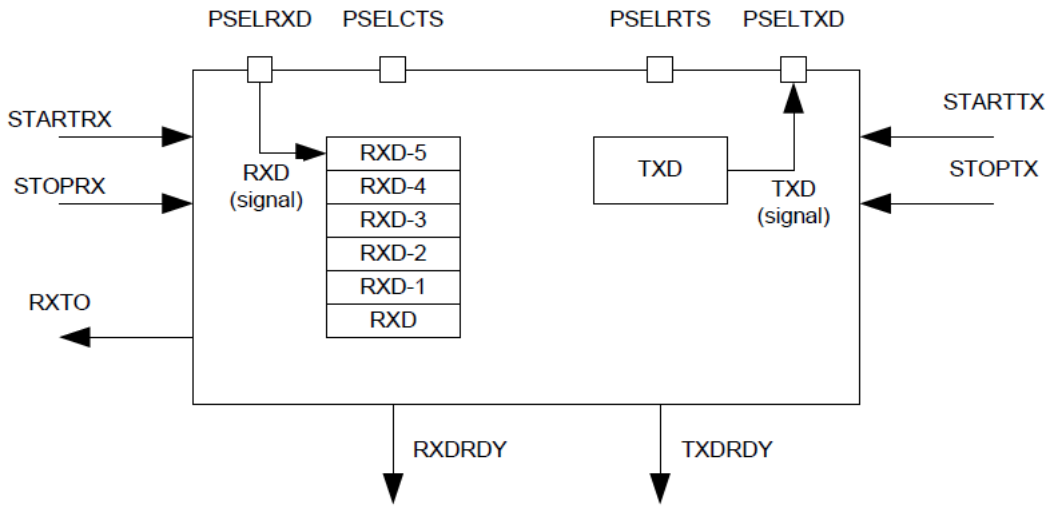


Figure 160: UART configuration

Pin configuration

The different signals RXD, CTS (Clear To Send, active low), RTS (Request To Send, active low), and TXD associated with the UART are mapped to physical pins according to the configuration specified in the PSELRXD, PSELCTS, PSELRTS, and PSELTXD registers respectively.

If a value of 0xFFFFFFFF is specified in any of these registers, the associated UART signal will not be connected to any physical pin. The PSELRXD, PSELCTS, PSELRTS, and PSELTXD registers and their configurations are only used as long as the UART is enabled, and retained only for the duration the device is in ON mode. PSELRXD, PSELCTS, PSELRTS and PSELTXD must only be configured when the UART is disabled.

To secure correct signal levels on the pins by the UART when the system is in OFF mode, the pins must be configured in the GPIO peripheral as described in *Pin configuration* on page 531.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 128: GPIO configuration

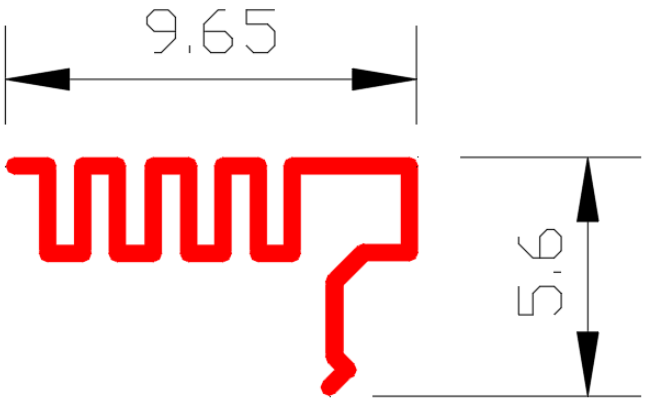
UART pin	Direction	Output value
RXD	Input	Not applicable
CTS	Input	Not applicable
RTS	Output	1
TXD	Output	1

UART electrical specification

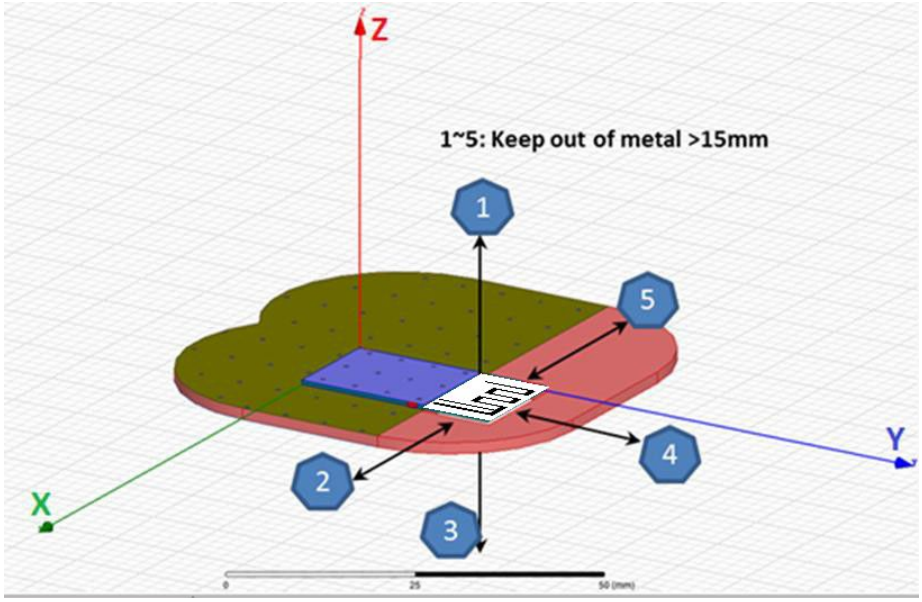
Symbol	Description	Min.	Typ.	Max.	Units
f_{UART}	Baud rate for UART[41].			1000	kbps
I_{UART1M}	Run current at max baud rate.		55		µA
$I_{UART115k}$	Run current at 115200 bps.		55		µA
$I_{UART1k2}$	Run current at 1200 bps.		55		µA
$I_{UART,IDLE}$	Idle current for UART		1		µA
$t_{UART,CTSH}$	CTS high time	1			µs
$t_{UART,START,LP}$	Time from STARTRX/STARTTX task to transmission started, low power mode		$t_{UART,STA}$ + t		µs
$t_{UART,START,CL}$	Time from STARTRX/STARTTX task to transmission started, constant latency mode		1		µs

8、PCB Printed Antenna Information

PCB Printed Antenna Dimension

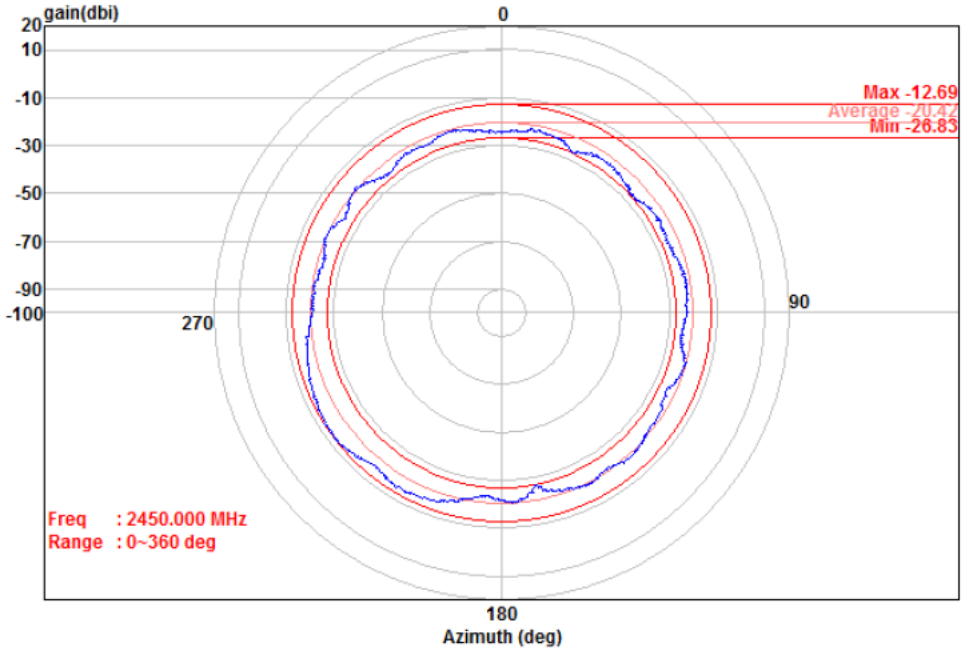


Antenna Keep Out Area Example


Z
1~5: Keep out of metal >15mm
1
2
3
4
5
X
Y

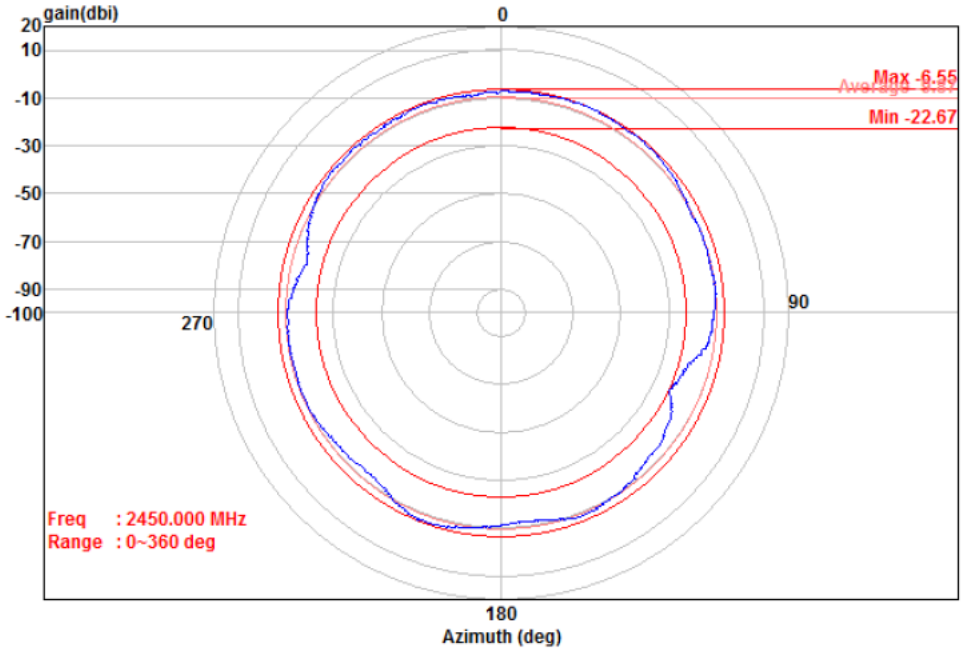
Module Radiation Pattern

VERTICAL_Antenna 2D Radiation Pattern @2450 MHz



Condition : 3m VERTICAL
Project Number:
Compy :
Model : PCB
Test Mode : 2450
Test Site : Chamber 966
Temp/Humi : 25/60

HORIZONTAL_Antenna 2D Radiation Pattern @2450 MHz



Condition : 3m HORIZONTAL
Project Number:
Compy :
Model : PCB
Test Mode : 2450
Test Site : Chamber 966
Temp/Humi : 25/60

APPENDIX A: CERTIFICATION NOTICES

Federal Communications Commission (FCC) Statement

15.21
You are cautioned that changes or modifications not expressly approved by the part responsible for compliance could void the user's authority to operate the equipment.

15.105(b)
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.
However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-Reorient or relocate the receiving antenna.
-Increase the separation between the equipment and receiver.
-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
-Consult the dealer or an experienced radio/TV technician for help.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
1) this device may not cause harmful interference, and
2) this device must accept any interference received, including interference that may cause undesired operation
of the device.

FCC RF Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment.
This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.
This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.
Note: The end product shall has the words "Contains Transmitter Module FCC ID: 2AMPPAI00240"

Canada, Industry Canada (IC)

This Class B digital apparatus complies with Canadian ICES-003
Cet appareil numérique de classe B est conforme à la norme NMB-003.

Le present appareil est conforme aux CNR d'Industrie Canada applicables auxappareils radio exempts de licence.L'exploitation est autorisée aux deux conditions suivantes:
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage adioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Déclaration d'exposition aux radiations:
Cet équipement est conforme aux limites d'exposition au rayonnement ISED établies pour un environnement non contrôlé.
Cet équipement doit être installé et utilisé à une distance minimale de 20 cm entre le radiateur et votre corps.

Cet émetteur ne doit pas être co-localisé ou fonctionner en conjonction avec une autre antenne ou un autre émetteur.

ICES-003 RF Radiation Exposure Statement

This equipment complies with ICES-003 radiation exposure limits set forth for an uncontrolled environment.
This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.
This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.
Note: The end product shall has the words “Contains Transmitter Module IC: 11471A-AI00240”

(Modular approval) End Product Labeling:

The final end product must be labeled in a visible area with the following: “Contains IC: 11471A-AI00240”.

OEMstatement

The Original Equipment Manufacturer (OEM) must ensure that the OEM modular transmitter must be labeled with its own FCC ID number. This includes a clearly visible label on the outside of the final product enclosure that displays the contents shown below. If the FCC ID is not visible when the equipment is installed inside another device, then the outside of the device into which the equipment is installed must also display a label referring to the enclosed equipment

The end product with this module may subject to perform FCC part 15 unintentional emission test requirement and be properly authorized.
This device is intended for OEM integrator only This radio transmitter (192170139/AA/00) has been approved by Innovation, Science and Economic Development Canada to operate with the antenna types listed Below, with the maximum permissible gain indicated. Antenna types not included in this list that Have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.
AI00240: PCB Antenna, 1 dBi

APPENDIX B: LABEL FOR FINISHED PRODUCT

Contains Transmitter Module FCC ID: 2AMPPAI00240
and IC : 11471A-AI00240

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
1) this device may not cause harmful interference, and
2) this device must accept any interference received, including interference that may cause the device undesired operation of.

Version Information

Date	number	Description
2021.07.22	V1.0	Initial Version

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