

EWN-8822CSE3AA

SPECIFICATION V2.1

IEEE 802.11b/g/n/a/ac SDIO Wireless

+ Bluetooth 2.1/3.0/4.2/5.0 Module



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1 General Specifications

The module provides a complete solution for a high-performance integrated wireless and Bluetooth device. It provides SDIO interface for WiFi and HS-UART interface for Bluetooth. The module complies with IEEE 802.11 a/b/g/n/ac 2T2R MIMO standard, and Maximum PHY data rate up to 173.3 Mbps using 20 MHz bandwidth, 400 Mbps using 40 MHz bandwidth, and 866.7 Mbps using 80 MHz bandwidth.

2 Features

2.1 WLAN

- Supports 802.11ac 2x2, Wave-2 compliant with MU-MIMO
- Completes 802.11n MIMO solution for 2.4GHz and 5GHz band
- Maximum PHY data rate up to 173.3Mbps using 20MHz bandwidth, 400Mbps using 40 MHz bandwidth, and 866.7Mbps using 80MHz bandwidth
- ❖ Backward compatible with 802.11a/b/g devices while operating at 802.11n data rates
- Backward compatible with 802.11a/n devices while operating at 802.11ac data rates
- Complies with SDIO 1.1/2.0/3.0 for WLAN with clock rate up to 208MHz
- support standard SDIO v3.0 (up to SDR104 mode at 208 MHz) host interfaces
- complies with HS-UART with configurable baud rate for Bluetooth
- ❖ IEEE 802.11a/b/g/n/ac compatible WLAN
- IEEE 802.11e QoS Enhancement(WMM)
- ❖ IEEE 802.11i (WPA, WPA2). Open, shared key and pair-wise key authentication
- IEEE 802.11h DFS, TPC, Spectrum Measurement
- ❖ IEEE 802.11k Radio Resource Measurement
- Channel management and co-existence
- Wi-Fi Direct supports wireless peer to peer
- CCA on secondary through RTS/CTS handshake
- Supports TCP/UDP/IP checksum offload
- Two Transmit and Two Receive paths
- 5MHz/10MHz/20MHz/40MHz/80MHz bandwidth transmission
- Supports 2.4GHz and 5GHz band channels



- Short Guard Interval(400ns)
- Sounding packet

2.2 Bluetooth

- Compatible with Bluetooth v2.1 and v3.0 Systems
- Supports Bluetooth 4.1 features
- Supports Bluetooth 4.2 LE Secure Connection by upper layer software upgrade
- Support Bluetooth 5.0 and LE 5.0 system (BT5.2 Logo Compliant)
- Supports all packet types in basic rate and enhanced data rate
- Supports pico-nets in a scatter-net
- Supports Secure Simple Pairing
- Bluetooth 5.0 Dual Mode support: Simultaneous LE and BR/EDR

3 System Block Diagram

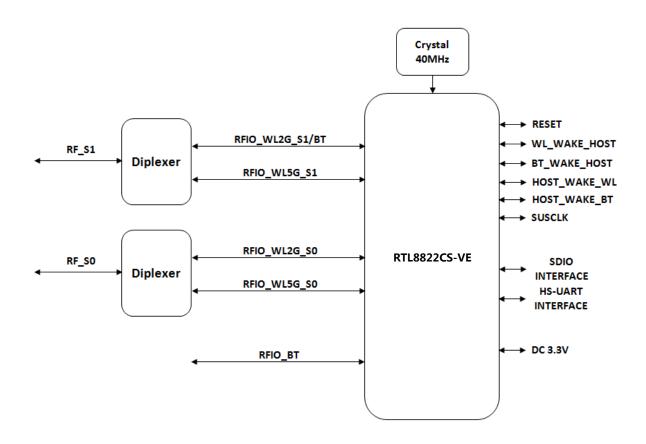


FIG 1 EWN-8822CSE3AA Block Diagram



4 PHY Specification

4.1 Wi-Fi Specification

Table 1 EWN-8822CSE3AA Wi-Fi RF Parameters

Table 1 EWN-8822CSE3AA Wi-Fi RF Parameters					
Protocol	IEEE 802.11b/g/n/a/ac				
Interface	SDIO 1.1 / 2.0 / 3.0				
	2.4GHz band CH1~CH14/240				
	5GHz Band CH36~CH48/51				
Frequency	CH52~CH64/5250-5350MHz CH100~CH140/5470-5725MHz				
		/5725-5850MHz			
	2.4G&5G Band Refer to Chann	el Plan Domain Code			
Bandwidth	20/40/80 MHz				
	Maximum PHY data rate up to	173.3 Mbps using 20MHz bandwidth;			
PHY Rate	Maximum PHY data rate up to	400 Mbps using 40MHz bandwidth;			
	Maximum PHY data rate up to 866.7 Mbps using 80MHz bandwidth .				
Frequency Error	<±10ppm/802.11b/g/n/a/ac				
	-20dB/±11MHz/OFDM;				
Mask	-28dB/±20MHz/OFDM;				
iviask	-30dB/±11MHz/DSSS, CCK;				
	-50dB/±20MHz/DSSS, CCK.				
	802.11b (2.4G 11Mbps):	21±1dBm			
2.4 G	802.11g (2.4G 54Mbps):	20±1dBm			
Transmit Power	802.11n (2.4G HT20 MCS7):	17±1dBm			
	802.11n (2.4G HT40 MCS7):	18±1dBm			
	Other TX power	rate see the "power by rate"			
	802.11b (2.4G 1Mbps):	≤-13dB			
	802.11b (2.4G 11Mbps):	≤-13dB			
2.4 G	802.11g (2.4G 6Mbps):	≤-8dB			
EVM	802.11g (2.4G 24Mbps):	≤-19dB			
	802.11g (2.4G 54Mbps):	≤-28dB			



Module: EWN-8822CSE3AA 802.11n (2.4G HT20 MCS4): ≤-22dB 802.11n (2.4G HT20 MCS7): ≤-30dB 802.11n (2.4G HT40 MCS0): ≤-8dB ≤-22dB 802.11n (2.4G HT40 MCS4): ≤-30dB 802.11n (2.4G HT40 MCS7): 802.11a (5G 54Mbps): 22±1dBm 802.11n (5G HT20 MCS7): 21±1dBm 802.11n (5G HT40 MCS7): 21±1dBm 5**G** 21±1dBm 802.11ac (5G VHT20 MCS8): **Transmit Power** 802.11ac (5G VHT40 MCS9): 21±1dBm 802.11ac (5G VHT80 MCS9): 22±1dBm Other TX power rate see the "power by rate" 802.11a (5G 6Mbps): ≤-8dB 802.11a (5G 24Mbps): ≤-19dB ≤-28dB 802.11a (5G 54Mbps): 802.11n (5G HT20 MCS0): ≤-8dB ≤-22dB 802.11n (5G HT20 MCS4): 802.11n (5G HT20 MCS7): ≤-30dB 802.11n (5G HT40 MCS0): ≤-8dB 802.11n (5G HT40 MCS4): ≤-22dB 802.11n (5G HT40 MCS7): ≤-30dB 5**G EVM** 802.11ac (5G VHT20 MCS0): ≤-8dB 802.11ac (5G VHT20 MCS5): ≤-25dB 802.11ac (5G VHT20 MCS8): ≤-33dB 802.11ac (5G VHT40 MCS0): ≤-8dB 802.11ac (5G VHT40 MCS5): ≤-25dB 802.11ac (5G VHT40 MCS9): ≤-35dB 802.11ac (5G VHT80 MCS0): ≤-8dB 802.11ac (5G VHT80 MCS5): ≤-25dB 802.11ac (5G VHT80 MCS9): ≤-35dB 802.11b (2.4G 1Mbps): -91dBm (Max.) -97dBm (Typ.) 2.4G **Receive Sensitivity** 802.11b (2.4G 11Mbps): -85dBm (Max.) -93dBm (Typ.) @ PER<10% 802.11g (2.4G 6Mbps): -87dBm (Max.) -96dBm (Typ.)



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	802.11g (2.4G 24Mbps):	-79dBm (Max.)	-83dBm (Typ.)
	802.11g (2.4G 54Mbps):	-70dBm (Max.)	-77dBm (Typ.)
	802.11n (2.4G HT20 MCS0):	-87dBm (Max.)	-95dBm (Typ.)
	802.11n (2.4G HT20 MCS4):	-75dBm (Max.)	-80dBm (Typ.)
	802.11n (2.4G HT20 MCS7):	-69dBm (Max.)	-77dBm (Typ.)
	802.11n (2.4G HT40 MCS0):	-84dBm (Max.)	-92dBm (Typ.)
	802.11n (2.4G HT40 MCS4):	-72dBm (Max.)	-76dBm (Typ.)
	802.11n (2.4G HT40 MCS7):	-66dBm (Max.)	-73dBm (Typ.)
	802.11a (5G 6Mbps):	-87dBm (Max.)	-94dBm (Typ.)
	802.11a (5G 24Mbps):	-79dBm (Max.)	-88dBm (Typ.)
	802.11a (5G 54Mbps):	-70dBm (Max.)	-79dBm (Typ.)
	802.11n (5G HT20 MCS0):	-87dBm (Max.)	-93dBm (Typ.)
	802.11n (5G HT20 MCS4):	-75dBm (Max.)	-80dBm (Typ.)
	802.11n (5G HT20 MCS7):	-69dBm (Max.)	-77dBm (Typ.)
	802.11n (5G HT40 MCS0):	-84dBm (Max.)	-92dBm (Typ.)
	802.11n (5G HT40 MCS4):	-72dBm (Max.)	-76dBm (Typ.)
5G	802.11n (5G HT40 MCS7):	-66dBm (Max.)	-73dBm (Typ.)
Receive Sensitivity @ PER<10%	802.11ac (5G VHT20 MCS0):	-87dBm (Max.)	-94dBm (Typ.)
	802.11ac (5G VHT20 MCS5):	-71dBm (Max.)	-76dBm (Typ.)
	802.11ac (5G VHT20 MCS8):	-64dBm (Max.)	-72dBm (Typ.)
	802.11ac (5G VHT40 MCS0):	-84dBm (Max.)	-91dBm (Typ.)
	802.11ac (5G VHT40 MCS5):	-68dBm (Max.)	-72dBm (Typ.)
	802.11ac (5G VHT40 MCS9):	-59dBm (Max.)	-68dBm (Typ.)
	802.11ac (5G VHT80 MCS0):	-81dBm (Max.)	-87dBm (Typ.)
	802.11ac (5G VHT80 MCS5):	-65dBm (Max.)	-70dBm (Typ.)
	802.11ac (5G VHT80 MCS9):	-56dBm (Max.)	-65dBm (Typ.)

4.2 BT Specification

Table 2 EWN-8822CSE3AA Bluetooth RF Parameters

Protocol BTv2.1+EDR/BTv3.0/BTv3.0+HS/BT v4.2/BT v5.0			
Interface	UART		
Frequency	2400 MHz ~ 2483.5 MHz (79 channels)		
Modulation	GFSK, π/4-DQPSK, 8-DPSK		



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PHY Rate	1Mbps for Basic Rate; 2、3 Mbps for Enhanced Data Rate; 1、2 Mbps for BLE
Transmit Power	9±1dBm, typical
Receive Sensitivity	<-89dBm @ BER=0.1% for GFSK (1Mbps); <-90dBm @ BER=0.01% for π/4-DQPSK (2Mbps); <-83dBm @ BER=0.01% for 8-DPSK (3Mbps); <-90dBm @ PER=30.8% for BLE
Maximum Input level	GFSK(1Mbps): -20dBm; π/4-DQPSK (2Mbps): -20dBm; 8-DPSK(3Mbps): -20dBm.

5 Other Specifications

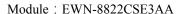
Table 3 Other Specifications

iusie s outre, opeenieudions			
Operating Temperature	0°C~+70°C		
Storage Temperature	Module: -20°C~+125°C		
	Package: -20℃~+70℃		
Operating Humidity RH 95%(Non-Condensing)			
Storage Humidity RH 95%(Non-Condensing)			
Humidity level Level 3			
Security WEP 64/128bit,WPA,WPA2,TKIP,AES,WAPI			
Other characteristics:	QoS-WMM, WMM-PS		
Operation System	Windows XP/Win7/Linux/Android		
ESD(IEC61000-4-2)	±1.5kV(Contact) @ RF Port		

6 DC Characteristics

Table 4 Power Supply Characteristics

Symbol	Symbol Parameter		Typical	Max.	Unit
VDD_3.3V	3.3V Supply Voltage	3.0	3.3	3.6	V
IDD_3.3V	3.3V Rating Current	-	-	800	mA
VDDIO	SDIO I/O Voltage	Depend on	the SDIO pro	otocol (1.8V d	or 3.3V)



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7 S11 Report

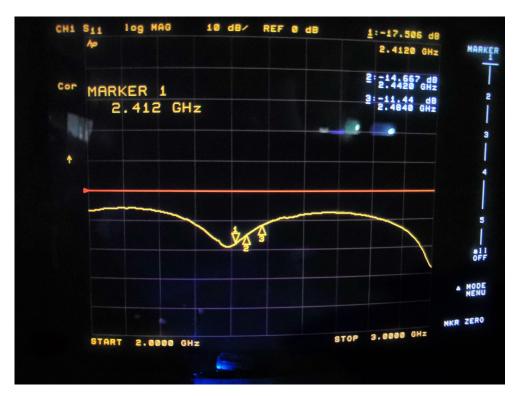


FIG 2 EWN-8822CSE3AA 2.4G Path A

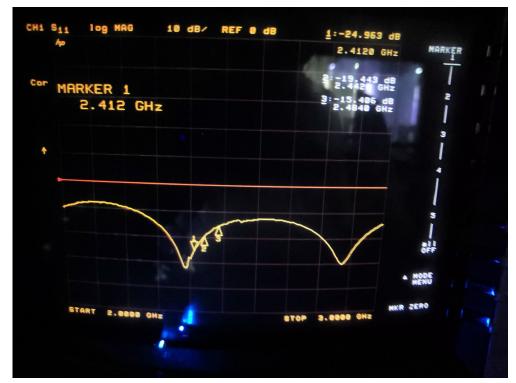
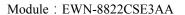


FIG 3 EWN-8822CSE3AA 2.4G Path B





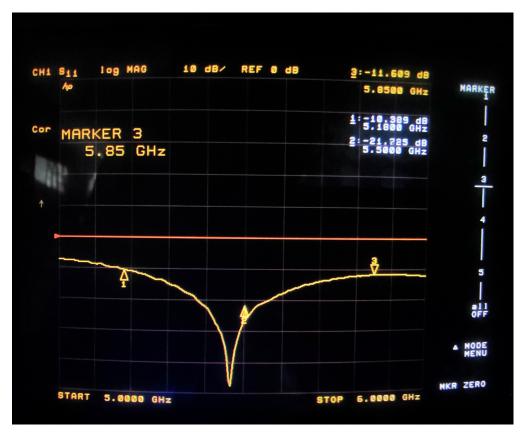


FIG 4 EWN-8822CSE3AA 5G Path A



FIG 5 EWN-8822CSE3AA 5G Path B



ARDATEK Module : EWN-8822CSE3AA

8 Module configurations

Module Dimension (L*W*T): 15.2±0.2mm*13.2±0.2mm*2.1±0.2mm.

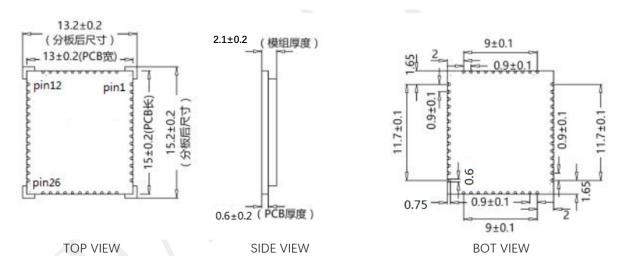


FIG 6 EWN-8822CSE3AA Module Dimension

Recommended Footprint:

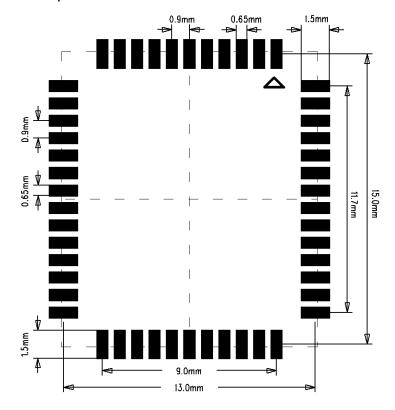


FIG 7 EWN-8822CSE3AA Module Dimension



ARDAIEK Module : EWN-8822CSE3AA

9 Pin Definition

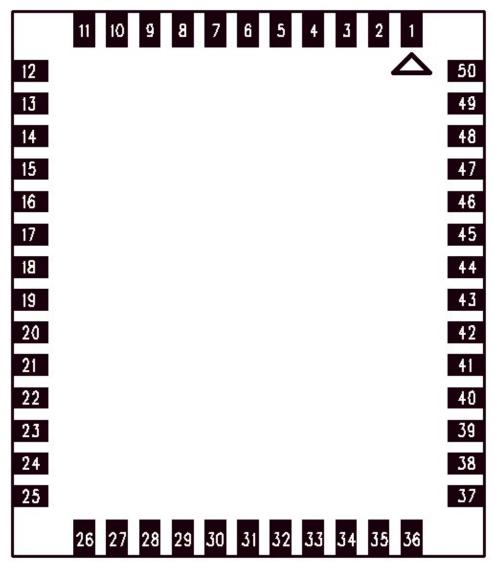


FIG 8 TOP VIEW

See Table 5 for the module hardware pin definition.

Table 5 EWN-8822CSE3AA Pin Description

Pin	Definition	Туре	Description	Default Pull	Power level
1	GND	-	Ground	-	-
2	Wi-Fi B	I/O	Wi-Fi Path B ANT I/O port	-	-
3	GND	-	Ground	-	-
4	GND	-	Ground	-	-
5	GND	-	Ground	-	-



Pin Definition Type Description Default Power level Pull 6 GND - Ground - - 7 GND - Ground - - 8 GND - Ground - - 9 Wi-Fi A I/O Wi-Fi Path A ANT I/O port - - 10 GND - Ground - - 11 GND - Ground - - 12 BT_ANT I/O Bluetooth ANT I/O port - - 13 GPIO6 I/O General Purpose Input/Output Pin PD Internal PD VDDIO 14 G_BT I/O General Purpose Input/Output Pin PD - - VDDIO 15 WL_REG_ON I General Purpose Input/Output Pin PD - VDDIO 16 WL_MEG_ON I General Purpose Input/Output Pin PD - VDDIO 17 SDIO_CAMD I/O SDIO interface clock		INDAILIN			Module : Ev	WN-8822CSE3AA
7 GND - Ground - - 8 GND - Ground - - 9 Wi-Fi A I/O Wi-Fi Path A ANT I/O port - - 10 GND - Ground - - 11 GND - Ground - - 12 BT_ANT I/O Bluetooth ANT I/O port - - 13 GPIO6 I/O General Purpose Input/Output Pin - - 14 G_BT I/O General Purpose Input/Output Pin - VDDIO 15 WL_REG_ON I General Purpose Input/Output Pin - VDDIO 16 WL_WAKE_HOST O WLAN to wake-up the host - VDDIO 17 SDIO_CAMD I/O SDIO interface command line Internal PU VDDIO 19 SDIO_DATA_3 I/O SDIO interface data line 3 Internal PU VDDIO 20 SDIO_DATA_2 I/O S	Pin	Definition	Туре	Description		Power level
8 GND - Ground - - 9 Wi-Fi A I/O Wi-Fi Path A ANT I/O port - - 10 GND - Ground - - 11 GND - Ground - - 12 BT_ANT I/O Bluetooth ANT I/O port - - 13 GPIO6 I/O General Purpose Input/Output Pin PD - - 14 G_BT I/O General Purpose Input/Output Pin PD VDDIO VDDIO 15 WL_REG_ON I General Purpose Input/Output Pin PD - VDDIO 16 WL_WAKE_HOST O WLAN to wake-up the host - VDDIO 17 SDIO_CMD I/O SDIO interface command line PU Internal PU VDDIO 18 SDIO_DATA_3 I/O SDIO interface data line 3 Internal PU VDDIO 20 SDIO_DATA_2 I/O SDIO interface data line 0 Internal PU VDDIO 21	6	GND	-	Ground	-	-
9 Wi-Fi A I/O Wi-Fi Path A ANT I/O port - -	7	GND	-	Ground	-	-
10	8	GND	-	Ground	-	-
11	9	Wi-Fi A	I/O	Wi-Fi Path A ANT I/O port	-	-
12 BT_ANT	10	GND	-	Ground	-	-
13	11	GND	-	Ground	-	-
13	12	BT_ANT	I/O	Bluetooth ANT I/O port	-	-
14 G_BT 1/O General Purpose Input/Output Pin PD VDDIO	13	GPIO6	I/O	General Purpose Input/Output Pin		VDDIO
16 WL_WAKE_HOST O WLAN to wake-up the host - VDDIO 17 SDIO_CMD I/O SDIO interface command line Internal PU VDDIO 18 SDIO_CLK I/O SDIO interface clock line - VDDIO 19 SDIO_DATA_3 I/O SDIO interface data line 3 Internal PU VDDIO 20 SDIO_DATA_2 I/O SDIO interface data line 2 Internal PU VDDIO 21 SDIO_DATA_0 I/O SDIO interface data line 0 Internal PU VDDIO 22 SDIO_DATA_1 I/O SDIO interface data line 1 Internal PU VDDIO 23 GND - Ground 24 WL_WAKE_HOST O WLAN to wake-up the host - VDDIO 25 GPIO7 I/O General Purpose Input/Output Pin - VDDIO 26 NC - No connect 27 PCM_SYNC I/O PCM SYNC signal - VDDIO 28 PCM_IN I PCM data input - VDDIO 29 PCM_OUT O PCM data output - VDDIO 30 PCM_CLK I/O PCM clock - VDDIO 31 SUSCLK I/O External low power clock input Internal PD VDDIO 32 GND - Ground	14	G_BT	I/O	General Purpose Input/Output Pin		VDDIO
SDIO_CMD	15	WL_REG_ON	I	General Purpose Input/Output Pin	-	VDDIO
SDIO_CMD	16	WL_WAKE_HOST	0	WLAN to wake-up the host	-	VDDIO
19 SDIO_DATA_3 I/O SDIO interface data line 3 PU VDDIO 20 SDIO_DATA_2 I/O SDIO interface data line 2 Internal PU VDDIO 21 SDIO_DATA_0 I/O SDIO interface data line 0 Internal PU VDDIO 22 SDIO_DATA_1 I/O SDIO interface data line 1 Internal PU VDDIO 23 GND - Ground 24 WL_WAKE_HOST O WLAN to wake-up the host - VDDIO 25 GPIO7 I/O General Purpose Input/Output Pin - VDDIO 26 NC - No connect 27 PCM_SYNC I/O PCM SYNC signal - VDDIO 28 PCM_IN I PCM data input - VDDIO 29 PCM_OUT O PCM data output - VDDIO 30 PCM_CLK I/O External low power clock input Internal PD Internal PD Internal PD Internal PD Internal PU VDDIO 31 SUSCLK I/O External low power clock input Internal PD Internal PU	17	SDIO _CMD	I/O	SDIO interface command line		VDDIO
19 SDIO_DATA_3 I/O SDIO interface data line 3 PU VDDIO 20 SDIO_DATA_2 I/O SDIO interface data line 2 Internal PU VDDIO 21 SDIO_DATA_0 I/O SDIO interface data line 0 Internal PU VDDIO 22 SDIO_DATA_1 I/O SDIO interface data line 1 Internal PU VDDIO 23 GND - Ground 24 WL_WAKE_HOST O WLAN to wake-up the host - VDDIO 25 GPIO7 I/O General Purpose Input/Output Pin - VDDIO 26 NC - No connect 27 PCM_SYNC I/O PCM SYNC signal - VDDIO 28 PCM_IN I PCM data input - VDDIO 29 PCM_OUT O PCM data output - VDDIO 30 PCM_CLK I/O PCM clock - VDDIO 31 SUSCLK I/O External low power clock input Internal PD	18	SDIO _CLK	I/O	SDIO interface clock line	-	VDDIO
SDIO_DATA_2 I/O SDIO interface data line 2 PU VDDIO SDIO_DATA_0 I/O SDIO interface data line 0 SDIO_DATA_1 I/O SDIO interface data line 0 SDIO_DATA_1 I/O SDIO interface data line 1 SDIO_DATA_1 I/O SDIO interface data line 0 Internal PU VDDIO SDIO_DATA_1 I/O SDIO interface data line 0 SDIO_DATA_1 I/O SDIO interface data line 0 Internal PU VDDIO SDIO_DATA_1 I/O SDIO interface data line 0 SDIO_DATA_1 I/O SDIO interface data line 0 Internal PU VDDIO SDIO_DATA_1 I/O SDIO interface data line 0 Internal PU VDDIO SDIO_DATA_1 I/O SDIO interface data line 0 Internal PU VDDIO SDIO_DATA_1 I/O SDIO interface data line 0 Internal PU VDDIO SDIO_DATA_1 I/O SDIO interface data line 0 Internal PU VDDIO SDIO_DATA_1 I/O SDIO interface data line 0 Internal PU VDDIO SDIO_DATA_1 I/O SDIO interface data line 1 Internal PU VDDIO SDIO_DATA_1 I/O SDIO interface data line 1 Internal PU VDDIO SDIO_DATA_1 I/O SDIO Internal SDIO Internal PU VDDIO SDIO_DATA_1 I/O SDIO Internal SDIO Internal PU VDDIO SDIO_DATA_1 I/O SDIO Internal SDIO Internal PU VDDIO SDIO_DATA_1 I/O SDIO Internal Internal PU VDDIO SDIO_DATA_1 I/O SDIO Internal Internal PU VDDIO SDIO_DATA_1 I/O SDIO Internal Internal PU VDDIO SDIO_DATA_1 I/O Internal INTERNA	19	SDIO _DATA_3	I/O	SDIO interface data line 3		VDDIO
SDIO_DATA_0	20	SDIO _DATA_2	I/O	SDIO interface data line 2		VDDIO
22 SDIO _DATA_1 I/O SDIO interface data line 1 PU VDDIO 23 GND - Ground - - 24 WL_WAKE_HOST O WLAN to wake-up the host - VDDIO 25 GPIO7 I/O General Purpose Input/Output Pin - VDDIO 26 NC - No connect - - - 27 PCM_SYNC I/O PCM SYNC signal - VDDIO 28 PCM_IN I PCM data input - VDDIO 29 PCM_OUT O PCM data output - VDDIO 30 PCM_CLK I/O PCM clock - VDDIO 31 SUSCLK I/O External low power clock input (32.768KHz) Internal PD VDDIO 32 GND - Ground - - -	21	SDIO _DATA_0	I/O	SDIO interface data line 0		VDDIO
24WL_WAKE_HOSTOWLAN to wake-up the host-VDDIO25GPIO7I/OGeneral Purpose Input/Output Pin-VDDIO26NC-No connect27PCM_SYNCI/OPCM SYNC signal-VDDIO28PCM_INIPCM data input-VDDIO29PCM_OUTOPCM data output-VDDIO30PCM_CLKI/OPCM clock-VDDIO31SUSCLKI/OExternal low power clock input (32.768KHz)Internal PDVDDIO32GND-Ground	22	SDIO _DATA_1	I/O	SDIO interface data line 1		VDDIO
25 GPIO7 I/O General Purpose Input/Output Pin - VDDIO 26 NC - No connect - - 27 PCM_SYNC I/O PCM SYNC signal - VDDIO 28 PCM_IN I PCM data input - VDDIO 29 PCM_OUT O PCM data output - VDDIO 30 PCM_CLK I/O PCM clock - VDDIO 31 SUSCLK I/O External low power clock input (32.768KHz) Internal PD VDDIO 32 GND - Ground - - -	23	GND	-	Ground	-	-
26 NC - No connect - - 27 PCM_SYNC I/O PCM SYNC signal - VDDIO 28 PCM_IN I PCM data input - VDDIO 29 PCM_OUT O PCM data output - VDDIO 30 PCM_CLK I/O PCM clock - VDDIO 31 SUSCLK I/O External low power clock input (32.768KHz) Internal PD VDDIO 32 GND - Ground - -	24	WL_WAKE_HOST	0	WLAN to wake-up the host	-	VDDIO
27PCM_SYNCI/OPCM SYNC signal-VDDIO28PCM_INIPCM data input-VDDIO29PCM_OUTOPCM data output-VDDIO30PCM_CLKI/OPCM clock-VDDIO31SUSCLKI/OExternal low power clock input (32.768KHz)Internal PDVDDIO32GND-Ground	25	GPIO7	I/O	General Purpose Input/Output Pin	-	VDDIO
28 PCM_IN I PCM data input - VDDIO 29 PCM_OUT O PCM data output - VDDIO 30 PCM_CLK I/O PCM clock - VDDIO 31 SUSCLK I/O External low power clock input (32.768KHz) PD VDDIO 32 GND - Ground	26	NC	-	No connect	-	-
29 PCM_OUT O PCM data output - VDDIO 30 PCM_CLK I/O PCM clock - VDDIO 31 SUSCLK I/O External low power clock input (32.768KHz) PD VDDIO 32 GND - Ground	27	PCM_SYNC	I/O	PCM SYNC signal	-	VDDIO
30 PCM_CLK I/O PCM clock - VDDIO 31 SUSCLK I/O External low power clock input (32.768KHz) PD VDDIO 32 GND - Ground	28	PCM_IN	I	PCM data input	-	VDDIO
31 SUSCLK I/O External low power clock input (32.768KHz) PD VDDIO 32 GND - Ground	29	PCM_OUT	0	PCM data output	-	VDDIO
31 SUSCLK 1/O (32.768KHz) PD VDDIO 32 GND - Ground	30	PCM_CLK	I/O	PCM clock	-	VDDIO
	31	SUSCLK	I/O	-		VDDIO
33 NC - No connect	32	GND	-	Ground	-	-
	33	NC	-	No connect	-	-



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Pin	Definition	Туре	Description	Default Pull	Power level
34	VDDIO	I/O	I/O voltage supply input (1.8V typ.)	-	VDDIO
35	NC	-	No connect	-	-
36	VDD_3.3V	I/O	Main power voltage source input (3.3V±10%)	-	DC 3.3V±0.3V
37	NC	-	No connect	-	-
38	BT_REG_ON	I	Enable pin for Bluetooth device ON:pull high;OFF:pull low External pull low to shut down BT	Internal PU	VDDIO
39	GND	-	Ground	-	-
40	UART_TXD	0	Bluetooth UART interface(connect to host UART RX)	-	VDDIO
41	UART_RXD	I	Bluetooth UART interface(connect to host UART TX)	-	VDDIO
42	UART_RTS_N	0	Bluetooth UART interface	-	VDDIO
43	UART_CTS_N	I	Bluetooth UART interface	-	VDDIO
44	SD_RESET	I	Reset pin for SDIO bus External pull low to reset SDIO bus	Internal PU	VDDIO
45	G_WL	I/O	General Purpose Input/Output Pin	Internal PD	VDDIO
46	GND	-	Ground	-	-
47	NC	-	No connect	-	-
48	GND	-	Ground	-	-
49	HOST_WAKE_BT	I	Host wake-up Bluetooth	Internal PD	VDDIO
50	BT_WAKE_HOST	0	Bluetooth to wake-up the host	Output High	VDDIO

Note: The internal pull-up/down resistances of the chip are about 50K~100K ohm.



10 Module Photos





FIG 9 TOP VIEW

FIG 10 BOTTOM VIEW

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11 Key material list

Table 6 EWN-8822CSE3AA Key material list

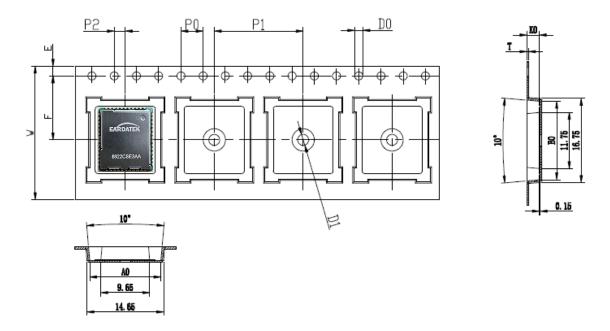
Туре	Model	Footprint	QTY.
	LD18D2450LAN-D118/T		
Diplexers	FLT18D24254959D-3268B-V2	1608	2PCS
	FLT18D24254959D-3288B		
IC	RTL8822CS-VE-CG	QFN76	1 PCS
Crystal	40MHz (CX/YDL/JWT/TJ)	X3225	1 PCS



ARDAIEK Module : EWN-8822CSE3AA

12 Package Information

Carrier dimension: (Unit:mm)



A0	В0	КО	P0	P1	P2
13.65±0.1	15. 75±0. 1	2.60±0.1	4.0±0.1	20.0±0.1	2.0±0.1
W	T	Е	F	D0	D1
24.0±0.3	0.3±0.05	1.75±0.1	11.50±0.1	Ø 1. 5 ^{+0. 1}	Ø 1. 50 ^{+0. 1}

FIG 11 Carrier size

Reel dimension: D=38cm 1400PCS Modules Per Reel

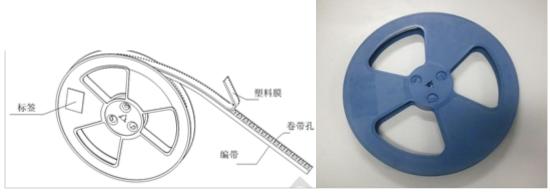


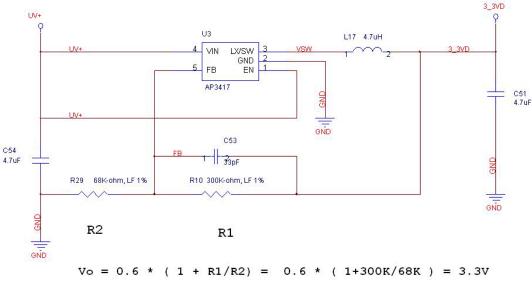
FIG 12 Reel FIG 13 Reel figure



13 Reference design

13.1 Power supply requirement

The module power supply voltage is DC+3.3V, and the maximum module current is 800mA. The power supply design needs to consider the output current and power interference. To avoid the +3.3V power supply from interfering with other circuits on the motherboard, it is recommended to supply to the module using the regulator circuit alone, the recommended DC-DC circuit structure shown in the figure below. A 4.7uF~10uF capacitor is connected in parallel at 3_3VD output to filter out the interference. A bead is connected in series at 3_3VD output. The bead and capacitor must be placed as close to the module as possible. If you need to share +3.3V with other circuits, consider whether the current of the shared power supply is sufficient.



Step-Down Regulator, Vfb=0.6V, 1A, 1.8MHz, ADJ, LF
FIG 14 Power supply Circuit schematic



13.2 System power on sequrence

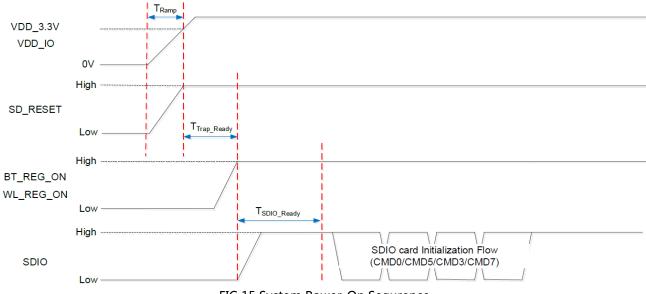


FIG 15 System Power-On Sequrence

Table 7 System Power-On Timing Parameters

	Min.	Typical	Max.	Unit	Description
T_{Ramp}	0.5	1.5	5	ms	The 3.3V or 1.8V power ramp up duration.
T_{Trap_Ready}	400	500	Х	ms	WLAN eFuse autoload. $T_{Trap_Ready} = 500ms$ (Typical)
T _{SDIO_Ready}	10	20	100	ms	SDIO Not Ready Duration. In this state, the Wi-Fi Module may respond to commands without the ready bit being set. After the ready bit is set, the host will initiate complete card detection procedure.

Table 8 DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Peak Current
VDD_3.3V (PIN36)	3.3V Supply Voltage	3.0V	3.3V	3.6V	0.8A

Table 9 Platform Power Rail Requirements

VDD_3.3V	VDD_3.3V	VDD_3.3V	Rise time	
Power range	Ripple	Noise	Min	Max
+/-0.165V	300mVpp@switching	0.5ms	5ms	



13.3 SDIO Interface

The SDIO interface has 4 data lines, a cock signal line and a command signal line. all of the SDIO lines must be equal length. In order to avoid mutual interference, SDIO lines should be avoided to be adjacent and parallel to other data lines, RF lines and power lines, and Surround the data line and clock line with ground copper.

13.4 RF circuit

Due to the SMD package, the RF port impedance must be offset after the module is soldered to the motherboard. In order to achieve the best performance,, it is recommended to add a PI-type matching network to the motherboard, as shown below (C11, R21,C6). The value of the PI type matching network needs to be debugged according to the actual motherboard to match RF port impedance to 50 Ohm.

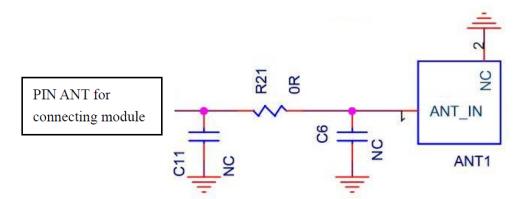


FIG 16 Connect 50 Ohm matching antenna reference circuit

The antenna ANT1 in the figure above must be 50 Ohm. If the antenna is not matched, it is recommended to add a set of PI type matching network at the front of the antenna to match the antenna. Generally, the antenna manufacturers will give Suggestions on matching parameters.

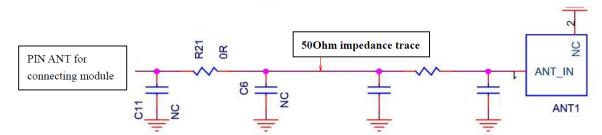


FIG 17 Connect the unmatched antenna reference circuit

The RF line layout should be matched according to 50ohm. The line impedance is related to the plate, plate thickness, line width and copper spacing. Professional software can be used to calculate the line width. Note: for multilayer plates, the plate thickness should calculate the



distance from RF routing layer to GND of the next layer. There are RF lines Layout principles:

1. RF line layout needs to match 50 ohms. The line width can be calculated by professional software. (Note: If it is a multi-layer board, The board thickness should calculate the distance from the RF trace layer to the next ground layer.)

- 2. The RF line must be surrounded by ground copper and ground holes.
- 3. The PI-type matching circuit for adjusting the impedance of the module is placed close to the module. The PI type matching circuit for matching the antenna is placed close to the antenna.

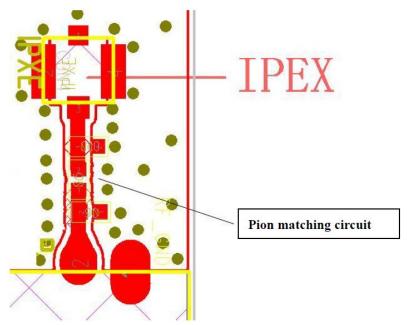


FIG 18 The PI type matching circuit Layout

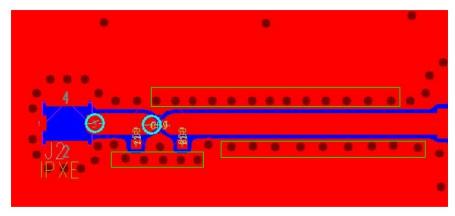


FIG 19 The RF line Layout



13.5 Application Circuit for SD_RESET and BT_REG_ON with Platform

There is internal pull-up, about 100K, resistor design in Module Pin38 and Pin44. If Host SOC need to control these pins, choose host GPIO without pull capability to avoid voltage divider. Middle range of IO voltage would affect Module booting up (FIG 20).

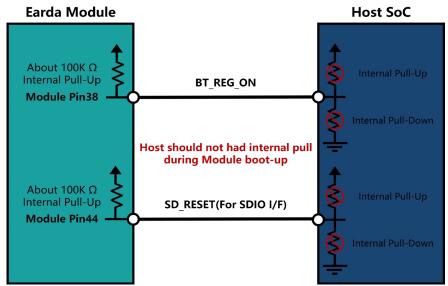


FIG 20 Host GPIO control GPIO9 and GPIO11

If Host GPIO has Pull-Down capability and it can't be avoided, suggest to add $10K\Omega$ Pull-Down resistor in circuit to ensure IO is in low level. In this way, Module internal Pull-Up $100K\Omega$ could be neglected (FIG 21). Please note external Pull-Down will cause additional static current. BT_REG_ON exists only high level and low level during power-on. Other uncertain voltage values may cause BT to fail to open.

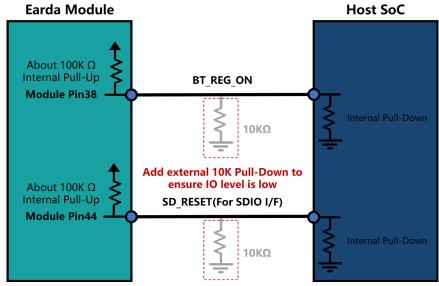


FIG 21 Add external pull down resistor to ensure low level



13.6 Motherboard interference avoidance

Motherboard interference comes from: high-speed data interface (HDMI), the Operating frequency of main chip, DDR, DC-DC power supply. The method of avoiding interference according to the characteristics of various signals is also different. The main methods of interference avoidance include:

- 1. keeping away from the source of interference;
- 2. Adding shields to avoid interference leakage;
- 3. Reasonable layout to eliminate interference.

13.6.1 Interface interference

When HDMI uses the 74.2MHz frequency, its 33x frequency is in the 2.4G band of Wi-Fi, which will seriously interfere with the Wi-Fi signal. If the HDMI frequency is 148.5MHz, although the 16x frequency is not in the Wi-Fi band, the isolation of the frequency is not good, and the Wi-Fi signal will be interfered to some extent. If the distance between the HDMI interface and the Wi-Fi module on the PCB is less than 5cm, the HDMI output display will interfere with the Wi-Fi signal, resulting in problems such as Wi-Fi connection failure and throughput drop. Therefore, keep the location of the Wi-Fi module away from the HDMI port on the hardware layout to avoid interference.

At the same time, if the Wi-Fi antenna is built-in the motherboard, its placement must also be carefully considered to be far from the interface interference. If the antenna is placed in an incorrect position, even if the module is shielded, the interference signal is coupled through the antenna, which will eventually result in a lower Wi-Fi throughput. (Note: In addition to interference, the placement of the internal antenna should also evaluate the effect of the metal interface, motherboard, and housing material on the antenna impedance.)



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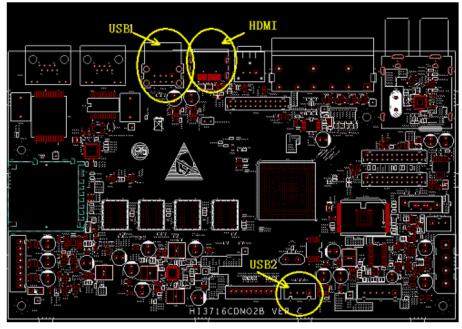


FIG 22 HDIM and USB interference

13.6.2 The main chip interferes with DDR

Because the main chips operate at about 800MHz or DDR2 operate at 667MHz, 3x frequency of 800MHz and 4x frequency of 667MHz are near 2.4GHz band. It must to place Wi-Fi modules and antennas far away from the main chip and DDR. It is strongly recommended that the main chip be isolated from the DDR by a shield. As shown in the figure below.

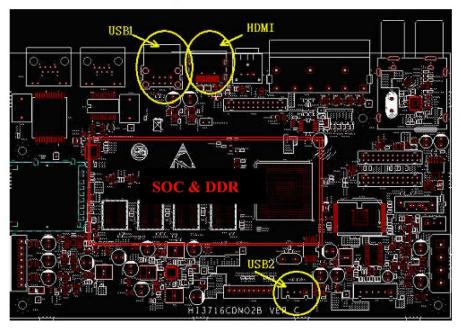


FIG 23 Main chip and DDR interference



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13.7 Recommended secondary reflux temperature curve

The number of reflux shall not exceed 2 times, and the tin feeding height of the half hole of the module shall be no less than 1/4.

The lead-free reflux curve requirements of Wi-Fi module products are shown in FIG 24:

Stage	Note	Pb-free assembly		
Average ramp-up T _L to Tp		3 °C/ second max.		
rate				
Preheat	Temperature min (T _{smin})	150℃		
	Temperature max	200℃		
	(Tsmax)			
	Time (t _{smin} to t _{smax})	60 - 120 seconds		
Time maintained	Temperature(T _L)	217℃		
above	Time (t _L)	60 - 150 seconds		
Peak package body temperature (Tp)		Tp must not exceed the specified		
		classification temp(Tc=245℃).		
Time(tp) within 5°C	of the specified	30 seconds		
classification tempera	ature (Tc)			
Ramp-down rate (Tp	to T _L)	6 °C / seconds max.		
Time 25°C to peak te	emperature	8 minutes max.		

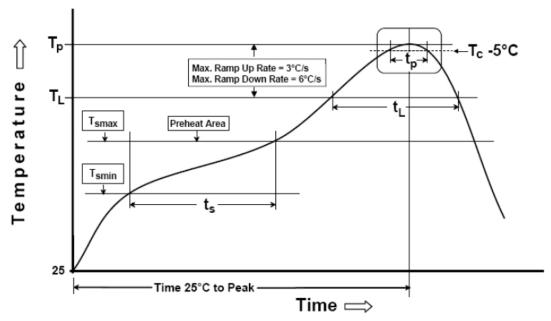


FIG 24 Furnace temperature curve

NOTE:

- 1.The maximum furnace temperature of the module is 260°C, don't exceed this temperature.
- 2. The gold plating thickness of the module pad is 2u".



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14 Revision History

Revision	Release Date	Summary	Revised By
V1.0	2022/01/25	First release	Jisheng Wang
V1.1	2022/06/17	Updata PHY Specification	Jisheng Wang
V1.2	2022/08/01	Updata Module Photos	Shuize Wang
V1.3	2022/12/19	Updata Pin Definition	Shuize Wang
V1.4	2023/01/05	Updata Key material list	Shuize Wang
V1.5	2023/02/02	Updata System Block Diagram, Module Photos and Reference design	Shuize Wang
V1.6	2023/04/23	Updata Module Laser Etching Silkscreen, Application Circuit for SD_RESET and BT_REG_ON with Platform	Shuize Wang
V2.0	2.0 Updata Module Laser Etching Silkscreen, Key material list; Add System power on sequrence		Shuize Wang
V2.1	2023/09/08	Updata Module Photos, Add FCC Statement	Shuize Wang

FCC Statement

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursua nt to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful inte rference in a residential installation. This equipment generates uses and can radiate radio frequency energy a nd, if not installed and used in accordance with the instructions, may cause harmful interference to radio com munications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turn ing the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help important announcement Important Note:

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator and your body.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter. Country Code selection feature to be disabled for products marketed to the US/Canada.

This device is intended only for OEM integrators under the following conditions:

- 1. The antenna must be installed such that 20 cm is maintained between the antenna and users, and
- 2. The transmitter module may not be co-located with any other transmitter or antenna,
- 3. For all products market in US, OEM has to limit the operation channels in CH1 to CH11 for 2.4G band by supplied firmware programming tool. OEM shall not supply any tool or info to the end-user regarding to Regulatory Domain change. (if modular only test Channel 1-11)

As long as the three conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Important Note:

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

The final end product must be labeled in a visible area with the following "Contains FCC ID: **2AMM6-8822CSE3AA** "

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01r01

2.2 List of applicable FCC rules

CFR 47 FCC PART 15 SUBPART C has been investigated. It is applicable to the modular transmitter

2.3 Specific operational use conditions

This module is stand-alone modular. If the end product will involve the Multiple simultaneously transmitting condition or different operational conditions for a stand-alone modular transmitter in a host, host manufacturer have to consult with module manufacturer for the installation method in end system.

2.4 Limited module procedures

Not applicable

2.5 Trace antenna designs

Not applicable

2.6 RF exposure considerations

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

2.7 Antennas

This radio transmitter **FCC ID:2AMM6-8822CSE3AA** has been approved by Federal Communications Commission to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Antenna No.	Model No. of antenna:	Type of antenna:	Gain of the antenna (Max.)		Frequency
	or antenna:		Antenna 1	Antenna 2	range:
Bluetooth	/	PCB Antenna	5.0	N/A	2402-2480MHz
2.4G Wi-Fi	/	PCB Antenna	5.0	5.0	2412-2462MHz
U-NII-1	/	PCB Antenna	6.0	6.0	5180-5240MHz
U-NII-2A	/	PCB Antenna	6.0	6.0	5260-5320MHz
U-NII-2C	/	PCB Antenna	6.0	6.0	5500-5720MHz
U-NII-3	/	PCB Antenna	6.0	6.0	5745-5825MHz

2.8 Label and compliance information

The final end product must be labeled in a visible area with the following" Contains FCC ID:2AMM6-8822CSE3AA".

2.9 Information on test modes and additional testing requirements

Host manufacturer is strongly recommended to confirm compliance with FCC requirements for the transmitter when the module is installed in the host.

2.10 Additional testing, Part 15 Subpart B disclaimer

Host manufacturer is responsible for compliance of the host system with module installed with all other applicable requirements for the system such as Part 15 B.

2.11 Note EMI Considerations

Host manufacture is recommended to use D04 Module Integration Guide recommending as "best practice" RF design engineering testing and evaluation in case non-linear interactions generate additional non-compliant limits due to module placement to host components or properties.

2.12 How to make changes

This module is stand-alone modular. If the end product will involve the Multiple simultaneously transmitting condition or different operational conditions for a stand-alone modular transmitter in a host, host manufacturer have to consult with module manufacturer for the installation method in end system. According to the KDB 996369 D02 Q&A Q12, that a host manufacture only needs to do an evaluation (i.e., no C2PC required when no emission exceeds the limit of any individual device (including unintentional radiators) as a composite. The host manufacturer must fix any failure.