SPECIFICATION
TCM3903

Bluetooth 4.1 Class2 Module

RF&BB

TCM3903_SPECIFICATION_V1.0

Rev.1.0

Oct 02, 2018

Telechips

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Revision History

Date	Revision	Description
2018-10-02	1.0.0	Initial release Bluetooth V4.1 Class 2 Module

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1 Introduction

The TCM3903 is the optimal solution for voice and data applications that require a Bluetooth SIG standard Host Controller Interface(HCI) via UART and PCM/I2S audio interface support.
In addition, the serial enhanced coexistence interface is available for WLAN devices.

This module has adopted BCM20713 industrial WLBGA chipset.

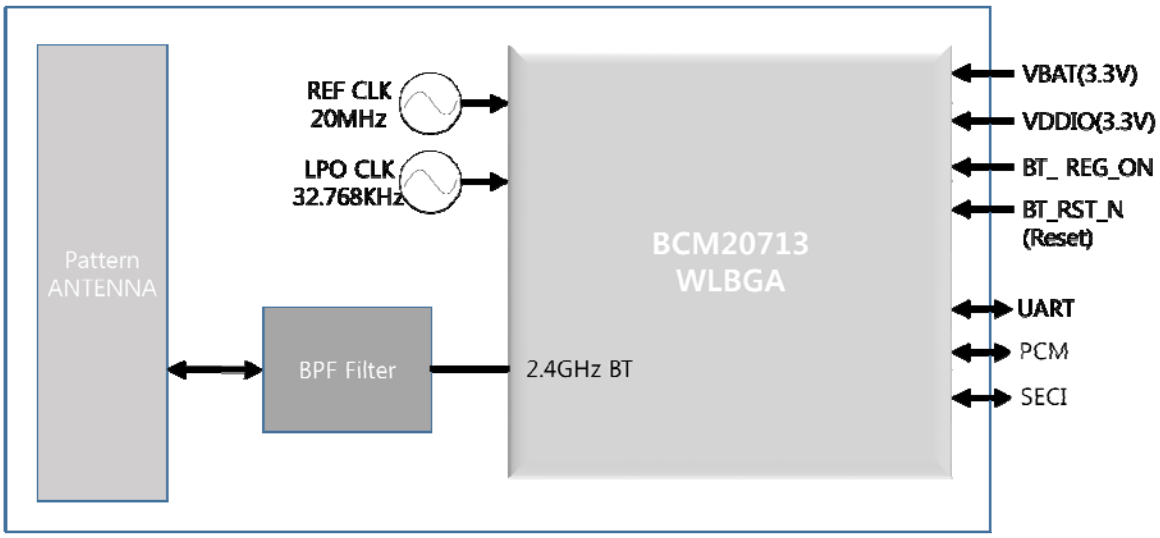


Figure 1.1 TCM3903 Block Diagram

2 Features

- Bluetooth 4.1 + EDR compliant
- Bluetooth Low Energy
- Programmable output power control meets Class1, Class2.
- High speed UART port(Up to 4Mbps)
- PCM/I2S digital audio interface
- Enhanced Coexistence Interface with 3-wire(SECI_OUT, SECI_IN, BT_STATUS)
- Supports Broadcom SmartAudio, wide-band speech, SBC codec and pccket loss concealment.
- Use supply voltage up to 5.5V
- Ultra-low power consumption
- Built-in PCB pattern antenna
- Built-in 32.768KHz LPO clock oscillator
- Operating temperature range(-40℃ ~+85℃)
- Competitive size (12mm x 10mm x 1.9T : LGA 32-pin)

3 Pin description

3.1 Pin Assignment

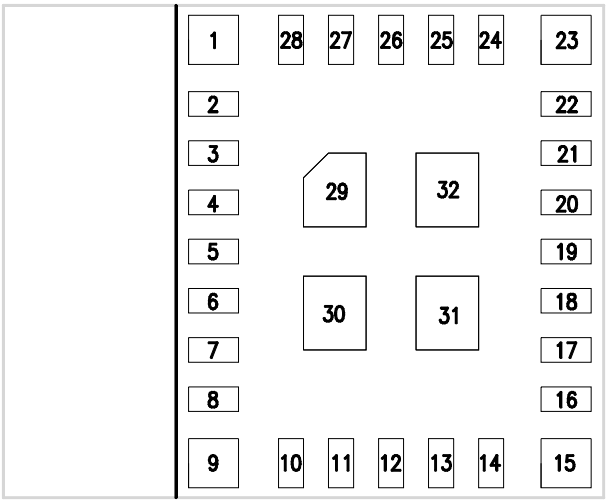


Figure 3.1 Pin Diagram (Top view)

Table 3.1 Pin Description

No.	Name	Type	Description
1	GND	GND	Ground connection
2	VDDIO_3V3	P	I/O voltage supply input
3	Reserved(LPO)	I	Reserved external LPO (32.768KHz)[1)]
4	GND	GND	Ground connection
5	GND	GND	Ground connection
6	GND	GND	Ground connection
7	GND	GND	Ground connection
8	GND	GND	Ground connection
9	ANT	I/O	Internal Antenna port
10	Reserved(RF)	I/O	RF In / Out port[2)]
11	GND	GND	Ground connection
12	VBAT_3V3	P	Main power voltage source input
13	BT_RST_N	I	Active-low reset input. Requires an external 10Kohm pull-up resistor
14	BT_REG_ON	I	Internal Regulator – High : ON / Low : OFF
15	GND	GND	Ground connection
16	UART_TX	O	UART transmit data
17	UART_RX	I	UART receive data
18	UART_RTS	O	UART request to send output
19	UART_CTS	I	UART clear to send input
20	SECI_OUT	O	Enhanced coexistence UART interface. BT_TXD
21	HOST_WAKE / SECI_IN	I/O	This pin can be mapped to following I/O functions. - Host wake-up. If not used, requires an external 10Kohm pull-up resistor - Enhanced coexistence UART interface. BT_RXD
22	BT_WAKE / GPIO_0	I/O	Bluetooth device wake-up. If not used, requires an external 10Kohm pull-up resistor
23	GND	GND	Ground connection
24	BT_STATUS	O	Enhanced coexistence UART interface. Normal GPIO
25	PCM_OUT	O	PCM data out
26	PCM_IN	I	PCM data in
27	PCM_CLK	I/O	PCM clock
28	PCM_SYNC	I/O	PCM sync signal
29	GND	GND	Ground connection
30	GND	GND	Ground connection
31	GND	GND	Ground connection
32	GND	GND	Ground connection

1) Pin.3 Reserved(External LPO) : This pin is not used because there is an internal LPO.
2) Pin.10 Reserved(RF) : This pin is not used because there is an internal matching.
3) All digital I/O has internal pull-up or pull-down values which are around 60Kohm

4 Electrical Specification

4.1 Absolute Maximum Rating

Table 4.1 Absolute maximum rating

Symbol	Description	Min.	Max.	Unit
VBAT	Input Supply Voltage	-0.3	5.5	V
VDDIO	I/O Voltage for Digital/Bluetooth/SDIO	-0.3	3.6	V

4.2 Recommended Operating Rating

Table 4.2 Recommended operating rating

Symbol	Min	Typ.	Max.	Unit
Operating Temperature	-40	25	85	℃
Storage Temperature	-40	25	85	℃
VBAT	2.5	3.3	5.5	V
VDDIO	1.8	3.3	3.6	V

4.3 Current Consumption

Table 4.3 Current consumption

Test Mode	DUT Status	VBAT : 3.3V	VDDIO : 3.3V
BDR(1Mbps)[Note.1]	Class 2 @ 2dBm Tx power (DH5 / 3-DH5)	45	0.1
	Rx @ -70dBm Rx power(DH5/3-DH5)	34	0.1
BDR(2 or 3Mbps)[Note.2]	Class 2 @ 2dBm Tx power (DH5 / 3-DH5)	45	0.1
	Rx @ -70dBm Rx power(DH5/3-DH5)	42	0.1
Sleep	UART transport active Internal LPO clock available	0.05	0.03

(Unit : mA)

Note.1
- Transmit(BDR): Current level during transmit of basic rate packet, GFSK output power=2dBm
- Receive(BDR): Current level during receive of a basic rate packet

Note.2
- Transmit(EDR): Current level during transmit of 2 or 3Mbps rate packet
- Receive(EDR): Current level during receive of 2 or 3Mbps rate packet

5 Timing and AC Characteristics

5.1 Power ON/OFF Timing

The TCM3903 startup and firmware boot is held off while the RESET pin is deasserted.

The TCM3903 has an integrated power-on reset circuit which completely resets all circuits to a known power on state. This action can also be driven by BT_RST_N signal, which can be used to externally control the device, forcing it into a power-on reset state.

Note:

- VBAT and VDDIO should not rise 10%-90% faster than 200 microseconds.
- VBAT should be up before VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.
- BT_RST_N signal input is an active-low signal. This signal must be driven high or low (not left floating).
- The TCM3903 requires an external pull-up or pull-down resistor on the BT_RST_N input.
- BT_RST_N and BT_REG_ON controlled by GPIO of HOST

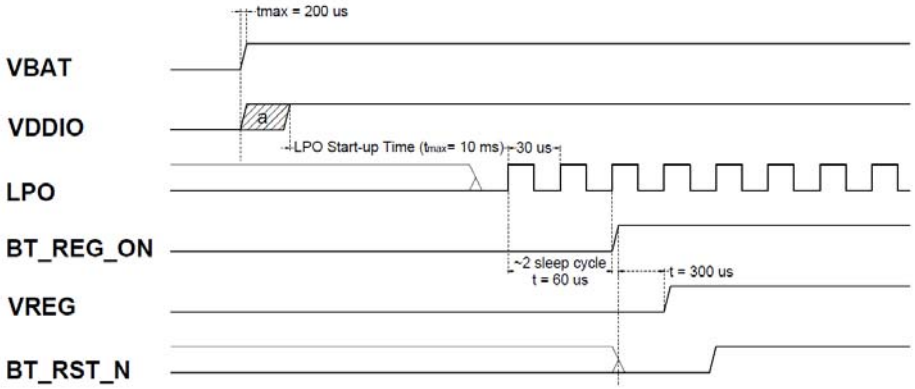


Figure 5.1 Startup Timing from BT_RST_N

5.2 UART Timing

Table 5.1 UART timing specifications

Description	Min	Typ.	Max.	Unit
Delay time, UART_CTS_N low to UART_TXD valid	-	-	24	Baudout cycles
Setup time, UART_CTS_N high before midpoint of stop bit	-	-	10	ns
Delay time, midpoint of stop bit to UART RTS_N high	-	-	2	Baudout cycles

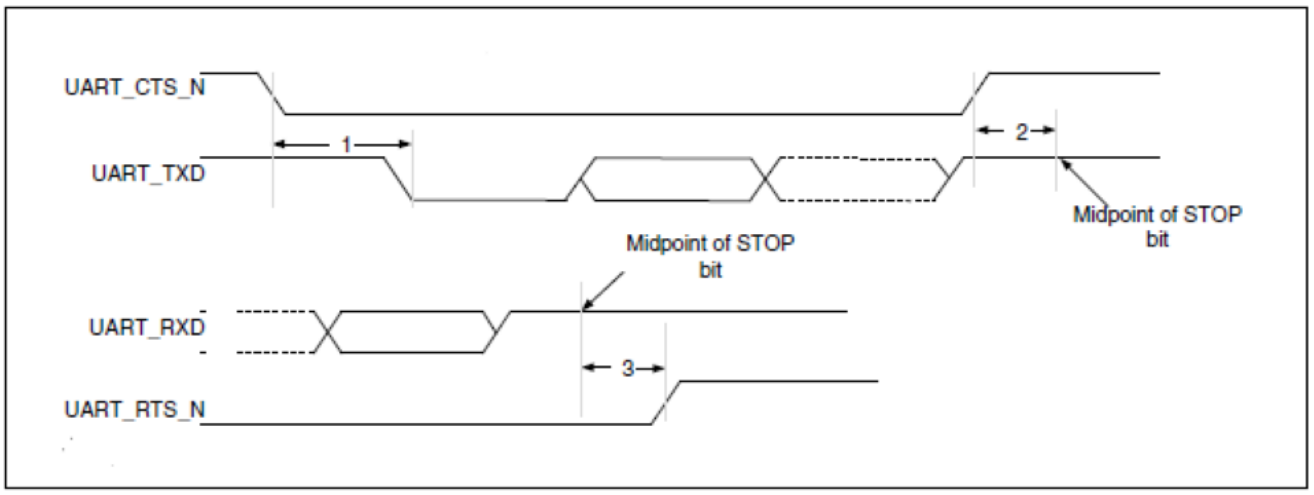


Figure 5.1 UART timing

5.3 PCM Timing

Table 5.2 PCM interface timing specifications (short frame synchronization, master mode)

Description	Min	Typ.	Max.	Unit
PCM bit clock frequency	128	-	2048	KHz
'PCM bit clock HIGH time	128	-	-	ns
PCM bit clock LOW time	209	-	-	ns
Delay from PCM_BCLK rising edge to PCM_SYNC high	-	-	50	ns
Delay from PCM_BCLK rising edge to PCM_SYNC low	-	-	50	ns
Delay from PCM_BCLK rising edge to data valid on PCM_OUT	-	-	50	ns
Setup time for PCM_IN before PCM_BCLK falling edge	50	-	-	ns
Hold time for PCM_IN after PCM_BCLK falling edge	10	-	-	ns
Delay from falling edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	-	-	50	ns

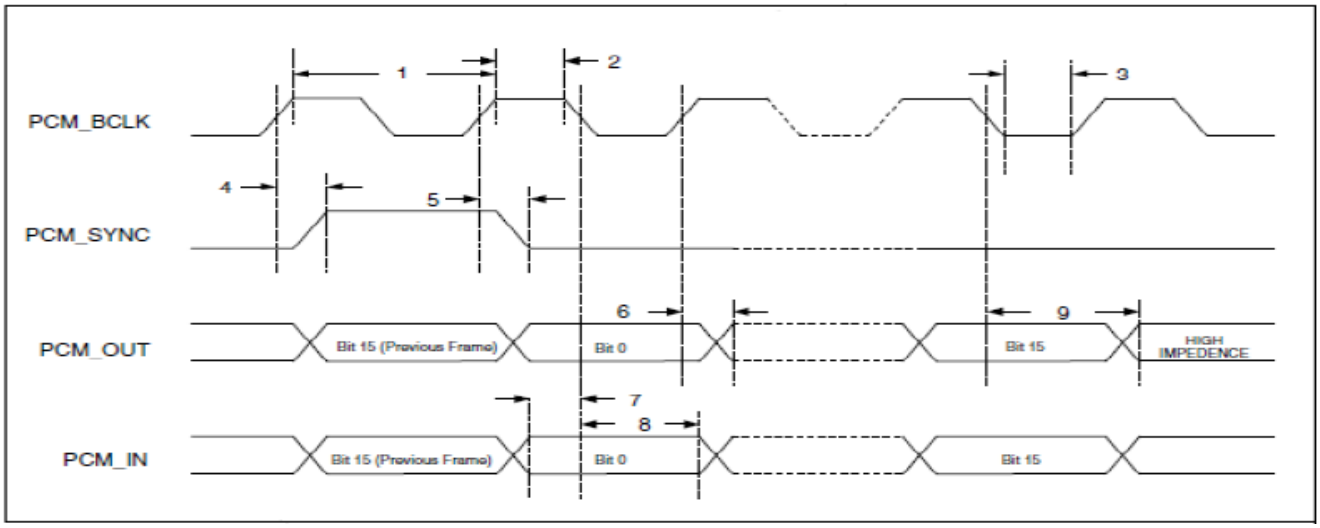


Figure 5.1 PCM interface timing (short frame synchronization, master mode)

Table 5.3 PCM interface timing specifications (short frame synchronization, slave mode)

Description	Min	Typ.	Max.	Unit
PCM bit clock frequency	128	-	2048	KHz
PCM bit clock HIGH time	209	-	-	ns
PCM bit clock LOW time	209	-	-	ns
Setup time for PCM_SYNC before falling edge of PCM_BCLK	50	-	-	ns
Hold time for PCM_SYNC after falling edge of PCM_BCLK	10	-	-	ns
Hold time for PCM_OUT after PCM_BCLK falling edge	-	-	175	ns
Setup time for PCM_IN before PCM_BCLK falling edge	50	-	-	ns
Hold time for PCM_IN after PCM_BCLK falling edge	10	-	-	ns
Delay from falling edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	-	-	100	ns

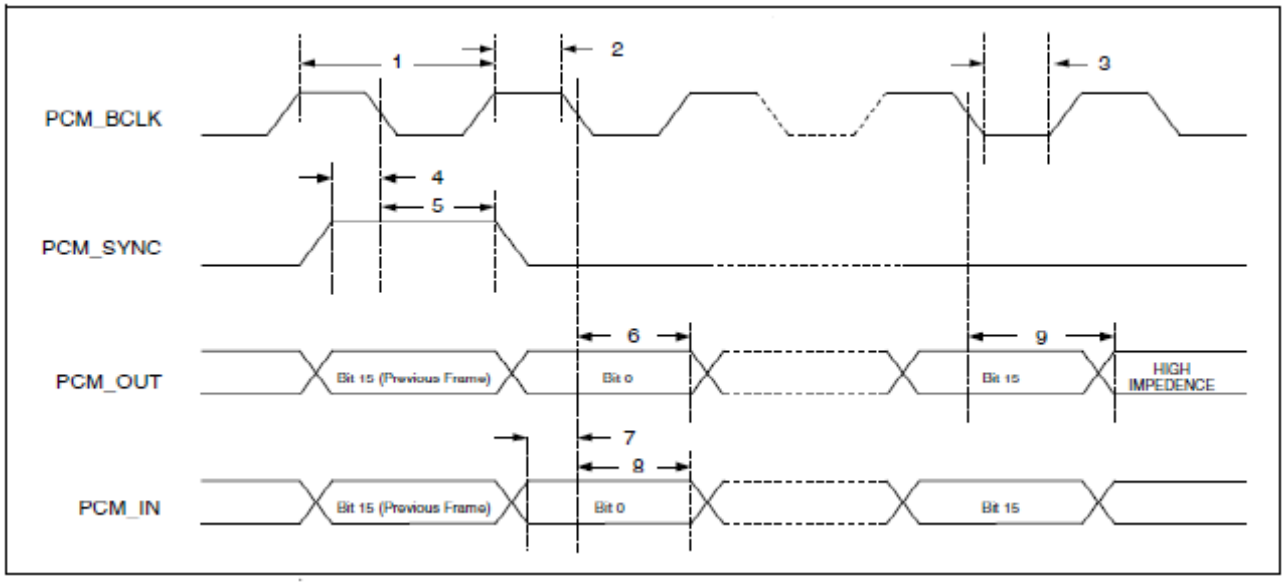


Figure 5.2 PCM interface timing (short frame synchronization, slave mode)

Table 5.4 PCM interface timing specifications (Long frame synchronization, master mode)

Description	Min	Typ.	Max.	Unit
PCM bit clock frequency	128	-	2048	KHz
'PCM bit clock HIGH time	209	-	-	ns
PCM bit clock LOW time	209	-	-	ns
Delay from PCM_BCLK rising edge to PCM_SYNC high during first bit time	-	-	50	ns
Delay from PCM_BCLK rising edge to PCM_SYNC low during third bit time	-	-	50	ns
Delay from PCM_BCLK rising edge to data valid on PCM_OUT	-	-	50	ns
Setup time for PCM_IN before PCM_BCLK falling edge	50	-	-	ns
Hold time for PCM_IN after PCM_BCLK falling edge	10	-	-	ns
Delay from falling edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	-	-	50	ns

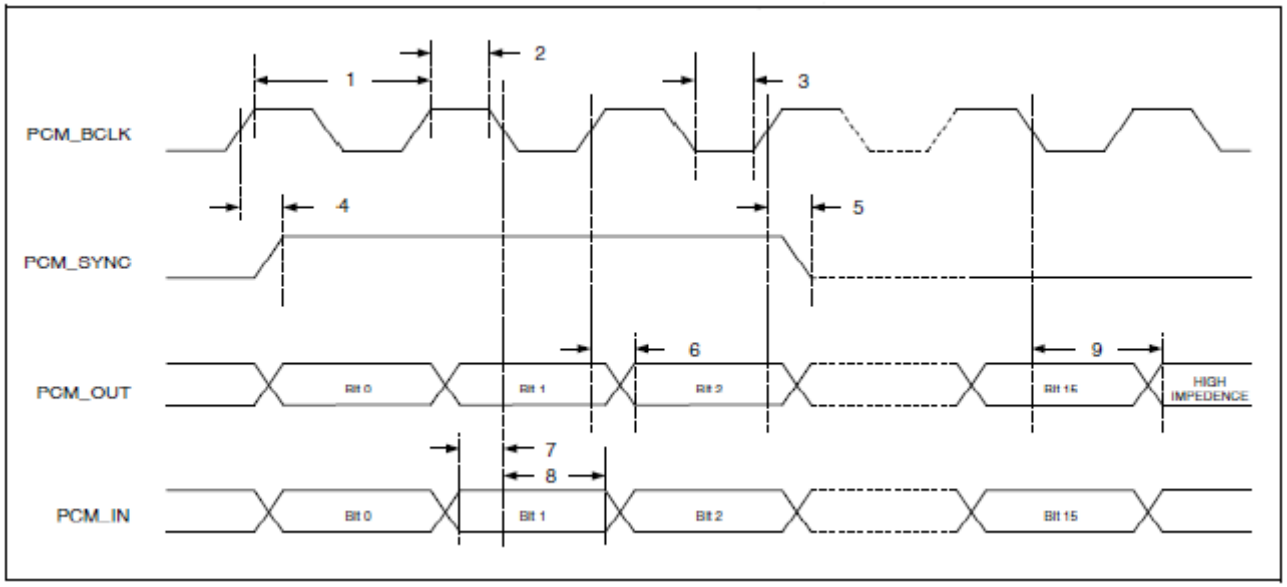


Figure 5.3 PCM interface timing (Long frame synchronization, master mode)

Table 5.5 PCM interface timing specifications (Long frame synchronization, slave mode)

Description	Min	Typ.	Max.	Unit
PCM bit clock frequency	128	-	2048	KHz
PCM bit clock HIGH time	209	-	-	ns
PCM bit clock LOW time	209	-	-	ns
Setup time for PCM_SYNC before falling edge of PCM_BCLK during first bit time	50	-	-	ns
Hold time for PCM_SYNC after falling edge of PCM_BCLK during second bit period.(PCM_SYNC may go low any time from second bit period to last bit period)	10	-	-	ns
Delay from rising edge of PCM_BCLK or PCM_SYNC (whichever is later) to data valid for first bit on PCM_OUT	-	-	50	ns
Hold time for PCM_OUT after PCM_BCLK falling edge	-	-	175	
Setup time for PCM_IN before PCM_BCLK falling edge	50	-	-	ns
Hold time for PCM_IN after PCM_BCLK falling edge	10	-	-	ns
Delay from falling edge of PCM_BCLK or PCM_SYNC (whichever is later) during last bit in slot to PCM_OUT becoming high impedance	-	-	100	ns

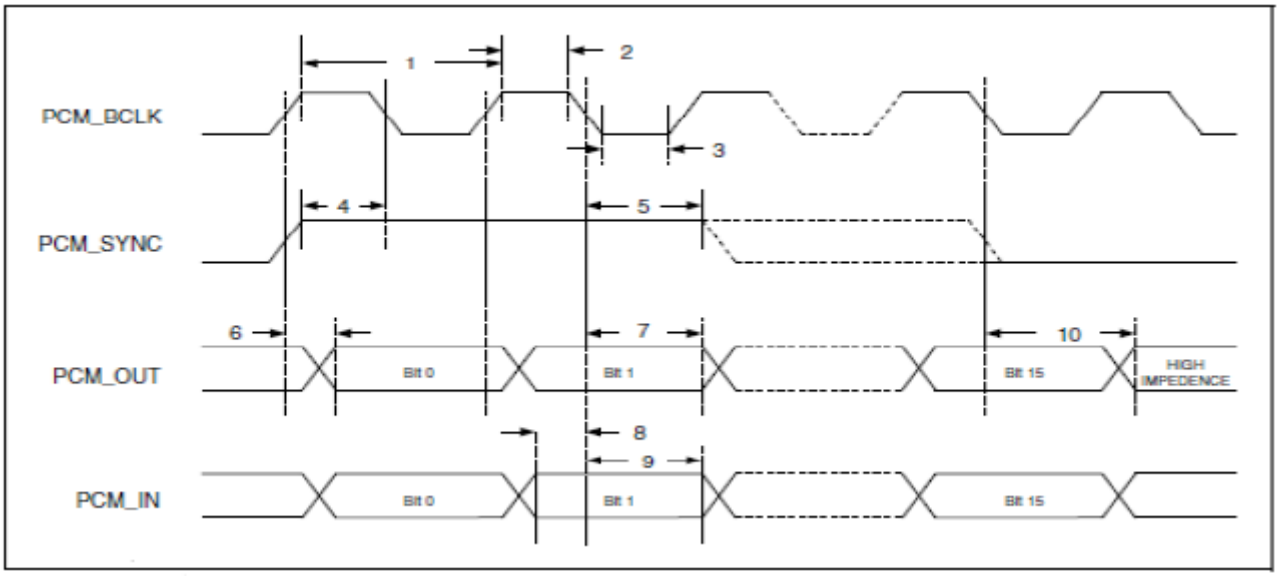


Figure 5.4 PCM interface timing (Long frame synchronization, slave mode)

6 RF Specification

Nomal Condition : 25deg.C, VBAT=3.3V, VDDIO=3.3V

Table 6.1 RF Specification

Transmitter	***Min***	***Typ***	***Max***	**Unit**
BDR				
Output Power(Class 2)	0	2[1]	4	dBm
Frequency range	2401	-	2480	MHz
20dB bandwidth	-	-	1	MHz
Adjacent Channel Power				
[M-N]=2	-	-	-20	dBm
[M-N]>=3	-	-	-40	dBm
Modulation Characteristics				
Delta f1avg	140	-	175	KHz
Delta f2max (at 99.9%)	99.9	-	-	%
Delta f2avg / Delta f1avg	0.8	-	-	%
Initial Carrier Frequency Tolerance	-75	-	75	KHz
Carrier Frequency Drift				
1slot	-25	-	25	KHz
3slot / 5slot	-40	-	40	KHz
Maximum drift rate	-20	-	20	KHz/50uS
EDR				
EDR Relative Power for DQPSK / 8DPSK	-4	-	1	dBm
EDR Carrier Frequency Stability and Modulation Accuracy				
wi	-75	-	75	KHz
wi+wo	-75	-	75	KHz
wo	-10	-	10	KHz
RMS DEVM(DQPSK)	-	-	20	%
Peak DEVM(DQPSK)	-	-	35	%
99% DEVM(DQPSK)	99	-	-	%
RMS DEVM(8DPSK)	-	-	13	%
Peak DEVM(8DPSK)	-	-	25	%
99% DEVM(8DPSK)	99	-	-	%
Receiver	**Min**	**Typ**	**Max**	**Unit**
BDR				
Sensitivity(BER=<0.1%) for GFSK	-70	-	-	dBm
Maximum input Level(BER=<0.1%)	-20	-	-	dBm
EDR				
Sensitivity(BER=<0.007%) for DQPSK	-77	-		dBm
Sensitivity(BER=<0.007%) for 8DPSK	-77	-		dBm

[1] Output power is the conduction measurement. Radiation output power is lower than the indicated value. The output power specification during production is controlled from -6 to +4 dBm at the coupler.

Bluetooth LE(Low Energy)	Min	Typ	Max	Unit
Output Power	-	-	10	dBm
Modulation Characteristics				
Delta f1avg	225	-	275	KHz
Delta f2max (at 99.9%)	99	-	-	%
Delta f2avg / Delta f1avg	0.8	-	-	%
Carrier Frequency Offset and Drift				
Frequency Offset	-	-	150	KHz
Frequency Drift	-	-	50	KHz
Drift Rate	-	-	20	KHz
Receiver Sensitivity(PER<30.8%)	-70	-	-	dBm
Maximum Input Signal Level(PER<30.8%)	-10	-	-	dBm
PER Report Integrity (-30dBm Input)	50	-	65.4	%

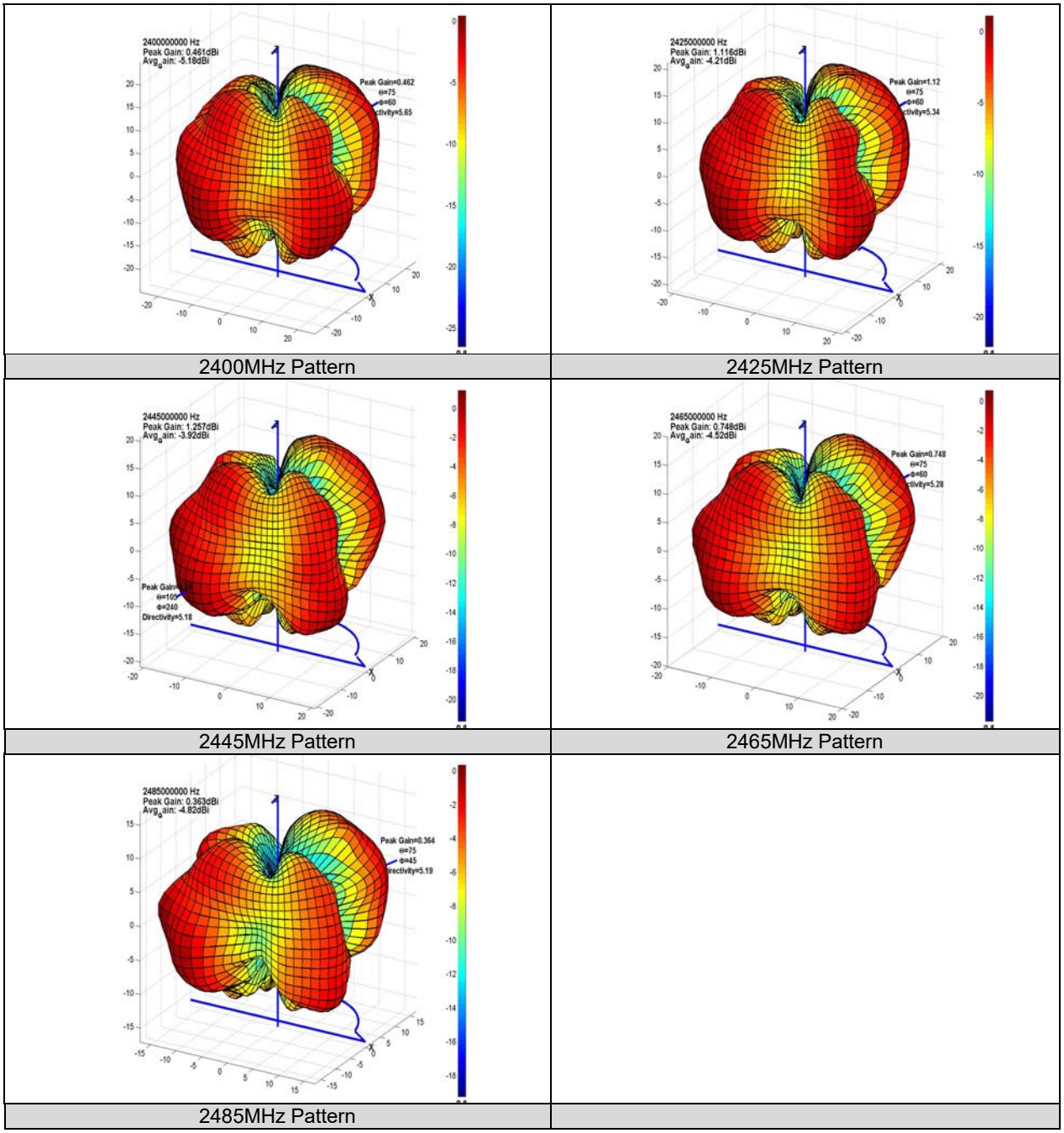
7 Internal Pattern Antenna Specification

7.1 Antenna Gain

Table 7.1 Antenna Gain

Frequency	Efficiency	Average Gain	Max Gain	Max Position
2400MHz	30.3 %	-5.2 dBi	0.5 dBi	Theta75/Pie150
2425MHz	37.8 %	-4.2 dBi	1.1 dBi	Theta75/Pie150
2445MHz	40.5 %	-3.9 dBi	1.3 dBi	Theta105/Pie330
2465MHz	35.2 %	-4.5 dBi	0.7 dBi	Theta75/Pie150
2485MHz	32.9 %	-4.8 dBi	0.4 dBi	Theta75/Pie135

7.2 Antenna 3D Radiation Pattern



2400MHz Pattern | 2425MHz Pattern

2445MHz Pattern | 2465MHz Pattern

2485MHz Pattern

Figure 7.1 3D Radiation Pattern

8 Interface Description

8.1 UART

The UART physical interface is a standard, 4-wire(RX, TX, RTS, CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate can be selected via a vendor-specific UART HCI commend. The interface supports Bluetooth UART HCI specifications. The default baud rate is 115.2Kbaud.

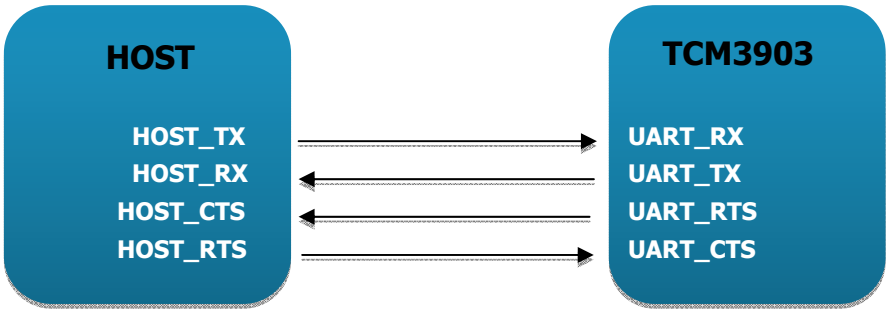


Figure 8.1 UART Interface Connection

8.2 PCM/I2S

The TCM3903 PCM interface can connect to linear PCM codec devices in master or slave mode. In master mode, the device generates the PCM_BCLK and PCM_SYNC signals. In slave mode, these signals are provided by another master on the PCM interfaces as inputs to the device.

The PCM interface supports the industry standard formats for I2S, left-justified or right-justified.

The host can adjust the PCM interface configuration using vendor-specific HCI commands or it can be setup in the configuration file.

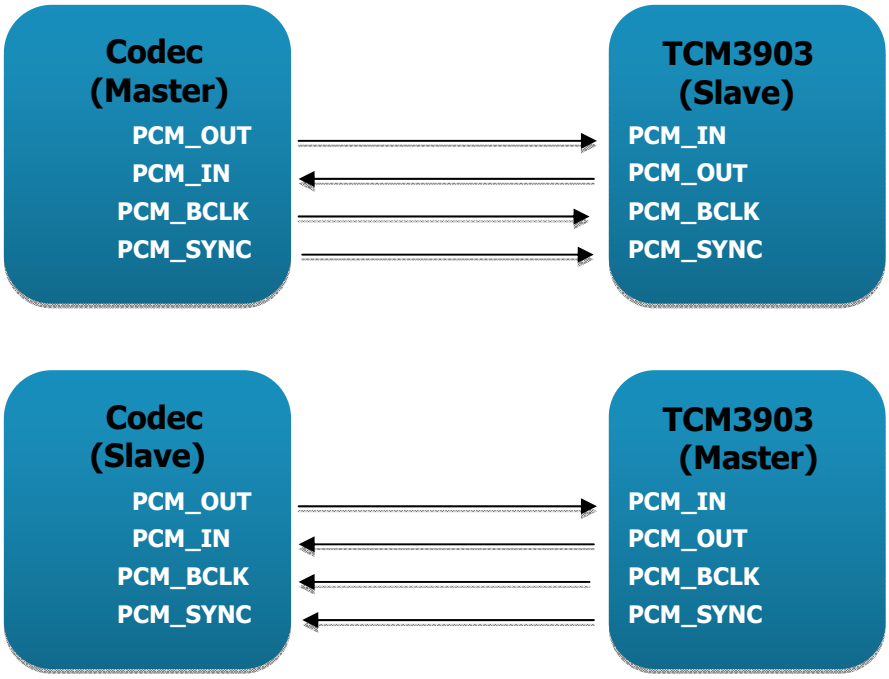


Figure 8.2 PCM Interface Connection

8.3 SECI

The TCM3903 provides extensions and collaborative coexistence to the standard Bluetooth AFH for direct communication with WLAN devices. Collaborative coexistence enables WLAN and Bluetooth to operate simultaneously in a single device. The device supports industry-standard coexistence signaling, including 802.15.2, and supports WLAN solutions.

- Enhanced coexistence data can be exchanged over SECI_IN and SECI_OUT
- It supports generic UART communication between WLAN and Bluetooth devices.
- Up to 48-bits of coexistence data can bel exchanged

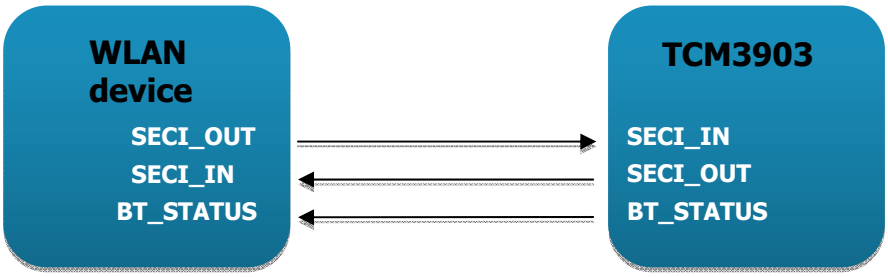


Figure 8.3 SECI Interface Connection

9 Mechanical Information

(Unit : mm)

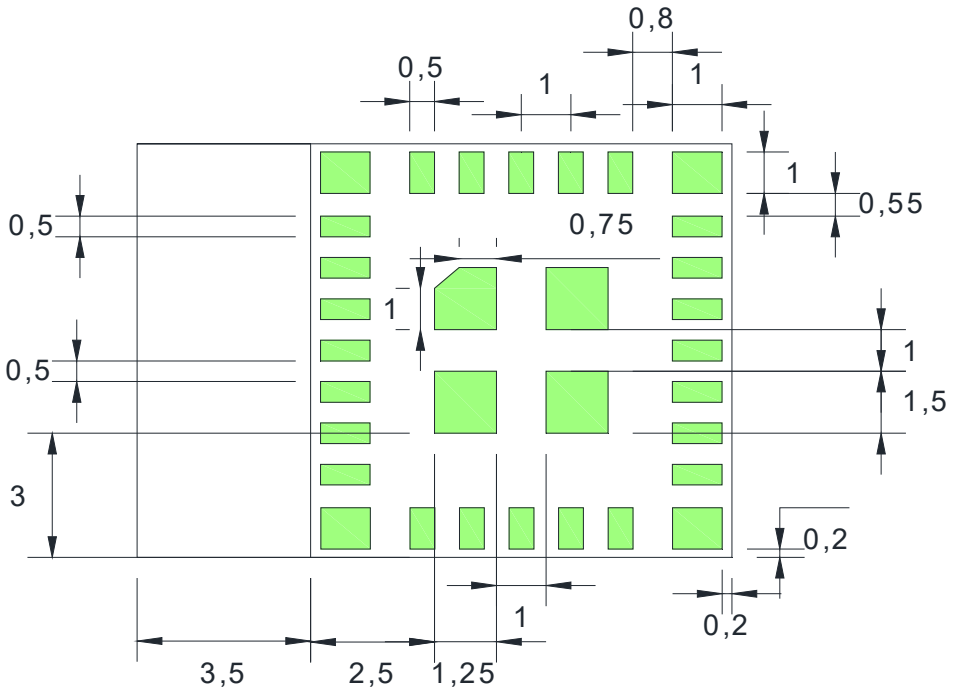


Figure 9.1 32-pin LGA package Mechanical Information (TOP VIEW)

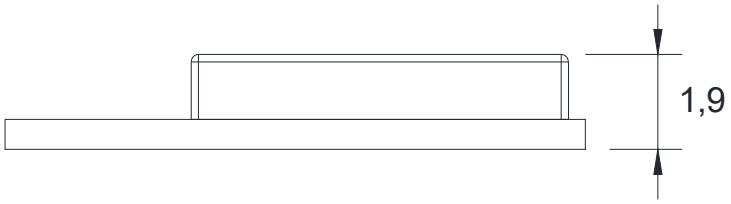
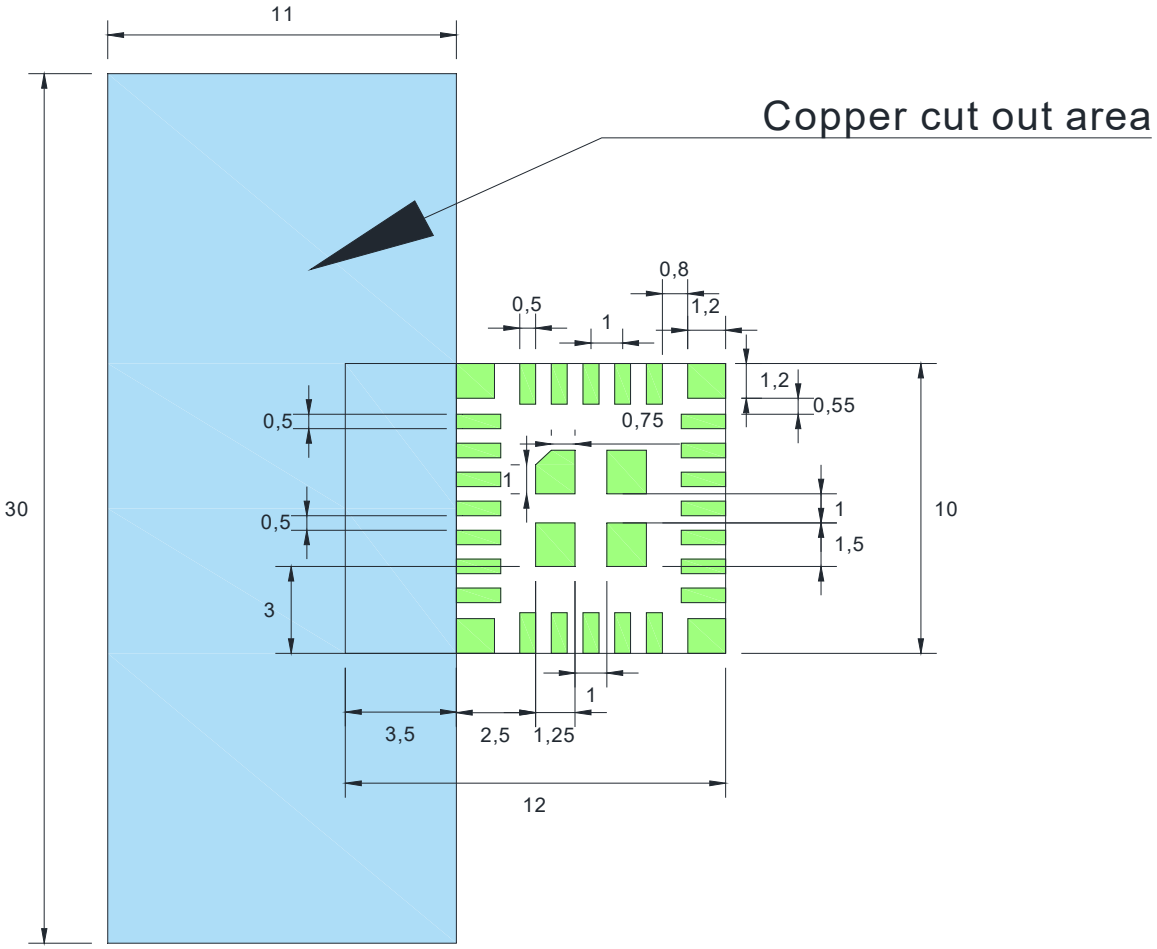


Figure 9.2 Side View



※ Antenna part should be placed outside the PCB

Figure 9.3 PCB Footprint recommendation

10 Reference Peripheral Circuit

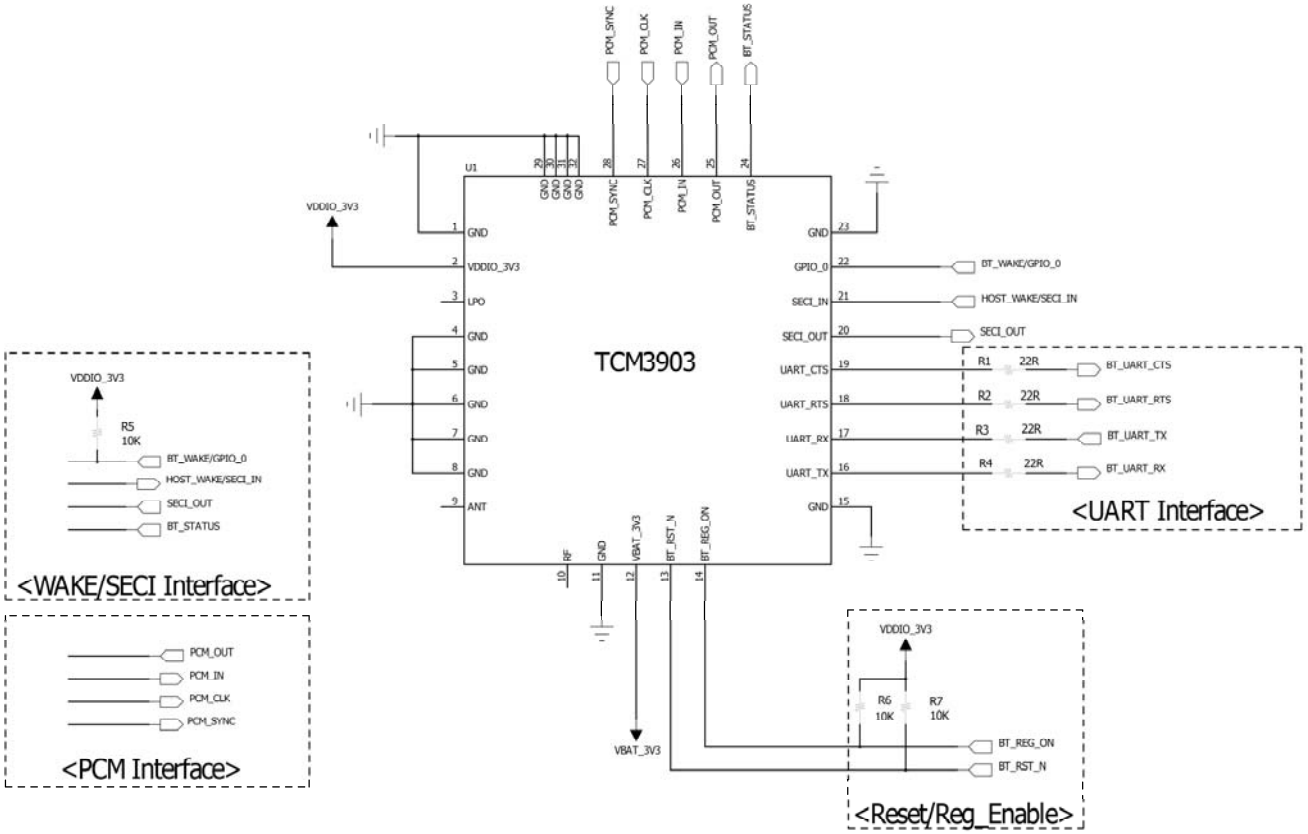
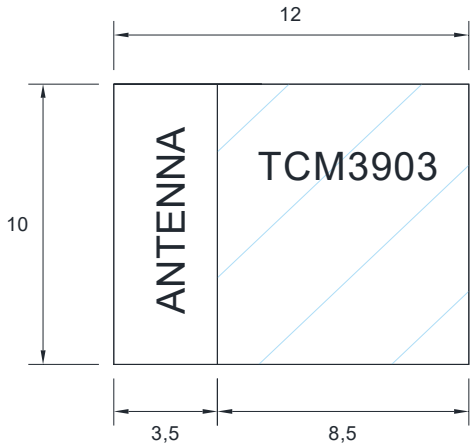


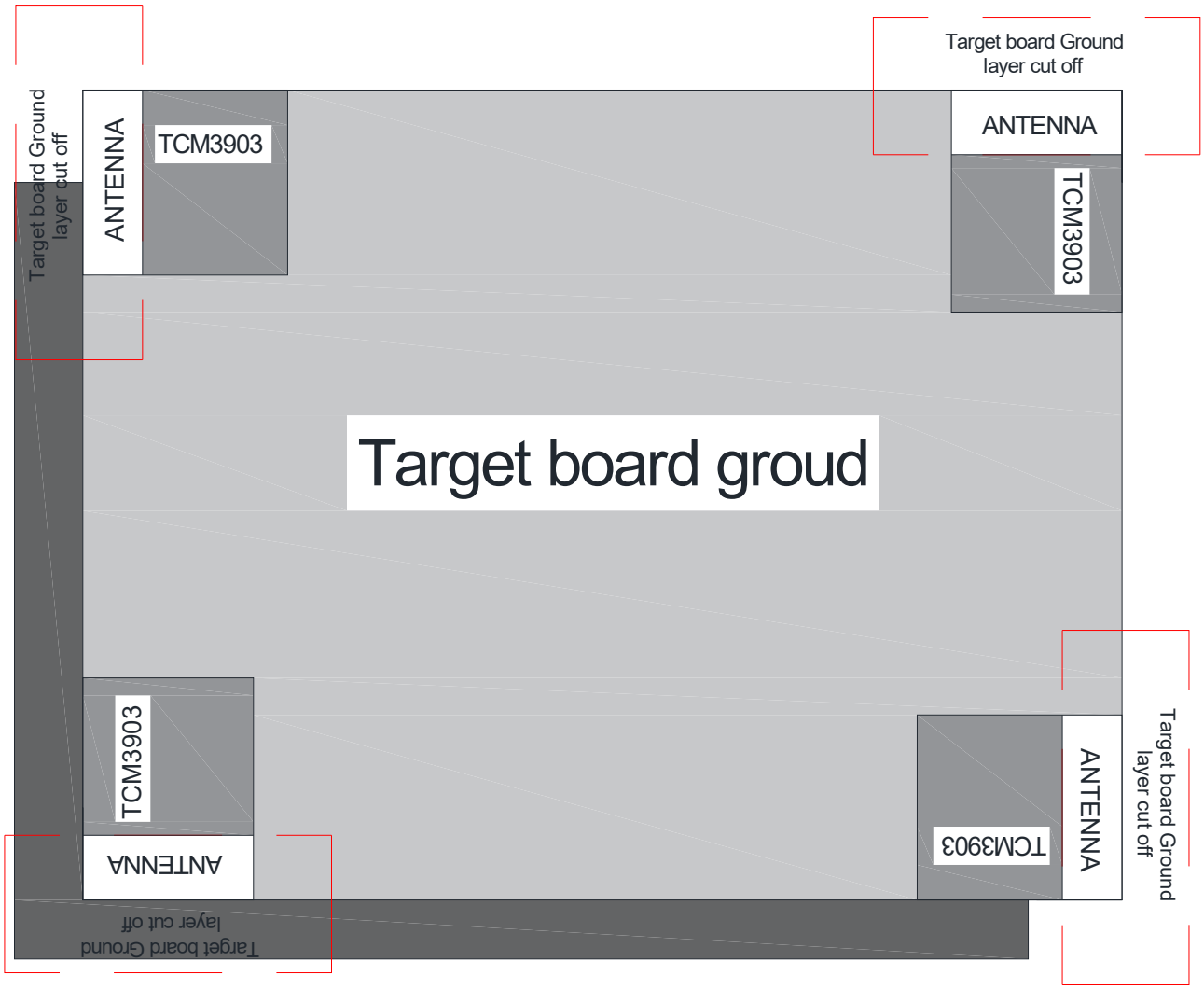
Figure 10.1 Reference Peripheral Circuit

11 Antenna Design Guide

11.1 Antenna Field in Module



11.2 Module position on Target board



12 SMT Temperature Sequence (Pb-free)

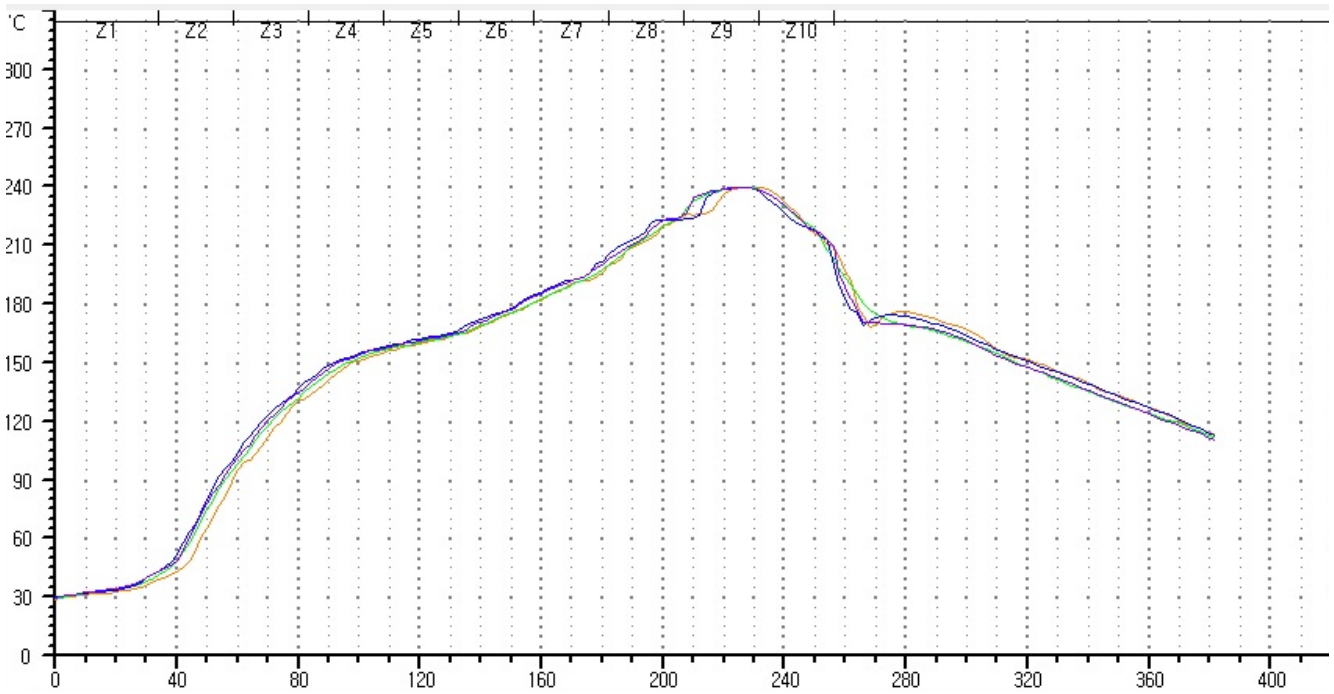


Figure 12.1 SMT Temperature Sequence

Certifications

Certified under FCC Part 15
Certified in Canada by IC to RSS-247
Manufacturer Model : TCM3903
FCC ID: 2ALS3-3903
IC: 22661-3903
Product Marketing Name (PMN): Bluetooth module

FCC Statement
This device complies with Part 15 of the FCC rules. Operation is subject to the following conditions: (1)This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

FCC Caution
Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

Important Note

OEM Responsibilities to comply with FCC and Industry Canada Regulations

The TCM3903 Module has been certified for integration into products only by OEM integrators under the following conditions:

1. The antenna(s) must be installed such that a minimum separation distance of 20cm is maintained between the radiator (antenna) and all persons at all times.
2. The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter.

As long as the two conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

IMPORTANT NOTE: In the event that these conditions cannot be met (for certain configurations or co-location with another transmitter), then the FCC and Industry Canada authorizations are no longer considered valid and the FCC ID and IC Certification Number cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC and Industry Canada authorization.

Label of the end product
The final end product must be labeled in a visible area with the following " Contains FCC ID: 2ALS3-3903" and " Contains IC : 22661-3903". If the size of the end product is larger than 8x10cm, then the following FCC part 15.19 statement has to also be available on the label: This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

Canada Statement
“This device complies with Industry Canada’s license-exempt RSSs.
Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference,
including interference that may cause undesired operation of the device.”

« Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement. »

Exposure to Radio Frequency Energy
“To comply with FCC and Industry Canada RF radiation exposure limits for general population, the antenna(s) used for this transmitter must be installed such that a minimum separation distance of 20cm is maintained between the radiator (antenna) and all persons at all times and must not be co-located or operating in conjunction with any other antenna or transmitter.”