Bluetooth Stereo Audio Module- BTZ-983H

BTZ-983H Bluetooth® Stereo Audio Module Data Sheet

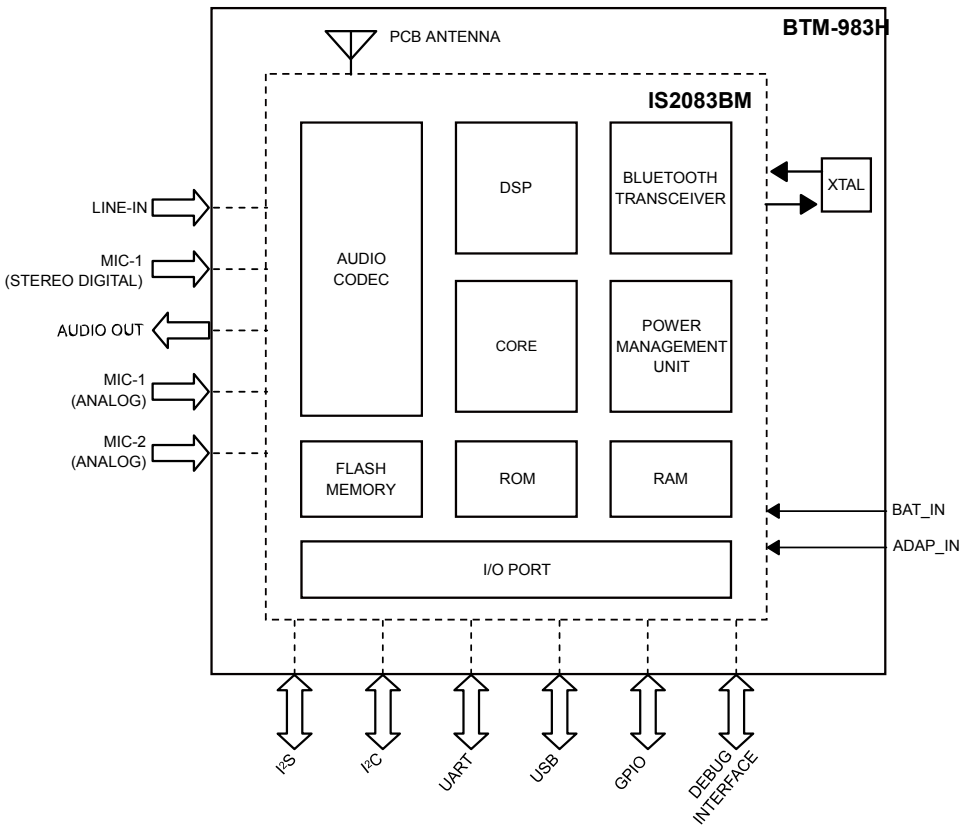
Introduction

The BTZ-983H, based on Microchip's dual-mode IS2083 system-on-chip (SoC) device, is an RF-certified, fully integrated module with high-performing voice and audio post-processing capability for Bluetooth audio applications. Tuning for Noise Reduction, Acoustic Echo Cancellation (AEC), and EQ filtering can be customized with an easy-to-use GUI Configuration Tool. This flexible platform provides multiple digital and analog audio interfaces including stereo microphones, I^2S, Line-In and a stereo audio DAC. It supports easy firmware upgrades via UART, USB and Over-the- Air (OTA).

This turn-key solution module pre-programmed with firmware that enables Bluetooth audio playback, for a plug-and-play solution. Control settings for LED drivers and other peripherals can be set via the Configuration Tool. Advanced developers can use the Software Development Kit (SDK) to implement their embedded applications.

Note: Contact your local sales representative for more information about the Software Development Kit (SDK).

Figure 1. BTZ-983H Module Block Diagram



The BTZ-983H module supports the following Bluetooth profiles and codecs:

- Profiles:
  - Hands-free Profile (HFP) 1.7, Headset Profile (HSP) 1.2, Advanced Audio Distribution Profile (A2DP) 1.3, Serial Port Profile (SPP) 1.2, Audio/Video Remote Control Profile (AVRCP) 1.6, and Phone Book Access Profile (PBAP) 1.2
- Codecs:
  - Advanced Audio Codec (AAC) and Sub-band Coding (SBC)

Features

- Qualified for Bluetooth v5.0 Specification
  - HFP 1.7, HSP 1.2, A2DP 1.3, SPP 1.2, AVRCP 1.6, and PBAP 1.2
  - Bluetooth classic (BR/EDR) and Bluetooth Low Energy
  - General Attribute Profile (GATT) and General Access Profile (GAP)
  - Bluetooth Low Energy Data Length Extension (DLE) and secure connection
- SDK
  - 8051 MCU debugging
  - 24-bit program counter and data pointer modes
- Multi-Link
  - A2DP (maximum 3 devices)
  - HFP (maximum 3 devices)
- Concert Mode and Stereo Mode
- Audio Interfaces
  - Stereo line input
  - Two analog microphones
  - One stereo digital microphone
  - Stereo audio Digital-to-Analog converter (DAC)
  - Inter-IC (I^2S) Sound input/output
  - I^2S Master Clock (MCLK)/reference clock
- USB, UART, and Over-the-Air (OTA) firmware upgrade
- Built-In Lithium-Ion and Lithium Polymer Battery Charger (up to 350 mA charging current)
- Compact Surface Mount Module:
  - 27 mm x 15 mm x 2.5 mm
  - Castellated surface mount pads
  - Module shield
- Integrated 3V and 1.8V Configurable Switching Regulator and Low-Dropout (LDO)

RF/Analog

- Frequency Spectrum: 2.402 GHz to 2.480 GHz
- Receive Sensitivity: –86.5 dBm(BRD), -85.5dBm (2 Mbps EDR, at 0.01% BER) , -78dBm(3MEDR) (Min)
- Programmable Transmit Output Power:
  - Up to +6.5 dBm (typical) for Basic Data Rate (BDR)
  - Up to +6.0 dBm (typical) for Enhanced Data Rate (EDR)

DSP Voice and Audio Processing

- 16/32-bit DSP Core with Enhanced 32-Bit Precision, Single Cycle Multiplier
- 64 Kbps A-Law, μ-Law Pulse Code Modulation (PCM), or Continuous Variable Slope Delta (CVSD) modulation for Synchronous Connection-Oriented (SCO) Channel Operation
- 8/16 kHz Noise Reduction (NR)
- 8/16 kHz Acoustic Echo Cancellation (AEC)

- Modified Sub-Band Coding (mSBC) Decoder for Wideband Speech
- Packet Loss Concealment (PLC) for SBC and AAC Codecs Only

Audio Codec

- SBC and AAC
- 20-bit Audio Stereo DAC with Signal-to-Noise Ratio (SNR) 95 dB
- 16-bit Audio Stereo Analog-to-Digital Converter (ADC) with SNR 90 dB
- 16-bit/24-bit I^2S Digital Audio
  - 8 kHz, 16 kHz, 44.1 kHz, and 48 kHz sampling frequency for SBC and AAC

Peripherals

- Successive Approximation Register Analog-to-Digital Converter (SAR ADC) with Dedicated Channels:
  - Battery voltage detection and adapter voltage detection
  - Charger thermal protection and ambient temperature detection
- UART (with hardware flow control)
- USB (full-speed USB 1.1 interface)
- Inter-Integrated Circuit (I^2C™) Master
- One Pulse Width Modulation (PWM) Channel
- Two LED Drivers
- Up to 18 General Purpose Inputs/Outputs (GPIOs)
- 2-wire 8051 MCU Joint Test Action Group (JTAG) Debug

Operating Conditions

- Operating Voltage: 3.2V to 4.2V
- Operating Temperature: –40°C to +85°C

Compliance

- Bluetooth Special Interest Group (SIG)
- Certified to the United States (FCC), Canada (ISED)
- RoHS Compliant

Applications

- Portable Speaker
- Multiple Speakers
- Headphones

FIGURE 1-2: BTZ-983H MODULE

2. Device Overview

The BTZ-983H stereo audio module is built around the IS2083BM SoC, which integrates the dual-mode baseband, modem, radio transceiver, PMU, MCU, crystal, and a DSP dedicated for audio and voice applications. Users can configure the BTZ-983H module by using the SDK or the IS208x_Config_GUI_Tool (Config Tool).

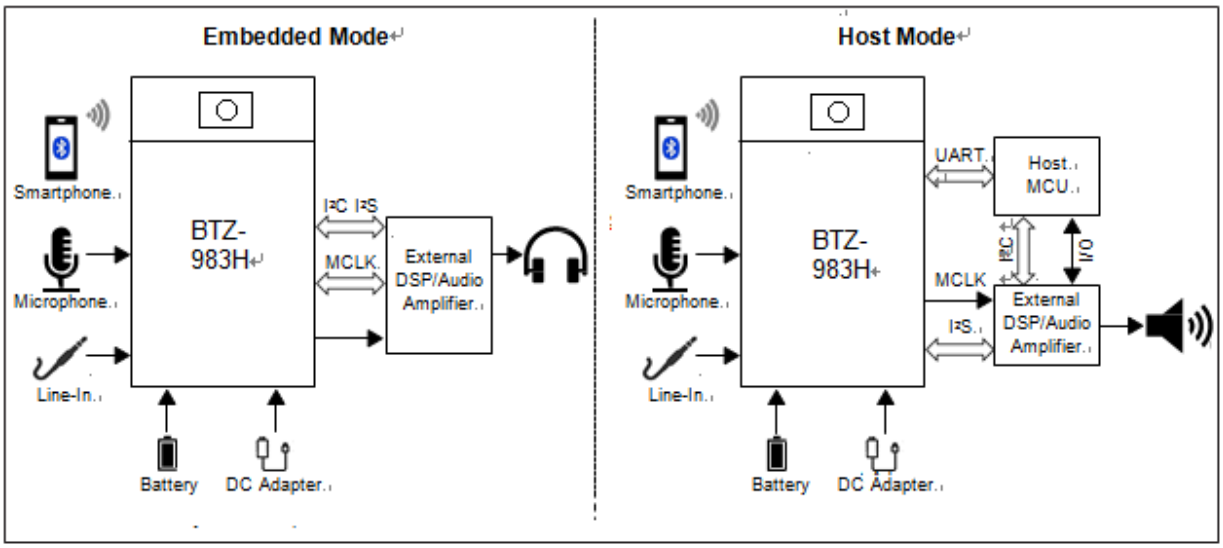
There are two modes of operation:

- Host mode:
  - Interfaces with an external MCU over UART for application specific system control.
  - The multi-speaker (MSPK) solution can reside on this MCU.
- Embedded mode:
  - No external MCU involved.
  - BTZ-983H acts as an MCU to control all peripherals to provide various speaker features.
  - Integrates the MSPK firmware on the module.
  - Simple system control can be implemented in the module MCU by using the SDK.
  - DSP parameters such as equalizer settings can be set using the Config Tool.

Note: The SDK and Config Tool are available for download at: http://www.microchip.com/BM83.

The following figure illustrates the Embedded mode and Host mode of the BTZ-983H module.

Figure 2-1. BTZ-983H Module Application Modes



The following table provides the features of the BTZ-983H module.

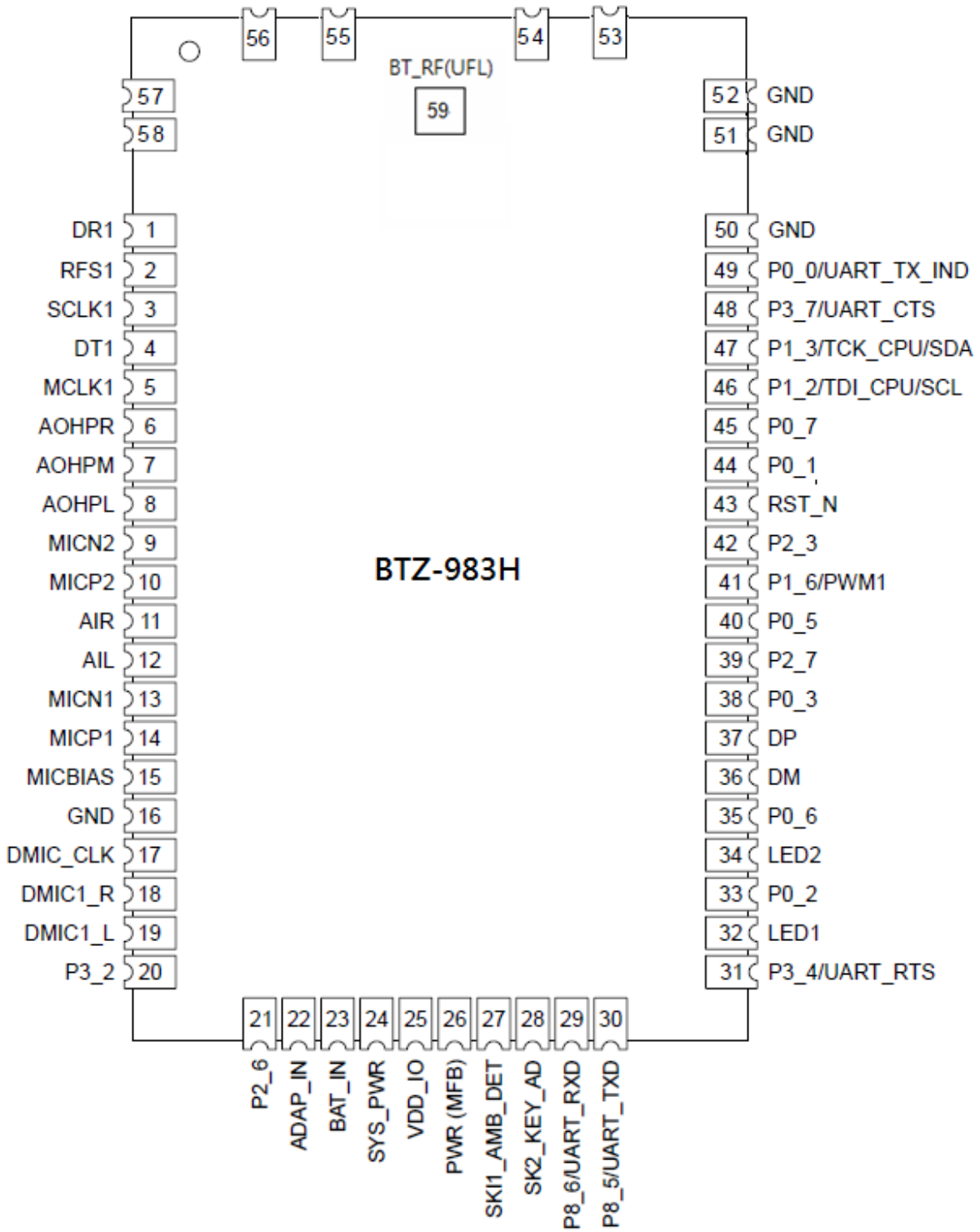
Table 2-1. BTZ-983H Module Features

Features	BTZ-983H
SoC	IS2083BM
Pin Count	59
Dimension	27 mm x 15 mm
RF	
PCB Antenna	Yes
Tx Power (typical)	+9 dBm (Class1)
RX Sensitivity	-90 dBm (2 Mbps EDR)
Bluetooth Power Class	Class 1
RF Shield	Yes
Audio	
Audio DAC Output	2-channel
DAC (Single-ended) SNR	-95 dB
DAC (Capless) SNR	-95 dB
ADC SNR	-90 dB
I^2S Audio (Input/Output) with Master Clock (MCLK) Output	Yes
Analog Auxiliary In	Yes
Analog Microphone	2
Stereo Digital Microphone	1
External Audio Amp Interface	Yes
Power	
Battery Input (BAT_IN)	3.8V (typ.)
DC Adapter Input (ADAP_IN)	5.0V (typ.)
Integrated BUCK Regulator	Yes
Battery Charger (350 mA charging current max)	Yes
Peripherals	
UART (with HW flow control)	Yes
I^2C Master	Yes
USB (full speed USB v1.1 interface)	Yes
SAR ADC	2
PWM	1
LED Driver	2
GPIOs	18
JTAG Debug Port (8051 MCU)	2-wire

2.1 BTZ-983H Module Pin Diagram

The following figure illustrates the pin diagram of the BTZ-983H module.

Figure 2-2. BTZ-983H Module Pin Diagram



2.2 BTZ-983H Module Pin Description

The following table describes the pin description of the BTZ-983H module.

Table 2-2. BTZ-983H Module Pin Description

Pin Number	Pin Name	Pin Type	Description
1	DR1	I	I^2S interface: digital left/right data
2	RFS1	I/O	I^2S interface: digital left/right clock
3	SCLK1	I/ O	I^2S interface: bit clock
4	DT1	O	I^2S interface: digital left/right data
5	MCLK1	O	I^2S interface: master clock
6	AOHPR	O	R-channel analog headphone output
7	AOHPM	O	Headphone common mode output/sense input
8	AOHPL	O	L-channel analog headphone output
9	MICN2	I	MIC 2 mono differential analog negative input
10	MICP2	I	MIC 2 mono differential analog positive input
11	AIR	I	R-channel single-ended analog input
12	AIL	I	L-channel single-ended analog input
13	MICN1	I	MIC 1 mono differential analog negative input
14	MICP1	I	MIC 1 mono differential analog positive input
15	MICBIAS	P	Electric microphone biasing voltage
16	GND	P	Ground reference
17	DMIC_CLK	O	Digital MIC clock output
18	DMIC1_R	I	Digital MIC right input
19	DMIC1_L	I	Digital MIC left input
20	P3_2	I/O	• General purpose I/O port P3_2 • By default, this is configured as AUX_IN DETECT
21	P2_6	I/O	General purpose I/O port P2_6
22	ADAP_IN	P	• 5V power adapter input • To charge the battery in the Li-ion battery powered applications • To be used for USB Device Firmware Upgrade (DFU) • Otherwise it can be left floating
23	BAT_IN	P	• Power supply input; voltage range: 3.2V to 4.2V • Source can either be a Li-ion battery or any other power rail on the host board

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Pin Number	Pin Name	Pin Type	Description
24	SYS_PWR	P	• System power output derived from the ADAP_IN or BAT_IN input • Only for internal use • Do not connect to any other devices • LED1 and LED2 can be connected to SYS_PWR
25	VDD_IO	P	I/O power supply, do not connect, for internal use only (connected to LDO31_VO)
26	PWR (MFB)	I	Multi-function push button and Power On key
27	SK1_AMB_DET	I	Temperature sense channel 1
28	SK2_KEY_AD	I	Temperature sense channel 2
29	P8_6 / UART_RXD	I/O	• General purpose I/O port P8_6 • UART RX data
30	P8_5 / UART_TXD	I/O	• General purpose I/O port P8_5 • UART TX data
31	P3_4 / UART_RTS	I/O	• General purpose I/O port P3_4 • System configuration pin (Application mode or Test mode) • UART RTS
32	LED1	I	LED driver 1
33	P0_2	I/O	• General purpose I/O port P0_2 • By default, this is configured as play/pause button (user configurable button)
34	LED2	I	LED driver 2
35	P0_6	I/O	• General purpose I/O port P0_6
36	DM	I/O	USB data minus data line
37	DP	I/O	USB data positive data line
38	P0_3	I/O	• General purpose I/O port P0_3 • By default, this is configured as reverse button (user configurable button)
39	P2_7	I/O	• General purpose I/O port P2_7 • By default, this is configured as volume up button (user configurable button)
40	P0_5	I/O	• General purpose I/O port P0_5 • By default, this is configured as volume down button (user configurable button)
41	P1_6 / PWM1	I/O	• General purpose I/O port P1_6 • PWM1 output
42	P2_3	I/O	General purpose I/O port P2_3
43	RST_N	I	System Reset pin (active-low)

.....continued

Pin Number	Pin Name	Pin Type	Description
44	P0_1	I/O	• General purpose I/O port P0_1 • By default, this is configured as forward button (user configurable button)
45	P0_7	I/O	General purpose I/O port P0_7
46	P1_2 / TDI_CPU / SCL	I/O	• General purpose I/O port P1_2 • CPU 2-wire debug data • I^2C SCL
47	P1_3 / TCK_CPU / SDA	I/O	• General purpose I/O port P1_3 • CPU 2-wire debug clock • I^2C SDA
48	P3_7 / UART_CTS	I/O	• General purpose I/O port P3_7 • UART CTS
49	P0_0 / UART_TX_IND	I/O	• General purpose I/O port P0_0 • By default, this is configured as an external codec reset (Embedded mode) • UART_TX_IND (active-high) used to wake-up the host MCU (Host mode)
50	GND	P	Ground reference
51	GND	P	Ground reference
52	GND	P	Ground reference
53	GND	P	Ground reference
54	GND	P	Ground reference
55	GND	P	Ground reference
56	GND	P	Ground reference
57	GND	P	Ground reference
58	GND	P	Ground reference
59	BT_RF(UFL)	-	External antenna connection (50ohm)

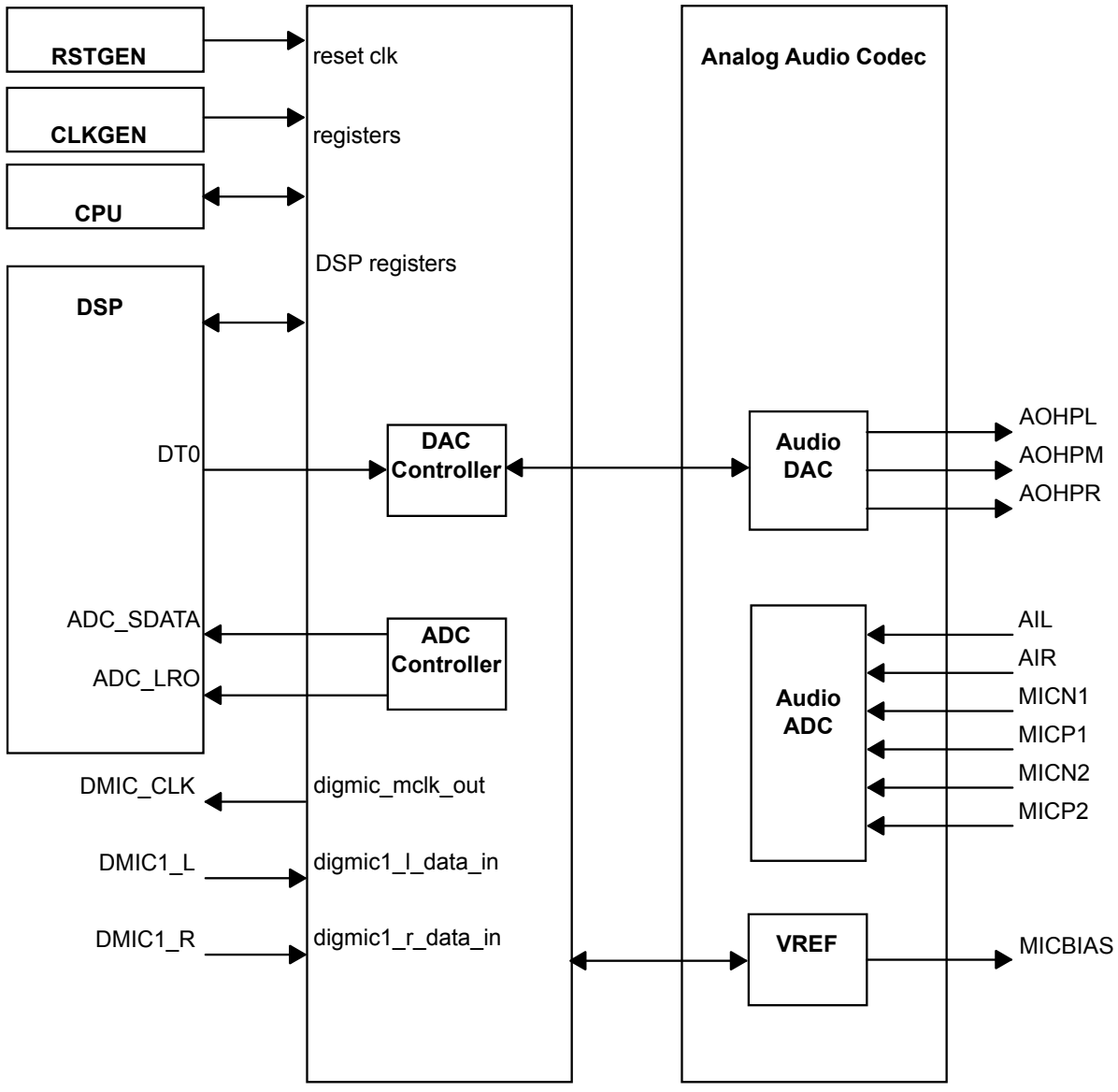
Note: The BTZ-983H module is pre-configured with Embedded mode (see, 6.4 General Purpose I/O Pins). The GPIOs mentioned in the preceding table can be configured using the Config Tool or the SDK.

3. Audio Subsystem

The input and output audios have different stages and each stage can be programmed to vary the gain response characteristics. For microphone, both single-ended inputs and differential inputs are supported. To maintain a high quality signal, a stable bias voltage source to the condenser microphone's Field-Effect Transistor (FET) is provided. The DC blocking capacitors can be used at both positive and negative sides of an input. Internally, this analog signal is converted to 16-bit, 8 kHz/16 kHz/44.1 kHz/48 kHz linear PCM data.

The following figure shows the audio subsystem.

Figure 3-1. Audio Subsystem



3.1 Digital Signal Processor

The BTZ-983H module integrates a high-performance DSP to provide excellent voice and audio user experience. The advanced speech features, such as AEC and NR are inbuilt. To reduce nonlinear distortion and echo cancellation, an

outgoing signal level to the speaker is monitored and adjusted to avoid saturation of speaker output or microphone input. Adaptive filtering is also applied to track the echo path impulse in response, to provide an echo free and full-duplex user experience.

The embedded noise reduction algorithm helps to extract clean speech signals from the noisy inputs captured by the microphones and improves communication.

In addition to NR/AEC function, audio effect functions such as Multiband Dynamic Range Compression (MB-DRC), virtual bass enhancement (VB), and audio widening (AW)), for A2DP audio streaming are also available to enhance the audio quality for various applications. For mono speaker/speakerphone and stereo headset applications, MB-DRC and VB can be enabled to have better audio clarity. For stereo speaker/speakerphone applications, in addition to MB-DRC and VB, AW can be enabled to provide better live audio effect for the users.

The following figures illustrate the signal processing flow of speakerphone applications for speech and audio signal processing.

Figure 3-2. Speech Signal Processing

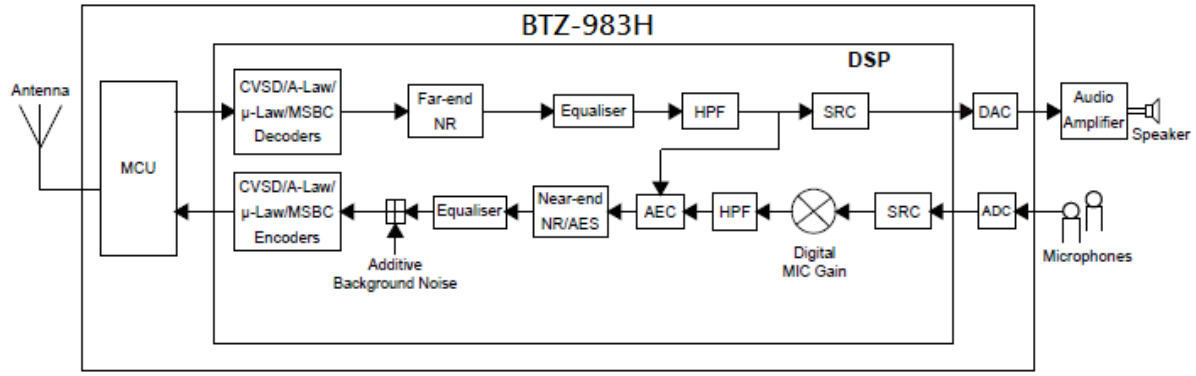
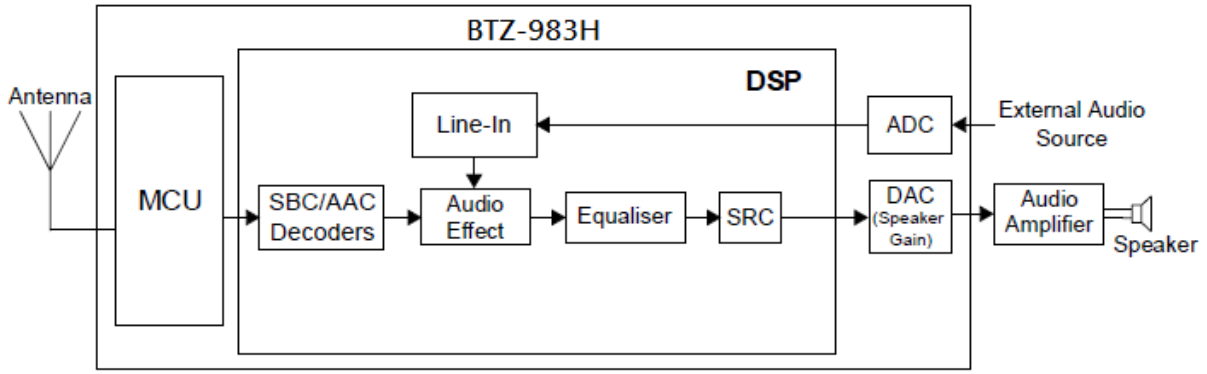


Figure 3-3. Audio Signal Processing



Note:

1. The DSP parameters can be configured using the Config Tool.
2. For more details on the DSP configuration and AEC tuning, refer to *Introduction to DSP Configuration Tool and AEC Tuning Guide (AN2432)*.

3.2 Codec

The built-in codec has a high SNR performance and it consists of an ADC, a DAC and an additional analog circuitry. The internal codec supports 20-bit resolution for DAC and 16-bit resolution for ADC.

- Interfaces
  - Two mono differential or single-ended MIC inputs

  - One stereo single-ended line input
  - One stereo single-ended line output
  - One stereo single-ended headphone output (capacitor-less connection)
- Built-in circuit
  - MIC bias
  - Reference and biasing circuitry
- Optional digital High Pass Filter (HPF) on ADC path
- Silence detection
  - To turn off the DSP and audio codec subsystem, if there is no Line-In data after UI configured time stamp.
- Anti-pop function (pop reduction system to reduce audible glitches)
- Sampling rates:
  - ADC/DAC/I^2S: 8 kHz, 16 kHz, 44.1 kHz, and 48 kHz

Note: The sampling rates can be selected in the **CODEC Setup** tab of Config Tool.

3.2.1 DAC Performance

The audio graphs in this section are produced in the following conditions:

- At room temperature
- Using BM83 EVB platform with BM83 module mounted on BM83 Carrier Board
- Input signal = 1 kHz sine tone, level sweep across -100 dBv to 6 dBv, frequency sweep across 20 Hz to 20 kHz at 1 Fs input level
- Various termination loads (16Ω, 32Ω, 100 kΩ)
- Analog gain = -3 dB; digital gain = 0 dB
- A-weighting applied, 22K bandwidth.

The following figures illustrate the DAC performance.

Figure 3-4 Gain Vs. Input Level at Various Loads (Capless Mode)

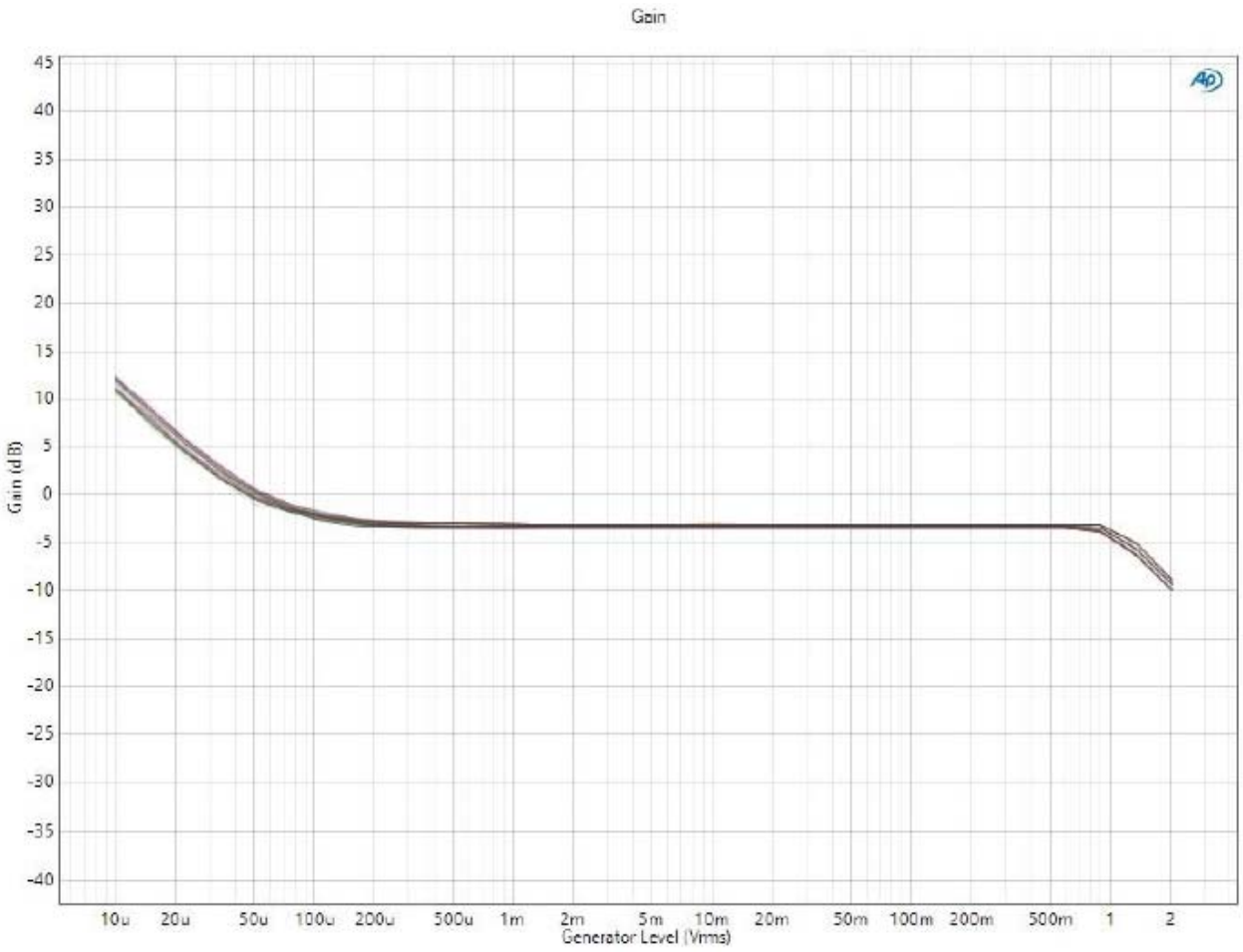


Figure 3-5 Gain Vs. Input Level at Various Loads (Single-ended Mode)

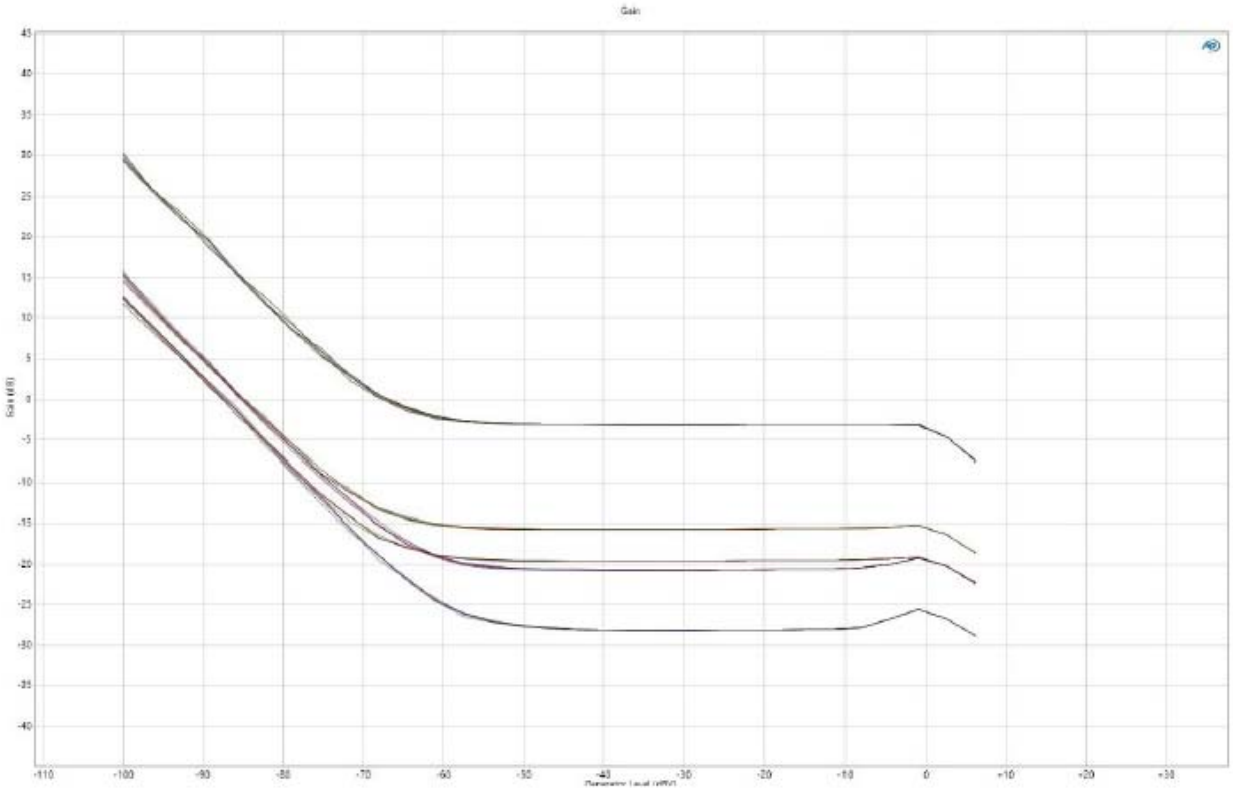


Figure 3-6 Gain Vs. Frequency at Various Loads (Capless Mode)

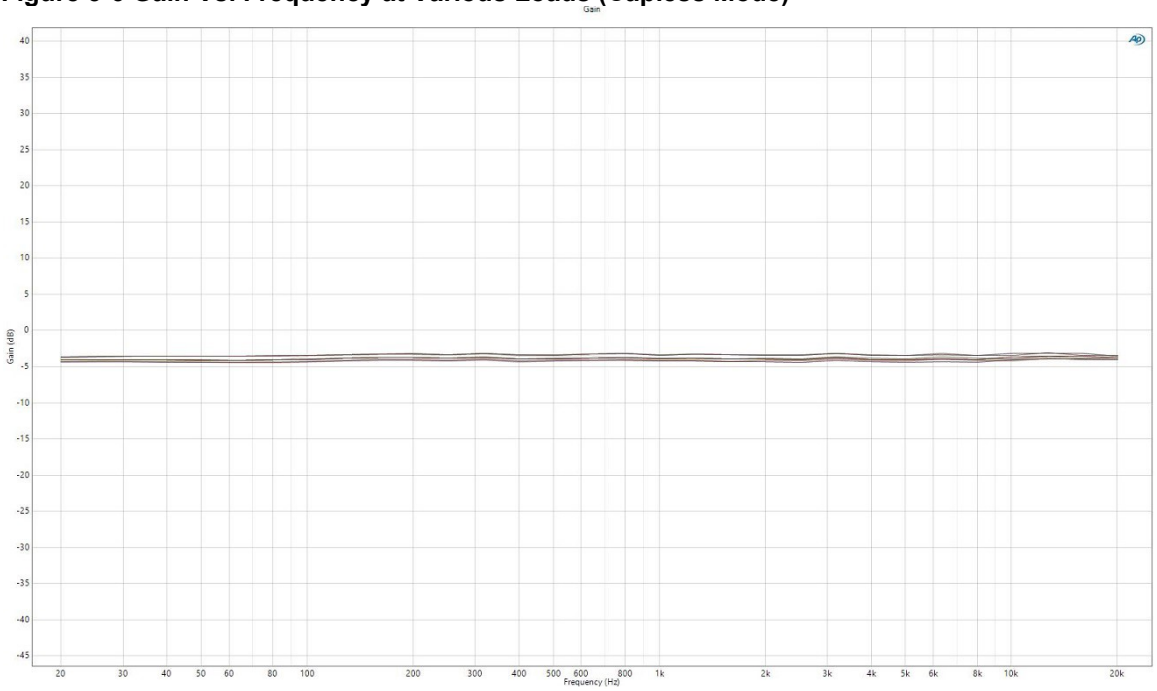


Figure 3-7. Gain Vs. Frequency at Various Loads (Single-ended Mode)

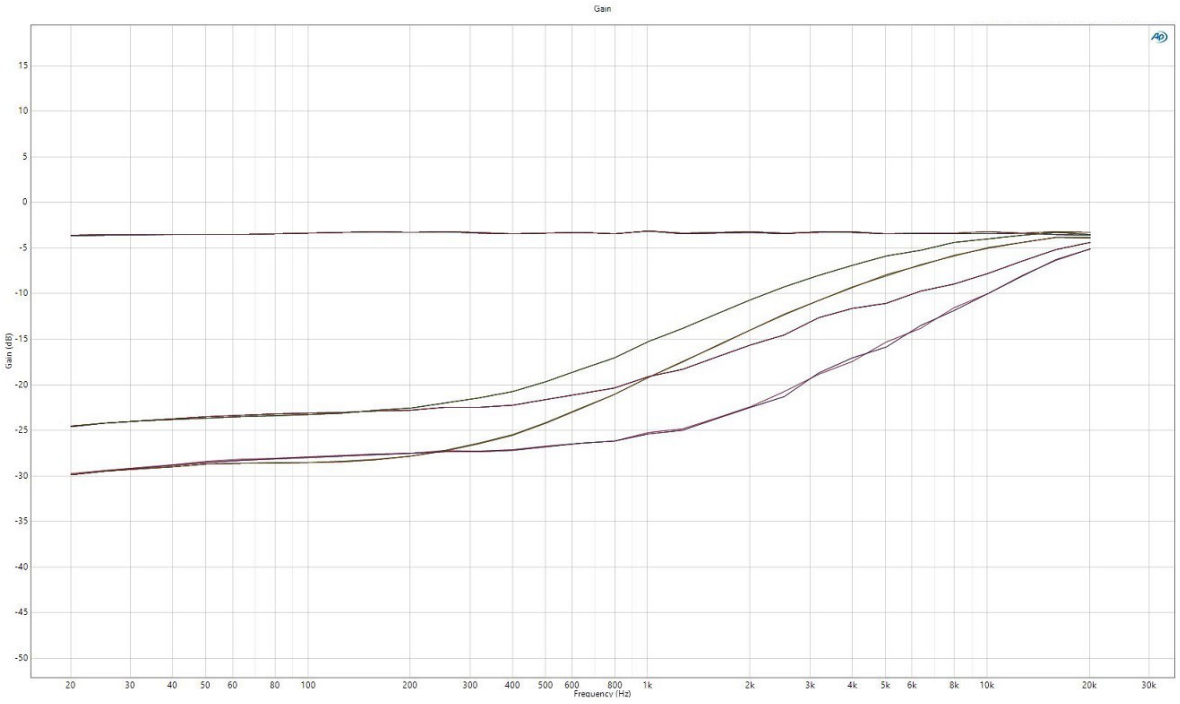


Figure 3-8. Level Vs. Frequency at Various Loads (Capless Mode)

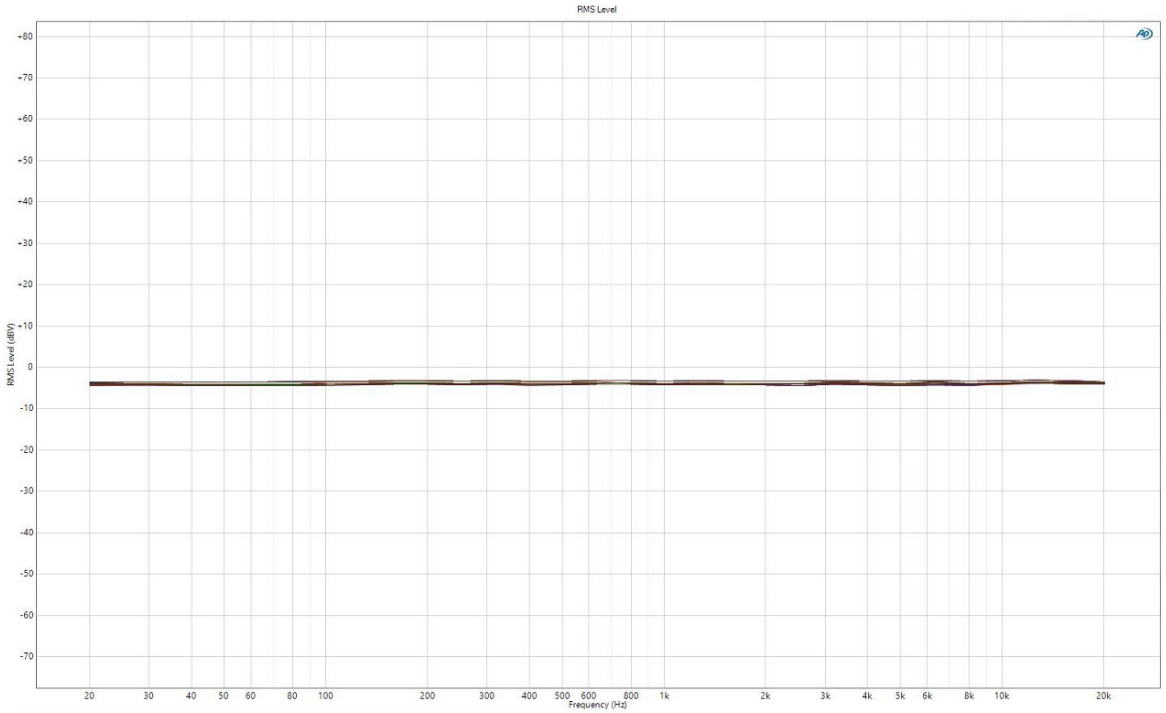


Figure 3-9. Level Vs. Frequency at Various Loads (Single-ended Mode)

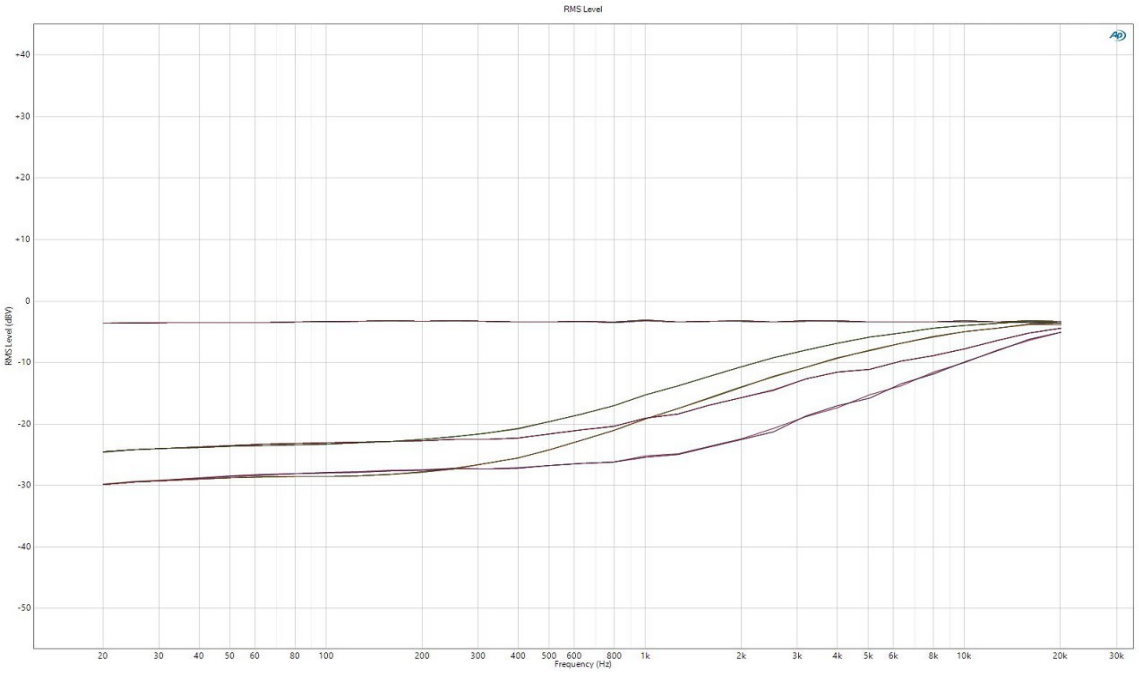


Figure 3-10. THD Ratio (%) Vs. Input Level at Various Loads (Capless Mode)

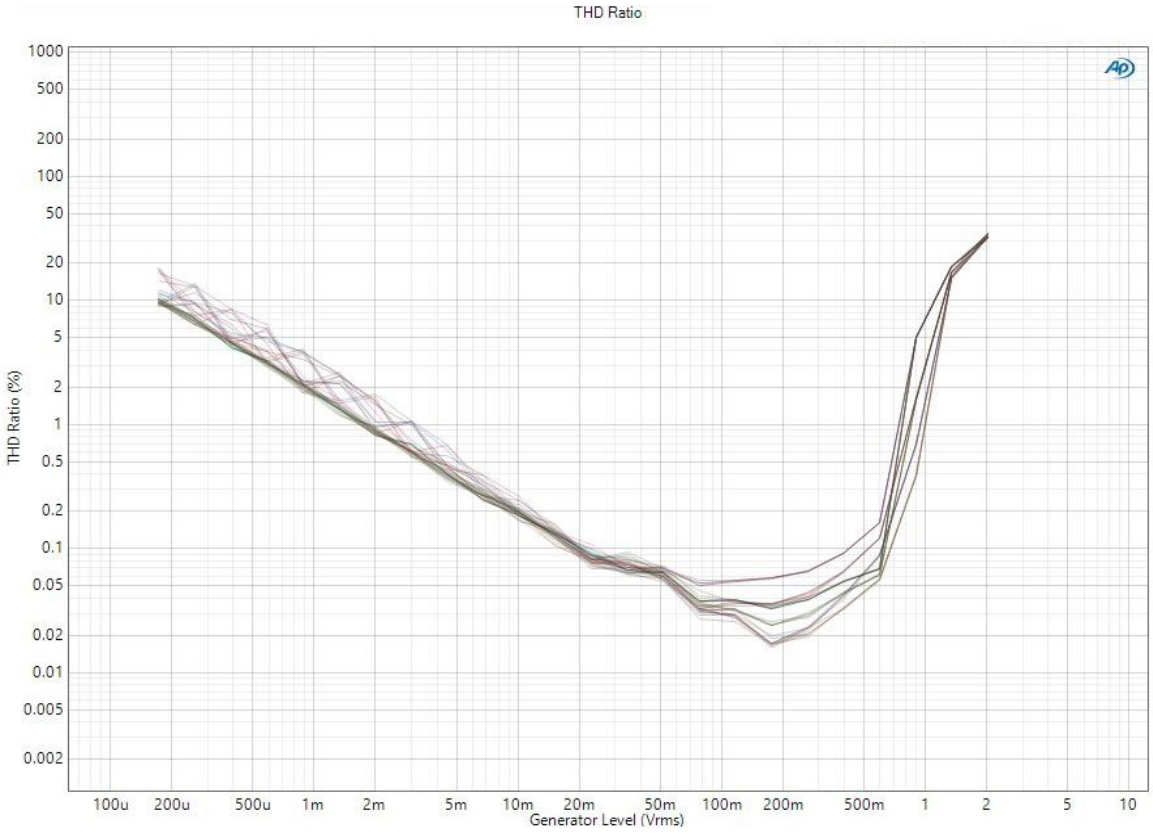


Figure 3-11 THD Ratio (dB) Vs. Input Level at Various Loads (Capless Mode)

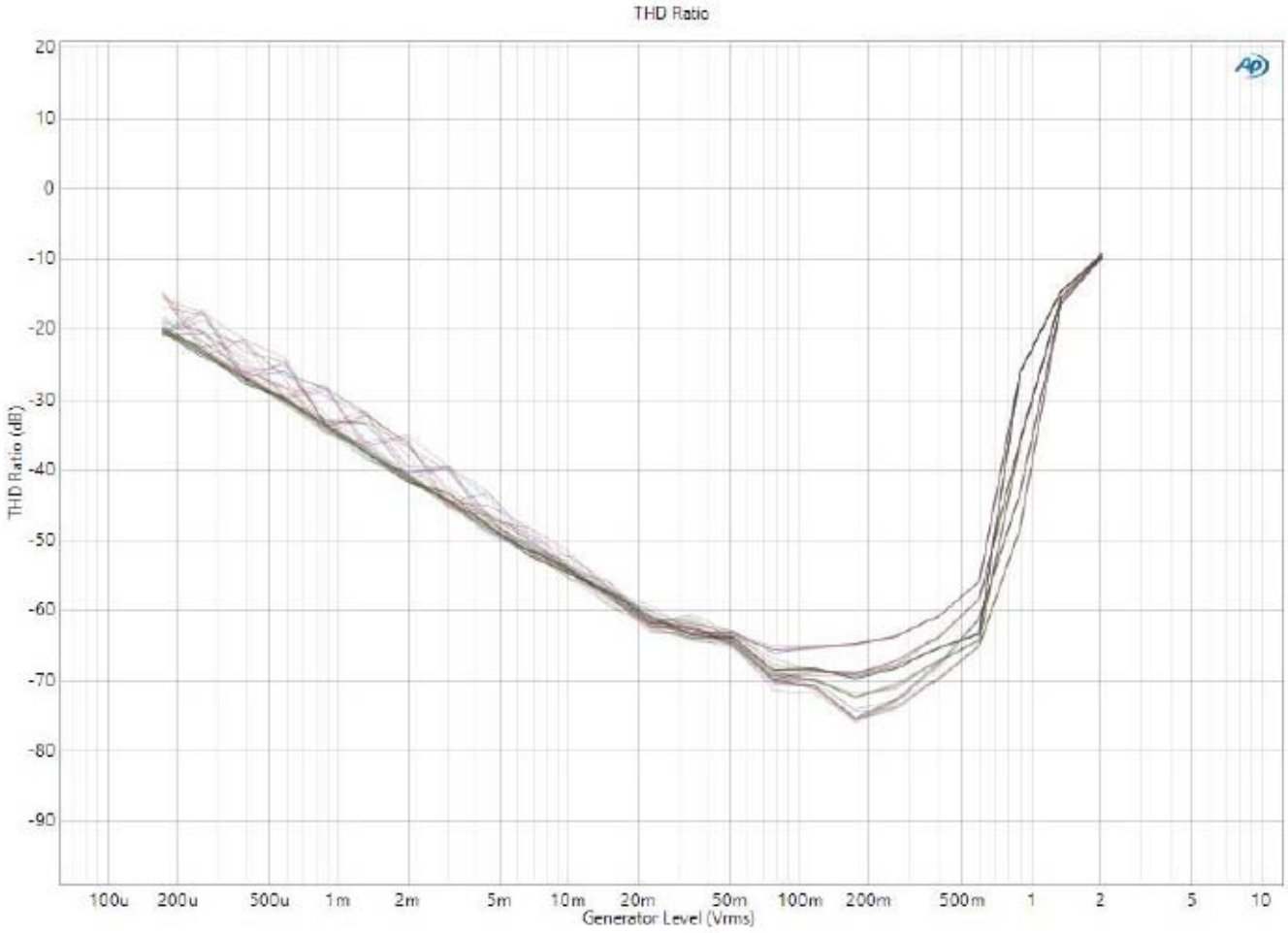


Figure 3-12 THD+N Ratio (%) Vs. Input Level at Various Loads (Capless Mode)

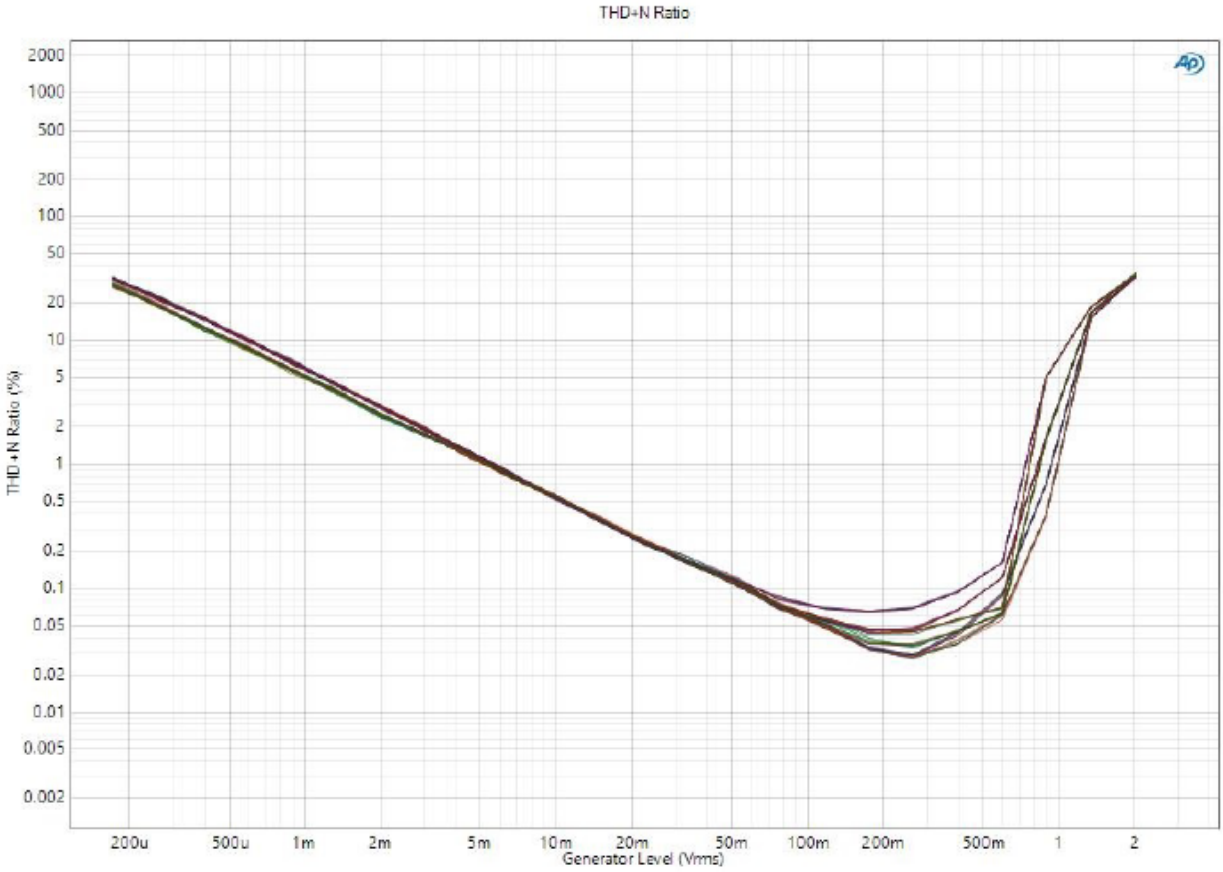


Figure 3-13 THD+N Ratio (%) Vs. Input Level at Various Loads (Capless Mode)

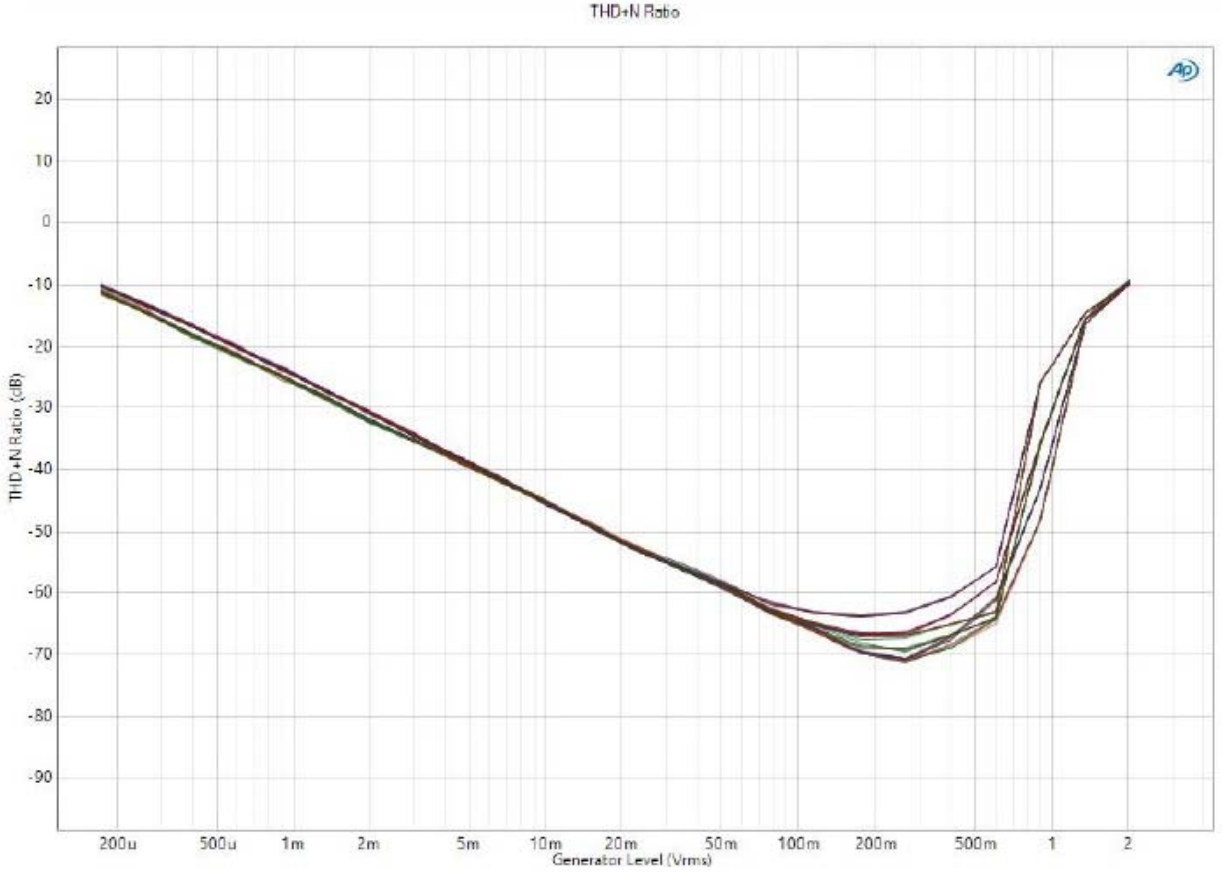


Figure 3-14 THD+N Ratio (%) Vs. Input Level at Various Loads (Single-ended Mode)

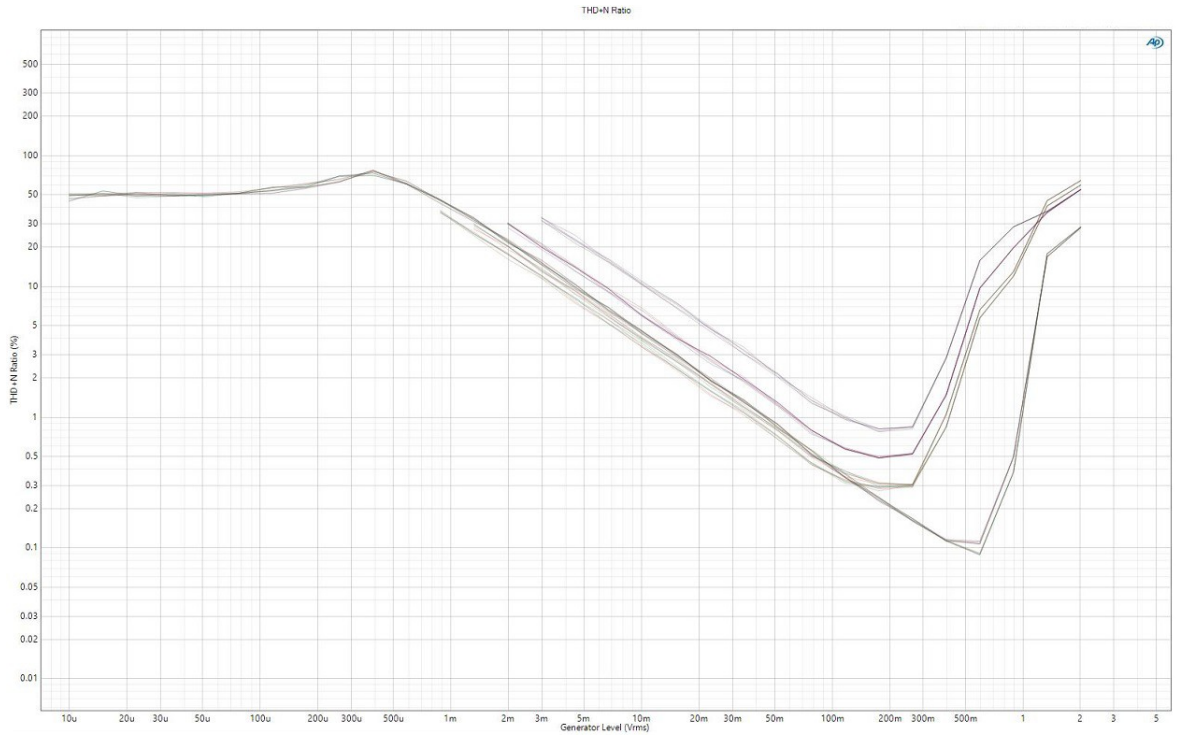


Figure 3-15 THD+N Ratio (dB) Vs. Input Level at Various Loads (Single-ended Mode)

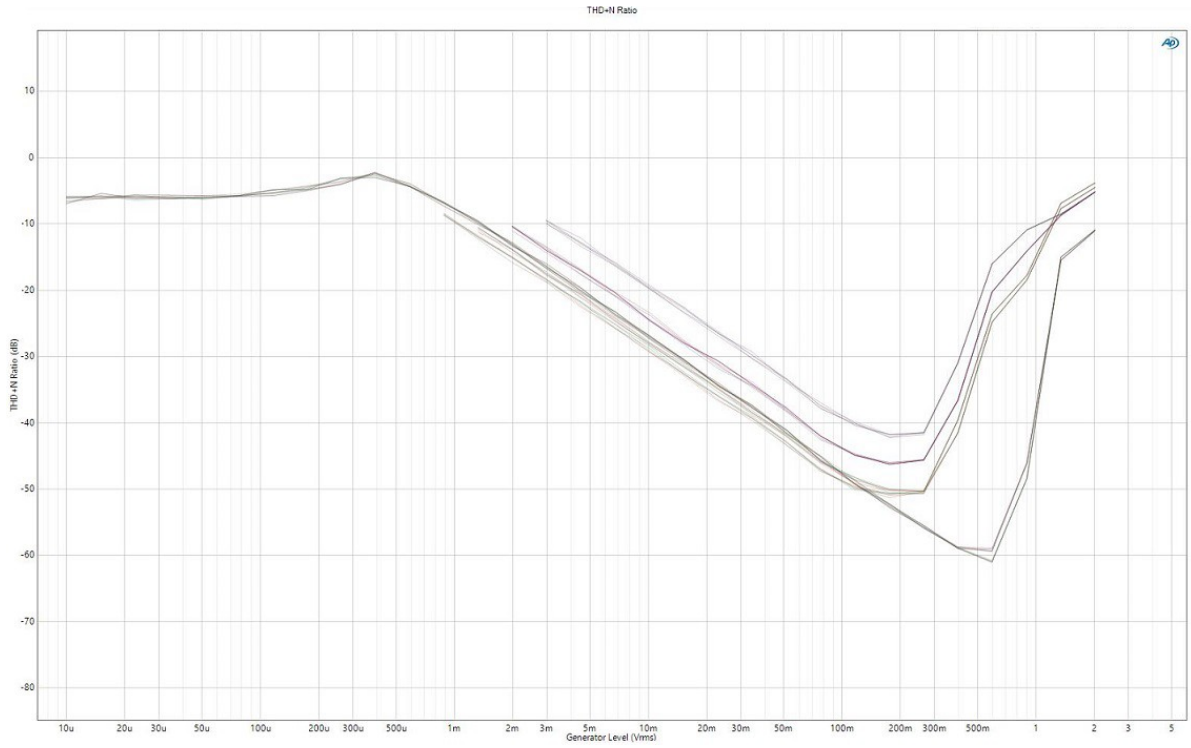


Figure 3-16 THD+N Ratio (%) Vs. Output Level at Various Loads (Capless Mode)

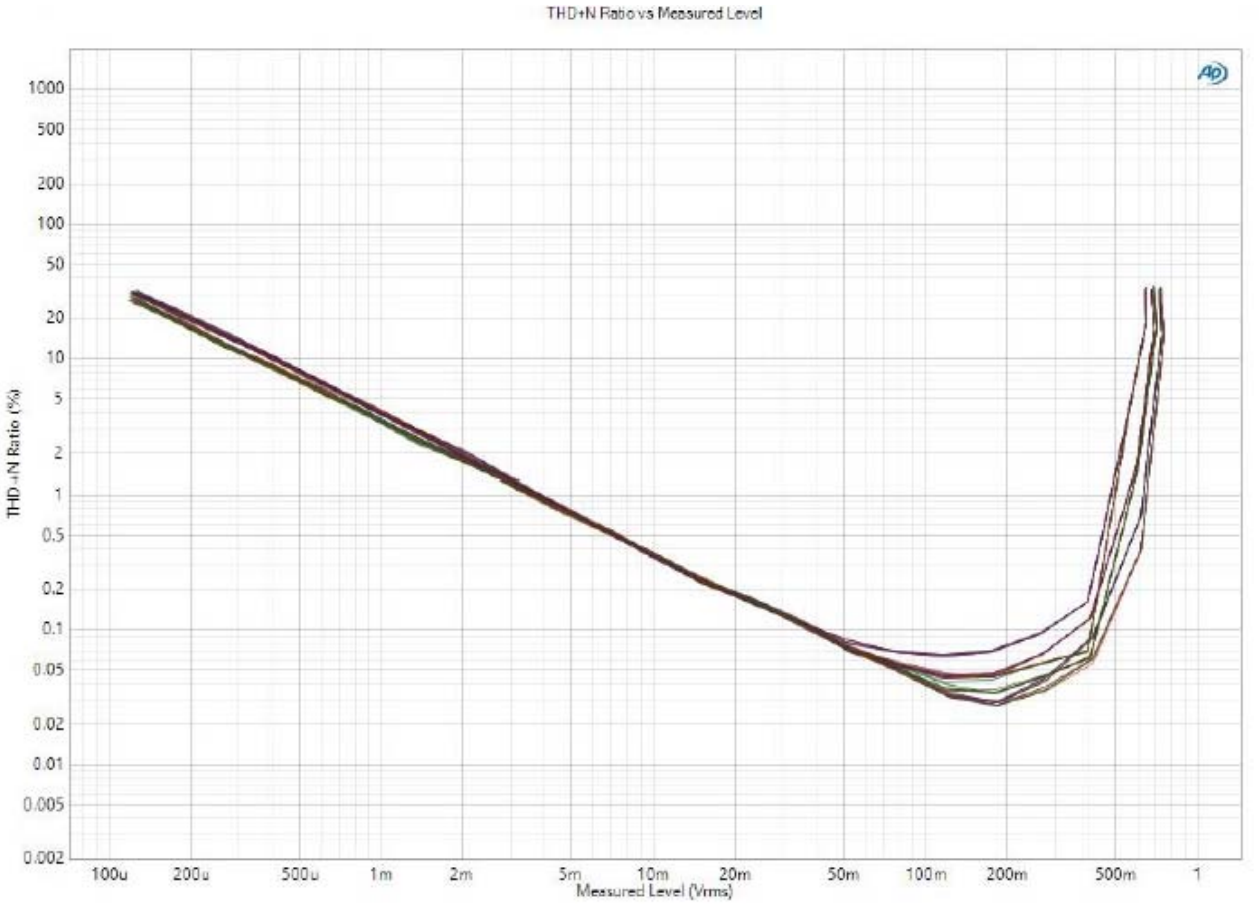


Figure 3-17. THD+N Ratio (dB) Vs. Output Level at Various Loads (Capless Mode)

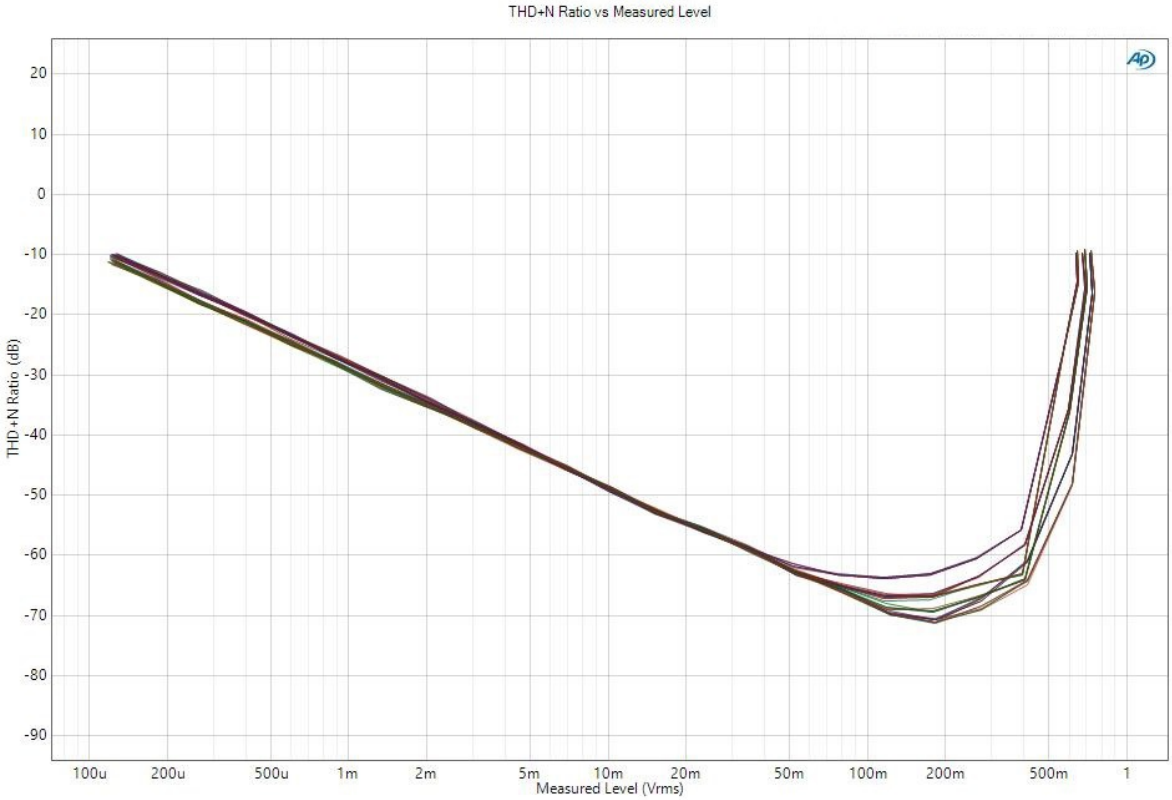


Figure 3-18. THD+N Ratio (%) Vs. Output Level at Various Loads (Single-ended mode)

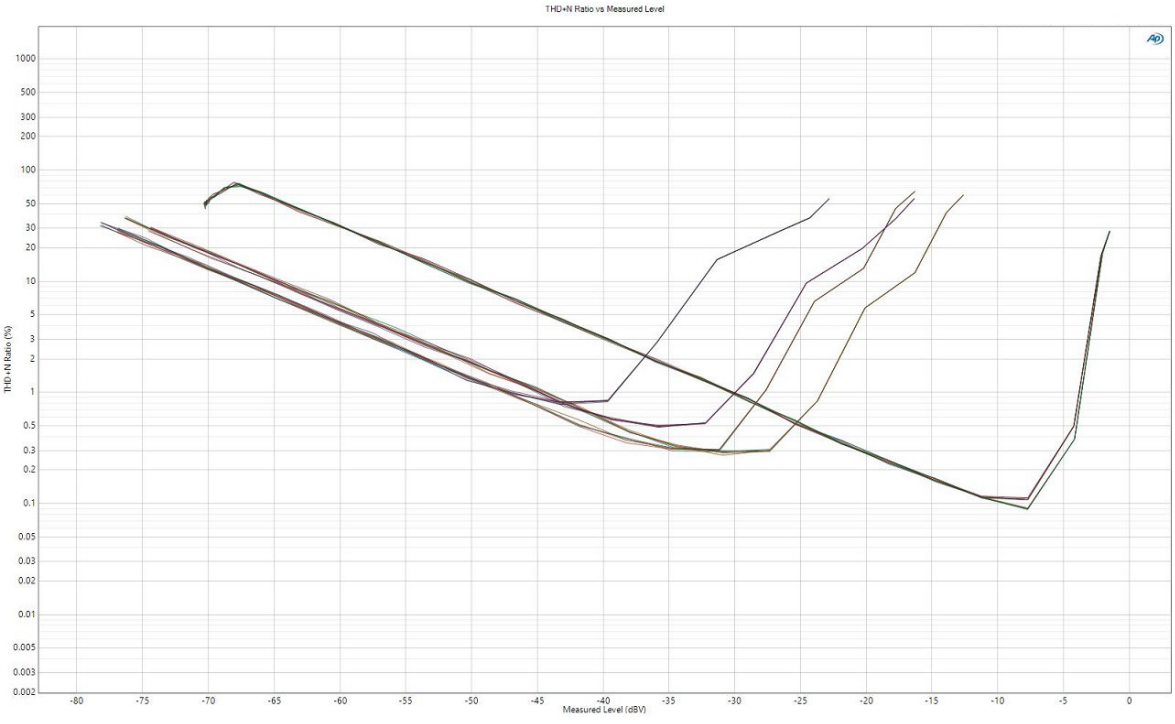
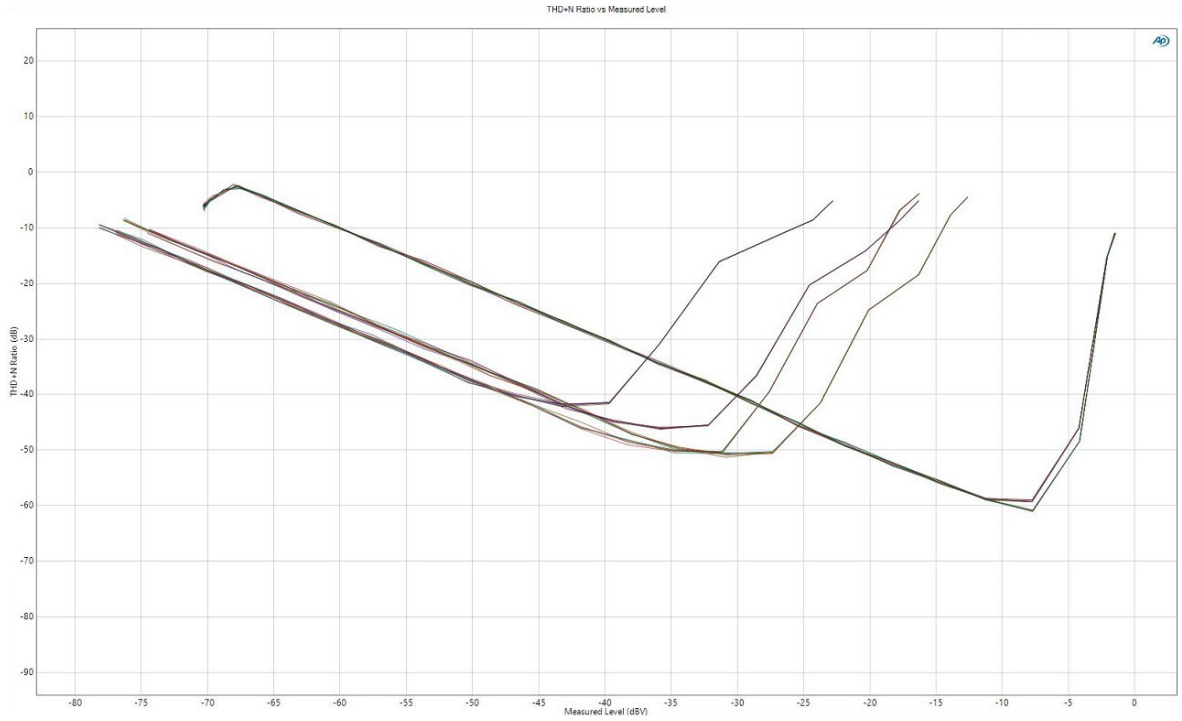


Figure 3-19. THD+N Ratio (dB) Vs. Output Level at Various Loads (Single-ended mode)



3.2.2 ADC Performance

The audio graphs in this section were produced in the following conditions:

- At room temperature
- Input signal = 1 kHz sine tone, level sweep across -100 dBv to 6 dBv, frequency sweep across 20 Hz to 20 kHz at 1 Fs input level
- Analog gain = -3 dB; digital gain = 0 dB
- A-weighting applied, 22K bandwidth

The following figures illustrate the ADC performance

Figure 3-20. Gain Vs. Input Level

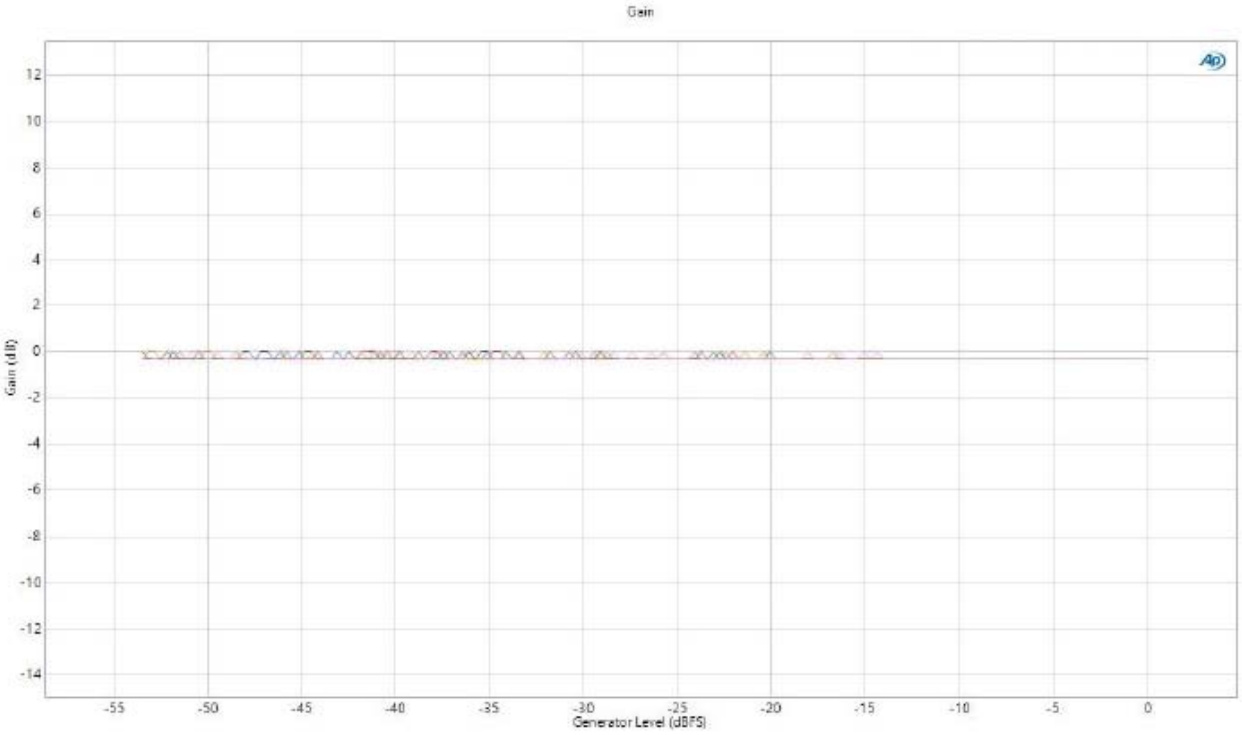


Figure 3-21. Gain Vs. Frequency

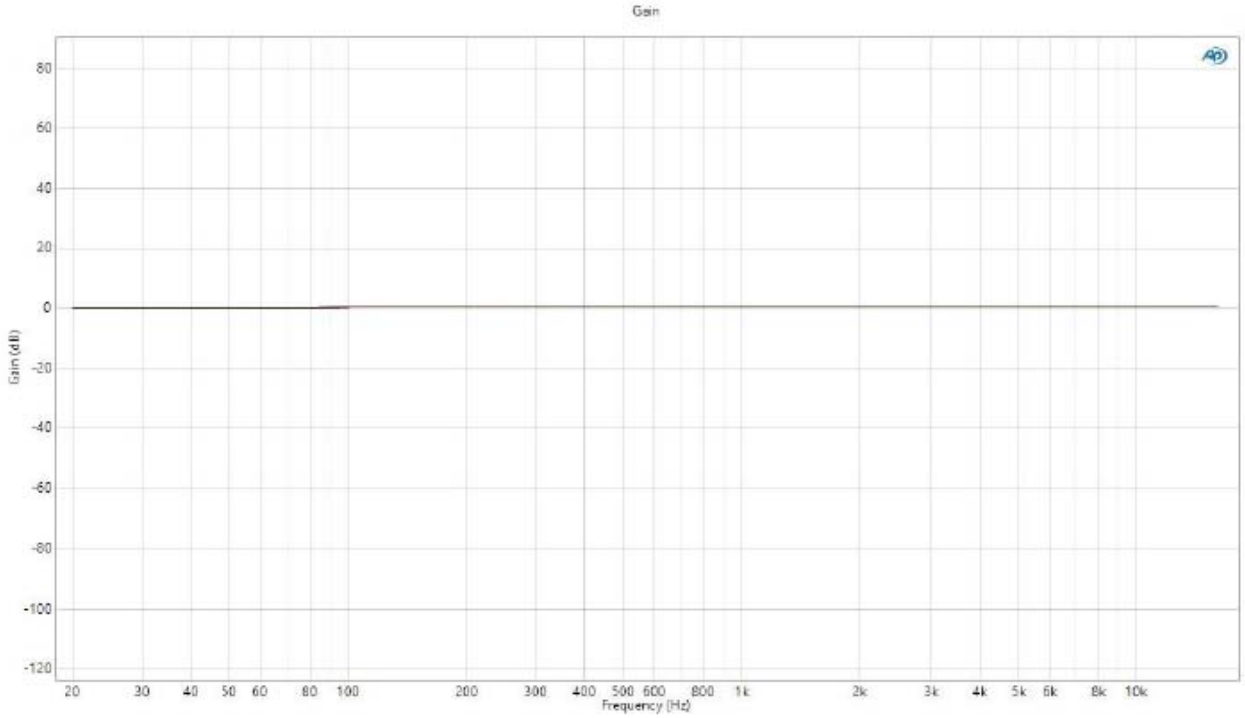


Figure 3-22. Output Level Vs. Input Level

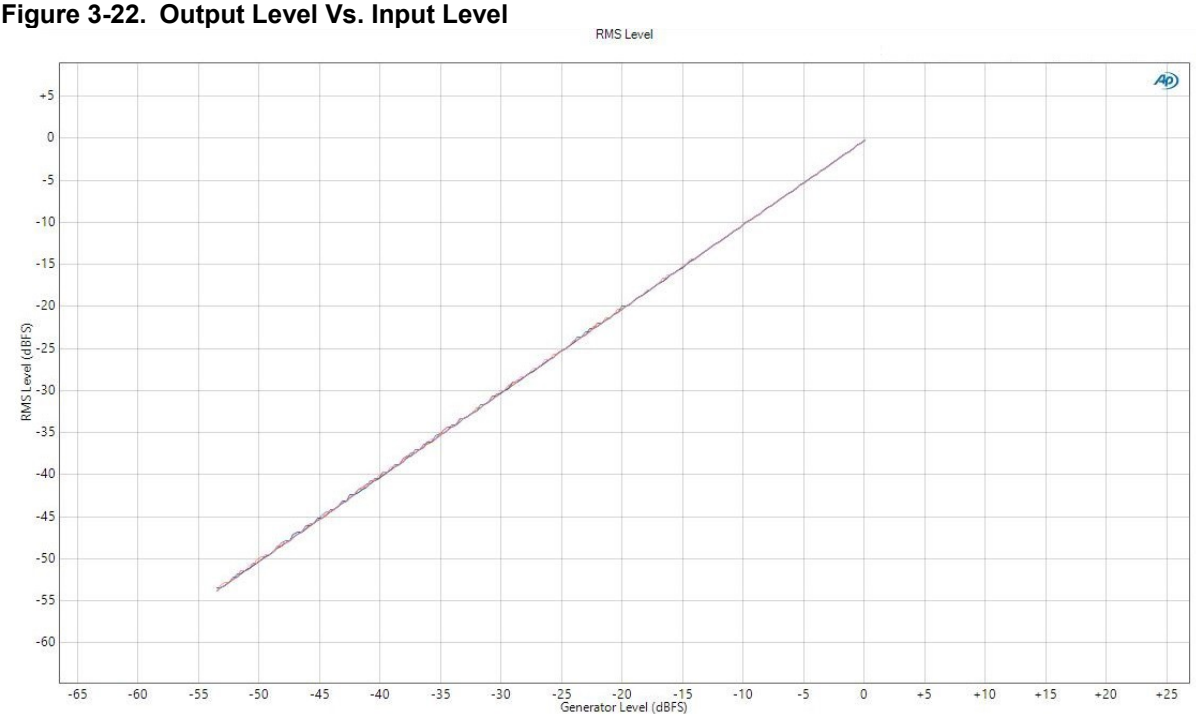


Figure 3-23. Level Vs. Frequency

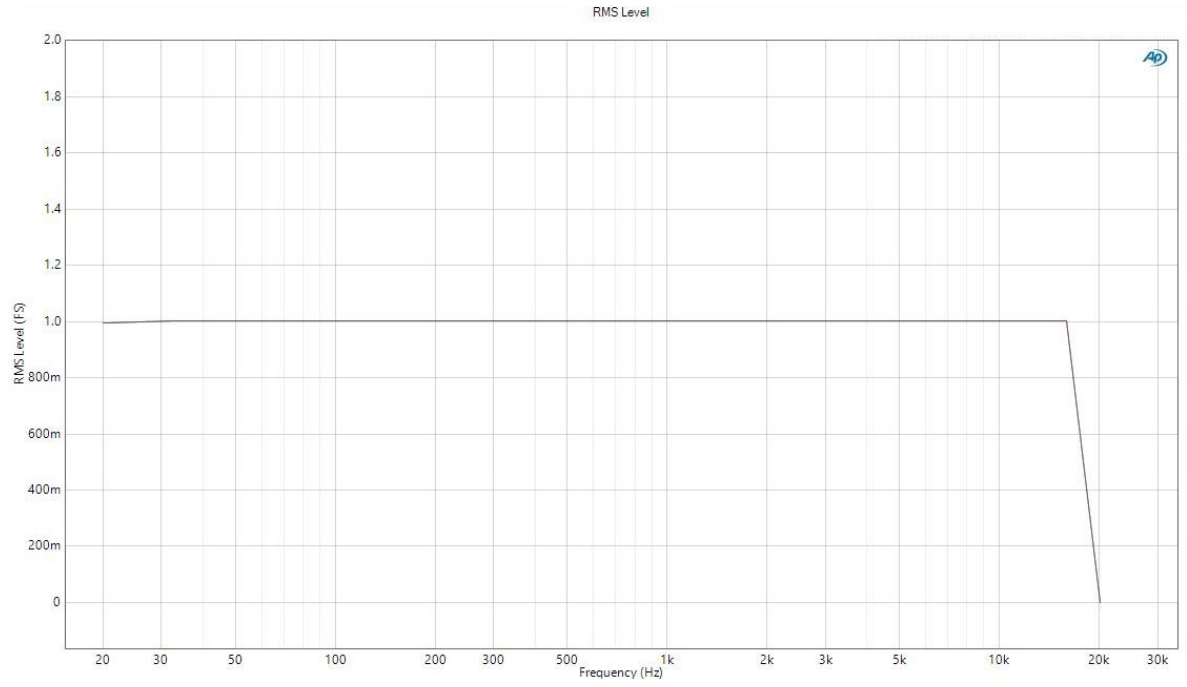


Figure 3-24. THD+N Ratio (%) Vs. Input Level

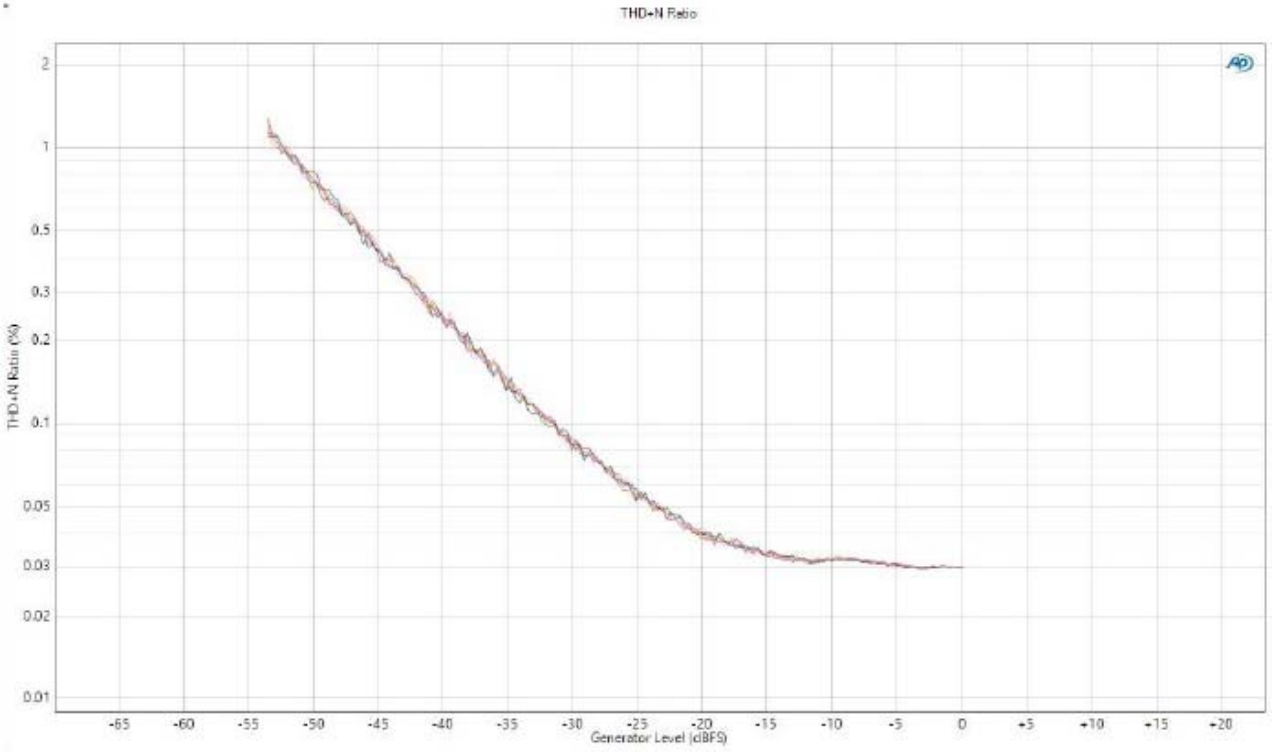


Figure 3-25. THD+N Ratio (dB) Vs. Input Level

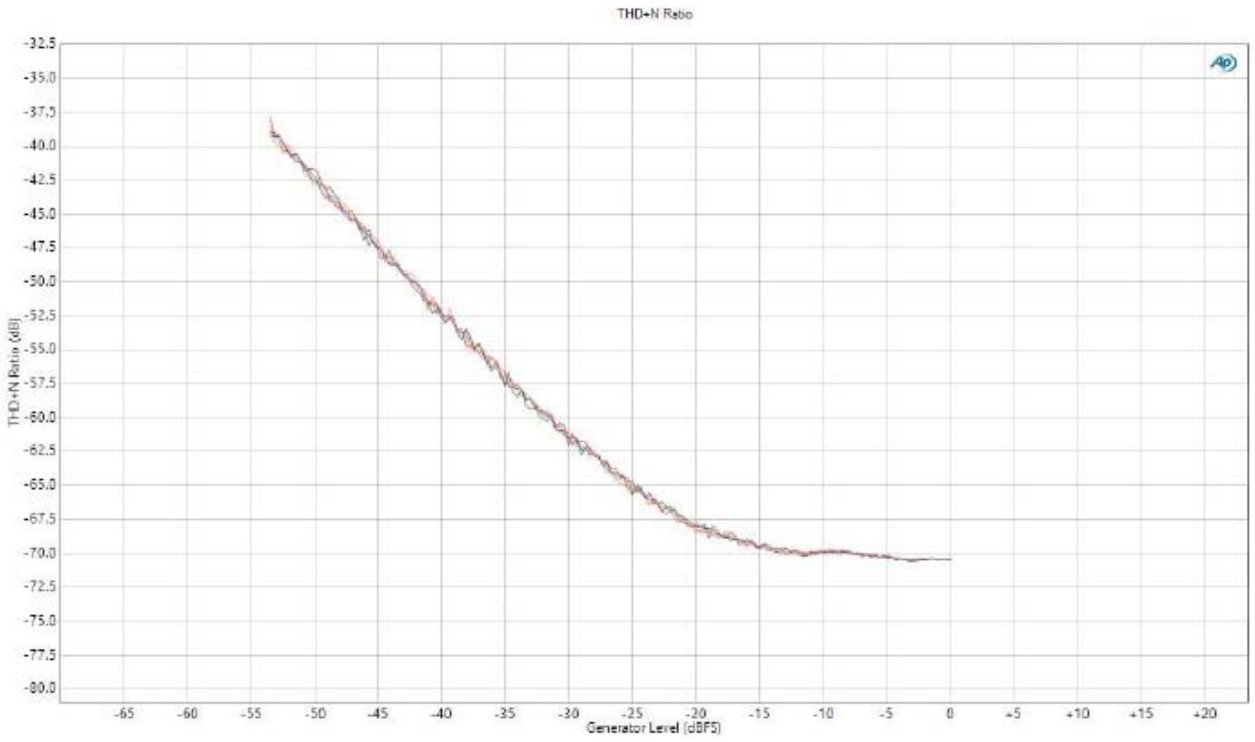


Figure 3-26. THD+N Ratio (%) Vs. Output Level

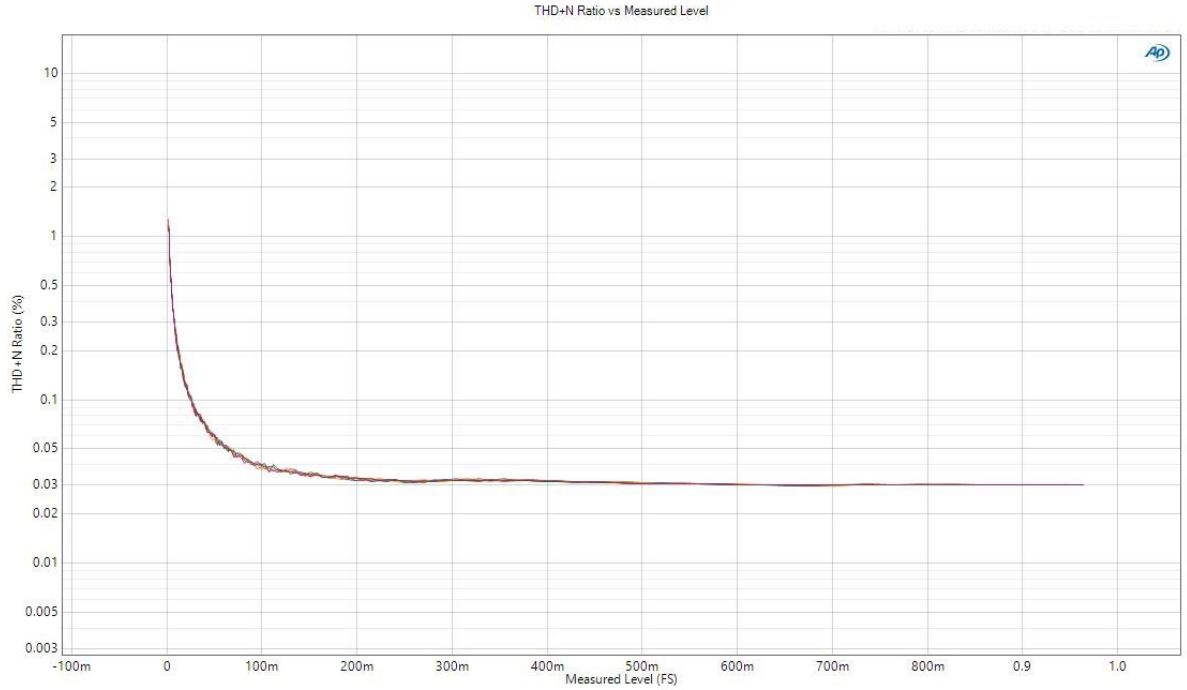


Figure 3-27. THD+N Ratio (dB) Vs. Output Level

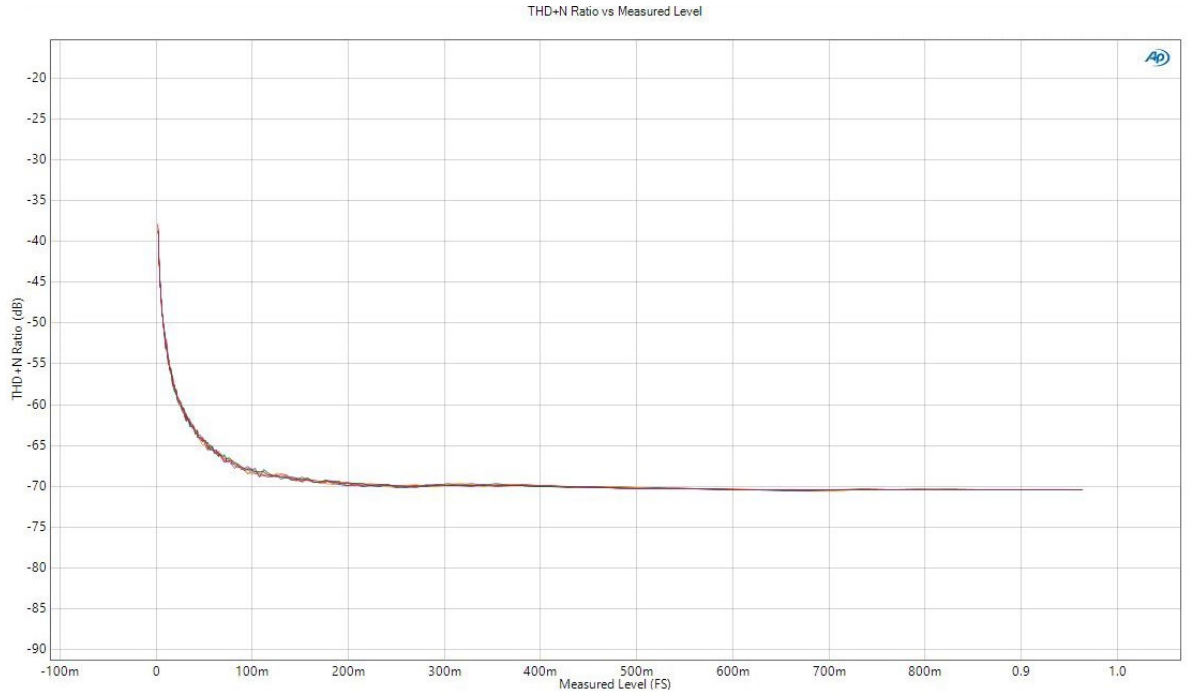


Figure 3-28. THD+N Ratio (%) Vs. Frequency

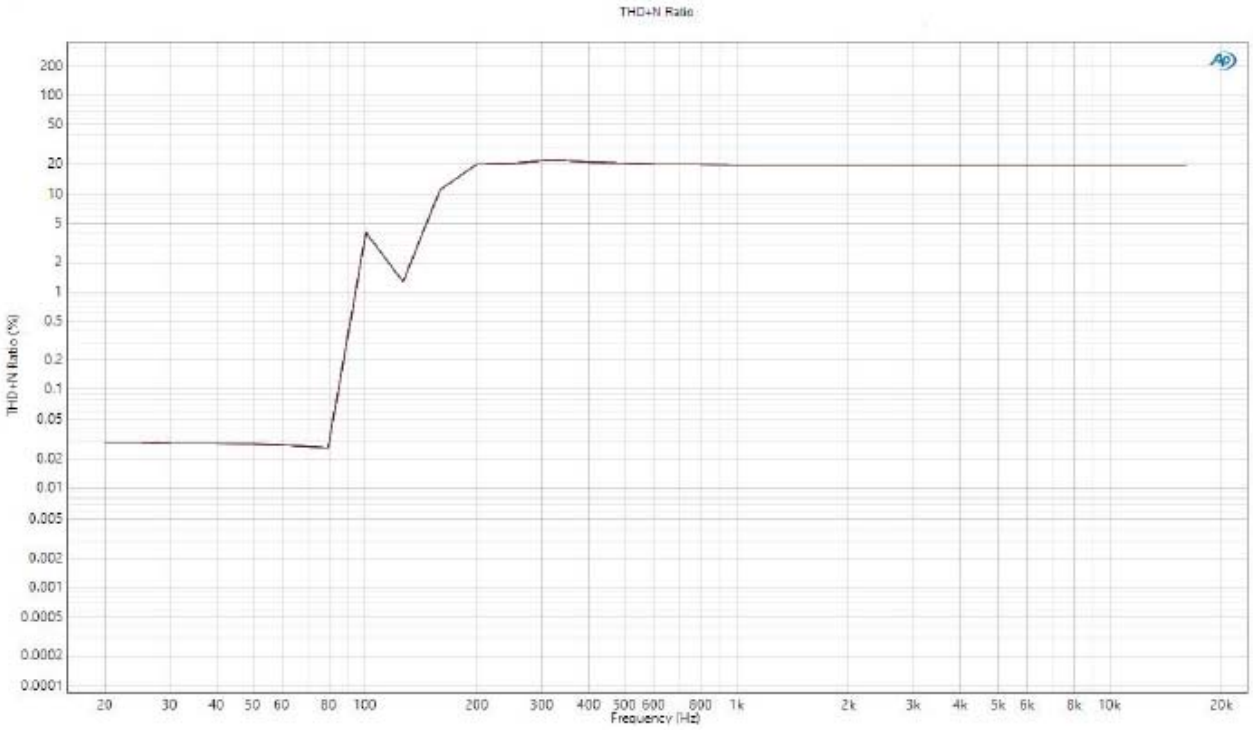
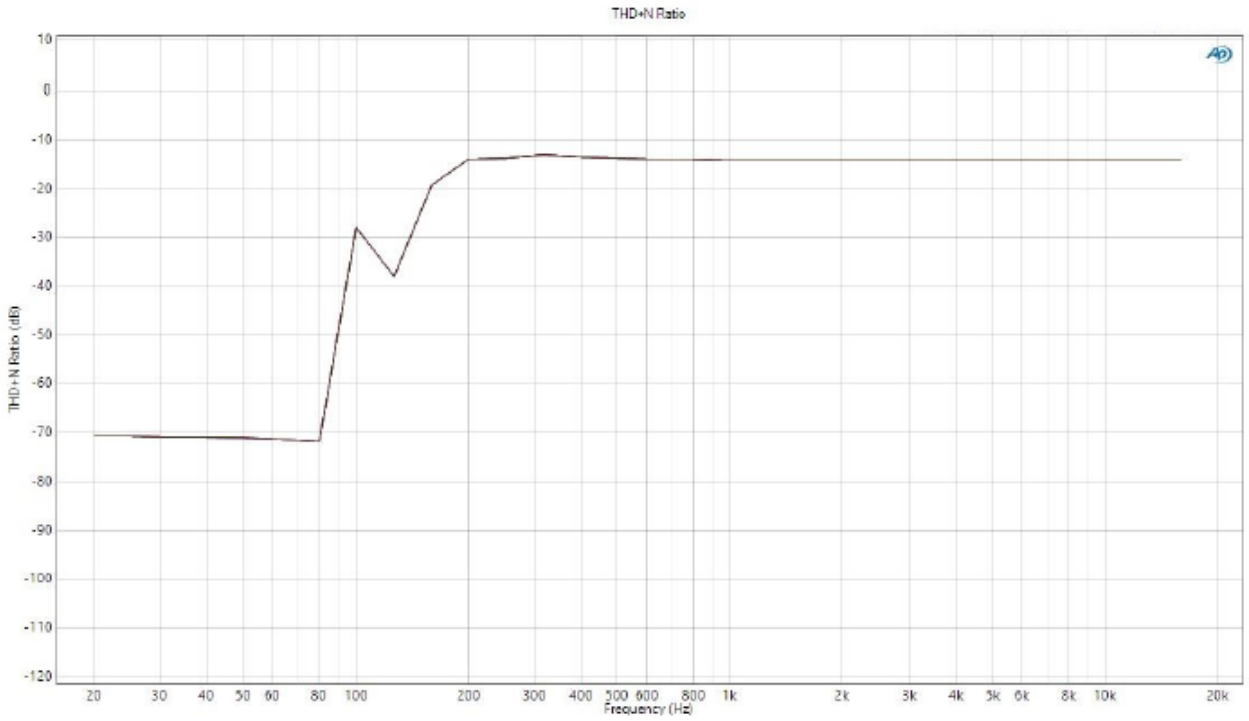


Figure 3-29. THD+N Ratio (%) Vs. Frequency



3.3 Auxiliary Port

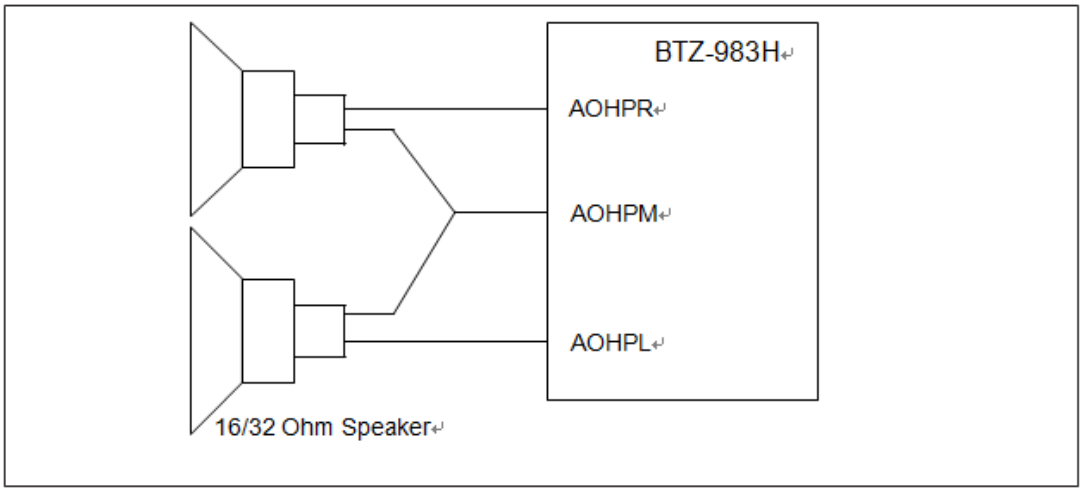
The BTZ-983H module supports one analog (Line-In, also called as Aux-In) signal from the external audio source. The analog (Line-In) signal can be processed by the DSP to generate different sound effects (MB-DRC and AW), which can be configured by using the Config Tool.

3.4 Analog Speaker Output

The BTZ-983H module supports the following analog speaker output modes:

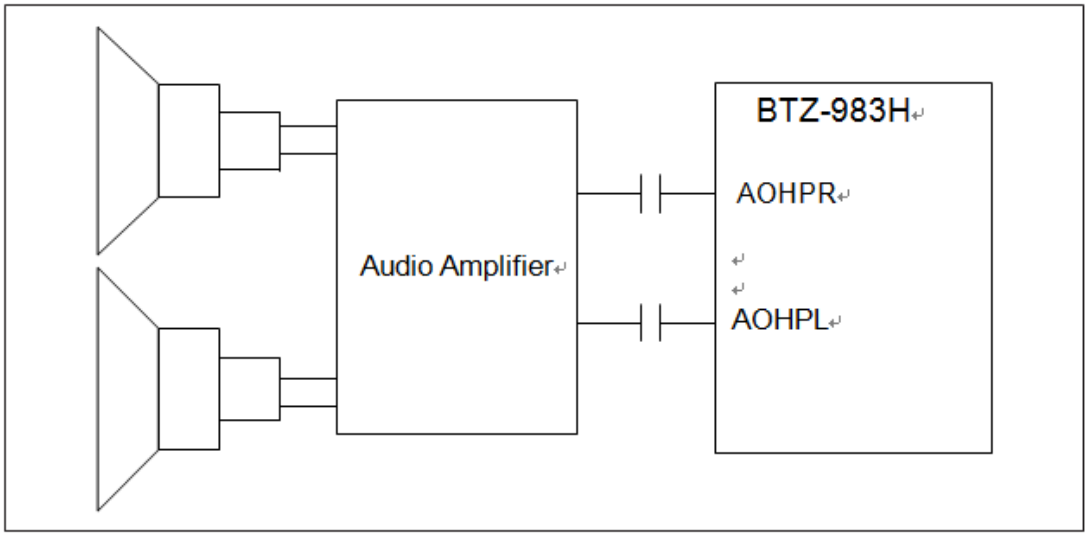
- Capless mode – recommended for headphone applications in which capless output connection helps to save the Bill of Materials (BOM) cost by avoiding a large DC blocking capacitor. The following figure illustrates the analog speaker output in Capless mode.

Figure 3-30. Analog Speaker Output - Capless Mode



- Single-Ended mode – used for driving an external audio amplifier where a DC blocking capacitor is required. The following figure illustrates the analog speaker output in Single-Ended mode.

Figure 3-31. Analog Speaker Output - Single-Ended Mode



3.5 Microphone Inputs

The BTZ-983H module supports up to two analog microphone channels and one stereo digital microphone. The digital microphone interface should only be used for Pulse Density Modulation (PDM) digital microphones (typically· MEMS microphones) up to about 4 MHz of clock frequency

Note: An 1^2S based digital microphone should use the external 1^2S port

4. Bluetooth Transceiver

The BTZ-983H module is designed and optimized for the Bluetooth 2.4 GHz system. It contains a complete RF Transmitter (TX)/Receiver (RX) section. An internal synthesizer generates a stable clock for synchronizing with another device.

4.1 Transmitter

The IS2083BM device has an internal Medium Power Amplifier (MPA) and a Low Power Amplifier (LPA). The MPA supports up to +10 dBm output power for Bluetooth Class1 applications, and the LPA supports +1 dBm output power for the Class 2 applications. The transmitter performs the I/Q conversion to minimize the frequency drift.

4.2 Receiver

- The Low-Noise Amplifier (LNA) operates with TR-Combined mode with LPA for single port application. It removes the need for an external TX/RX switch.
- The ADC is used to sample the input analog signal and convert it into a digital signal for demodulator analysis. A channel filter has been integrated into the receiver channel before the ADC, which is used to reduce the external component count and increase the anti-interference capability.
- The image rejection filter is used to reject the image frequency for low-Intermediate Frequency (IF) architecture and to reduce external Band Pass Filter (BPF) component for a super heterodyne architecture.
- Received Signal Strength Indicator (RSSI) signal feedback to the processor is used to control the RF output power to make a good trade-off for effective distance and current consumption.

4.3 Synthesizer

A synthesizer generates a clock for radio transceiver operation. There is a Voltage-Controlled Oscillator (VCO) inside with a tunable internal LC tank that can reduce variation for components. A crystal oscillator with an internal digital trimming circuit provides a stable clock for the synthesizer.

4.4 Modulator-Demodulator

- For Bluetooth 1.2 specification and below, 1 Mbps is the standard data rate based on the Gaussian Frequency Shift Keying (GFSK) modulation scheme. This BR modem meets BDR requirements of Bluetooth 2.0 with EDR specifications.
- For Bluetooth 2.0 and above specifications, EDR is introduced to provide the data rates of 1/2/3 Mbps.
- For baseband, both BDR and EDR utilize the same 1 MHz symbol rate and 1.6 kHz slot rate.
- For BDR, symbol 1 represents 1-bit. However, each symbol in the payload part of EDR packet represents 2/3 bits. This is achieved by using two different modulations – π/4 Differential Quadrature Phase Shift Keying (DQPSK) and 8-Differential Phase Shift Keying (DPSK).

4.5 Adaptive Frequency Hopping

The BTZ-983H module has an AFH function to avoid RF interference. It has an algorithm to check the nearby interference and to choose clear channel for transceiver Bluetooth signal.

5. Power Management Unit

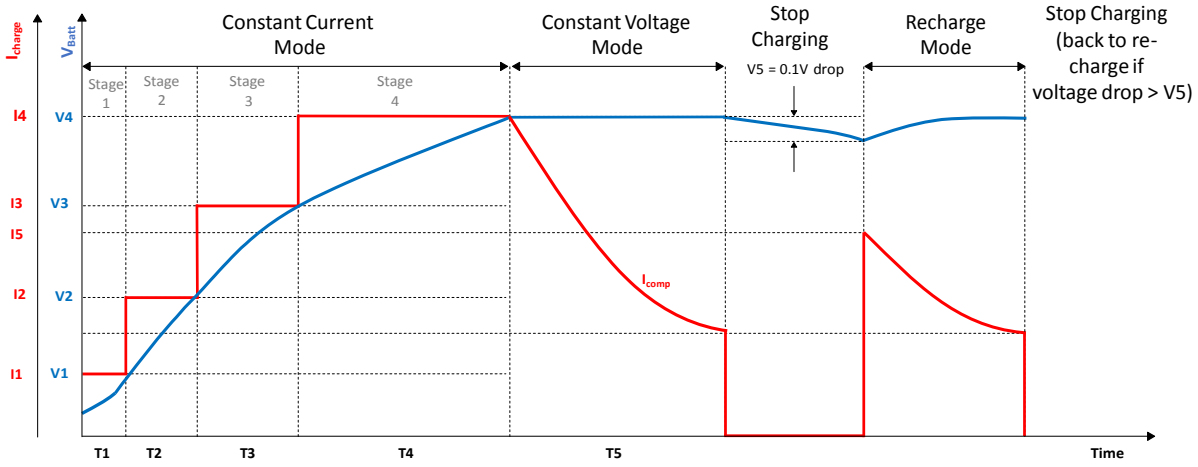
The on-chip PMU integrates the battery (lithium-ion and lithium-polymer) charger, and voltage regulator. A power switch is used to switch over the power source between the battery (BAT_IN) and an adapter (ADAP_IN). The PMU provides current to drive two LEDs.

The battery charger supports various modes with features listed below:

- Charging control using current sensor
- User-programmable current regulation
- High accuracy voltage regulation
- Constant current and constant voltage modes
- Stop charging and re-charging modes

The following figure illustrates the charging curve of a battery.

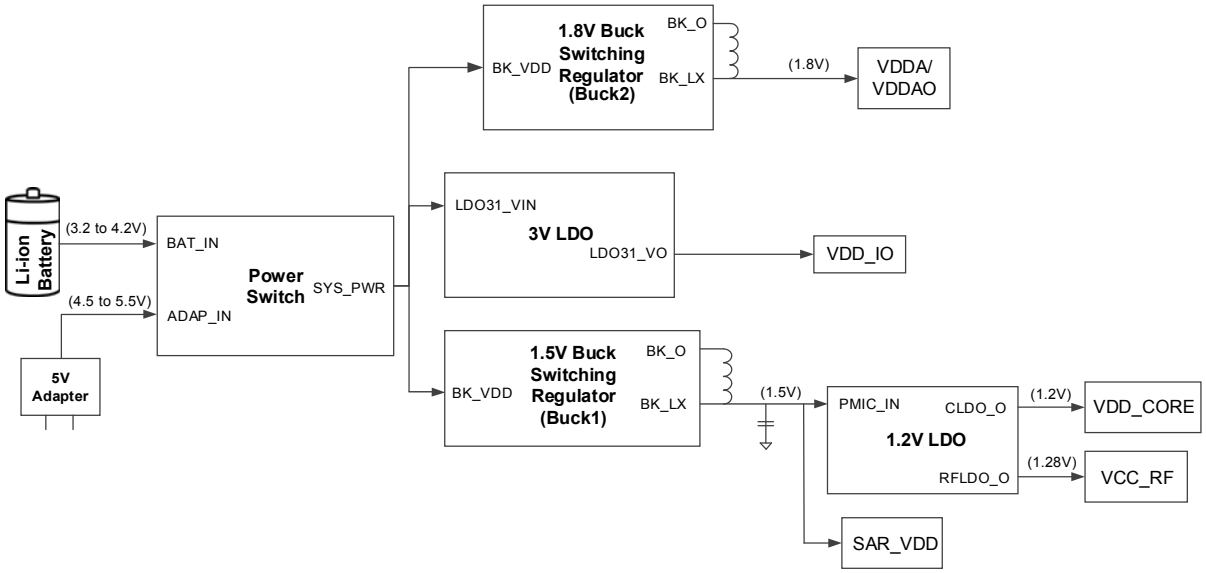
Figure 5-1. Battery Charging Curve



5.1 Power Supply

The BTZ-983H module is powered through the BAT_IN input pin. The following figure illustrates the connection from the BAT_IN pin to various other voltage supply pins of the IS2083BM SoC on the BTZ-983H module. The external 5V power adapter can be connected to ADAP_IN in order to charge the battery in battery powered applications or in USB applications. Otherwise the ADAP_IN pin can be left floating if there is no battery utilized at BAT_IN pin.

Figure 5-2. Power Tree Diagram

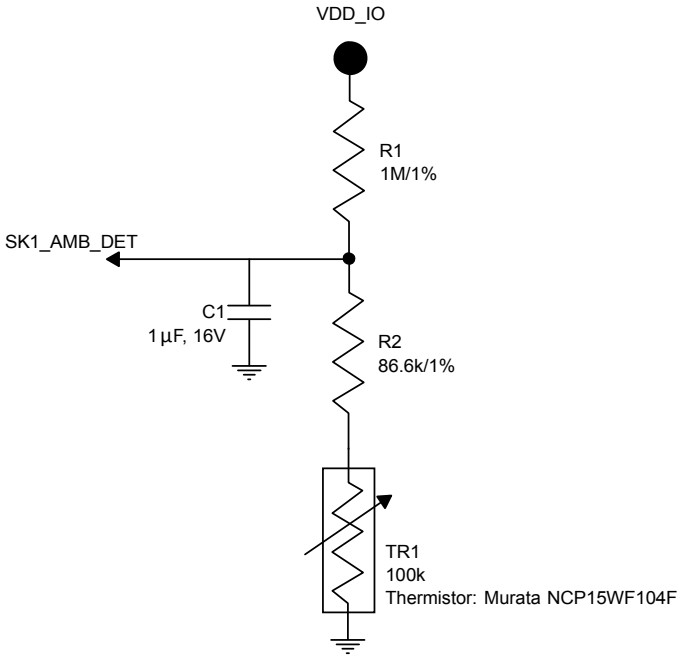


5.2 SAR ADC

The BTZ-983H module has a 10-bit Successive Approximation Register (SAR) ADC with ENOB (Effective Number of Bits) of 8-bits; used for battery voltage detection, adapter voltage detection, charger thermal protection, and ambient temperature detection. The input power of the SAR ADC is supplied by the 1.8V output of Buck2. The warning level can be programmed by using the Config Tool or the SDK.

The SK1 and SK2 are the ADC channel pins. The SK1 is used for charger thermal protection. The following figure illustrates the suggested circuit and thermistor, Murata NCP15WF104F. The charger thermal protection can avoid battery charge in a restricted temperature range. The upper and lower limits for temperature values can be configured by using the Config Tool.

Figure 5-3. Ambient Detection Circuit



Note: The thermistor must be placed close to the battery in the user application for accurate temperature measurements and to enable the thermal shutdown feature.

The following figures show SK1 and SK2 channel behavior.

Figure 5-4. SK1 Channel

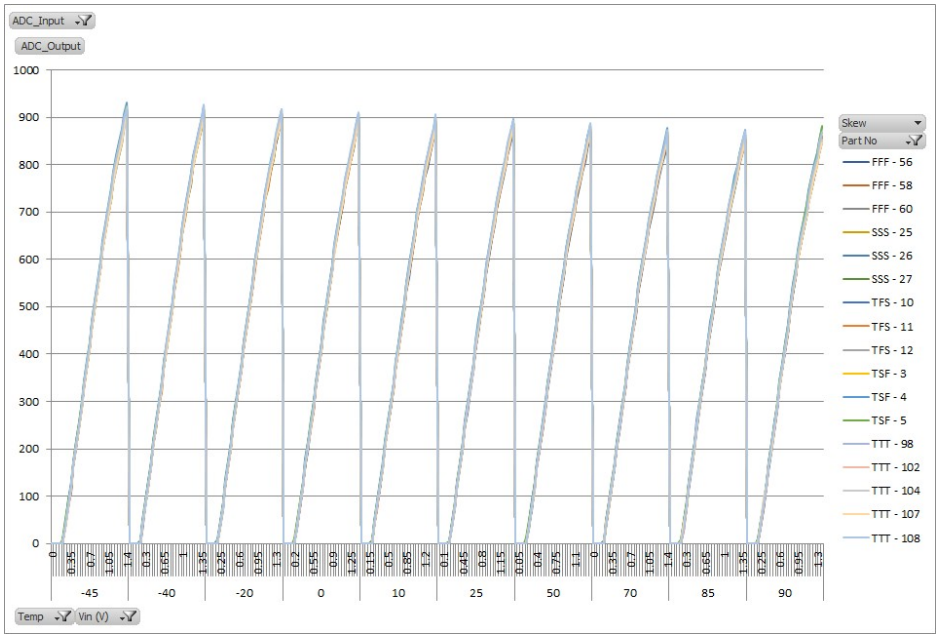
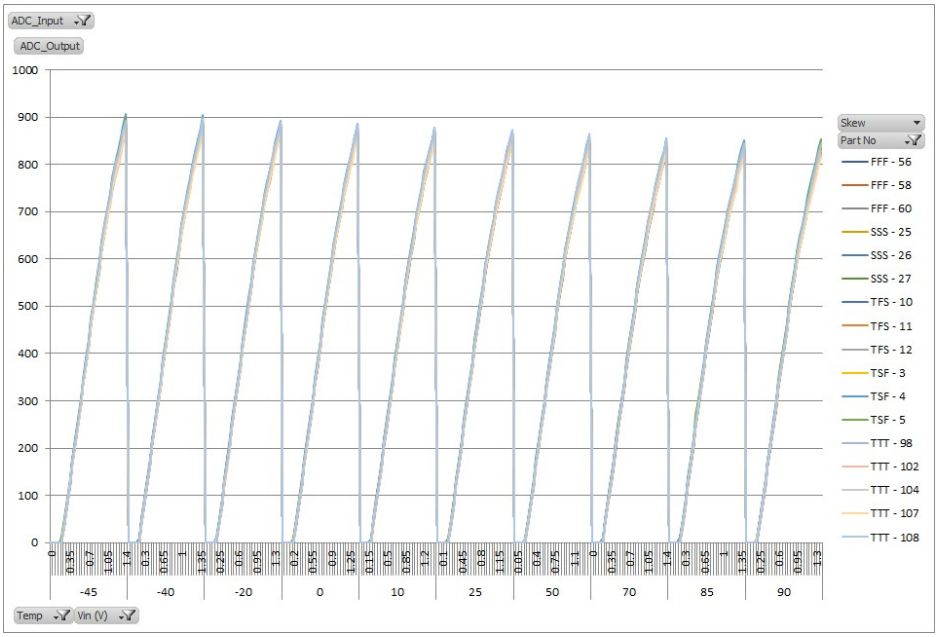


Figure 5-5. SK2 Channel

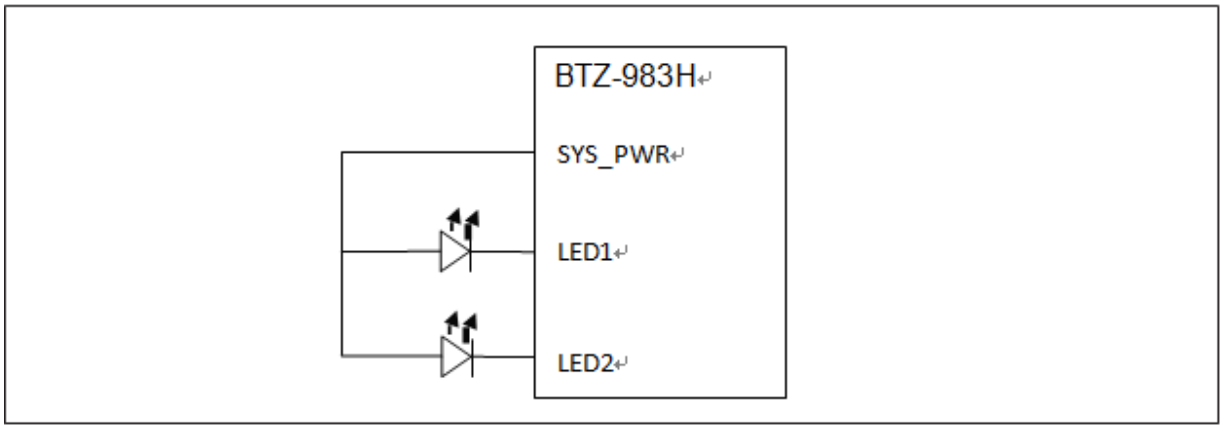


5.3 LED Drivers

The BTZ-983H module has two LED drivers to control external LEDs. The LED drivers provide enough sink current (16- step control and 0.35 mA for each step) and the LED can be connected directly to the BTZ-983H module. The LED settings can be configured by using the Config Tool.

The following figure illustrates the LED drivers in the BTZ-983H module.

Figure 5-6. LED Drivers

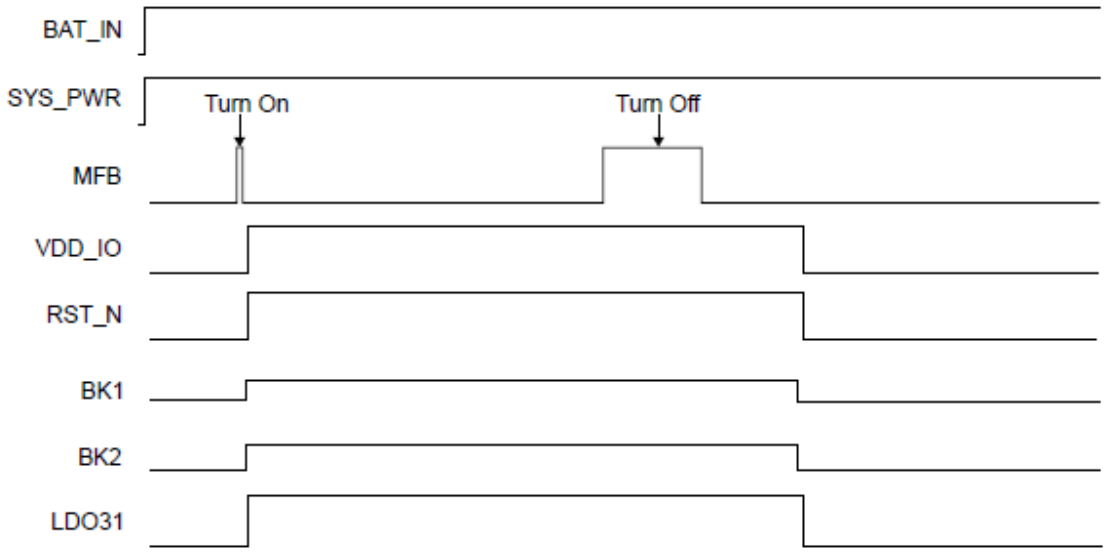


6. Application Information

6.1 Power On/Off Sequence

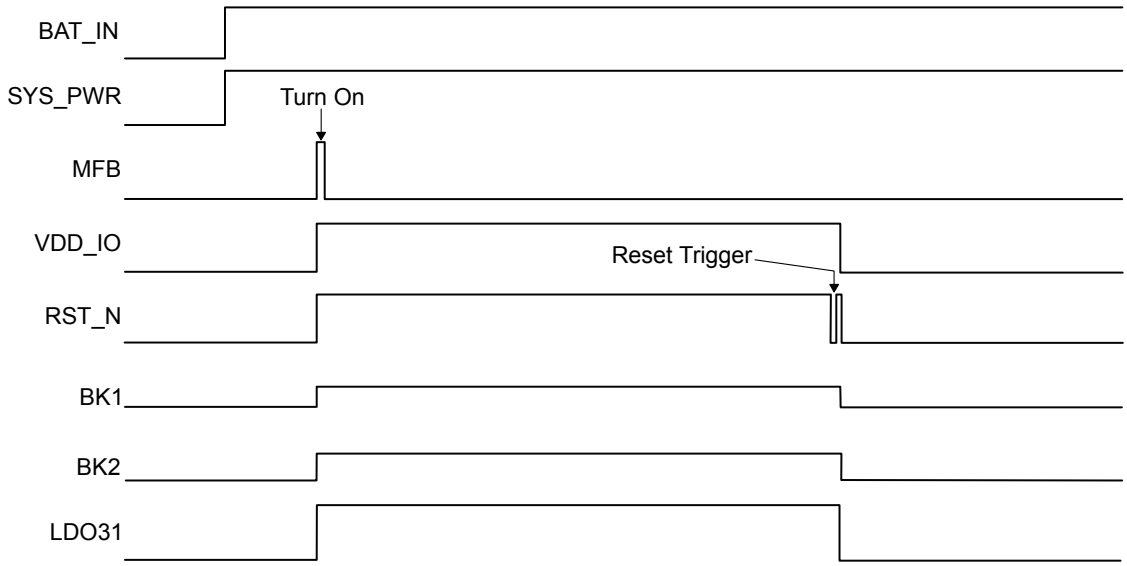
In Embedded mode, the MFB button is used to turn on and turn off the system. For Host mode, refer to 6.6 Host MCU Interface Over UART. The following figure illustrates the system behavior (Embedded mode) upon a MFB press event to turn on and turn off the system.

Figure 6-1. Timing Sequence of Power On/Off in Embedded Mode



The following figure illustrates the system behavior (Embedded mode) upon a MFB press event to turn on the system and then trigger a Reset event.

Figure 6-2. Timing Sequence of Power On and Reset Trigger in Embedded Mode

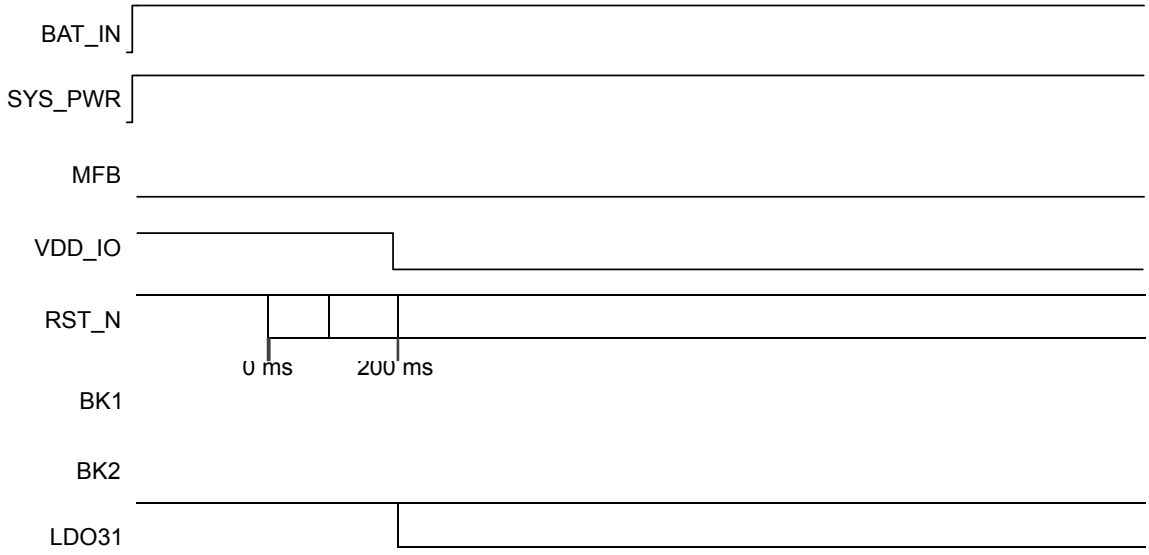


6.2 Reset

The Reset logic generates proper sequence to the device during Reset events. The Reset sources include external Reset, power-up Reset, and Watchdog Timer (WDT). The IS2083 SoC provides a WDT to Reset the chip. In addition, it has an integrated Power-on Reset (POR) circuit that resets all circuits to a known Power On state. This action can also be driven by an external Reset signal, which is used to control the device externally by forcing it into a POR state. The following figure illustrates the system behavior upon a RST_N event.

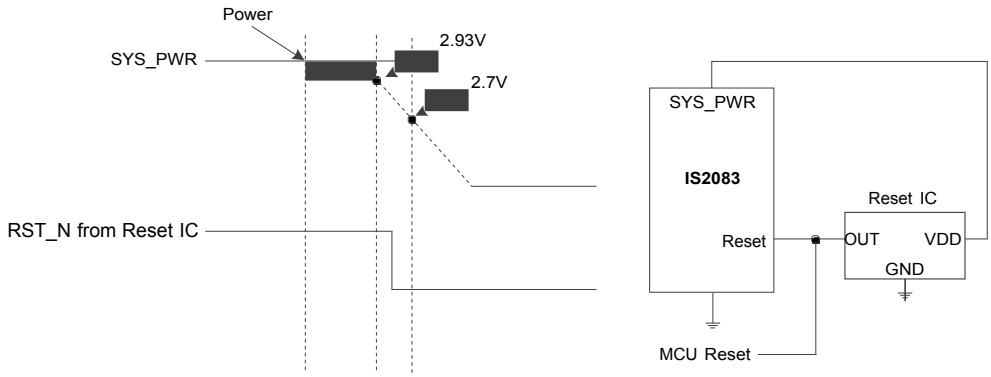
Note: The Reset (RST_N) is an active-low signal and can be utilized based on the application needs, otherwise, it can be left floating.

Figure 6-3. Timing Sequence of Reset Trigger



Note: RST_N pin has an internal pull-up, thus, RST_N signal will transition to high again upon releasing the RST_N button. This is an expected behavior of RST_N signal.

Figure 6-4. Timing Sequence of Power Drop Protection



Timing sequence of power drop protection:

- It is recommended to use the battery to provide the power supply at BAT_IN.
- If an external power source or a power adapter is utilized to provide power to BAT_IN, it is recommended to use a voltage supervisor Integrated Circuit (IC).
- The Reset IC output pin, RST_N, must be open drain type and threshold voltage as 2.93V.
- The RST_N signal must be fully pulled low before SYS_PWR power drop to 2.7V.

6.3 Configuring and Programming

6.3.1 Test Mode

The BTZ-983H module can be configured by using the Config Tool and the firmware is programmed by using the isUpdate tool. The following table provides the settings for configuring the BTZ-983H module for Test mode or Application mode.

Table 6-1. BTZ-983H Module - Test Mode Configuration Settings

Pins	Status	Mode
P3_4	Low	Test mode
	Floating	Application mode

Note: The BTZ-983H module provides Test mode, which allows customers to use existing module manufacturing and testing equipment and flow to test the BTZ-983H modules without reinvesting in new test equipment. New customers are encouraged to use the new RF test modes defined for this device.

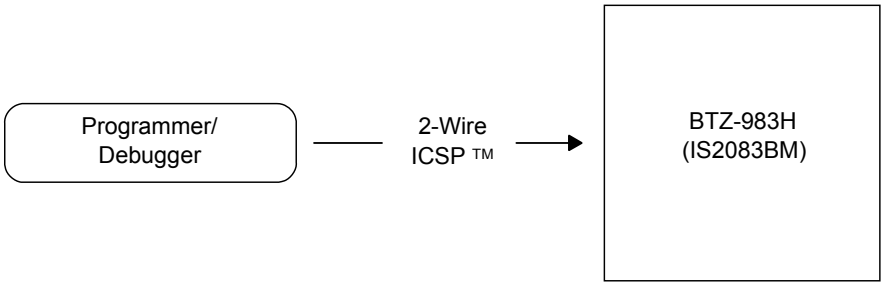
Test mode allows an external UART host to communicate with the BTZ-983H using Bluetooth vendor commands over the UART interface. The host can interface with the driver firmware on the BTZ-983H module to perform TX/RX operations and to collect/report Bit Error Rate (BER) and other RF performance parameters. These values can then be used to accept/reject the device and/or calibrate the module.

6.3.2 2-wire JTAG Program and Debug

The BTZ-983H (IS2083BM) provides physical interface for connecting and programming the memory contents, see the following figure. For all the programming interfaces, the target device (IS2083BM) must be powered, and all required signals must be connected. In addition, the interface must be enabled through a special initialization sequence.

Note: For more details on 2-wire prog/debug, refer to the *IS2083 SDK User's Guide* and *IS2083 SDK Debugger User's Guide* .

Figure 6-5. 2-wire In-Circuit Serial Programming (ICSP) Interface



The 2-wire ICSP port can be used to program the memory content. This interface uses the following two communication lines to transfer data to and from the BTZ-983H (IS2083BM) device being programmed:

- Serial Program Clock (TCK_CPU)
- Serial Program Data (TDI_CPU)

These signals are described in the following sections. The following table describes the signals required for the 2-wire ICSP interface.

Table 6-2. 2-wire Interface Pin Description

Pin Name	Pin Type	Description
RST_N	I	Reset pin
VDD_IO, ADAP_IN, BAT_IN	P	Power supply pins

.....continued		
Pin Name	**Pin Type**	**Description**
GND	P	Ground pin
TCK_CPU	I	Primary programming pin pair: Serial Clock
TDI_CPU	I/O	Primary programming pin pair: Serial Data

6.3.2.1 Serial Program Clock (TCK_CPU)

TCK_CPU is the clock that controls the TAP controller update and the shifting of data through the instruction or selected data registers. TCK_CPU is independent of the processor clock, with respect to both frequency and phase.

6.3.2.2 Serial Program Data (TDI_CPU)

TDI_CPU is the data input/output to the instruction or selected data registers and the control signal for the TAP controller. This signal is sampled on the falling edge of TDI_CPU for some TAP controller states.

6.4 General Purpose I/O Pins

The BTZ-983H module provides up to 18 GPIOs that can be configured by using the Config Tool. The following table provides the default I/O functions of the BTZ-983H module.

Note: The MFB pin must be configured as the power On/Off key and the remaining pins are user configurable pins.

Table 6-3. GPIO Assigned Pins Function(1)

Pin Name	Function Assigned
P0_0	External codec reset
P0_1	Forward (FWD) button
P0_2	Play or Pause (PLAY/PAUSE) button
P0_3	Reverse (REV) button
P0_5	Volume decrease (VOL_DN) button
P0_6	Available for user configuration
P0_7	Available for user configuration
P1_2	I^2C SCL (muxed with 2-wire CPU debug data)
P1_3	I^2C SDA (muxed with 2-wire CPU debug clock)
P1_6	PWM
P2_3	Available for user configuration
P2_6	Available for user configuration
P2_7	Volume increase (VOL_UP) button
P3_2	Line-In detect
P3_4	SYS_CFG (muxed with UART_RTS)(2)
P3_7	UART_CTS
P8_5	UART_TXD(3)(4)
P8_6	UART_RXD(3)(4)
MFB	MFB

Note:

1. This table reflects the default IO assignment for the turn-key solution. The GPIOs are user configurable.
2. GPIO P3_4 is used to enter Test mode during reset. If the user wants to use this pin to control external peripherals, care must be taken to ensure this pin is not pulled LOW and accidentally enters Test mode.
3. Microchip recommends to reserve UART port (P8_5 and P8_6) for Flash download in Test mode during production.
4. Currently, GPIOs ports P8_5 and P8_6 APIs (button detect driver) are not implemented.

6.5 I²S Interface

The BTZ-983H module provides an I²S digital audio input, output or input/output interface to connect with the external codec or DSP. It provides 8, 16, 44.1, 48, 88.2, and 96 kHz sampling rates for 16-bit and 24-bit data formats. The following are the BTZ-983H module interface signals:

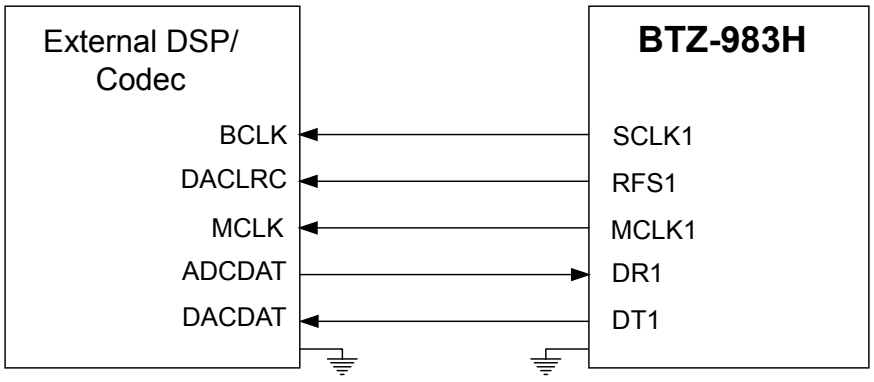
- MCLK1 – Master Clock (BTZ-983H output)
- SCLK1– Serial/Bit Clock (BTZ-983H input/output)
- DR1 – Receive Data (BTZ-983H input)
- RFS1 – Receive Frame Sync (BTZ-983H input/output)
- DT1 – Transmit Data (BTZ-983H output)

Note: The I²S parameters can be configured by using the Config Tool.

I²S supports the following modes:

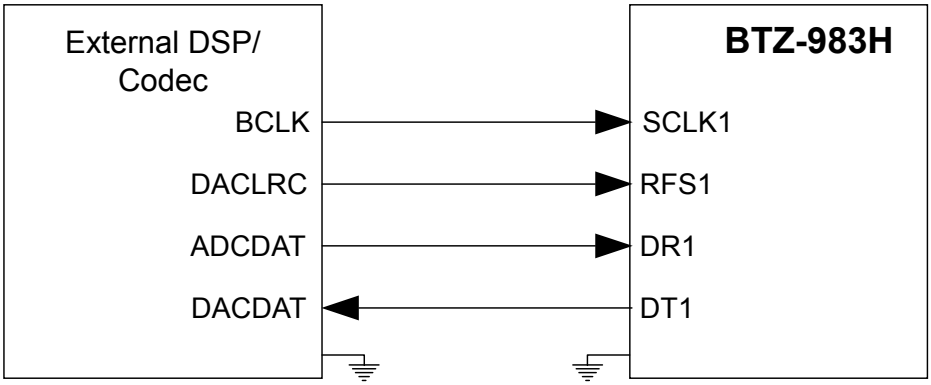
- Master mode
  - The BTZ-983H serves as a master to provide clock and frame synchronous signals for the master/slave data synchronizations, as illustrated in the following figures. The MCLK1 is the master clock output provided to an external I²S device to drive its system clock and save crystal cost. The MCLK is optional and is not required if the external I²S device can drive its system clock on its own.

Figure 6-6. BTZ-983H Module in I²S Master Mode



- Slave mode
  - The BTZ-983H serves as a slave to receive clock and frame synchronous signals from the external codec or DSP devices, as illustrated in the following figure.

Figure 6-7. BTZ-983H Module in I²S Slave Mode



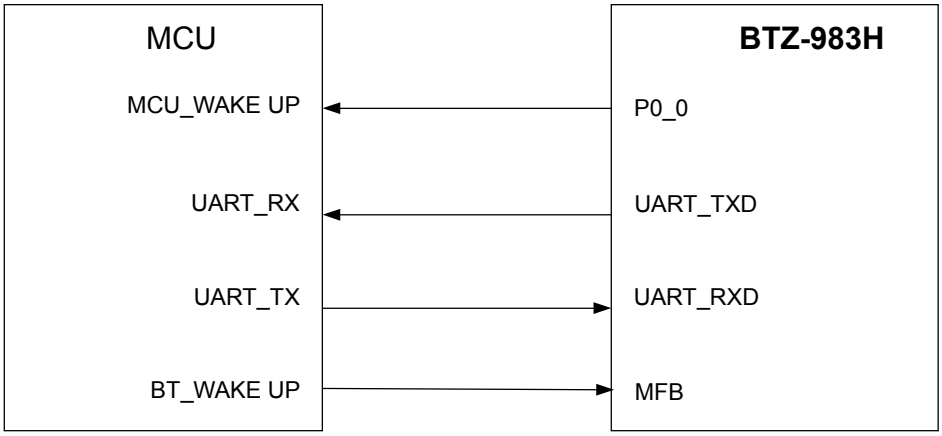
Note: Use the Config Tool to configure the BTZ-983H module as a master/slave.

6.6 Host MCU Interface Over UART

The BTZ-983H module supports UART commands, which enable an external MCU to control the BTZ-983H module. The following figure illustrates the UART interface between the BTZ-983H module and an external MCU. An external MCU can control the BTZ-983H module over the UART interface and wake up the module with the MFB and P0_0 pins.

Refer to *SPKcommandset tool* to get a list of functions supported by the BTZ-983H module and how to use the Config Tool for configuring UART and UART command set tool.

Figure 6-8. Host MCU Interface Over UART



Note: For the latest SPKcommandset tool, refer to http://www.microchip.com/BM83.

The following figures illustrate the timing sequences of various UART control signals.

Figure 6-9. Timing Sequence of Power On/Off

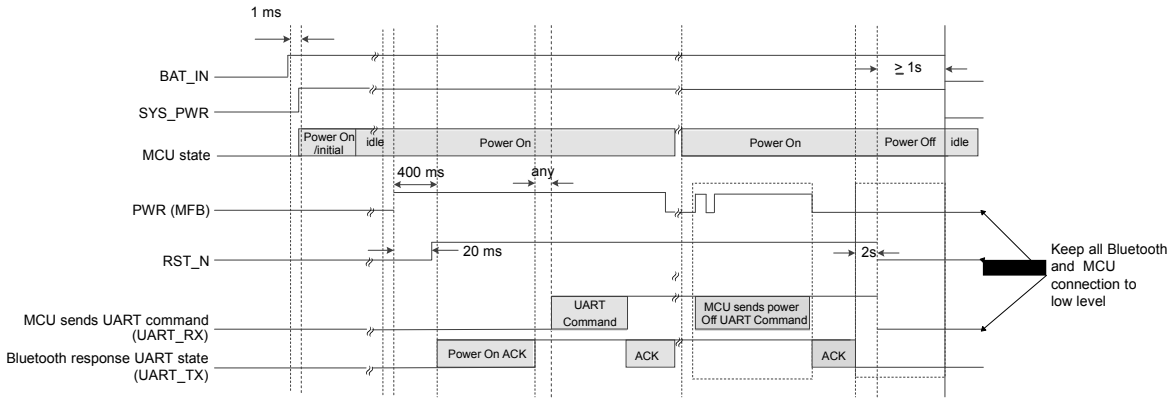


Figure 6-10. Timing Sequence of RX Indication After Power On State

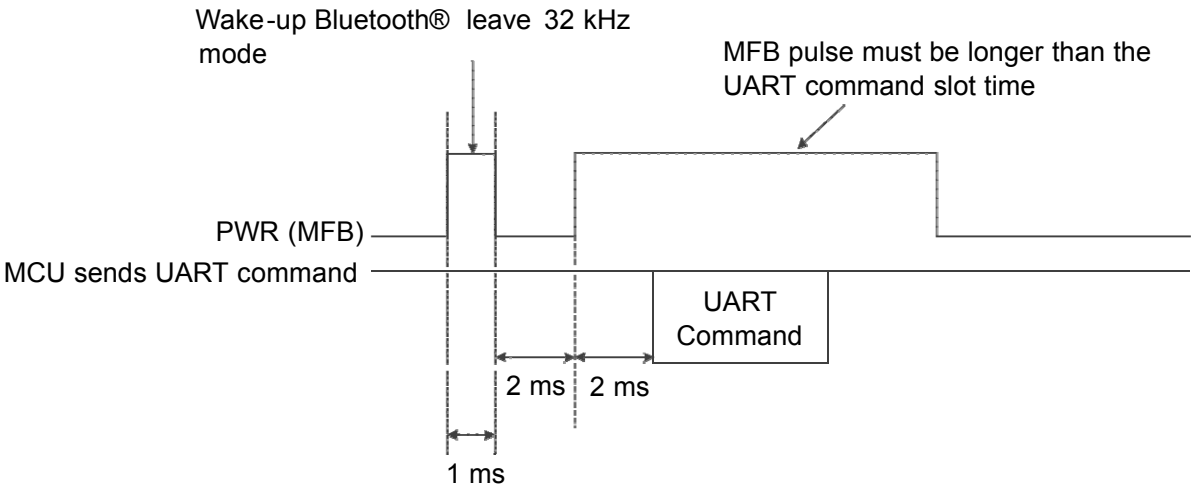
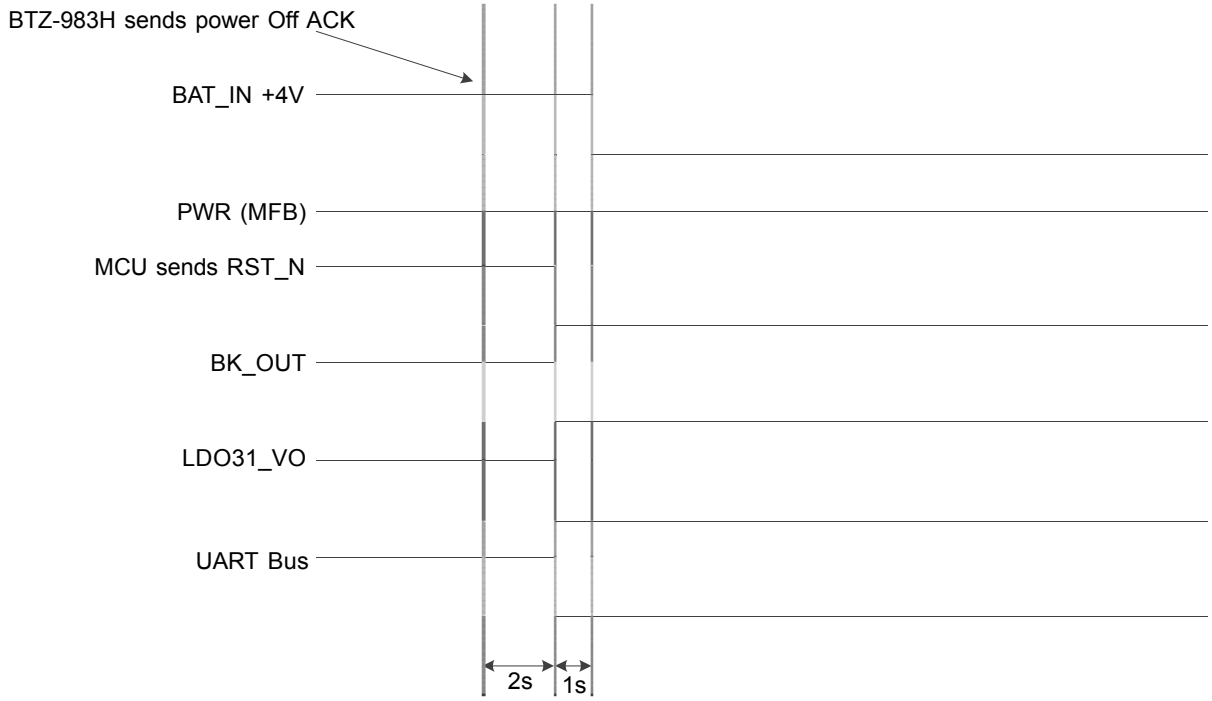


Figure 6-11. Timing Sequence of Power Off State



Timing sequence of power Off state:

- For a byte write: 0.01 ms x 32 clock x 2 = 640 µs.
- It is recommended to have ramp-down time more than 640 µs during the power Off sequence to ensure safe operation of the device.

Figure 6-12. Timing Sequence of Power On (NACK)

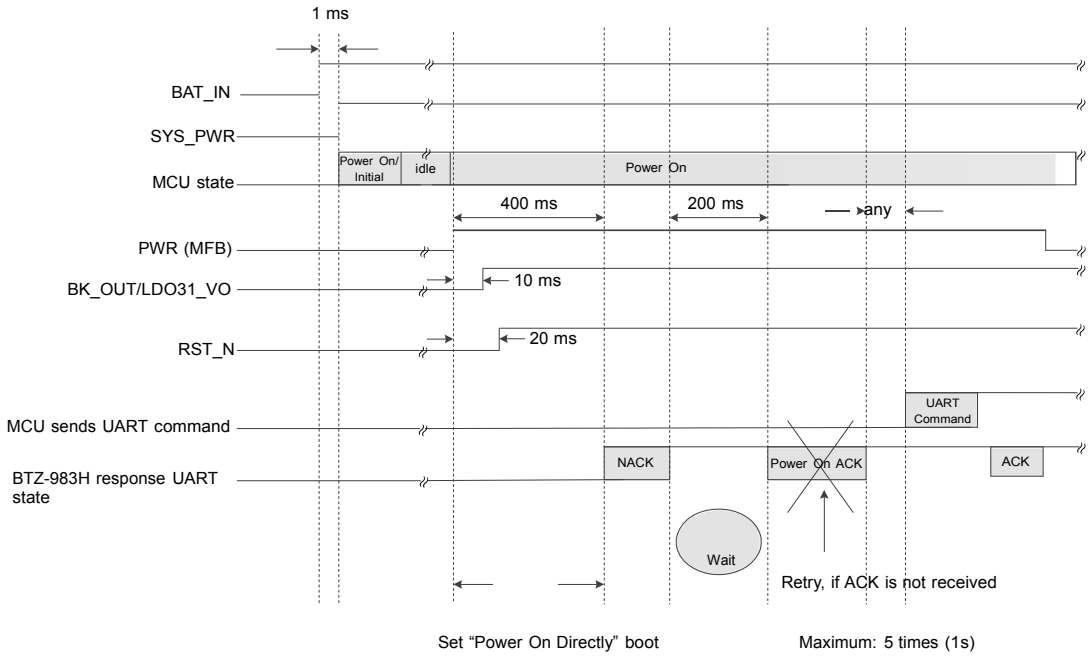
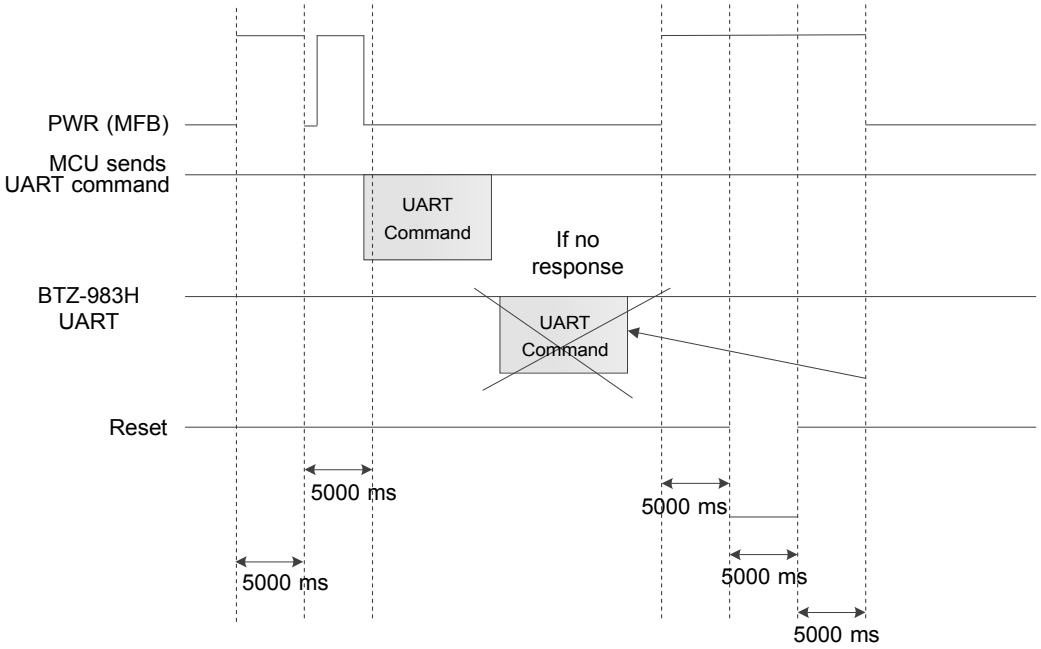


Figure 6-13. Reset Timing Sequence in No Response From Module to Host MCU

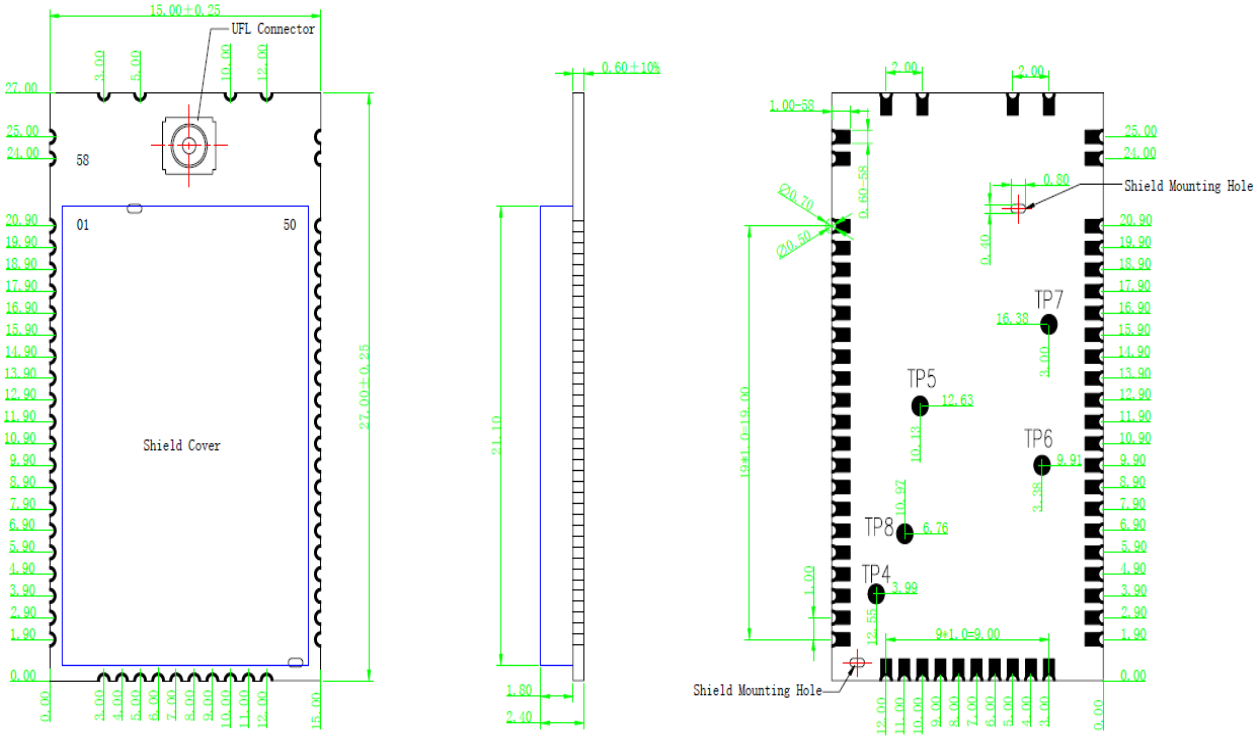


If the BTZ-983H module does not respond to the host MCU's UART command, the MCU re-sends the UART command. If the BTZ-983H module does not respond within 5 secs, the MCU forces the system to reset.

7. Physical Dimensions

The following figures illustrate the PCB dimension and the recommended PCB footprint of the BTZ-983H module.

Figure 7-1. BTZ-983H Module PCB Dimension



8. Electrical Specifications

This section provides an overview of the BTZ-983H stereo audio module electrical characteristics. The following table provides the absolute maximum ratings for the BTZ-983H module.

Table 8-1. Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Unit
Ambient temperature under bias	-40	—	+85	°C
Storage temperature	-40	—	+150	°C
Battery input voltage (BAT_IN)	—	—	+4.3	V
Adapter input voltage (ADAP_IN)	—	—	+7	V
Maximum output current sink by any I/O pin	—	—	12	mA
Maximum output current sourced by any I/O pin	—	—	12	mA

⚠ CAUTION Stresses listed in the preceding table cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions and those indicated in the operation listings of this specification are not implied. Exposure to maximum rating conditions for extended periods affects device reliability.

The following tables provide the recommended operating conditions and the electrical specifications of the BTZ-983H module.

Table 8-2. Recommended Operating Conditions (1)

Parameter	Min.	Typ.	Max.	Unit
Battery input voltage (BAT_IN)	3.2	3.8	4.2	V
Adapter input voltage (ADAP_IN)(2)	4.5	5	5.5	V
Operation temperature ($T_{OPERATION}$)	-40	+25	+85	ºC

1. The recommended operating condition tables reflect a typical voltage usage for the device.
2. ADAP_IN is recommended to be used to charge the battery in battery powered applications, and/or applications with USB functionality, else ADAP_IN can be left floating.

Table 8-3. I/O and Reset Level (1)

Parameter		Min.	Typ.	Max.	Unit
I/O supply voltage (VDD_IO)		3.0	3.3	3.6	V
I/O voltage levels					
VIL input logic levels low		0	—	0.8	V
VIH input logic levels high		2.0	—	3.6	V
VOL output logic levels low		—	—	0.4	V
VOH output logic levels high		2.4	—	—	V
RST_N	Input low to high threshold point	—	—	1.87	V
	Input high to low threshold point	1.25	—	—	V

.....continued				
Parameter	**Min.**	**Typ.**	**Max.**	**Unit**
Threshold voltage	—	1.6	—	V

1. These parameters are characterized, but not tested on production device.

Table 8-4. Battery Charger (1)

Parameter		Min.	Typ.	Max.	Unit
Adapter input voltage (ADAP_IN)		4.6(2)	5.0	5.5	V
Supply current to charger only		—	3	4.5	mA
Maximum battery fast charge current	Headroom(3) > 0.7V (ADAP_IN = 5V)	—	350	—	mA
	Headroom = 0.3V to 0.7V (ADAP_IN = 4.5V)	—	175(4)	—	mA
Trickle charge voltage threshold		—	3	—	V
Battery charge termination current (% of fast charge current)		—	10	—	%

1. These parameters are characterized, but not tested on production device.
2. It needs more time to get battery fully charged when ADAP_IN = 4.5V.
3. Headroom = VADAP_IN – VBAT_IN.
4. When VADAP_IN – VBAT_IN > 2V, the maximum fast charge current is 175 mA for thermal protection.

Table 8-5. SAR ADC Operating Conditions

Parameter	Condition	Min.	Typ.	Max.	Unit
Shutdown current (I_{OFF})	PDI_ADC = 1	—	—	1	µA
Resolution	—	—	10	—	bits
Effective Number of Bits (ENOB)	—	7	8	—	bits
SAR core clock (F_{CLOCK})	—	—	0.5	1	MHz
Conversion time per channel (T_{CONV})	10 F_{CLOCK} cycles	10	20	—	µs
Offset error (E_{OFFSET})	—	-5	—	+5	%
Gain error (E_{GAIN})	—	—	—	+1	%
ADC SAR core power-up (t_{PU})	PDI_ADC transitions from 1 to 0	—	—	500	ns
Input voltage range (V_{IN})	Channel 8 (SK2 Pin)	0.25	—	1.4	V
	Channel 9 (SK1 Pin)	0.25	—	1.4	V
	Channel 10 (OTP)	0.25	—	1.4	V
	Channel 11 (ADAP_IN Pin)	2.25	—	12.6	V
	Channel 12 (BAT_IN Pin)	1.0	—	5.6	V

Table 8-6. LED Driver [1]

Parameter	Min.	Typ.	Max.	Unit
Open-drain voltage	—	—	3.6	V
Programmable current range	0	—	5.25	mA
Intensity control	—	16	—	step
Current step	—	0.35	—	mA
Power-down open-drain current	—	—	1	μA
Shutdown current	—	—	1	μA

1. These parameters are characterized, but not tested on production device.

Table 8-7. Audio Codec Analog-to-Digital Converter [1,4]

Parameter (Condition)	Min.	Typ.	Max.	Unit
Resolution	—	—	16	Bit
Output sample rate	8	—	48	kHz
SNR ratio[2] (at MIC or Line-In)	—	91	—	dB
Digital gain	-54	—	4.85	dB
Digital gain resolution	—	2 to 6	—	dB
MIC boost gain	—	20	—	dB
Analog gain	—	—	60	dB
Analog gain resolution	—	2.0	—	dB
Input full-scale at maximum gain (differential)	—	4	—	mV/rms
Input full-scale at minimum gain (differential)	—	800	—	mV/rms
3 dB bandwidth	—	20	—	kHz
Microphone mode (input impedance)	—	24	—	kΩ
THD+N ratio[3]	—	0.04	—	%
THD+N ratio[3]	—	-68	—	dB

1. These parameters are characterized, but not tested on production device.
2. T = 25°C, VDD = 1.8V, 1 kHz sine wave input, bandwidth = 20 Hz to 20 kHz.
3. f_{in} = 1kHz sine tone, analog gain = -3 dB, digital gain = 0 dB, bandwidth = 22K, A-weighted, sweep across -100 dBv to 6 dBv.

Table 8-8. Audio Codec Digital-to-Analog Converter[1,5]

Parameter (Condition)	Min.	Typ.	Max.	Unit
Over-sampling rate	—	128	—	*f*s
Resolution	16	—	20	Bit
Output sample rate	8	—	48	kHz
SNR ratio[2](at Capless mode) for 48 kHz	—	95	—	dB
SNR[2](at Single-ended mode) for 48 kHz	—	95	—	dB

.....continued

Parameter (Condition)		Min.	Typ.	Max.	Unit
Digital gain		-54	—	4.85	dB
Digital gain resolution		—	2 to 6	—	dB
Analog gain		-28	—	3	dB
Analog gain resolution		—	1	—	dB
Output voltage full-scale swing (AVDD = 1.8V)		495	742.5	—	mV/rms
Maximum output power (16Ω load)		—	34.5	—	mW
Maximum output power (32Ω load)		—	17.2	—	mW
Allowed load	Resistive	16	—	—	Ω
	Capacitive	—	—	500	pF
THD Ratio (3)		0.15	0.02	0.05	%
THD Ratio (3)		-75	-70	-65	dB
THD+N Ratio (3)		0.03	0.04	0.05	%
THD+N Ratio (3)		-72	-70	-65	dB
SNR ratio (at 16Ω load) (4)		—	95	—	dB

1. These parameters are characterized, but not tested on production device.
2. T = 25°C, VDD = 1.8V, 1 kHz sine wave input, bandwidth = 20 Hz to 20 kHz.
3. f_{in}=1 kHz sine tone, analog gain = -3dB, digital gain = 0dB, bandwidth = 22K, A-weighting applied, sweep across -100 dBv to 6 dBv level, with various loads (16Ω, 32Ω, 100 kΩ)
4. f_{in} = 1 kHz, bandwidth = 20 Hz to 20 kHz, A-weighted, -1 dBFS signal, load =16Ω.

Table 8-9. Transmitter Section Class 1 (MPA Configuration) for BDR and EDR(1,4)

Parameter(2,3)	Bluetooth Specification	Frequency (MHz)	Min.	Typ.	Max.	Unit
Transmit power BDR	0 to 20	2402	8.5	10.0	11.5	dBm
		2441	7.5	9.0	10.5	dBm
		2480	6.5	8.0	9.5	dBm
Transmit power EDR 2M	0 to 20	2402	8.5	10.5	11.5	dBm
		2441	7.5	9.0	10.5	dBm
		2480	6.0	7.5	9.0	dBm
Transmit power EDR 3M	0 to 20	2402	8.5	10.0	11.5	dBm
		2441	7.5	9.0	10.5	dBm
		2480	6.0	7.5	9.0	dBm

1. These parameters are characterized, but not tested on production device.
2. The RF transmit power is the average power measured for the mid-channel (Channel 39).
3. The RF transmit power is calibrated during production using the MP tool and MT8852 Bluetooth test equipment.
4. Test condition: VCC_RF = 1.28V, temperature +25ºC.

Table 8-10. Transmitter Section Class 2 (LPA Configuration) for BDR and EDR [1,4]

Parameter[2,3]	Bluetooth Specification	Frequency (MHz)	Min.	Typ.	Max.	Unit
Transmit power BDR	-6 to 4	2402	-1.5	-0.5	1.5	dBm
		2441	-1.5	-0.5	1.5	dBm
		2480	-1.5	-0.5	1.5	dBm

1. These parameters are characterized, but not tested on production device.
2. The RF transmit power is the average power measured for the mid-channel (Channel 39).
3. The RF transmit power is calibrated during production using the MP tool and MT8852 Bluetooth test equipment.
4. Test condition: VCC_RF = 1.28V, temperature +25ºC.

Table 8-11. Receiver Section for BDR/EDR/Bluetooth Low Energy[1,2]

Parameter	Bluetooth Specification	Modulation	Frequency (MHz)	Min.	Typ.	Max.	Unit
Sensitivity at 0.1% BER	≤-70	GFSK	2402	-91	-90.5	-89	dBm
			2441	-91	-90.5	-89	dBm
			2480	-90.5	-89.5	-86.5	dBm
Sensitivity at 0.01% BER	≤-70	π/4 DQPSK	2402	-93	-91.5	-90	dBm
			2441	-93	-91.5	-90	dBm
			2480	-89.5	-88.5	-85.5	dBm
	≤-70	8 DPSK	2402	-85	-83.5	-82	dBm
			2441	-85	-83.5	-82	dBm
			2480	-82	-80	-78	dBm
Sensitivity at 0.1% BER	≤-70	Bluetooth Low Energy	-	—	-92	—	dBm

1. These parameters are characterized, but not tested on production device.
2. Test condition: VCC_RF = 1.28V with temperature +25ºC.

Table 8-12. BTZ-983H System Current Consumption(1,2,3,6,7,8)

Modes	Condition	Role	Packet Type	Current (Typ.)	Unit
A2DP mode	Internal codec, iOS Master	Slave	2DH5/3DH5	12.05	mA
	Internal codec, Android™ Slave	Master	3DH5	12.32	mA
Sniff mode(4)	Internal codec, Bluetooth Low Energy disabled	Slave	DM1	548	µA
		Master	2DH1/3DH1	555	µA
	Internal codec, Bluetooth Low Energy enabled	Slave	DM1	832	µA
		Master	2DH1/3DH1	863	µA
SCO/eSCO connection	Mute at both far end and near end	Slave	2EV3	14.1	mA
		Master	2EV3	13.94	mA
Inquiry Scan	Bluetooth Low Energy disabled	—	—	1.35	mA
	Bluetooth Low Energy enabled	—	—	1.70	mA
Standby mode	System off	Slave	—	2.81	µA
		Master	—	2.85	µA

.....continued

Modes	Condition	Role	Packet Type	Current (Typ.)	Unit
RF modes(5)	Continuous TX mode	Modulation OFF, PL0	—	59	mA
		Modulation ON, PL0	—	30	mA
		Modulation OFF, PL2	—	35.5	mA
		Modulation ON, PL2	—	22	mA
	Continuous RX mode	Packet count disable	—	49	mA
		Packet count enable	—	38.5	mA

1. VBAT_IN = 3.8V; current measured across BAT_IN.
2. BM83 module (mounted on BM83 Carrier Board) configured in standalone mode (internal codec) with SBC, used for measurements; no LEDs, no speaker load.
3. iPhone®6 (iOS v12.2) and OnePlus6 (Android Oxygen version 9.0.3) used for measurements.
4. Auto-unsniff mode is disabled. Sniff interval is 500 ms by default; observed time to enter sniff mode is approximately 20 secs.
5. RF TX power is set to 10 dBm.
6. Current measurements average over a period of 120 secs.
7. Distance between DUT (BTZ-983H) and Bluetooth source (smartphone) is 30 cms.
8. All measurements are taken inside a shield room.

8.1 Timing Specifications

The following figures illustrate the timing diagram of the IS2083BM/BTZ-983H in I²S and PCM modes.

Figure 8-1. Timing Diagram for I²S Modes (Master/Slave)

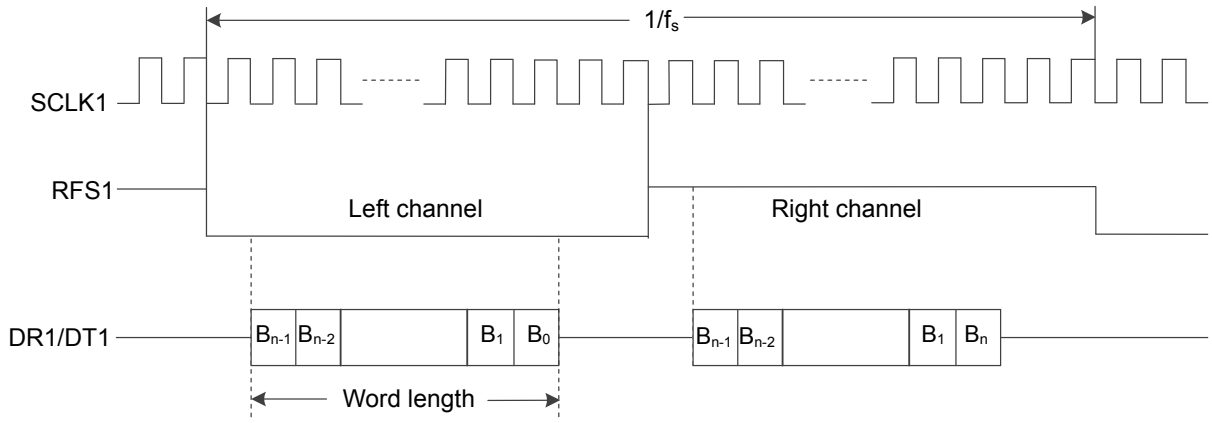
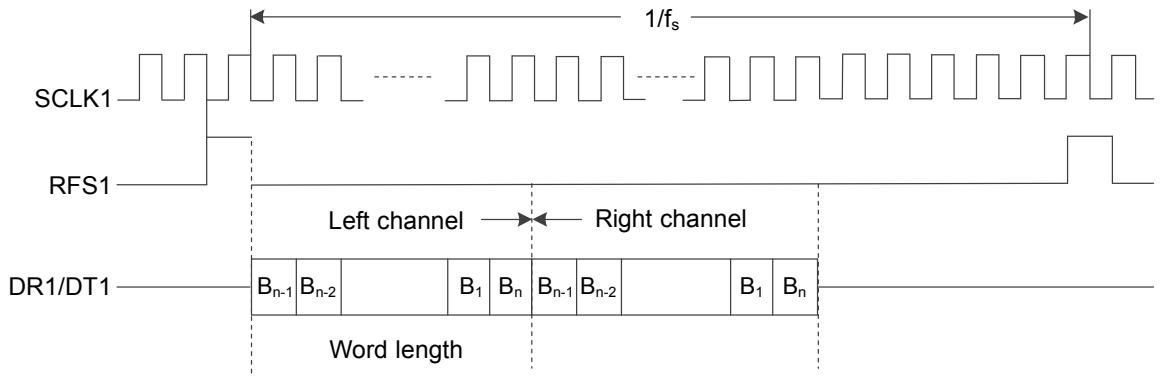
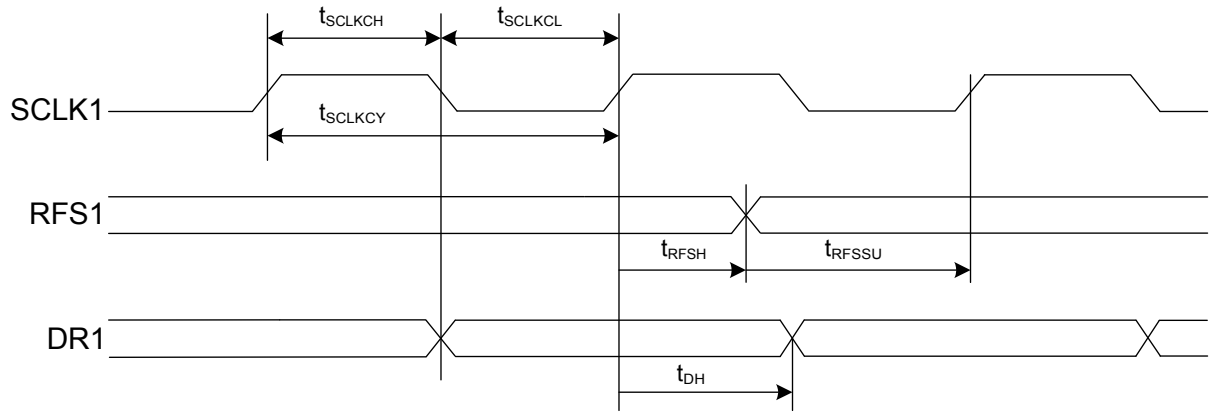


Figure 8-2. Timing Diagram for PCM Modes (Master/Slave)



The following figure illustrates the timing diagram of the audio interface.

Figure 8-3. Audio Interface Timing Diagram



The following table provides the timing specifications of the audio interface.

Table 8-13. Audio Interface Timing Specifications (1)

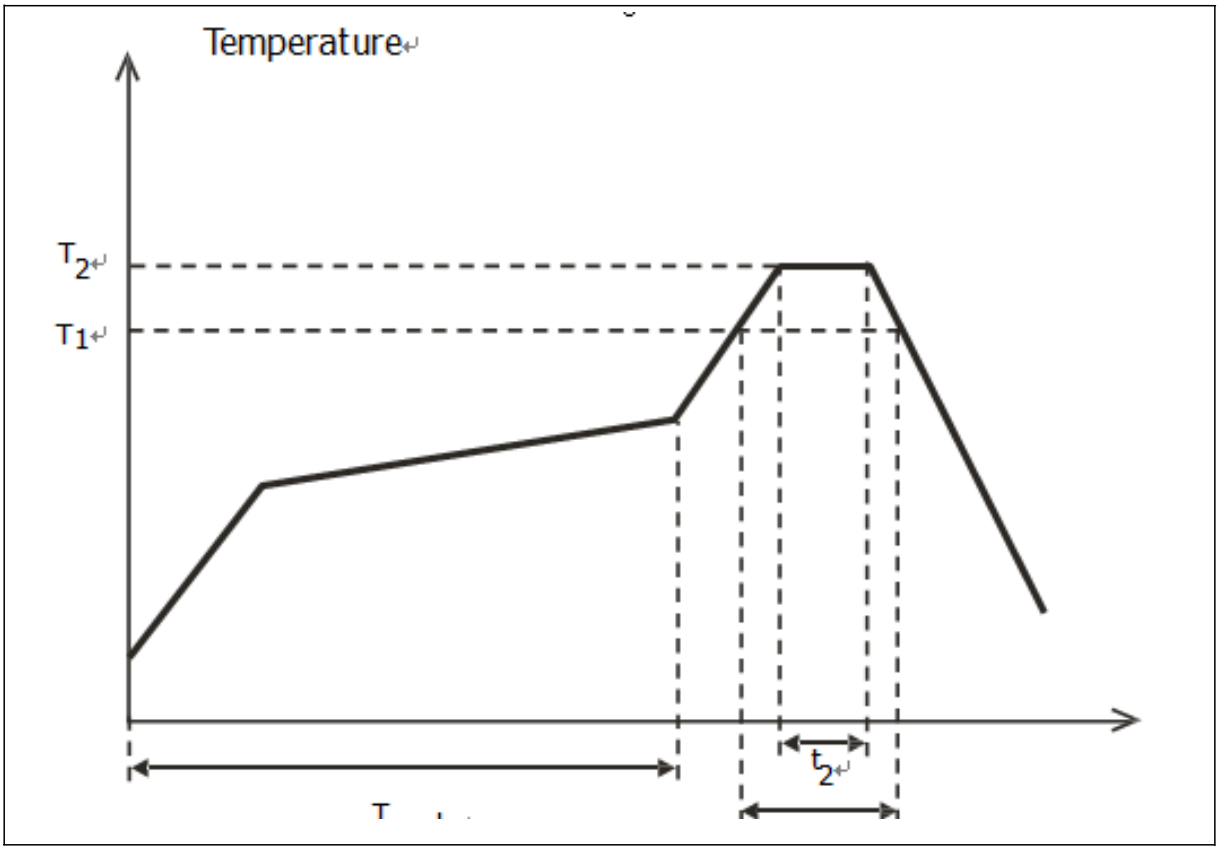
Parameter	Symbol	Min.	Typ.	Max.	Unit
SCLK1 duty ratio	d_{SCLK}	—	50	—	%
SCLK1 cycle time	t_{SCLKCY}	50	—	—	ns
SCLK1 pulse width high	t_{SCLKCH}	20	—	—	ns
SCLK1 pulse width low	t_{SCLKCL}	20	—	—	ns
RFS1 setup time to SCLK1 rising edge	t_{RFSSU}	10	—	—	ns
RFS1 hold time from SCLK1 rising edge	t_{RFSH}	10	—	—	ns
DR1 hold time from SCLK1 rising edge	t_{DH}	10	—	—	ns

1. Test Conditions: Slave mode, *f*s = 48 kHz, 24-bit data, and SCLK1 period = 256 *f*s.

9.0 SOLDERING RECOMMENDATIONS

Reflow profile requirements		
Parameter Specification	**Reference**	**Specification**
Average temperature gradient in preheating		1~2.5°C/s to 175°C equilibrium.
Soak time	T_{soak}	120~180 seconds
Time above 217°C (T_1)	t_1	45~90 seconds
Peak temperature in reflow	T_2	250°C (–0/+5°C)
Time at peak temperature	t_2	6 seconds
Temperature gradient in cooling		6°C/second max.

FIGURE 9-1: REFLOW PROFILE



10. Ordering Information

The following table provides the BTZ-983H module ordering information.

Table 10-1. BTZ-983H Module Ordering Information

Module	Microchip IC	Description	Regulatory Certification
BTZ-983H	IS2083BM-232	Bluetooth 5.0 stereo audio module, Class 1 with shield	FCC, ISED, BQB

FCC Statement:

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) this device must accept any interference received, including interference that may cause undesired operation.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

—Reorient or relocate the receiving antenna.

—Increase the separation between the equipment and receiver.

—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced radio/TV technician for help.

Changes or modifications not expressly approved by the party responsible for compliance could void the user’s authority to operate the equipment.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 10mm between the radiator and a human body.

If the identification number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module, Contains FCC ID: 2AKCY-RL56BBLE.

Co-location of this module with other transmitters that operate simultaneously are required to be evaluated using the multi-transmitter procedures.

The host integrator must follow the integration instructions provided in this document and ensure that the composite-system end product complies with the requirements by a technical assessment or evaluation to the rules and to KDB Publication 996369.

The host integrator installing this module into their product must ensure that the final composite product complies with the requirements by a technical assessment or evaluation to the rules, including the transmitter operation and should refer to guidance in KDB 996369.

ISED Statement:

This device contains licence-exempt transmitter(s) that comply with Innovation, Science and Economic Development Canada's licence-exempt RSS(s). Operation is subject to the following two conditions:

(1) this device may not cause interference,

(2) this device must accept any interference, including interference that may cause undesired operation of the device.

L'émetteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

(1) L'appareil ne doit pas produire de brouillage;

(2) L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

If the identification number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module, Contains IC: 4706A-RL56BBLE.

This equipment complies with ISED radiation exposure limits set forth for an uncontrolled env ironment. This equipment should be installed and operated with a minimum distance of 25 mm between the radiator and a human body.

Cet équipement est conforme aux limites d'exposition aux rayonnements d'ISDE établies pou r un environnement non contrôlé. Cet équipement doit être installé et utilisé à une distance m inimale de 25 mm entre le radiateur et un corps humain.