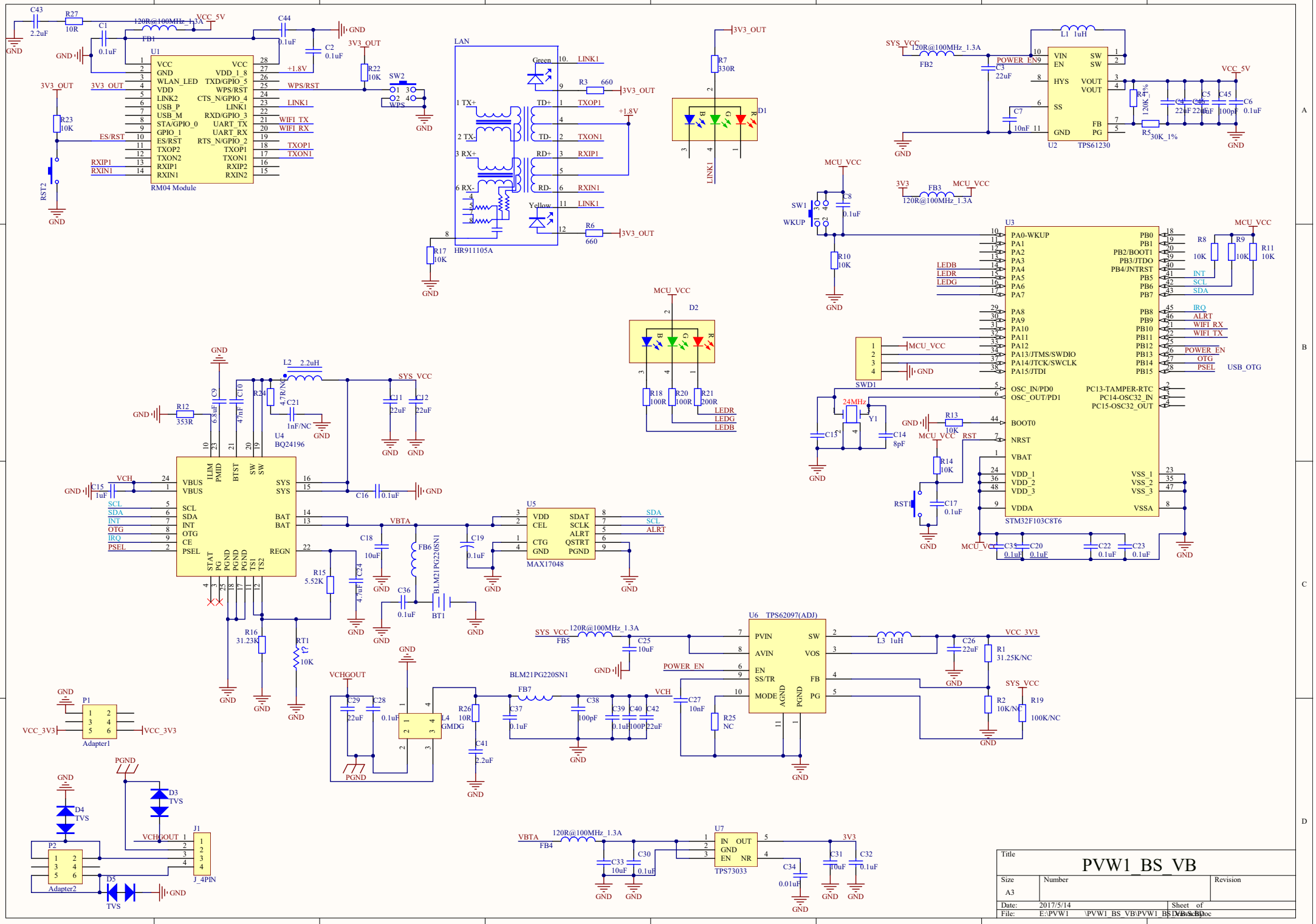
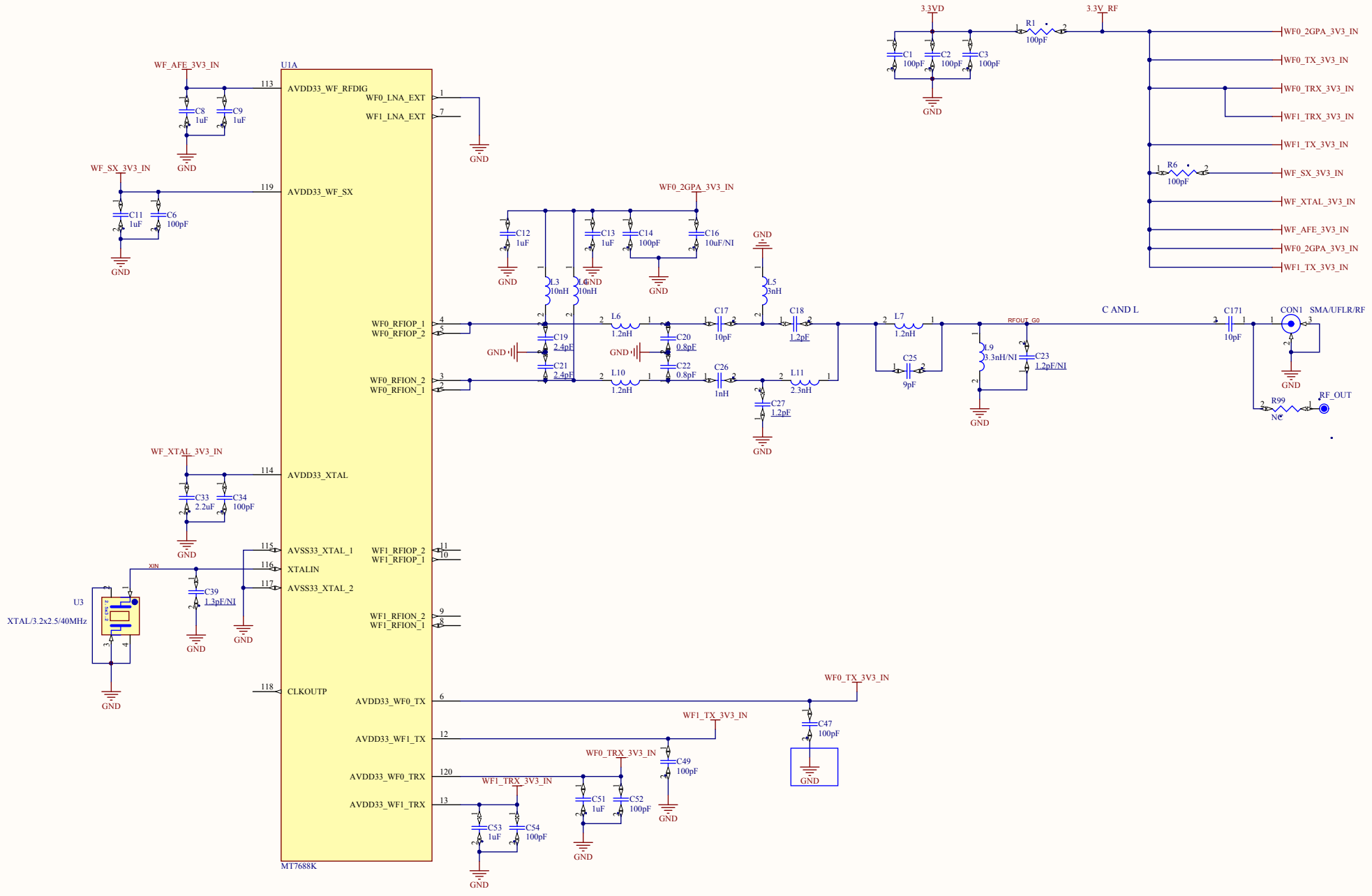
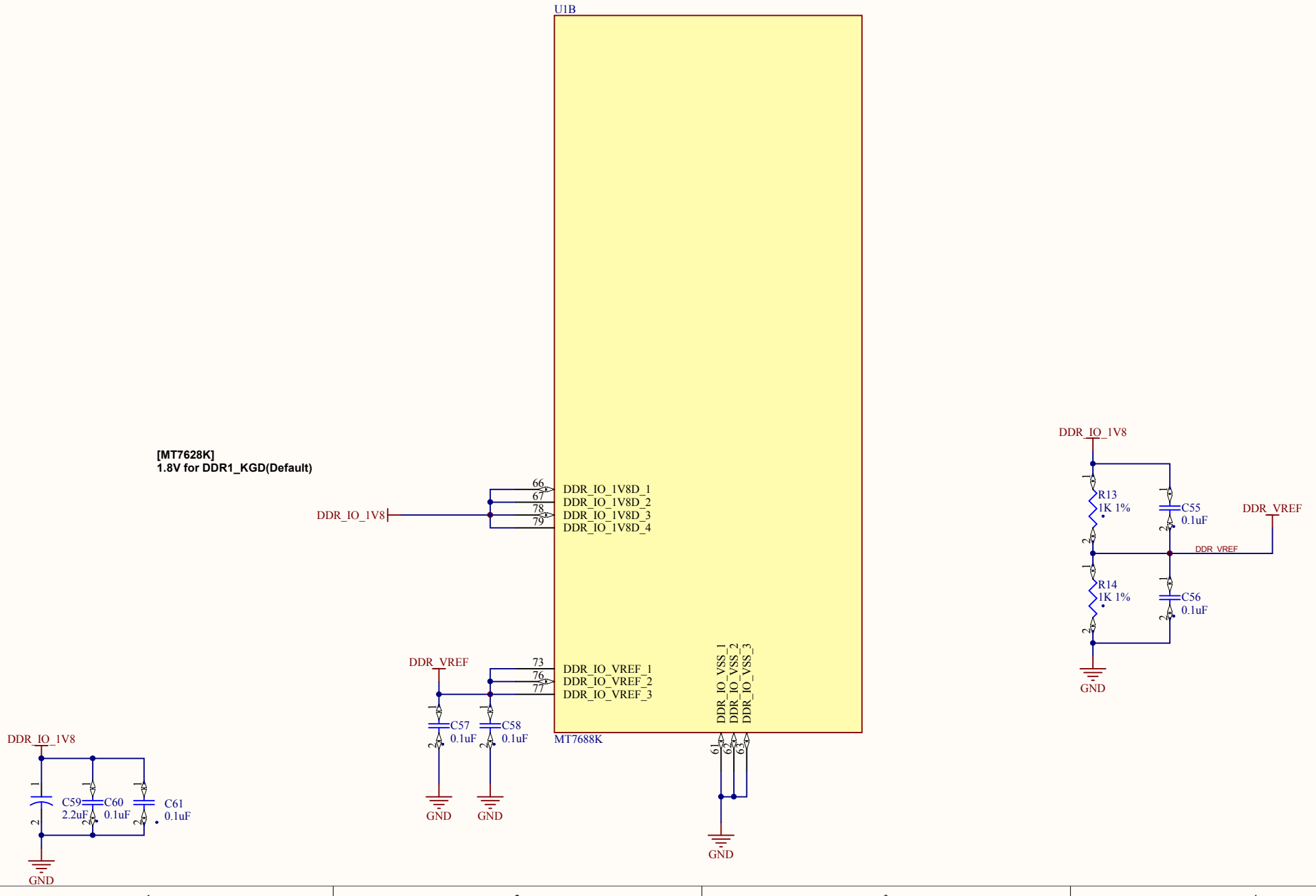
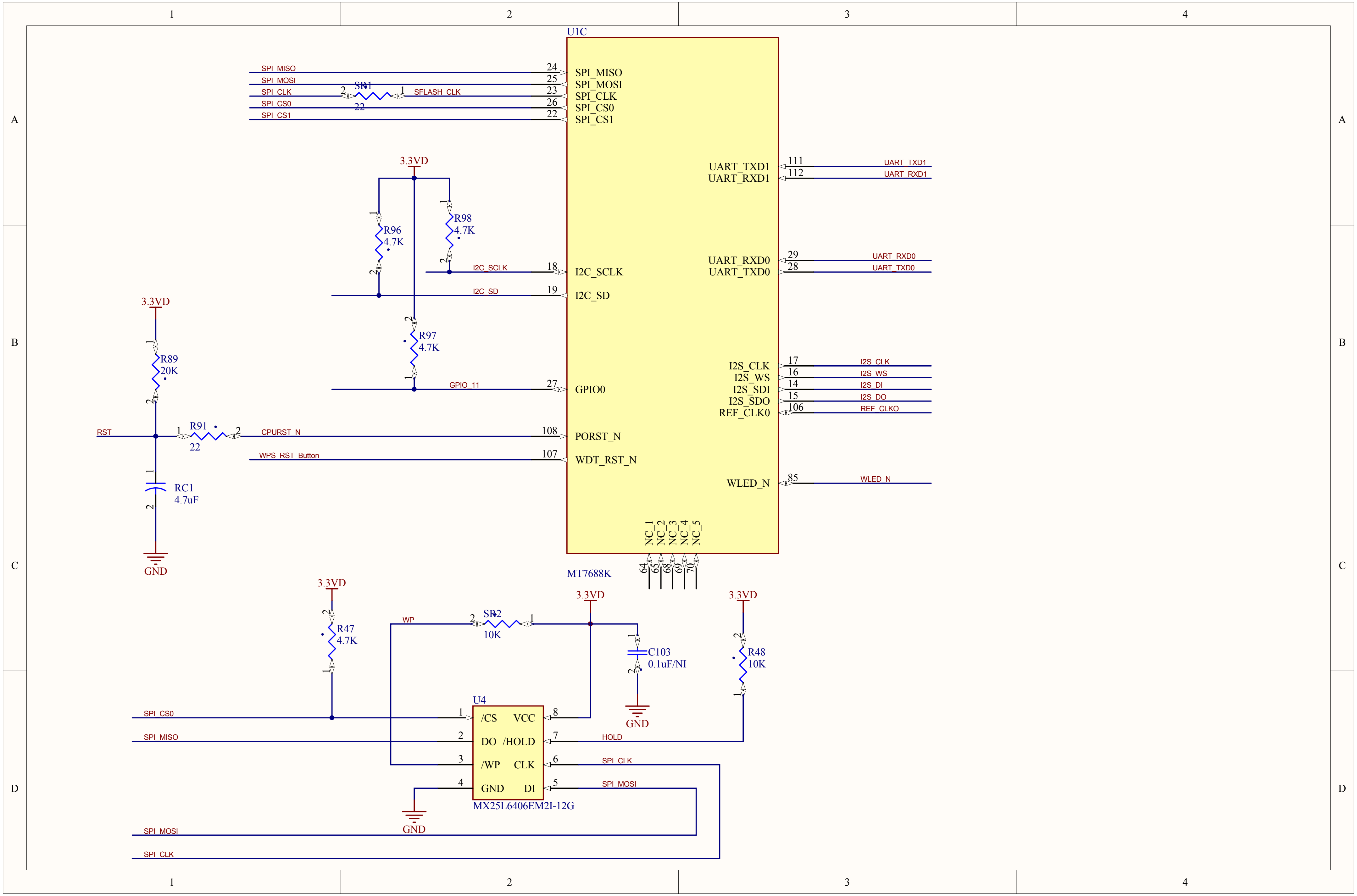
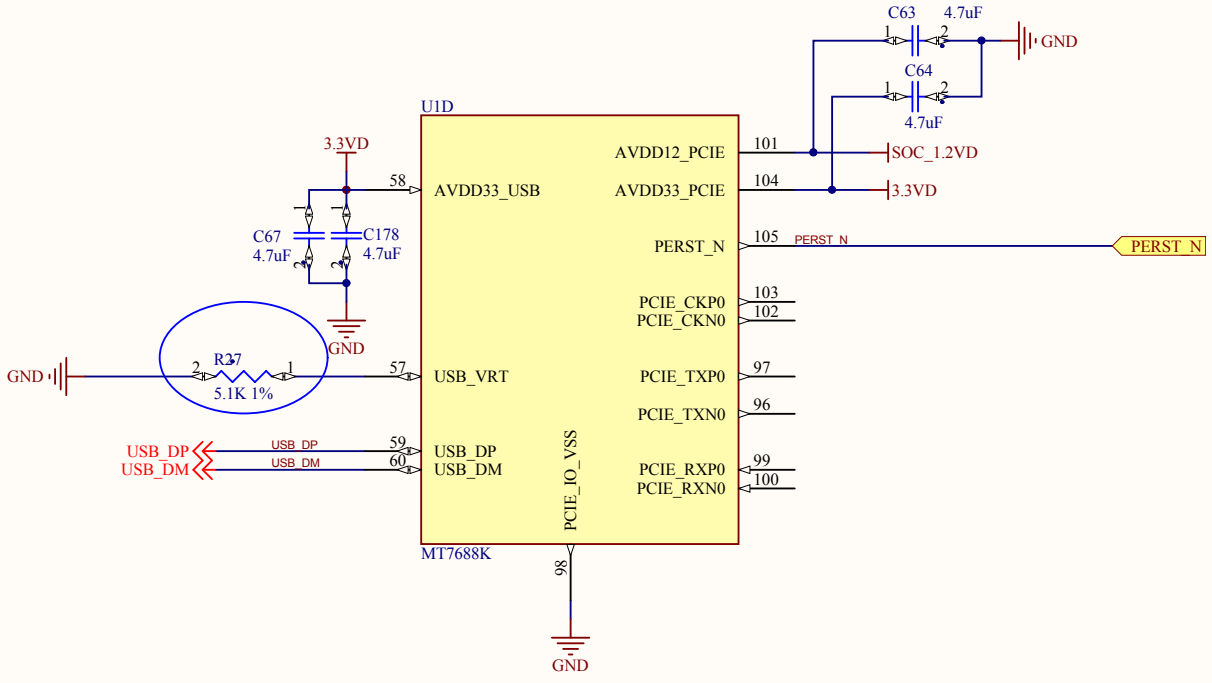

U1
RM04 Module
U2
TPS61230
U3
STM32F103C8T6
U4
BQ24196
U5
MAX17048
U6
TPS62097(ADJ)
U7
TPS73033
LAN
HR911105A
SWD1
USB_OTG
Adapter1
Adapter2
J_4PIN
BLM21PG220SN1
Title
PVW1_BS_VB
Size
A3
Number
Revision
Date: 2017/5/14
Sheet of
File: E:\PVW1 \PVW1_BS_VB\PVW1_BS_VB.SchDoc

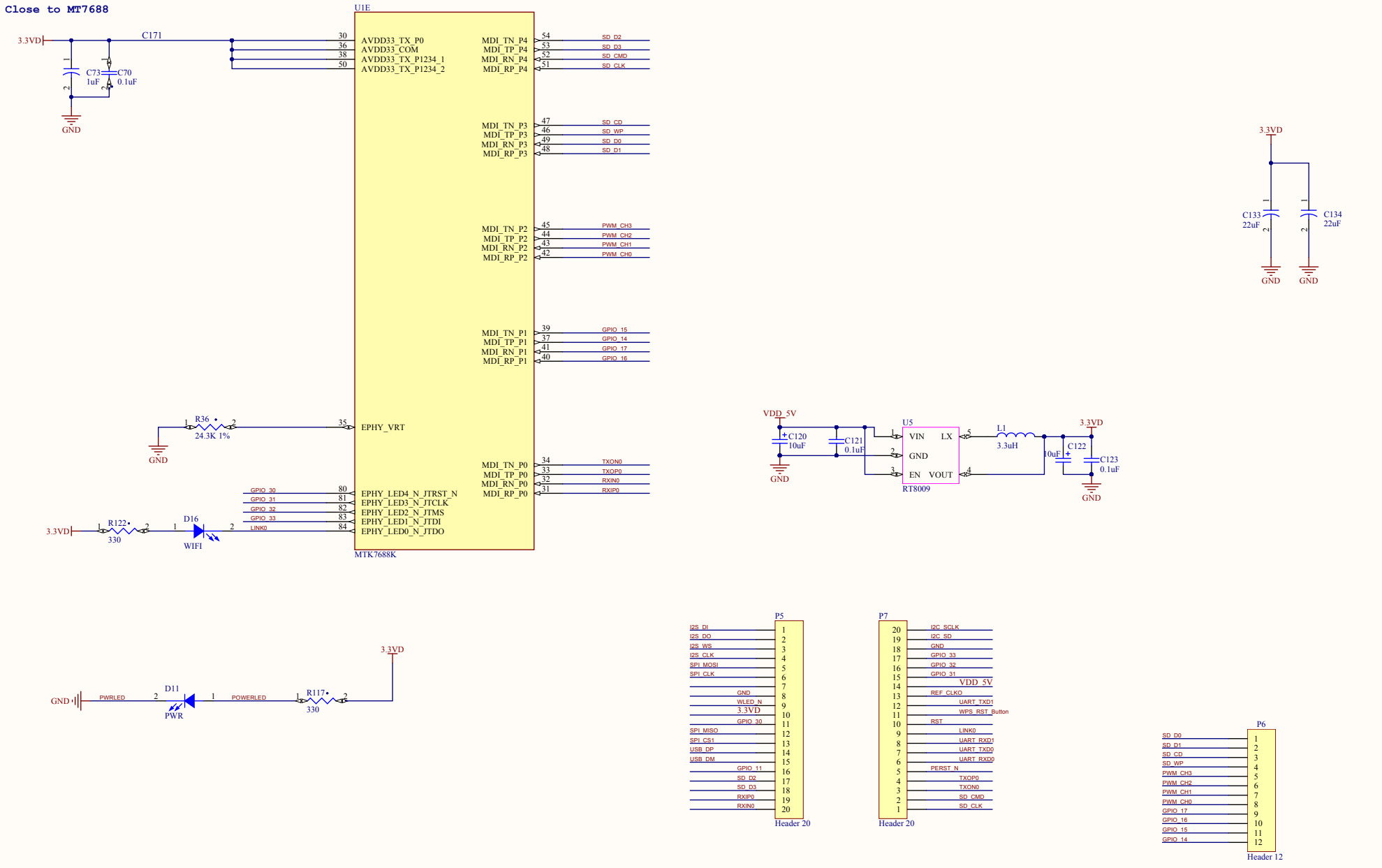

U1A
MT7688K
AVDD33_WF_RFDIG
AVDD33_WF_SX
AVDD33_XTAL
AVSS33_XTAL_1
XTALIN
AVSS33_XTAL_2
CLKOUTP
AVDD33_WF0_TX
AVDD33_WF1_TX
AVDD33_WF0_TRX
AVDD33_WF1_TRX
WF0_LNA_EXT
WF1_LNA_EXT
WF0_RFIOP_1
WF0_RFIOP_2
WF0_RFION_2
WF0_RFION_1
WF1_RFIOP_2
WF1_RFIOP_1
WF1_RFION_2
WF1_RFION_1
WF_AFE_3V3_IN
WF_SX_3V3_IN
WF_XTAL_3V3_IN
3.3VD
3.3V_RF
WF0_2GPA_3V3_IN
WF0_TX_3V3_IN
WF0_TRX_3V3_IN
WF1_TRX_3V3_IN
WF1_TX_3V3_IN
WF_SX_3V3_IN
WF_XTAL_3V3_IN
WF_AFE_3V3_IN
WF0_2GPA_3V3_IN
WF1_TX_3V3_IN
C AND L
RFOUT_G0
CON1
SMA/UFLR/RF
RF_OUT
XIN
U3
XTAL/3.2x2.5/40MHz
GND

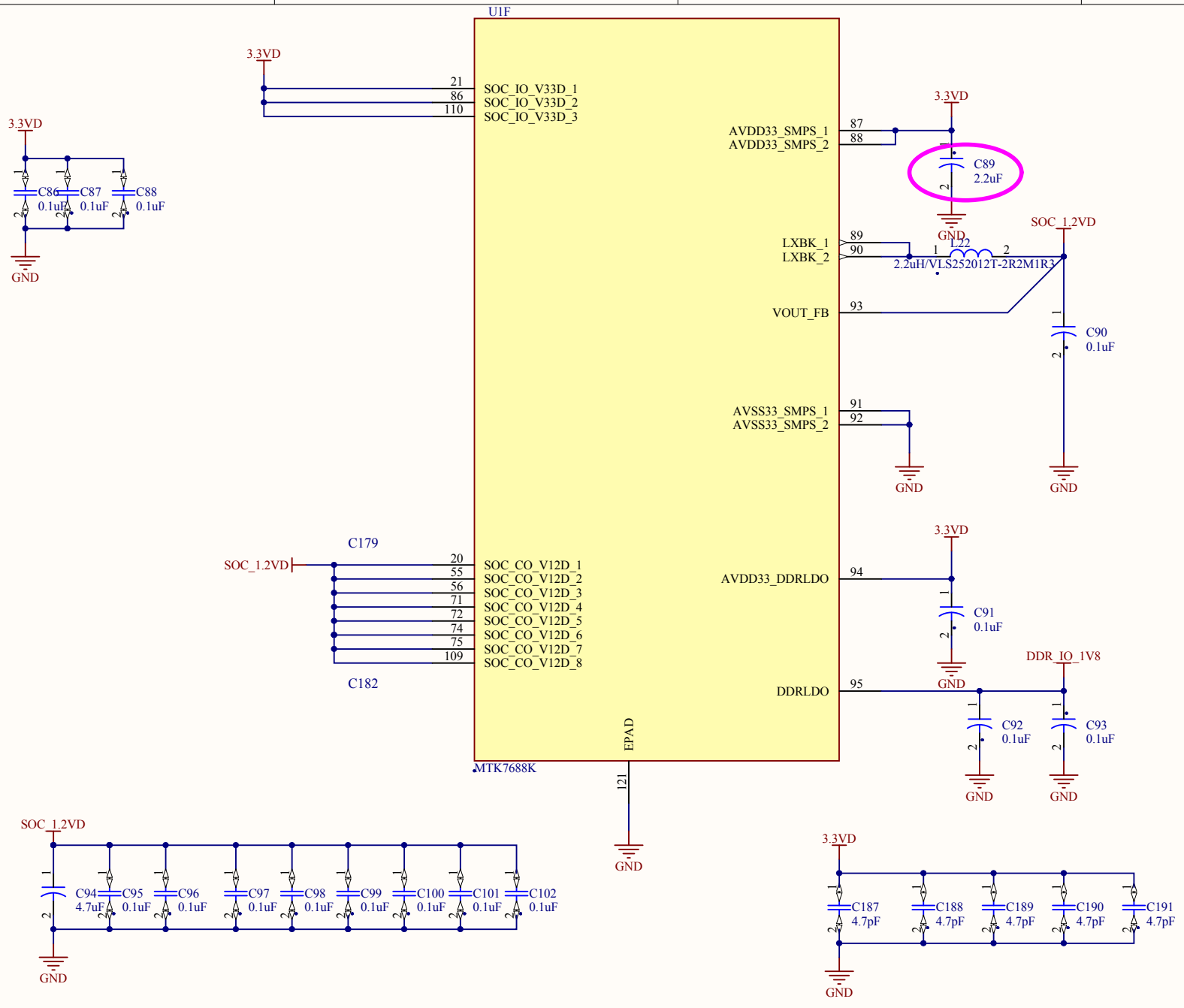

U1B
[MT7628K]
1.8V for DDR1_KGD(Default)
DDR_IO_1V8
66
67
78
79
DDR_IO_1V8D_1
DDR_IO_1V8D_2
DDR_IO_1V8D_3
DDR_IO_1V8D_4
DDR_VREF
73
76
77
DDR_IO_VREF_1
DDR_IO_VREF_2
DDR_IO_VREF_3
C57
0.1uF
C58
0.1uF
GND
GND
DDR_IO_VSS_1
DDR_IO_VSS_2
DDR_IO_VSS_3
61
62
63
GND
MT7688K
DDR_IO_1V8
C59
2.2uF
C60
0.1uF
C61
0.1uF
GND
DDR_IO_1V8
R13
1K 1%
C55
0.1uF
DDR_VREF
DDR_VREF
R14
1K 1%
C56
0.1uF
GND



U1C
SPI_MISO
SPI_MOSI
SPI_CLK
SPI_CS0
SPI_CS1
SR1
22
SFLASH_CLK
UART_TXD1
UART_RXD1
UART_RXD0
UART_TXD0
3.3VD
R96
4.7K
R98
4.7K
R97
4.7K
I2C_SCLK
I2C_SD
GPIO_11
GPIO0
R89
20K
RST
R91
22
CPURST_N
PORST_N
WPS_RST_Button
WDT_RST_N
RC1
4.7uF
GND
I2S_CLK
I2S_WS
I2S_SDI
I2S_SDO
REF_CLK0
I2S_DI
I2S_DO
REF_CLKO
WLED_N
NC_1
NC_2
NC_3
NC_4
NC_5
MT7688K
R47
4.7K
WP
SR2
10K
C103
0.1uF/NI
R48
10K
U4
/CS
VCC
DO
/HOLD
/WP
CLK
GND
DI
HOLD
MX25L6406EM2I-12G

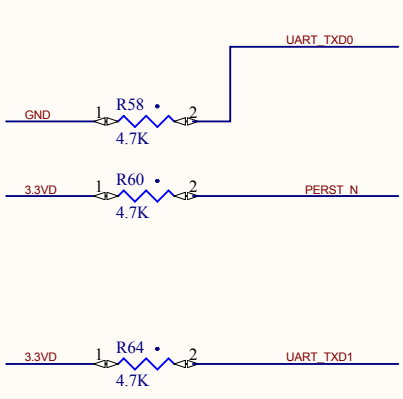

C63
4.7uF
GND
C64
4.7uF
U1D
3.3VD
AVDD12_PCIE
101
SOC_1.2VD
58
AVDD33_USB
AVDD33_PCIE
104
3.3VD
C67
4.7uF
C178
4.7uF
PERST_N
105
PERST_N
PERST_N
PCIE_CKP0
103
PCIE_CKN0
102
GND
R37
5.1K 1%
GND
57
USB_VRT
PCIE_TXP0
97
PCIE_TXN0
96
USB_DP
USB_DM
USB_DP
USB_DM
59
60
USB_DP
USB_DM
PCIE_IO_VSS
PCIE_RXP0
99
PCIE_RXN0
100
MT7688K
98
GND

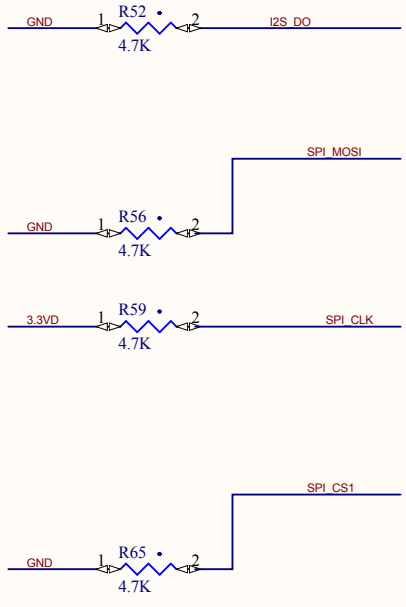

Close to MT7688
U1E
MTK7688K
3.3VD
C171
C73 1uF
C70 0.1uF
GND
AVDD33_TX_P0
AVDD33_COM
AVDD33_TX_P1234_1
AVDD33_TX_P1234_2
MDI_TN_P4
MDI_TP_P4
MDI_RN_P4
MDI_RP_P4
SD_D2
SD_D3
SD_CMD
SD_CLK
MDI_TN_P3
MDI_TP_P3
MDI_RN_P3
MDI_RP_P3
SD_CD
SD_WP
SD_D0
SD_D1
MDI_TN_P2
MDI_TP_P2
MDI_RN_P2
MDI_RP_P2
PWM_CH3
PWM_CH2
PWM_CH1
PWM_CH0
MDI_TN_P1
MDI_TP_P1
MDI_RN_P1
MDI_RP_P1
GPIO_15
GPIO_14
GPIO_17
GPIO_16
R36 24.3K 1%
EPHY_VRT
MDI_TN_P0
MDI_TP_P0
MDI_RN_P0
MDI_RP_P0
TXON0
TXOP0
RXIN0
RXIP0
GPIO_30
GPIO_31
GPIO_32
GPIO_33
LINK0
EPHY_LED4_N_JTRST_N
EPHY_LED3_N_JTCLK
EPHY_LED2_N_JTMS
EPHY_LED1_N_JTDI
EPHY_LED0_N_JTDO
R122 330
D16
WIFI
3.3VD
C133 22uF
C134 22uF
GND
VDD_5V
C120 10uF
C121 0.1uF
U5
VIN
GND
EN
LX
VOUT
RT8009
L1 3.3uH
C122 10uF
C123 0.1uF
3.3VD
GND
PWRLED
D11
PWR
POWERLED
R117 330
3.3VD
P5
I2S_DI
I2S_DO
I2S_WS
I2S_CLK
SPI_MOSI
SPI_CLK
GND
WLED_N
3.3VD
GPIO_30
SPI_MISO
SPI_CS1
USB_DP
USB_DM
GPIO_11
SD_D2
SD_D3
RXIP0
RXIN0
Header 20
P7
I2C_SCLK
I2C_SD
GND
GPIO_33
GPIO_32
GPIO_31
VDD_5V
REF_CLKO
UART_TXD1
WPS_RST_Button
RST
LINK0
UART_RXD1
UART_TXD0
UART_RXD0
PERST_N
TXOP0
TXON0
SD_CMD
SD_CLK
Header 20
P6
SD_D0
SD_D1
SD_CD
SD_WP
PWM_CH3
PWM_CH2
PWM_CH1
PWM_CH0
GPIO_17
GPIO_16
GPIO_15
GPIO_14
Header 12

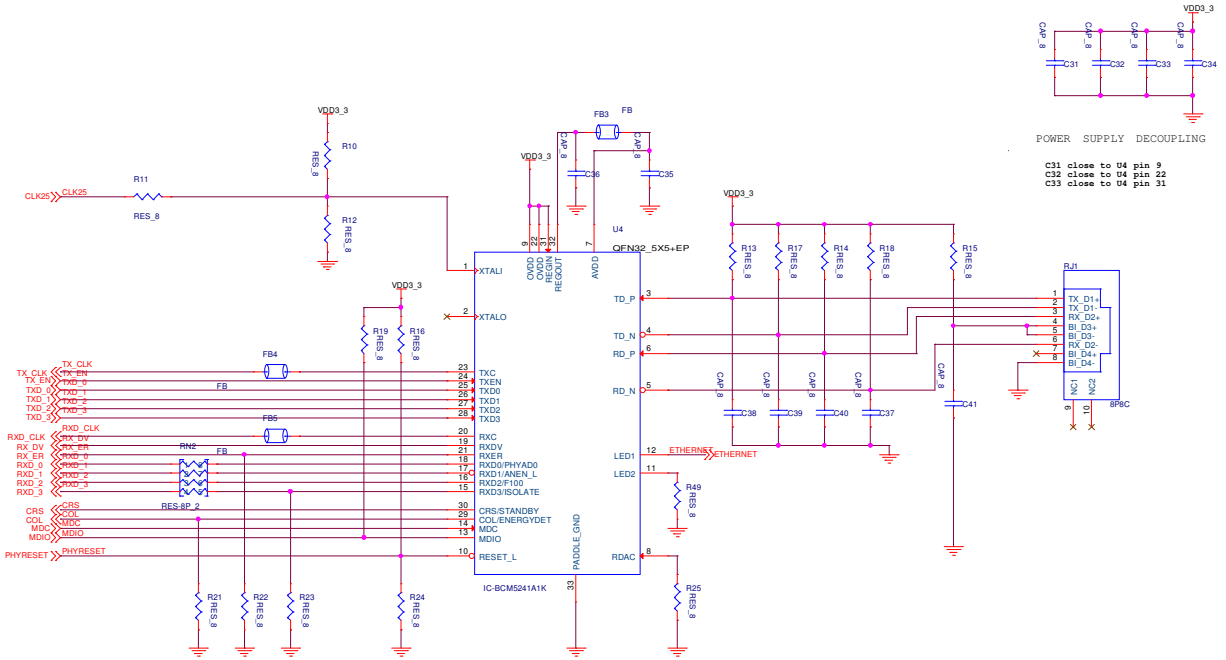

U1F
MTK7688K
3.3VD
SOC_IO_V33D_1
SOC_IO_V33D_2
SOC_IO_V33D_3
21
86
110
C86 0.1uF
C87 0.1uF
C88 0.1uF
GND
AVDD33_SMPS_1
AVDD33_SMPS_2
87
88
C89 2.2uF
LXBK_1
LXBK_2
89
90
L22
2.2uH/VLS252012T-2R2M1R3
SOC_1.2VD
VOUT_FB
93
C90 0.1uF
AVSS33_SMPS_1
AVSS33_SMPS_2
91
92
C179
SOC_1.2VD
SOC_CO_V12D_1
SOC_CO_V12D_2
SOC_CO_V12D_3
SOC_CO_V12D_4
SOC_CO_V12D_5
SOC_CO_V12D_6
SOC_CO_V12D_7
SOC_CO_V12D_8
20
55
56
71
72
74
75
109
C182
AVDD33_DDRLDO
94
C91 0.1uF
DDR_IO_1V8
DDRLDO
95
C92 0.1uF
C93 0.1uF
EPAD
121
C94 4.7uF
C95 0.1uF
C96 0.1uF
C97 0.1uF
C98 0.1uF
C99 0.1uF
C100 0.1uF
C101 0.1uF
C102 0.1uF
C187 4.7pF
C188 4.7pF
C189 4.7pF
C190 4.7pF
C191 4.7pF

Bootstrapping Pins Description

Pin Name	Boot Strapping Signal Name	Description
UART_TXD1	DBG_JTAG_MODE	0: JTAG_MODE 1: EPHY_LED (default)
PERST_N	XTAL_FREQ_SEL	0: 25 MHz DIP 1: 40 MHz SMD
I2S_SDO	DRAM_TYPE	1: DDR1 0: DDR2 [note] This pin is valid for MT7628AN only. It needs to be pull-low for 7628KN which only supports DDR1.
{SPI_MOSI SPI_CLK, SPI_CS1}	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes. 000: Boot from PLL (boot from SPI 3-Byte Addr) 001: Boot from PLL (boot from SPI 4-Byte Addr) 010: Boot from XTAL (boot from SPI 3-Byte Addr) 011: Boot from XTAL (boot from SPI 4-Byte Addr)
PAD_TXD0	EXT_BGCK	1: Test Mode 0: Normal (default)



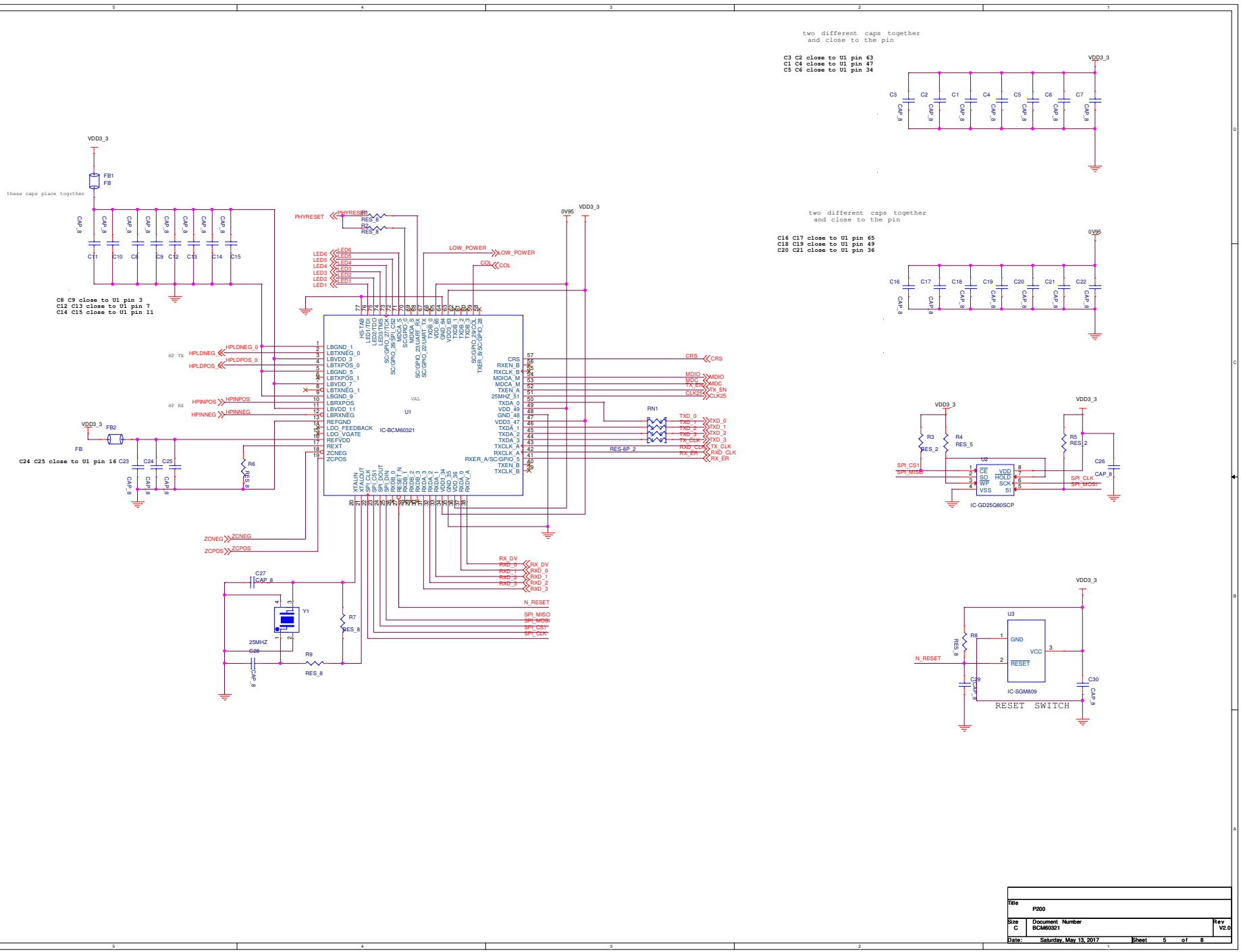




POWER SUPPLY DECOUPLING

C31 close to U4 pin 9
C32 close to U4 pin 22
C33 close to U4 pin 31

Title	P200	
Size C	Document Number BCM5241_PHY	Rev V2.0
Date: Saturday, May 13, 2017	Sheet 5 of 8	



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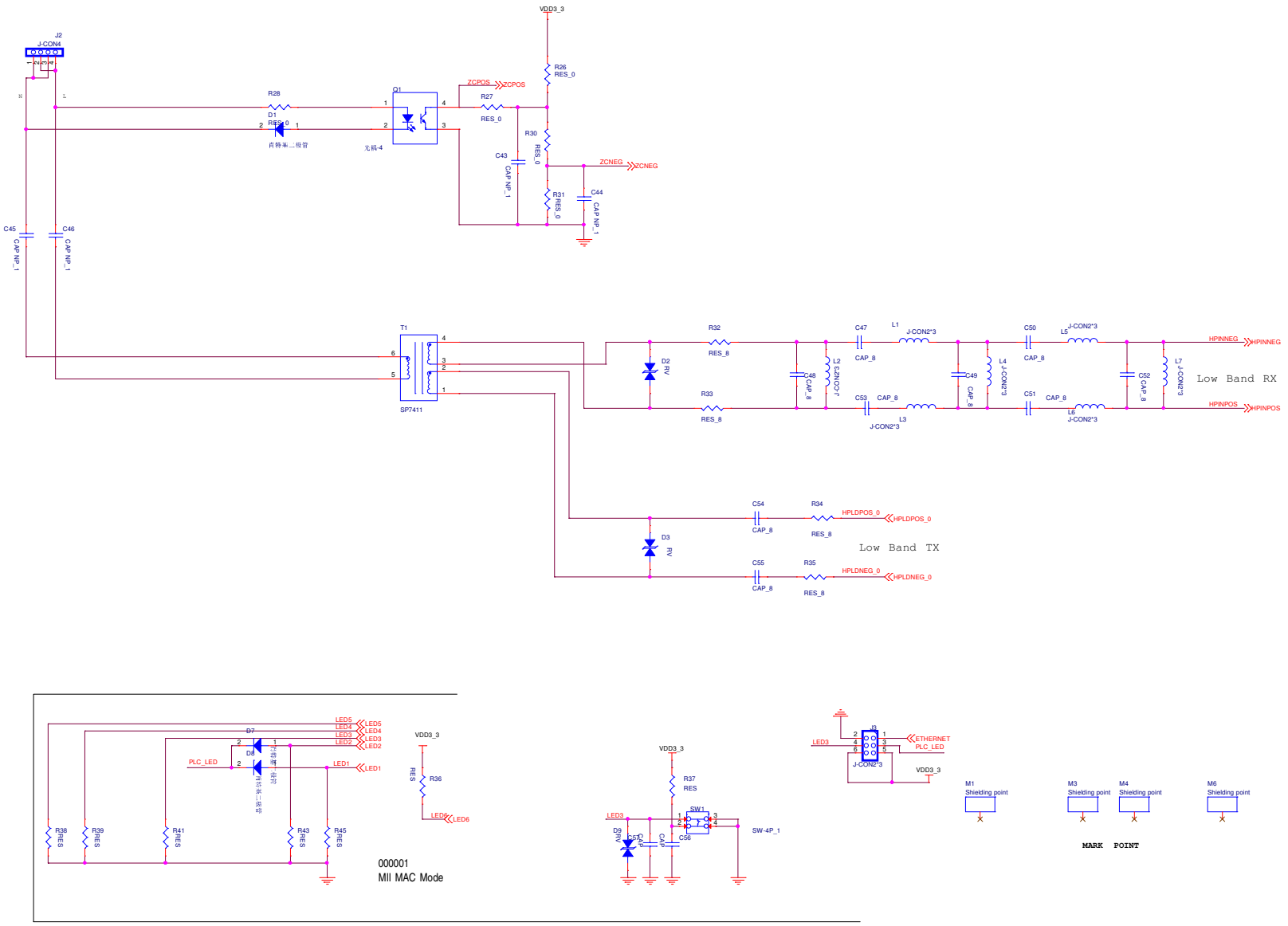
Date: Saturday, May 13, 2017	Sheet 5 of 8	



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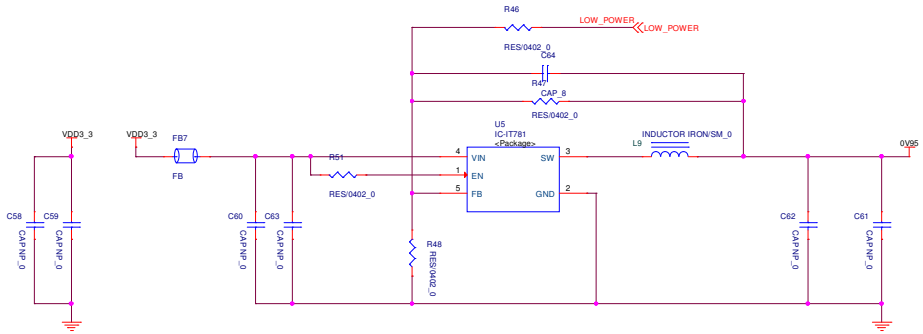
Date: Saturday, May 13, 2017	Sheet 6 of 8	



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