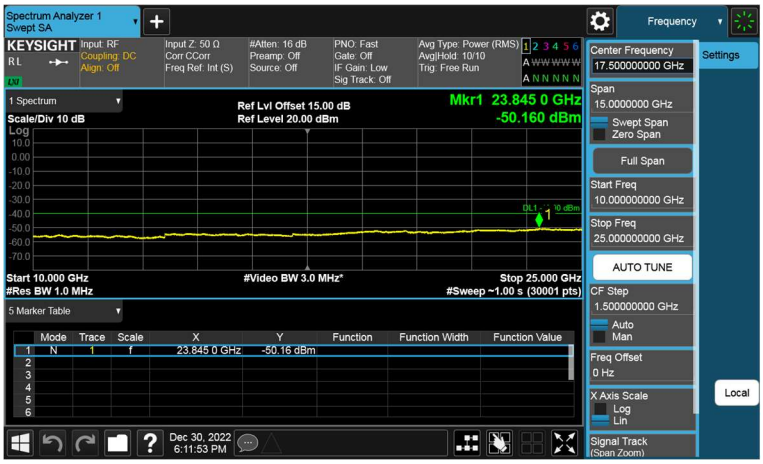
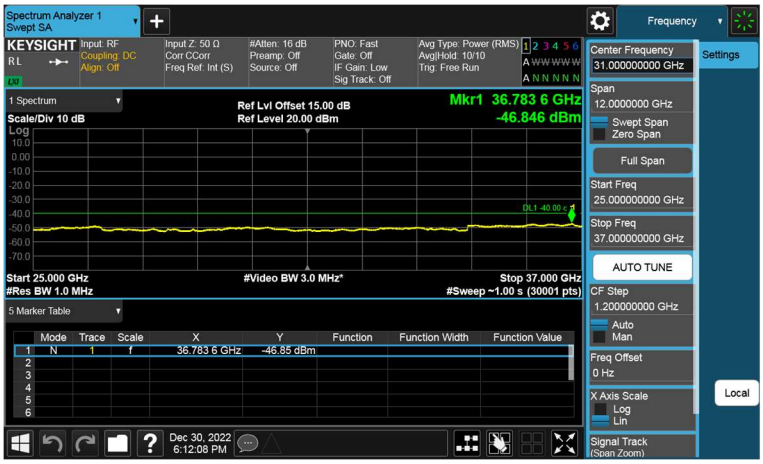
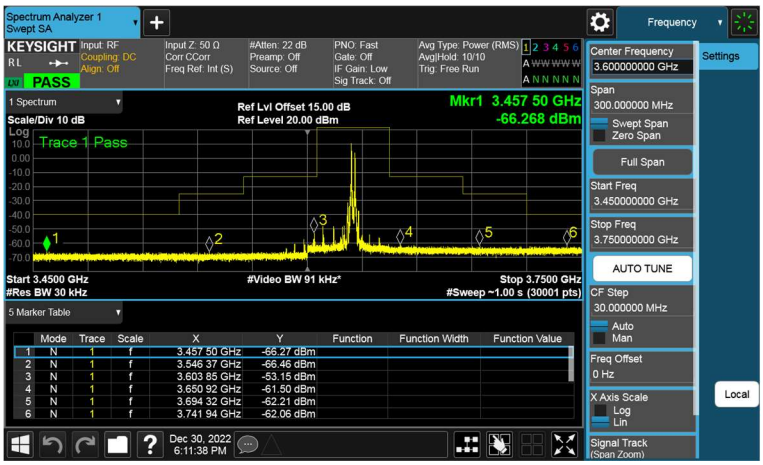
20M_20M_Q16_1RB_CSE2



20M_20M_Q16_1RB_CSE3



20M_20M_Q16_1RB_CSEpart96



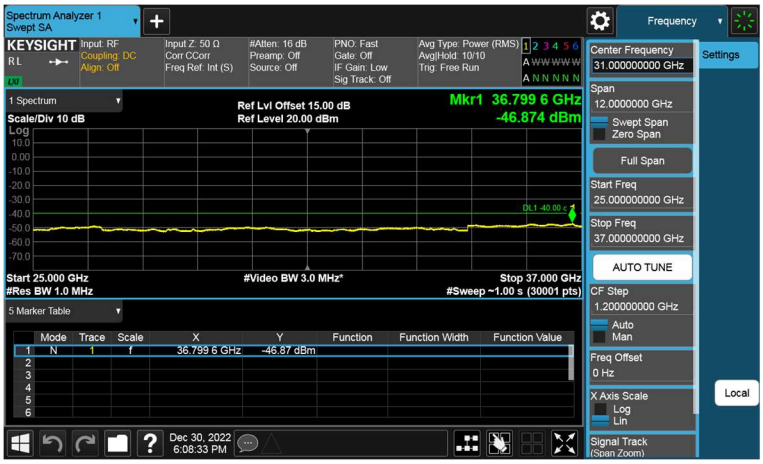
20M_20M_Q16_FULLRB_CSE0a

20M_20M_Q16_FULLRB_CSE0b

20M_20M_Q16_FULLRB_CSE1

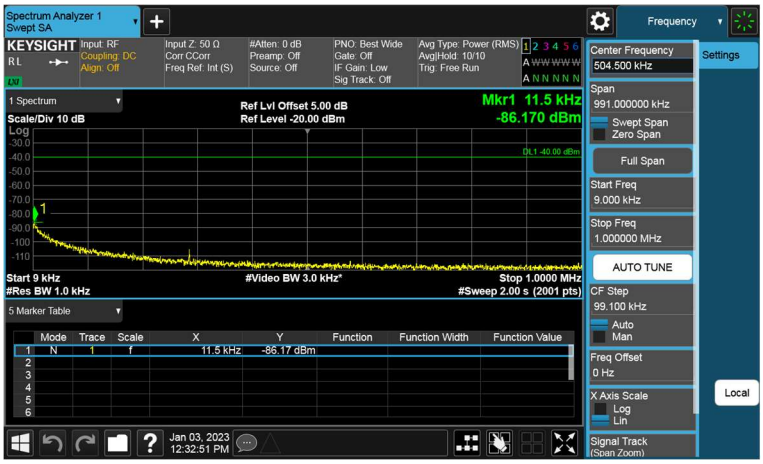
20M_20M_Q16_FULLRB_CSE2

20M_20M_Q16_FULLRB_CSE3



20M_20M_Q16_FULLRB_CSEpart96

20M_20M_Q64_1RB_CSE0a



20M_20M_Q64_1RB_CSE0b

20M_20M_Q64_1RB_CSE1

20M_20M_Q64_1RB_CSE2

20M_20M_Q64_1RB_CSE3

20M_20M_Q64_1RB_CSEpart96

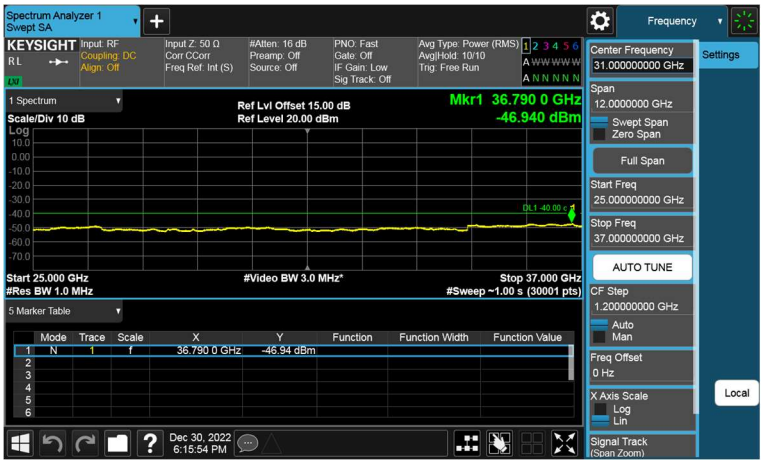
20M_20M_Q64_FULLRB_CSE0a

20M_20M_Q64_FULLRB_CSE0b

20M_20M_Q64_FULLRB_CSE1

20M_20M_Q64_FULLRB_CSE2

20M_20M_Q64_FULLRB_CSE3

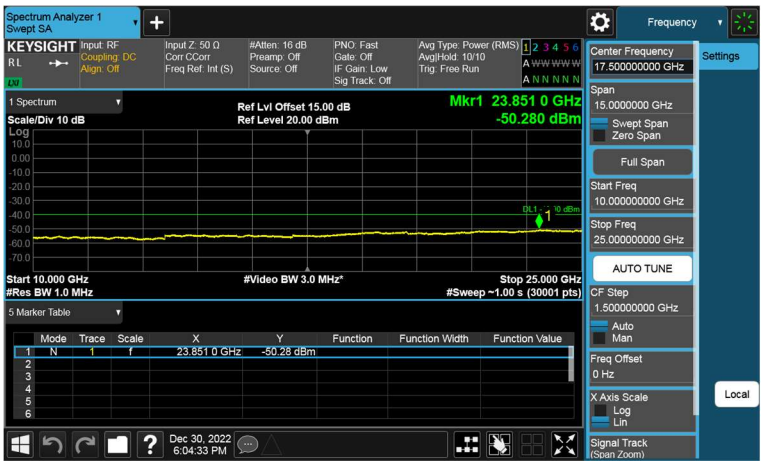


20M_20M_Q64_FULLRB_CSEpart96

20M_20M_QPSK_1RB_CSE0a

20M_20M_QPSK_1RB_CSE1

20M_20M_QPSK_1RB_CSE2



20M_20M_QPSK_1RB_CSE3

20M_20M_QPSK_1RB_CSEpart96

20M_20M_QPSK_1RRB_CSE0b

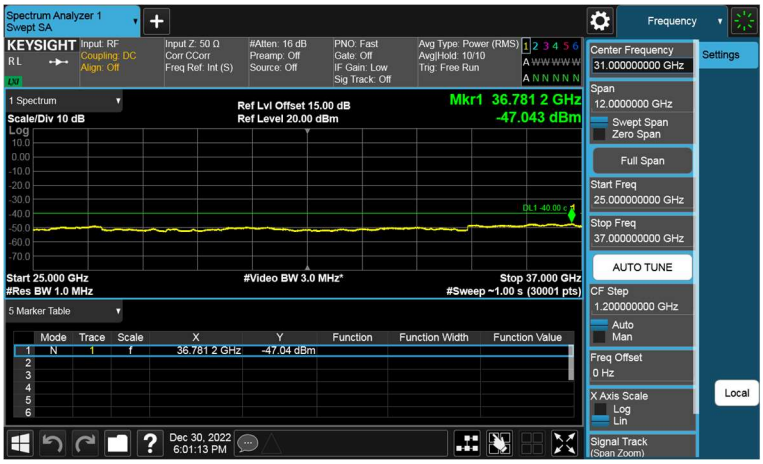
20M_20M_QPSK_FULLRB_CSE0a

20M_20M_QPSK_FULLRB_CSE0b

20M_20M_QPSK_FULLRB_CSE1

20M_20M_QPSK_FULLRB_CSE2

20M_20M_QPSK_FULLRB_CSE3



20M_20M_QPSK_FULLRB_CSEpart96

- End of the Report -