SIM7912&SIM7906 Hardware Design

LTE Module

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Version History

Date	Version	Description of change	Author
2021-07-30	V1.00	Initial release	Hongjun Tu Meng Zhang Wenke Gan
2021-10-28	V1.01	Update SIM7906 module data Update the Power on and Reset data Update the current consumption data Update the ESD data Update the 209 pin definition	Meng Zhang Wenke Gan
2021-12-06	V1.02	Update comment in PCIe	Meng Zhang
2022-03-07	V1.03	Exchanged LTE band B29&B30 to B28&B40 for SIM7912A&SIM7906A.	Wenke Gan
2023-05-07	V1.04	For SIM7912A adds LTE B48 For SIM7906A adds LTE B48	Wenke Gan

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1 Introduction

This document describes the electronic specifications, RF specifications, interfaces, mechanical characteristics and test results of the SIM7912 and SIM7906 module. With the help of this document，customers can quickly understand SIM7912 and SIM7906 module.

Associated with other software application notes and user guides, customers can use module to easily design and develop application products.

1.1 Product Outline

Aimed at the global market, SIM7912 is the LTE Cat 12 module and SIM7906 is the LTE Cat 6, which are supports wireless communication modes of LTE-TDD/LTE-FDD/HSPA+. SIM7912 supports DL 3CA or 2CA and SIM7906 supports DL 2CA only. The supported radio frequency bands are described in the **Table 1: SIM7912 frequency bands**.

Table 1: SIM7912 frequency bands

Network Type		SIM7912A	SIM7912E
LTE-FDD (with Rx-diversity)		B2/B4/B5/B7/B12/B13/B14/B17/B25/B26/B66/B71	B1/B3/B5/B7/B8/B20/B28/B32
LTE-TDD (with Rx-diversity)		B41/B48	B34/B38/B39/B40/B41/B43*/B46 */ B48*
CA	DL 3CA	B2+B4+B5/B13/B71;B2+B5+B66;B2+B13+B66;B2+B7+B12/B66;B4+B7+B12;B2+B2+B5/B12/B13/B66;B5+B5+B2/B66;B7+B7+B2/B4/B5;B66+B66+B2/B5/B13/B66;B41+B41+B25/B26/B41;	B1+B3+B3/B5/B7/B8/B20/B28/B38/B41;B1+B40+B40;B1+B41+B41;B1+B7+B20;B3+B3+B7/B20/B28;B3+B7+B7/B8/B20/B28;B3+B40+B40; B3+B41+B41;B7+B7+B20/B28;B40+B40+B40;B41+B41+B41
	DL 2CA	B12+B12/B25/B46*/B66;B13+B46*/B48*/B66;B14+B66;B19+B42*;B25+B25/B26/B41/B46*;B26+B41/B46*;B28+B40/B41/46*;B2+B2/B4/B5/B7/B12/B13/B28/B46*/B48*/B66/B71;B40+B40；B41+B41/B5/B7/B12/B13/B28/B46*/B71;B5+B5/B7/B12/B25/B4	B1+B1/B3/B5/B7/B8/B20/B28*/B38*/B40*/B41* B3+B3/B5/B7/B8/B20/B28/B38*/B40*/B41* B7+B5/B7/B8*/B20/B28;B20+B32/B38/B40; B38+B38;B40+B40;B41+B41;B48+B48*;

		0/B41B/46*/B48*/B66;B66+B66/B71;B7+B7/B12/B28/B46*;	
WCDMA		B2/B4/B5	B1/B3/B5/B8
GNSS		GPS/Galileo/GLONASS/BeiDou	GPS/Galileo/GLONASS/BeiDou

Table 2: SIM7906 frequency bands

Network Type		SIM7906A	SIM7906E
LTE-FDD (with Rx-diversity)		B2/B4/B5/B7/B12/B13/B14/B17/B25/B26/B28/B66/B71	B1/B3/B5/B7/B8/B20/B28/B32
LTE-TDD (with Rx-diversity)		B40/B41/B43*/B46*/B48	B34/B38/B39/B40/B41/B43*/B46*/B48
CA	**DL 2CA**	B12+B12/B25/B46*/B66;B13+B46*/B48*/B66;B14+B66;B19;B25+B25/B26/B41/B46*;B26+B41/B46*;B28+B4 0/B41/46*;B2+B2/B4/B5/B7/B12/B13/B28/B46*/B48*/B66/B71;B40+B4 0；B41+B41/B4+B4/B5/B7/B12/B13/B28/B46*/B71;B5+B5/B7/B12/B25/B4 0/B41B/46*/B48*/B66;B66+B66/B71;B 7+B7/B12/B28/B46*;	B1+B1/B3/B5/B7/B8/B20/B28*/B38*/B40*/B41* B3+B3/B5/B7/B8/B20/B28/B38*/B40*/B41* B7+B5/B7/B8*/B20/B28;B20+B32/B38/B40; B38+B38;B40+B40;B41+B41;B48+B48*;
WCDMA		B2/B4/B5	B1/B3/B5/B8
GNSS		GPS/Galileo/GLONASS/BeiDou	GPS/Galileo/GLONASS/BeiDou

NOTE

1. GNSS function is optional.
2. “*” function is optional.

With a physical dimension of 39.5mm * 37.0mm * 2.8mm, module can meet almost all requirements for M2M applications.

SIM7912 and SIM7906 are an SMD type module and can be embedded in applications through its 300 LGA pins

With the 300 LGA pins, module owns rich interfaces, includes USB2.0/USB3.0, PCIe, SDIO (SD Card), SIM card, digital audio (I2S or PCM), ADCs, I2C, UART, GPIOs, five antennas for 3G/4G and GNSS.

1.2 Hardware Block Diagram

The block diagram of SIM7912&SIM7906 is shown in the following figure.

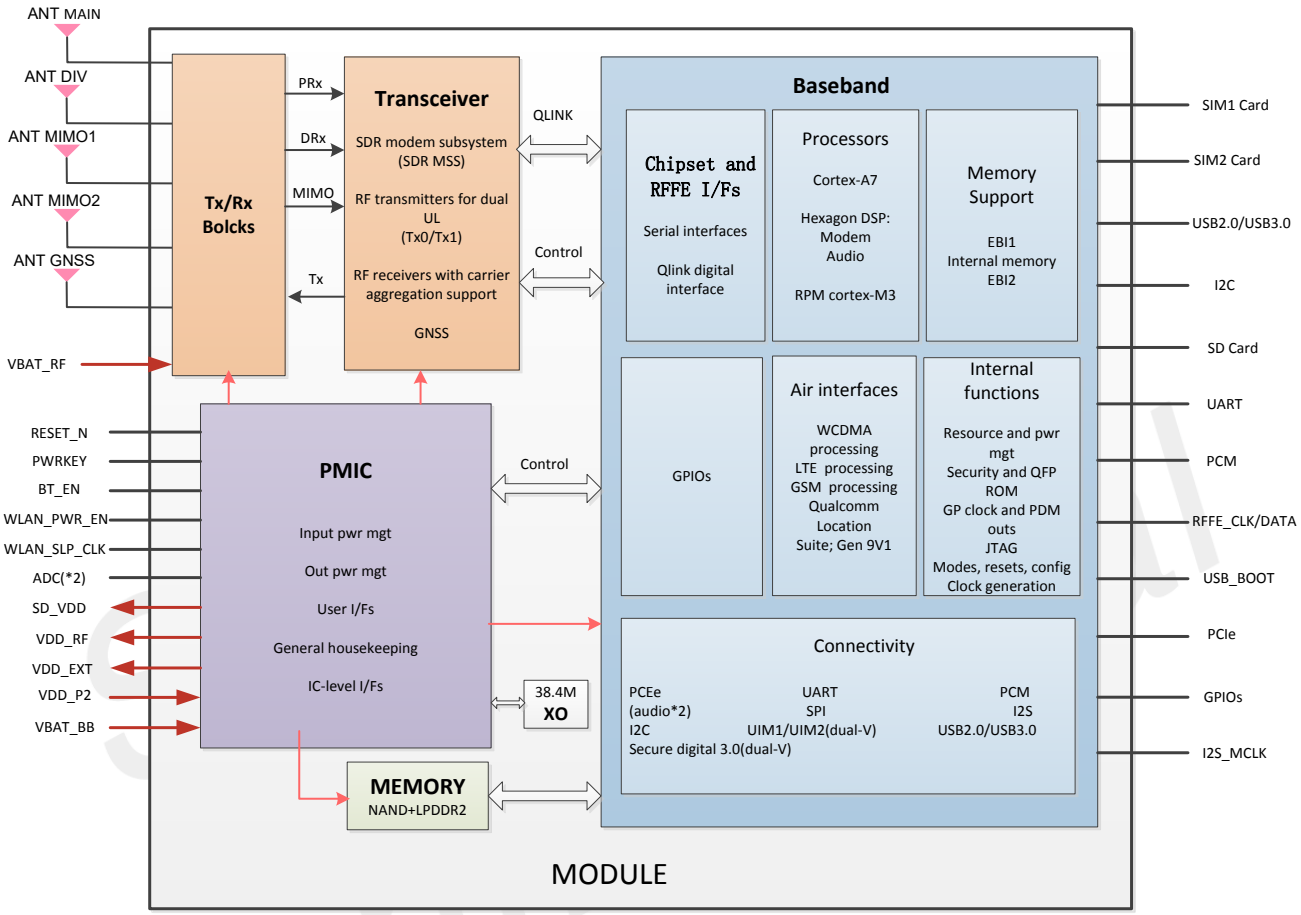

Figure 1: SIM7912&SIM7906 module block diagram

1.3 Feature Overview

Table 3: Key features

Feature	Implementation
Power supply	● VBAT:3.3V～4.3V ● Typical: 3.8V
Transmit power	● Class 3 (23dBm±2dB) for LTE-TDD bands ● Class 3 (23dBm±2dB) for LTE-FDD bands ● Class 3 (24dBm+1/-3dB) for WCDMA bands
LTE Features	● Support FDD/TDD LTE Category 12 with CA and MIMO ● Support uplink QPSK and 16-QAM and **64-QAM modulation

	● Support downlink QPSK, 16-QAM and 64-QAM and **256-QAM modulation ● Support 1.4MHz to 60MHz (3×CA) RF bandwidth ● Support 4×4 MIMO in DL direction ● FDD: Max 600Mbps (DL)/150Mbps (UL) ● TDD: Max 430Mbps (DL)/90Mbps (UL)
Antenna	● Main antenna interface (ANT_MAIN) ● Rx-diversity antenna interface (ANT_DIV) ● MIMO antenna interfaces (ANT_MIMO1, ANT_MIMO2) ● GNSS antenna interface (ANT_GNSS)
Network Indication	● Two pins (NET_MODE and NET_STATUS) to indicate network connectivity status
GNSS Features	● GNSS engine: GPS/GLONASS/BeiDou/Galileo ● Protocol: NMEA
SMS	● Text and PDU mode ● Point to point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
SIM interface	● Support identity card: 1.8V/ 3.0V ● Include SIM1 and SIM2 interfaces ● Support Dual SIM single standby
PCIe interface	● Comply with PCI Express Specification Revision 2.1 and support 5Gbps per lane ● Used for data transmission
UART interface	● Support up to three UART ● Data rate up to 4 Mbps
I2C interface	● Support I2C ● Data rate up to 400 Kbps
PCM interface	● Used for audio function with external codec ● Support 16-bit linear data format ● Support long frame synchronization and short frame synchronization ● Support master and slave modes, but must be the master in long frame synchronization
SDIO interface	● Support 4bit SD card or 4bit eMMC, meet SDIO3.0 specification ● 1.8V or 3.0V dual-voltage operation for SD card ● Data rate up to 200Mbps
USB interface	● Comply with USB 3.0 and 2.0 specifications, with maximum transmission rates up to 5Gbps on USB 3.0 and 480Mbps on USB 2.0 ● Used for AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentence output, and voice over USB* ● Support USB serial drivers for: Windows 7/8/8.1/10; Linux 2.6/3.x/4.1~4.15; ● Android 4.x/5.x/6.x/7.x/8.x/9.x
Firmware upgrade	● Firmware upgrade over USB2.0 interface
Physical characteristics	● Size: 39.5mm*37mm*2.8mm ● Weight: Almost 8.38 g

Temperature range	● Normal operation temperature: -30°C to +75°C ● Extended operation temperature: -40°C to +85°C ● Storage temperature: -40°C to +90°C
RoHS	● All hardware components are fully compliant with EU RoHS directive

NOTE

1. “*” means under development.
2. “**” means SIM7912 supported，SIM7906 unsupported.

2 Package Information

2.1 Pin Assignment Overview

The following figure shows the pin assignment of SIM7912&SIM7906.

SIM7912&SIM7906

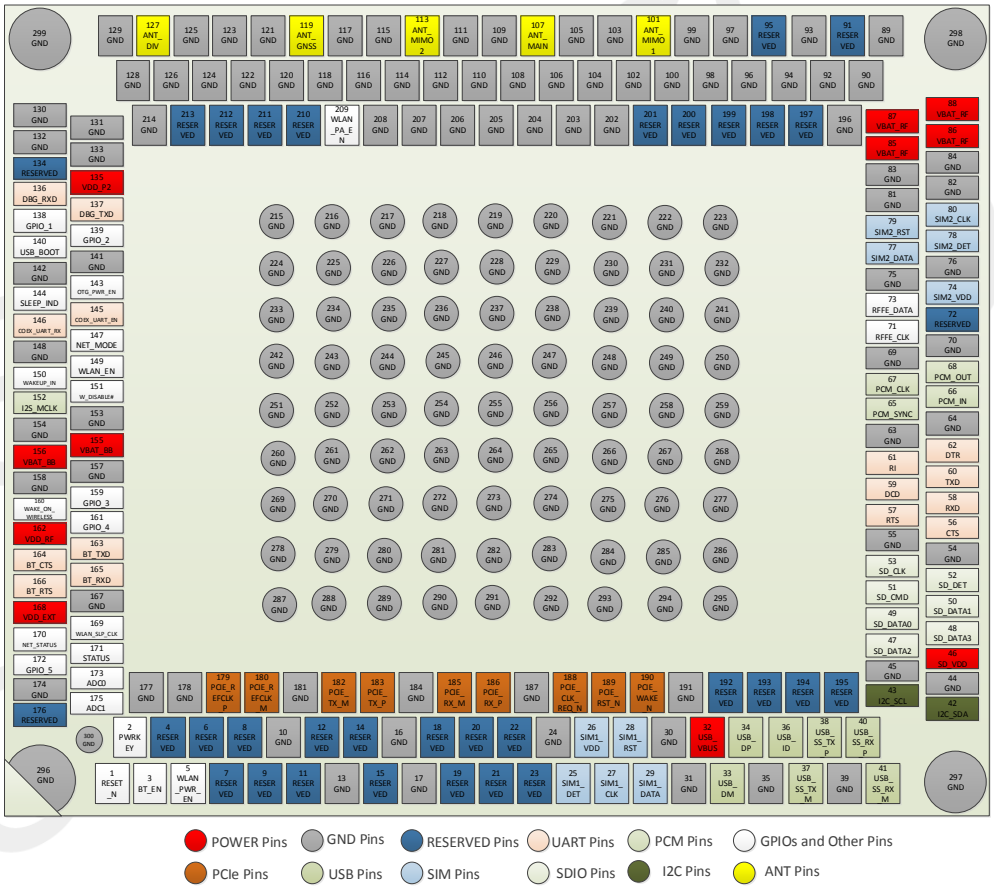

Figure 2: Pin assignment

NOTE

1. Keep all RESERVED pins and unused pins unconnected.
2. GND pins 215~299 should be connected to ground in the design.

2.2 Pin Description

Table 4: IO parameters definition

Pin type	Description
PI	Power Input
PO	Power Output
AI	Analog Input
AIO	Analog Input /Output
DIO	Bidirectional Digital Input /Output
DI	Digital Input
DO	Digital Output
PU	Pull Up
PD	Pull Down
OD	Open Drain

Table 5: DC parameters definition

Voltage domain	Parameter		Min	Typ	Max
P2	VDD_P2=1.8V				
	V_{OH}	High level output	1.4V	-	-
	V_{OL}	Low level output	0V	-	0.45V
	V_{IH}	High level input	1.3V	-	2V
	V_{IL}	Low level input	0.3V	-	0.58V
	VDD_P2=3.0V				
	V_{OH}	High level output	2.15V	-	-
	V_{OL}	Low level output	0V	-	0.35V
	V_{IH}	High level input	1.8V	-	3.15V
	V_{IL}	Low level input	0.3V	-	0.7V
P3	VDD_P3=1.8V				
	V_{OH}	High level output	1.35V	-	1.8V
	V_{OL}	Low level output	0V	-	0.45V

	V_{IH}	High level input	1.3V		2.1V
	V_{IL}	Low level input	0.3V	-	0.5V
P4/P5	VDD_P4/P5=1.8V				
	V_{OH}	High level output	1.45V	-	1.8V
	V_{OL}	Low level output	0V	-	0.4V
	V_{IH}	High level input	1.26V	-	2.1V
	V_{IL}	Low level input	0V	-	0.36V
	VDD_P4/P5=3.0V				
	V_{OH}	High level output	2.4V	-	3V
	V_{OL}	Low level output	0V	-	0.4V
	V_{IH}	High level input	2.1V	-	3.05V
	V_{IL}	Low level input	0V	-	0.57V

Table 6: Pin description

Power supply					
Pin name	**Pin No.**	**Electrical description**		**Description**	**Comment**
VBAT_BB	155, 156	PI	V_{MAX}=4.3V V_{TYP} =3.8V V_{MIN}=3.3V	Input power supply for module's BB part	It must be provided with sufficient current up to 1.0A.
VBAT_RF	85,86, 87, 88	PI	V_{MAX}=4.3V V_{TYP} =3.8V V_{MIN}=3.3V	Input power supply for module's RF part	It must be provided with sufficient current up to 1.5A in a transmitting burst.
VDD_P2	135	PI	VDD_P2 =SD_VDD or VDD_P2 =VDD_EXT	SD card power supply	If an SD card is used, connect VDD_P2 to SD_VDD. If an eMMC* is used or SDIO interface is unused, connect VDD_P2 to VDD_EXT.
VDD_EXT	168	PO	V_{TYP} =1.8V	Provide 1.8V for external circuit.	Iomax=50mA
VDD_RF	162	PO	V_{TYP} =2.85V	Provide 2.85V for external RF circuit.	Iomax=120mA
GND	10, 13, 16, 17, 24, 30, 31, 35, 39, 44, 45, 54, 55, 63, 64, 69, 70, 75, 76, 81, 82, 83, 84, 89, 90, 92, 93, 94, 96, 97, 98, 99, 100, 102, 103, 104, 105, 106, 108, 109, 110, 111, 112, 114, 115, 116, 117, 118, 120, 121, 122, 123, 124, 125, 126, 128, 129, 130, 131, 132, 133, 141, 142, 148, 153, 154, 157, 158, 167, 174, 177, 178, 181, 184, 187, 191, 196, 202~208, 214~299				Ground
Turn on/off					

Pin name	Pin No.	Electrical description		Description	Comment
RESIN_N	1	DI,PU	P3	Reset the module, active low	1.8V power domain. Pulled up internally. Active low.
PWRKEY	2	DI,PU	P3	Power on/off the module, active low	1.8V power domain. Pulled up internally. Active low.
Status indication					
Pin name	**Pin No.**	**Electrical description**		**Description**	**Comment**
NET_MODE	147	DO	P3	Indicate the module's network registration mode	1.8V power domain. If unused, keep it open.
NET_STATUS	170	DO	P3	Indicate the module's network activity status	1.8V power domain. If unused, keep it open.
STATUS	171	DO	P3	Indicate the module's operation status	1.8V power domain. If unused, keep it open.
USB interface					
Pin name	**Pin No.**	**Electrical description**		**Description**	**Comment**
USB_VBUS	32	PI	V_{MAX}=5.25V V_{MIN}=3.3V	USB VBUS detection	Not support charge
USB_ DP	34	AIO		Differential USB bi-directional data plus	Required 90Ω differential impedance Compliant with USB 2.0 standard specifications
USB_ DM	33	AIO		Differential USB bi-directional data minus	
USB_SS_TX_P	38	AO		USB3.0 super-speed transmit data plus	Required 90Ω differential Impedance Compliant with USB 3.0 standard specifications
USB_SS_TX_M	37	AO		USB3.0 super-speed transmit data minus	
USB_SS_RX_P	40	AI		USB3.0 super-speed receive data plus	
USB_SS_RX_M	41	AI		USB3.0 super-speed receive data minus	
USB_ID	36	DI	P3	OTG identification	1.8V power domain. If unused, keep it open.
OTG_PWR_EN	143	DO,PD	P3	USB OTG power supply DC-DC enable signal	1.8V power domain. If unused, keep it open.
SIM interface					
Pin name	**Pin No.**	**Electrical description**		**Description**	**Comment**
SIM1_VDD	26	PO	**For 1.8V SIM:**	Power supply for SIM1 card	Either 1.8V or 3.0V is supported by the module

			V_{MAX}=1.9V V_{MIN}=1.7V **For 3.0V SIM:** V_{MAX}=3.05V V_{MIN}=2.75V		automatically. If unused, please keep open
SIM1_DATA	29	DIO	P4	SIM1 card data signal, which has been pulled up to SIM1_VDD by a 20K resistor internally	
SIM1_CLK	27	DO	P4	SIM1 clock signal	
SIM1_RST	28	DO	P4	SIM1 reset signal	
SIM1_DET	25	DI	P3	SIM1 card detect signal, which need pulled up to VDD_EXT by a 470K resistor externally	
SIM2_VDD	74	PO	**For 1.8V SIM:** V_{MAX}=1.9V V_{MIN}=1.7V **For 3.0V SIM:** V_{MAX}=3.05V V_{MIN}=2.75V	Power supply for SIM2 card	
SIM2_DATA	77	DIO	P4	SIM2 card data, which has been pulled up to SIM2_VDD by a 20K resistor internally	
SIM2_CLK	80	DO	P4	SIM2 clock signal	
SIM2_RST	79	DO	P4	SIM2 reset signal	
SIM2_DET	78	DI	P3	SIM2 card detect, which need pulled up to VDD_EXT by a 470KR resistor externally	
SPI interface					
Pin name	**Pin No.**	**Electrical description**		**Description**	**Comment**
SPI_CS_N		DO	P3	SPI chip select	
SPI_CLK		DO	P3	SPI clock	
SPI_MOSI		DO	P3	Master output slaver input	
SPI_MISO		DI	P3	Master input slaver output	
Main UART interface					

Pin name	Pin No.	Electrical description		Description	Comment
CTS	56	DO	P3	Clear to send	1.8V power domain. If unused, keep it open. Default use for AT command
RTS	57	DI	P3	Request to send	
RXD	58	DI	P3	Receive data	
DCD	59	DO	P3	Data Carrier detect	
TXD	60	DO	P3	Transmit data	
RI	61	DO	P3	Ring indicator	
DTR	62	DI	P3	Data terminal ready, sleep mode control: Pulled up by default. Pulling down to low level will wake up the module.	

BT interface*					
Pin name	**Pin No.**	**Electrical description**		**Description**	**Comment**
BT_EN	3	DO	P3	BT function enable control	1.8V power domain. If unused, keep it open.
BT _TXD	163	DO	P3	Transmit data	1.8V power domain. If unused, keep it open. BT UART interface pin by default. Can be multiplexed into SPI_MOSI.
BT _CTS	164	DO	P3	Clear to send	1.8V power domain. If unused, keep it open. BT UART interface pin by default. Can be multiplexed into SPI_CLK.
BT_RXD	165	DI	P3	Receive data	1.8V power domain. If unused, keep it open. BT UART interface pin by default. Can be multiplexed into SPI_MISO.
BT _RTS	166	DI	P3	Request to send	1.8V power domain. If unused, keep it open. BT UART interface pin by default. Can be multiplexed into SPI_CS.

Debug UART interface					
Pin name	**Pin No.**	**Electrical description**		**Description**	**Comment**

DBG_ RXD	136	DI	P3	Receive data	1.8V power domain. If unused, keep it open.
DBG_ TXD	137	DO	P3	Transmit data	

PCM & I2C interface					
Pin name	**Pin No.**	**Electrical description**		**Description**	**Comment**
I2C_SCL	43	OD		I2C clock signal	1.8V power domain. An external pull-up resistor is required. If unused, keep it open.
I2C_SDA	42	OD		I2C data signal	
PCM_SYNC	65	DIO	P3	PCM synchronous signal	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_IN	66	DI	P3	PCM data input	1.8V power domain. If unused, keep it open.
PCM_CLK	67	DO	P3	PCM clock output	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_OUT	68	DO	P3	PCM data output	1.8V power domain. If unused, keep it open.
I2S_MCLK	152	DO	P3	I2S master clock output	Provide a digital clock output for an external audio codec. If unused, keep it open.

ADC interface					
Pin name	**Pin No.**	**Electrical description**		**Description**	**Comment**
ADC0	173	AI	1.875V	Analog to digital converter input0	If unused, keep it open.
ADC1	175	AI	1.875V	Analog to digital converter input1	If unused, keep it open.

PCIe interface					
Pin name	**Pin No.**	**Electrical description**		**Description**	**Comment**
PCIe_REF CLK_P	179	AIO		PCIe reference clock plus	Required 90Ω differential impedance
PCIe_REF CLK_M	180	AIO		PCIe reference clock minus	
PCIe_TX_M	182	AO		PCIe transmit minus	

PCIe_TX_P	183	AO		PCIe transmit plus	
PCIe_RX_M	185	AI		PCIe receive minus	
PCIe_RX_P	186	AI		PCIe receive plus	
PCIe_CLK_REQ_N	188	DI	P3	PCIe clock request	In master mode, it is an input signal. In slave mode, it is an output signal. If unused, keep it open.
PCIe_WAKE	190	DI	P3	PCIe wake-up	In master mode, it is an input signal. In slave mode, it is an output signal. If unused, keep it open.
PCIe_RST	189	DO	P3	PCIe reset	In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.

WLAN Control interface*

Pin name	Pin No.	Electrical description		Description	Comment
WLAN_PWR_EN	5	DO	P3	WLAN power supply enable control	1.8V power domain. If unused, keep it open.
COEX_UART_TX	145	DO	P3	LTE/WLAN coexistence signal	1.8V power domain. If unused, keep it open.
COEX_UART_RX	146	DI	P3	LTE/WLAN coexistence signal	1.8V power domain. If unused, keep it open.
WLAN_EN	149	DO	P3	WLAN function enable control	1.8V power domain. Active high. If unused, keep it open.
WAKE_ON_WIRELESS	160	DI	P3	Wake up module by an external Wi-Fi module	1.8V power domain. Active low. If unused, keep it open.
WLAN_SLP_CLK	169	DO	P3	WLAN sleep clock	If unused, keep it open.

SDIO interface

Pin name	Pin No.	Electrical description		Description	Comment
SD_VDD	46	PO	1.8/3.0V	**SD card application**: SDIO pull up power source. Connected it to VDD_P2. **eMMC application**: Keep it open when used for eMMC	

SD_DATA0	49	DIO	P2	SDC data bit 0 or eMMC* data bit 0	Required 50Ω impedance If unused, keep it open.
SD_DATA1	50	DIO	P2	SDC data bit 1 or eMMC data bit 1	
SD_DATA2	47	DIO	P2	SDC data bit 2 or eMMC data bit 2	
SD_DATA3	48	DIO	P2	SDC data bit 3 or eMMC data bit 3	
SD_CMD	51	DIO	P2	SDC command output	
SD_CLK	53	DO	P2	SDC clock output	
SD_DET	52	DI,PU	P3	SD card insertion detection	1.8V power domain, If unused, keep it open.

Other interface

Pin name	Pin No.	Electrical description		Description	Comment
GPIO_1	138	IO,PD	P3	General purpose input/output ports	1.8V power domain, If unused, keep it open.
GPIO_2	139	IO,PU	P3		
GPIO_3	159	IO,PD	P3		
GPIO_4	161	IO,PD	P3		
GPIO_5	172	IO,PD	P3		
USB_BOOT	140	DI	P3	Force the module into emergency download mode	1.8V power domain. Active high. If unused, keep it open.
SLEEP_IND	144	DO	P3	Sleep indication	1.8V power domain, If unused, keep it open.
WAKEUP_IN	150	DI,PU	P3	Sleep mode control	1.8V power domain. Pulled up by default. Low level wakes up the module. If unused, keep it open.
W_DISABLE#	151	DI,PU	P3	Airplane mode control	1.8V power domain. Pulled up by default. In low voltage level, the module will enter airplane mode. If unused, keep it open.
WLAN_PA_EN	209	DI,PD	P3	WLAN PA Enable	Default in LTE mode, Pull-down to the GND. Can switch to WLAN mode.

Antenna Tuner control interface

Pin name	Pin No.	Electrical description		Description	Comment
RFFE_CLK	71	DO	P3	RFFE serial interface for	1.8V power domain,

RFFE_DATA	73	DIO	P3	external tuner control	If unused, keep it open.
Antenna interface					
Pin name	**Pin No.**	**Electrical description**		**Description**	**Comment**
ANT_MAIN	107	AIO		Main antenna interface supporting all bands	50Ω impedance
ANT_DIV	127	AI		RXD antenna interface supporting all bands	50Ω impedance If unused, keep them open.
ANT_ MIMO1	101	AI		4×4 MIMO antenna interface supporting all bands	50Ω impedance If unused, keep them open.
ANT_MIMO2	113	AI		4×4 MIMO antenna interface supporting all bands	50Ω impedance If unused, keep them open.
ANT_GNSS	119	AI		GNSS antenna interface	50Ω impedance If unused, keep them open.
RESERVED interface					
RESERVED	4, 6~9, 11, 12, 14, 15, 18, 19, 20, 21, 22, 23, 72, 91, 95, 134, 176, 192, 193, 194, 195, 197, 198, 199, 200, 201, 210, 211, 212, 213, 300			Reserved for future use	Keep these pins unconnected.

NOTE

1. "*" means under development.
2. The I2C signals need pull up to VDD_EXT by 2.2K resistors out of the module.
3. If not use SDIO function, the VDD_P2 pin should connect to VDD_EXT pin out of the module.
4. Do not pull up USB_BOOT during normal power up.
5. Unused and RESERVED pins should keep open.
6. Recommend ESD protect components out of the module for used interfaces.
7. All GND pins should be connected to the customer's main PCB.
8. GPIO2 will become low level when the module starts up.
9. Pin 209 in V1.01 module is reserved.

2.3 Mechanical Dimensions

The following figure shows the mechanical dimensions of SIM7912&SIM7906.

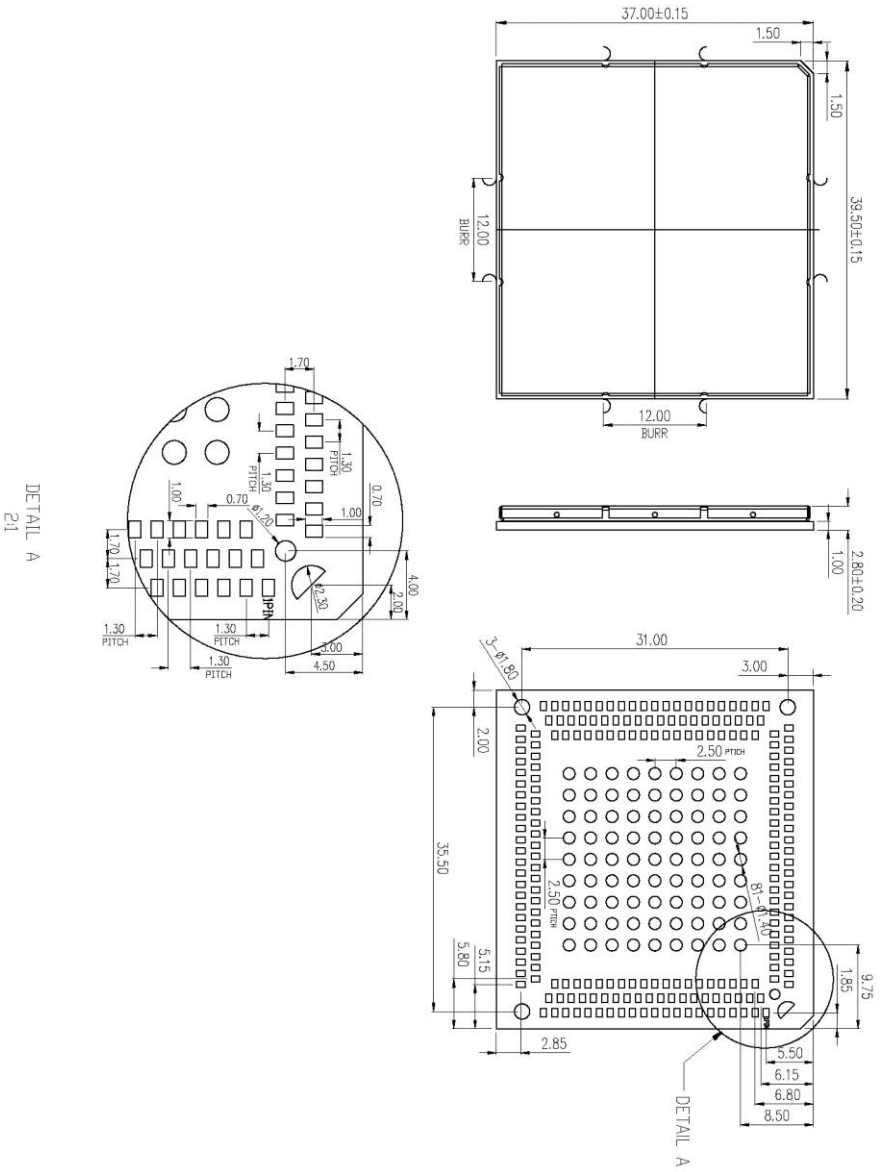

Figure 3: Dimensions of SIM7912&SIM7906 (unit: mm)

3 Interface Application

3.1 Power Supply

Module provides six VBAT pins dedicated to connection with an external power supply. There are two separate voltage domains for VBAT.

- Four VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's baseband part

The following table shows details of VBAT pins and ground pins.

Table 7: VBAT pins electronic characteristics

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	85, 86, 87, 88	Power supply for the module's RF part	3.3	3.8	4.3	V
VBAT_BB	155, 156	Power supply for the module's baseband part	3.3	3.8	4.3	V

3.1.1 Power Supply Design Guide

The power supply range of the module is from 3.3V to 4.3V. Please make sure the input voltage will never drop below 3.3V. The following figure shows the voltage drop during Tx power in 3G and 4G networks.

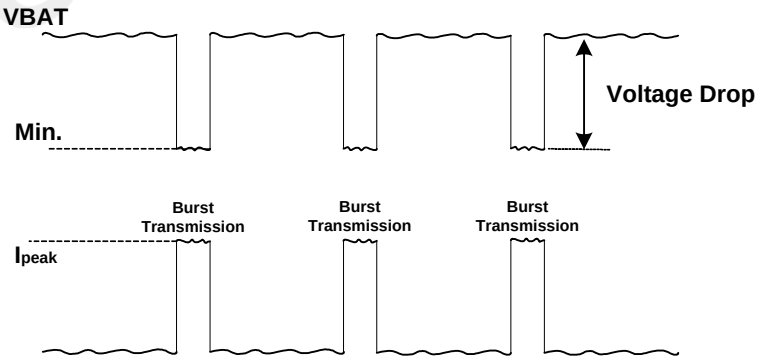

Figure 4: Power Supply Limits during Burst Transmission

To decrease the voltage dropping, make sure that the capacitors of VBAT net must not less than 640uF. The following figure shows the reference circuit of power supply for the VBAT.

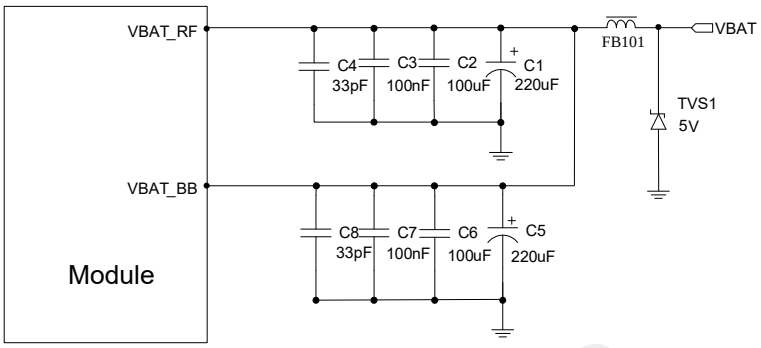

Figure 5: Power supply reference circuit

In this reference circuit, some multi-layer ceramic chip (MLCC) capacitors (0.1/1uF) with low ESR in high frequency band can be used for EMI suppression.

NOTE

1. Both C1 and C5 are 220 μF tantalum capacitor (ESR=0.7Ω).
2. C3, C4, C7 and C8 are multi-layer ceramic chip (MLCC) capacitors from 0.1uF to 1uF with low ESR in high frequency band, which can be used for EMC performance.
3. TVS1 is used for surge protection.

Table 8: Recommended TVS1 list

No.	Manufacturer	Part Number	Power dissipation	Package
1	Js-ele	ESDBW5V0A1	5V	DFN1006-2L
2	Prisem	PESDHC2FD4V5BH	4.5V	DFN1006-2L
3	Way-on	WS05DPF-B	5V	DFN1006-2L
4	Will semi	ESD5611N	5V	DFN1006-2L
5	Will semi	ESD56151W05	5V	SOD-323
6	Way-on	WS4.5DPV	4.5V	DFN1610-2L

Power supply layout guidelines:

- Both VBAT and return path should be as short and wide as possible to minimize the voltage drop.
- The width of VBAT_BB trace should be no less than 1.5mm, and the width of VBAT_RF trace should be no less than 2mm.
- These capacitors should be placed as closely as possible to the VBAT_BB and VBAT_RF pins.
- The VBAT trace should pass through TVS and capacitors, and then pass through the VBAT pins. The small value capacitors should be placed close to the VBAT pins.

- The customer's PCB design must have a solid ground plane throughout the board as the primary reference plane for most signals.

3.1.2 Recommended Power Supply Circuit

It is recommended to use a switching mode power supply or a linear regulator power supply. Make sure it can provide the current up to 3A at least.
The following figure shows the linear regulator reference circuit with 5V input and 3.8V output.

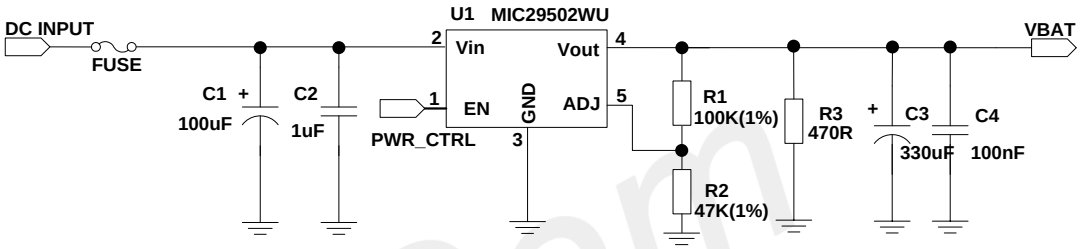

Figure 6: Linear regulator reference circuit

NOTE

An extra minimum load of R3 is required, to ensure it work properly under light load in sleep mode and power off mode. For the details about minimum load, please refer to specification of MIC29502WU.

The following figure shows the switching mode power supply reference circuit with 5~12V input and 3.8V output.

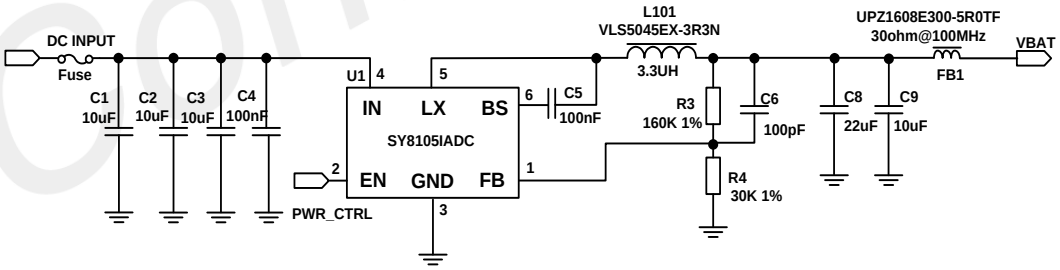

Figure 7: Switching mode power supply reference circuit

NOTE

1. In order to avoid damaging the module, please do not switch off the power supply when module works normally. Only after the module is shut down by PWRKEY or AT command, then the power supply can be cut off.

2. It is suggested that customer's design should have the ability to switch off the power supply for module in abnormal state, and then switch on the power to restart the module.
3. The PWR_CTRL signal recommend connect to the host and can be controlled.

3.1.3 Voltage Monitor

To monitor the VBAT voltage, the AT command “AT+CBC” can be used.

NOTE

For more details about voltage monitor commands, please refer to Document [1] in the appendix.

3.2 Power On and Off Module

3.2.1 Power On

Drive the PWRKEY pin to a low level and hold it for 1 seconds, then release, the module will be powered on. This pin is already pulled up internally. The electrical characteristics are listed in Table 10, and the following figure shows the power on circuit.

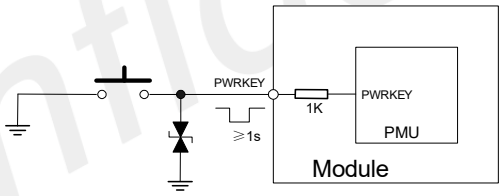

Figure 8: Power on the module use button

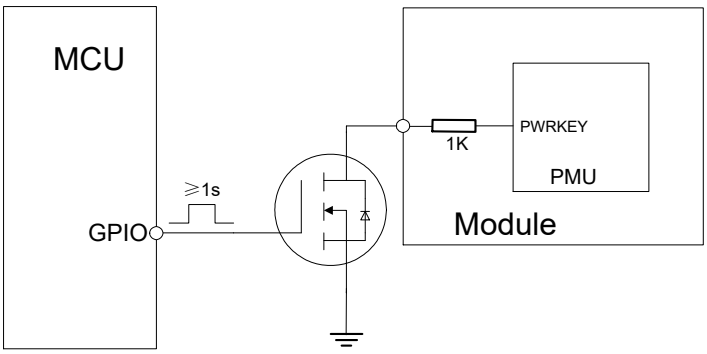

Figure 9: Power on the module use GPIO drive

Table 9: Definition of PWRKEY pin

Pin name	Pin no.	I/O	Functional description	Comment
PWRKEY	2	DI	Power on/off the module, active low	1.8V power domain. Pulled-up internally. Active low

The power on sequence is shown in the following figure.

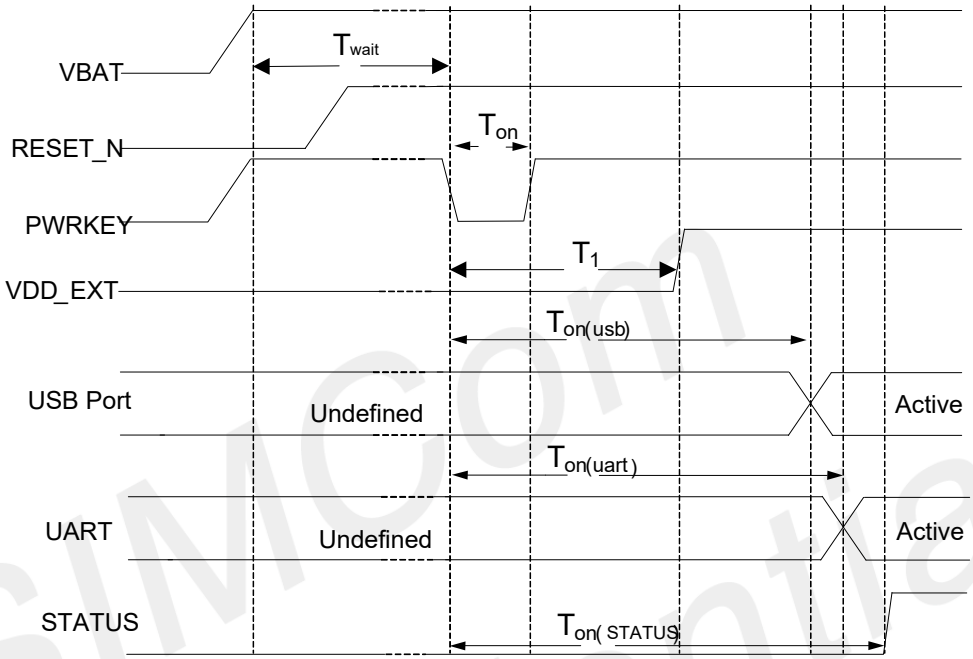

Figure 10: Power on sequence

Table 10: Power on timing and electronic characteristic

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{wait}	The waiting time from power supply available to power-on action	30	-	-	ms
T_{on}	The time of holding on PWRKEY pin to a low level	1000	-	-	ms
$T_{on(VDD\_EXT)}$	The time from power-on action to VDD_EXT ready	100	-	-	ms
$T_{on(usb)}$	The time from power-on action to USB port ready	11	12	-	s
$T_{on(uart)}$	The time from power-on issue to UART port ready	15	-	-	s
$T_{on(STATUS)}$	The time from power-on action to STATUS ready	-	25	-	s

NOTE

After enter force download mode, the PWRKEY pin need to release and don't pull low always. If not, the module will restart and then cause the download fail.

3.2.2 Power Off

The following methods can be used to power off the module.

- Method 1: Power off the module by holding the PWRKEY to a low level 2 second then release.
- Method 2: Power off the module by AT command “AT+CPOF”.

For details about “AT+CPOF”, please refer to Document [1] in the appendix.

NOTE

If the temperature is outside the range of -30~+70℃, some warning will be reported via AT port. If the temperature is outside the range of -40~+85℃, module will be powered off automatically.
For details about “AT+CPOF”, please refer to Document [1] in the appendix.

Normal power off action will make the module disconnect from the network, allow the software enter a safe state, and save key data before the module is powered off completely.

The power off sequence is shown in the following figure.

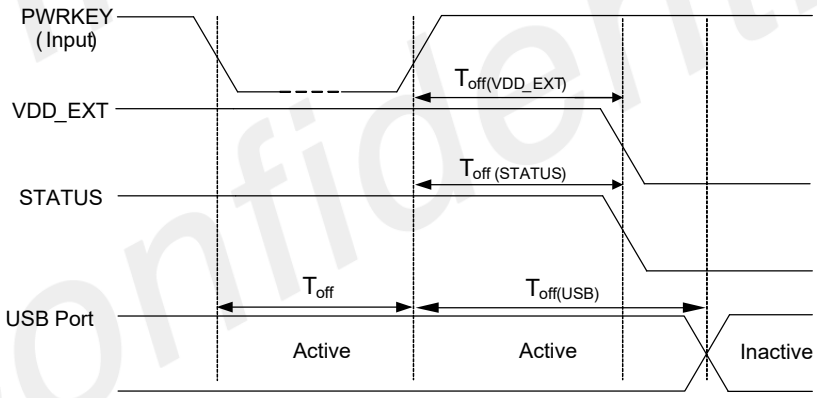

Figure 11: Power off sequence

Table 11: Power off timing and electronic characteristic

Symbol	Parameter	Time value			Unit
		Min.	Typ.	Max.	
T_{off}	The time of holding on PWRKEY pin to a low level	2.5	-	5	s
$T_{off(usb)}$	The time from power-off issue to USB port off	27	28	-	s
$T_{off(status)}$	The time from power-off issue to STATUS off	25	26	-	s

NOTE

1. In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, the power supply can be cut off.
2. When turning off module with AT command, please keep PWRKEY at high level after the execution of power-off command. Otherwise, the module will be turned on again after successful turn-off.

3.3 Reset Function

Module can be reset by driving the RESET_N pin down to a low level for 500ms at least and then releasing it.

The RESET_N signal has been internally pulled up to 1.8V, so there is no need to pull it up externally. Please refer to the following figure for the recommended reference circuit.

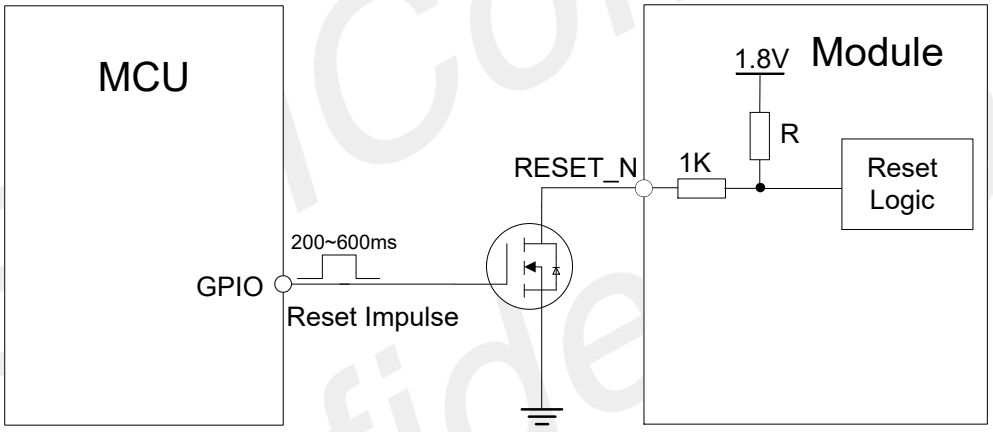

Figure 12: Reset the module use GPIO drive

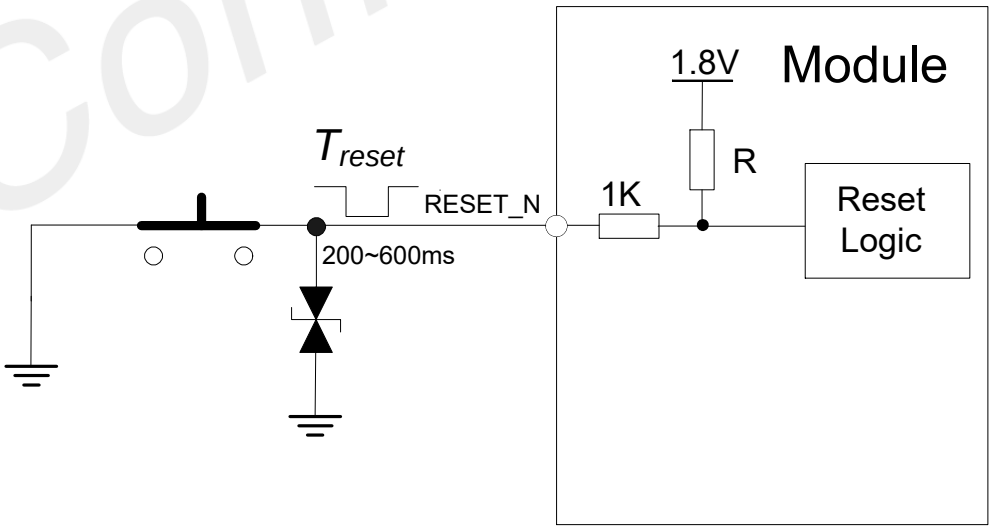

Figure 13: Reset the module use button

Table 12: Definition of RESET_N pin

Pin name	Pin no.	I/O	Functional description	Comment
RESET_N	1	DI	Reset the module active low	

Table 13: RESET electronic characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
T_{reset}	The time of holding on RESET_N pin to a low level	250	500	-	ms

The reset timing sequence of the module is shown in the following figure.

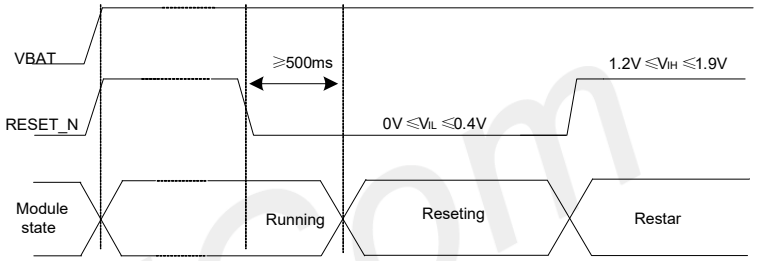

Figure 14: The reset timing sequence of the module

NOTE

Please ensure that there is no capacitance on RESET_N pin.

3.4 Output Power Management

Table 14: Output power management summary

Pin name	Pin no	Typical voltage (V)	Rated current (mA)	Sleep state	Comment
VDD_EXT	168	1.8	50	Always on	Output power supply for external IO pull up circuits
VDD_RF	162	2.8	150	Always on	Provide 2.85V for external RF circuit.
SD_VDD	46	1.8/3	150	Always on	SDIO pull up power source

3.5 USB Interface

Module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 3.0 and 2.0 specifications. This USB interface supports super speed (5Gbps) on USB 3.0 and high speed (480 Mbps) and full speed (12 Mbps) modes on USB 2.0.

The USB interface is used for AT command communication, data transmission, GNSS NMEA output, firmware upgrade and software debugging.

The following table shows the pin definition of USB interface.

Table 15: Definition of USB interface

Pin name	Pin no.	I/O	Functional description	Comment
USB_VBUS	32	PI	USB VBUS detection	Typical 5.0V Not support for charging
USB_ DP	34	AIO	Differential USB bi-directional data plus	Required 90Ω differential impedance Compliant with USB 2.0 standard specifications
USB_ DM	33	AIO	Differential USB bi-directional data minus	
USB_SS_TX_P	38	AO	USB3.0 super-speed transmit data plus	Required 90Ω differential Impedance Compliant with USB 3.0 standard specifications
USB_SS_TX_M	37	AO	USB3.0 super-speed transmit data minus	
USB_SS_RX_P	40	AI	USB3.0 super-speed receive data plus	
USB_SS_RX_M	41	AI	USB3.0 super-speed receive data minus	
USB_ID	36	DI	OTG identification	1.8V power domain. If unused, keep it open
OTG_PWR_EN	143	DO	OTG power control	1.8V power domain. If unused, keep it open

The following figure is the USB reference circuit.

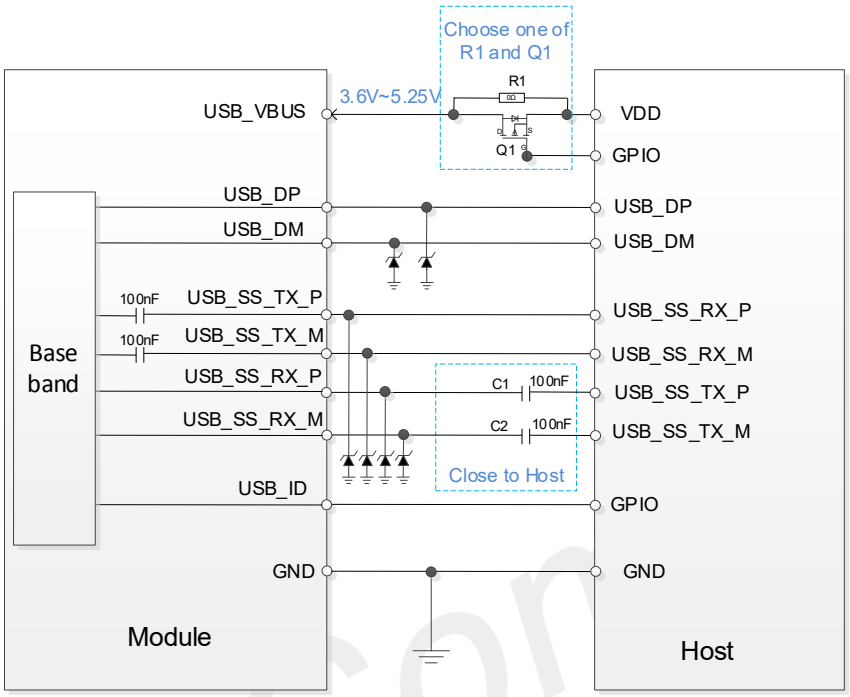

Figure 15: Reference Circuit of USB Application

NOTE

1. USB_VBUS is used for USB insertion detection. Its voltage input range is 3.6V~5.25V.
2. For sleep mode, if the Host does not support USB suspend mode, the input of USB_VBUS needs to be controlled by host. Choosing Q1 for placement.
3. For sleep mode, if the host supports USB suspend mode, USB_VBUS can be directly connected to VDD. Choosing R1 for placement.
4. The capacitors C1/C2 need to be placed close to the Host side.
5. Recommended add a 1Ω resistor in series and parallel varistor in USB3.0 for ESD protection.

HS USB DP/DM layout guidelines:

- Require differential trace impedance is 90±10% Ω.
- The intra-lane length mismatch of the differential signal lanes is less than 1mm.
- Gap from other signals keeps 3xline width.
- External components should be placed near the USB connector.
- Trace routes away from other sensitive signals (RF, audio, and 38.4M XO).
- Maximum PCB trace length cannot exceed 100mm outside of module, the shorter trace and more better.

SS USB TX/RX layout guidelines:

- Require differential trace impedance is 90±10% Ω.
- The intra-lane length mismatch of the differential signal lanes is less than 500um.

- Gap from other signals keeps 4xline width.
- Gap between Rx-to-Tx keeps 4xline width.
- External components should be placed near the USB connector.
- Trace routes away from other sensitive signals (RF, especially 2.4 GHz).
- Route differential pairs in the inner layers with a solid GND reference to have good impedance control and to minimize discontinuities.
- Keep isolation between the Tx pair, Rx pair, and DP/DM to avoid crosstalk.
- If core vias are used, use no more than two core vias per signal line to limit stubs.

3.6 PCIe Interface

Module provides one integrated PCIe (Peripheral Component Interconnect Express) interface which complies with the PCI Express Specification, Revision 2.1 and supports 5Gbps per lane. The PCIe interface of module is only used for data transmission

- PCI Express Specification Revision 2.1 compliance
- Data rate at 5Gbps per lane
- Can be used to connect to an external Ethernet IC (MAC and PHY) or WLAN IC

Table 16: Definition of PCIe interface

Pin name	Pin no.	I/O	Functional description	Comment
PCIE_REFCLK_P	179	AIO	PCIe reference clock plus	Required 90Ω differential impedance If unused, keep it open.
PCIE_REFCLK_M	180	AIO	PCIe reference clock minus	
PCIE_TX_M	182	AO	PCIe transmit0 minus	
PCIE_TX_P	183	AO	PCIe transmit0 plus	
PCIE_RX_M	185	AI	PCIe receive0 minus	
PCIE_RX_P	186	AI	PCIe receive0 plus	
PCIE_CLK_REQ_N	188	IO	PCIe clock request	In master mode, it is an input signal. In slave mode, it is an output signal. If unused, keep it open.
PCIE_WAKE_N	190	IO	PCIe wake-up	In master mode, it is an input signal. In slave mode, it is an output signal. If unused, keep it open.
PCIE_RST_N	189	IO	PCIe reset	In master mode, it is an output signal. In slave mode, it is an

				input signal. If unused, keep it open

PCIe interface layout guidelines:

- All other sensitive/high-speed signals and circuits must be protected from PCIe corruption.
- PCIe signals must be protected from noisy signals (clocks, SMPS).
- Each trace needs to be adjacent to a ground plane.
- Require differential trace impedance is 90±10% Ω.
- The intra-lane length mismatch of the differential signal lanes is less than 500um.
- Gap from other signals keeps 4xline width.
- Gap between Rx-to-Tx keeps 4xline width.
- Maximum PCB trace length cannot exceed 150mm outside of module, the shorter trace and more better.

In Root Complex Mode, the module is configured to act as a PCIe RC device. The following figure shows a reference circuit of PCIe RC mode.

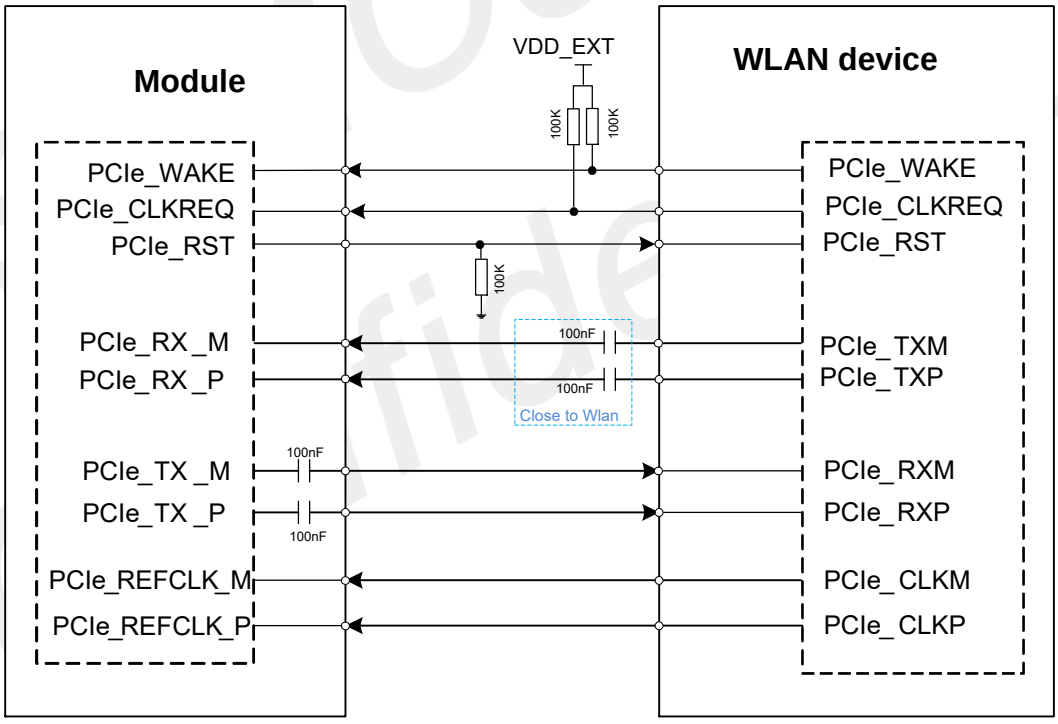

Figure 16: PCIe interface reference circuit (RC Mode)

In Endpoint Mode, the module is configured to act as a PCIe EP device. The following figure shows a reference circuit of PCIe EP mode

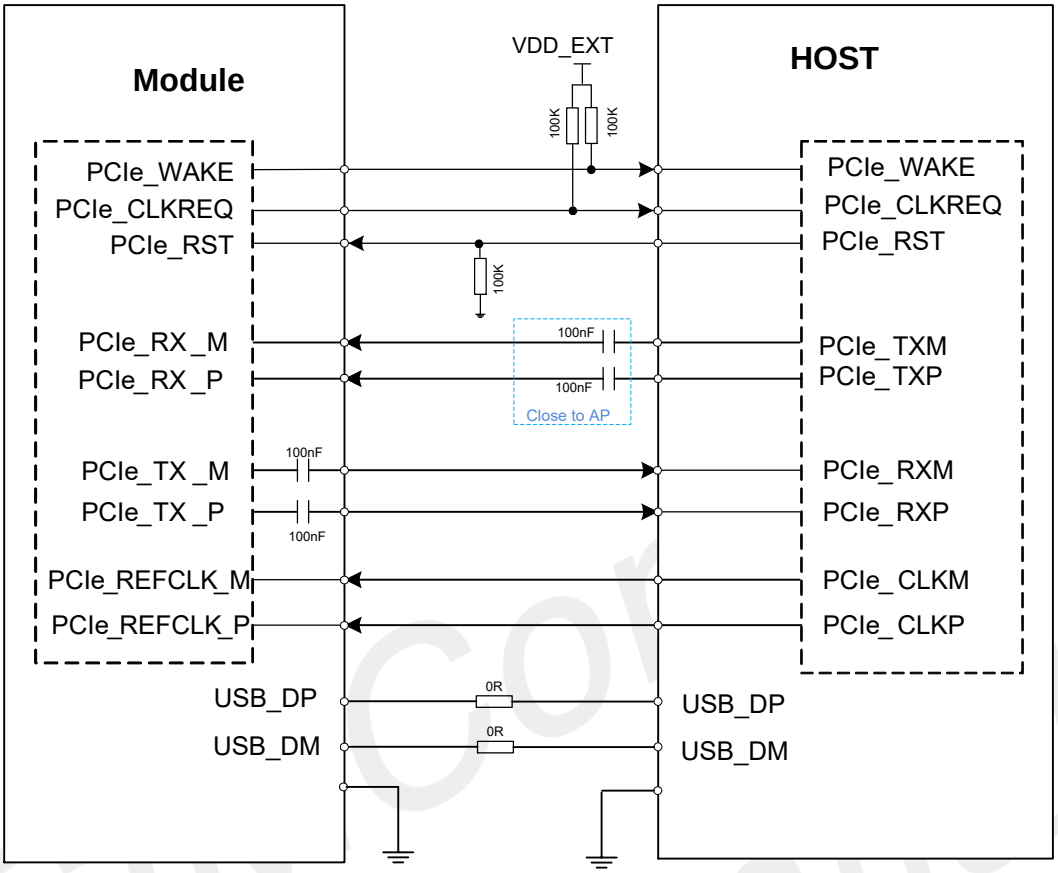

Figure 17: PCIe interface reference circuit (EP)

NOTE

1. USB is required because PCIe does not support features such as firmware upgrade, GNSS NMEA output and software debugging. Firmware upgrade must be over USB 2.0, while GNSS NMEA output and software debugging can be over USB 2.0/3.0 (USB 2.0 is recommended)
2. All the PCIe level of module is 1.8V. If it communicates with the 3.3V serial port level, a level conversion chip needs to be added in the middle.
3. The Endpoint mode of PCIe is under the development.

3.7 SDIO Interface

Module provides one SDIO interface which supports SD 3.0 protocol and eMMC*. The following table shows the pin definition.

Table 17: Definition of SDIO interface

Pin name	Pin no.	I/O	Functional description	Comment

SD_VDD	46	PO	**SD card application**: SDIO pull up power source. **eMMC application**: Keep it open when used for eMMC.	1.8V/3.0V configurable output. Cannot be used for SD card power supply.
SD_DATA0	49	DIO	SDIO data signal (bit 0)	Required 50Ω impedance If unused, keep it open.
SD_DATA1	50	DIO	SDIO data signal (bit 1)	
SD_DATA2	47	DIO	SDIO data signal (bit 2)	
SD_DATA3	48	DIO	SDIO data signal (bit 3)	
SD_CMD	51	DIO	SDIO command signal	
SD_CLK	53	DO	SDIO clock signal	
SD_DET	52	DI	SD card insertion detection	1.8V power domain. If unused, keep it open.

The following figure shows the SD card reference circuit.

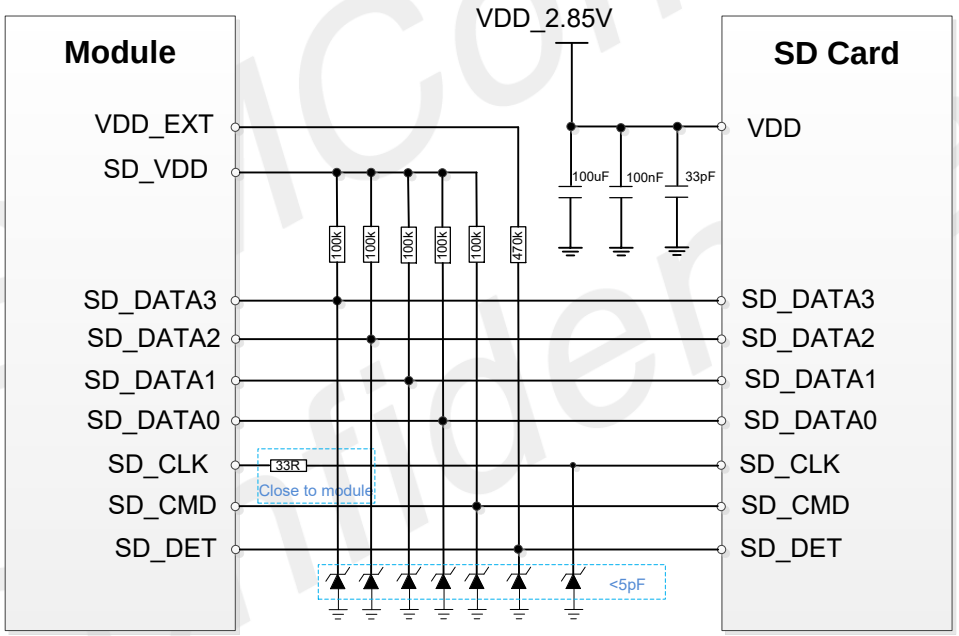

Figure 18: SD card reference circuit

NOTE

1. The voltage range of SD power supply is 2.7V~3.6V and a sufficient current up to 0.8A should be provided. As the maximum output current of SD_VDD is 50mA which can only be used for SDIO pull-up resistors, an external power supply is needed for SD card.
2. The load capacitance of SDIO bus needs to be less than 5pF.
3. If eMMC function is required, SD_DET need to be pull-down to GND.

SDIO interface layout guidelines:

- Require trace impedance is 36 to 50Ω.
- CLK to DATA/CMD length mismatch is less than 0.5mm.
- 30–35Ω termination resistance on clock net and placed close to the module.
- Gap from other signals keeps 1.5xline width.
- Gap lane-to-lane 1.5xline width.
- Bus capacitance load is less than 5pF.
- Trace routes away from other sensitive signals.
- Maximum PCB trace length cannot exceed 30mm out of the module for 104Mbps data rate, the shorter trace and more better.
- Maximum PCB trace length cannot exceed 100mm out of the module for 50Mbps data rate, the shorter trace and more better.
- It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1mm and the total routing length less than 100mm. The total trace length inside the module is 25mm, so the exterior total trace length should be less than 75mm.

3.8 SIM Interface

Module supports two SIM cards but single standby. SIM1 and SIM2 are dual-voltage 1.8 V or 3.0 V interfaces.

Table 18: Definition of SIM interface

Pin name	Pin no.	I/O	Functional description	Comment
SIM1_VDD	26	PO	Power supply for SIM1 card	
SIM1_DATA	29	DIO	SIM1 card data signal, which has been pulled up to SIM1_VDD by a 20K resistor internally	
SIM1_CLK	27	DO	SIM1 clock signal	
SIM1_RST	28	DO	SIM1 reset signal	
SIM1_DET	25	DI	SIM1 card detect signal, which need pulled up to VDD_EXT by a 470K resistor externally	1.8/3.0V voltage domain, SIM interface should be protected against ESD.
SIM2_VDD	74	PO	Power supply for SIM2 card	
SIM2_DATA	77	DIO	SIM2 card data, which has been pulled up to SIM2_VDD by a 20K resistor internally	If unused, please keep open
SIM2_CLK	80	DO	SIM2 clock signal	
SIM2_RST	79	DO	SIM2 reset signal	
SIM2_DET	78	DI	SIM2 card detect, which need pulled up to VDD_EXT by a 470KR resistor externally	

Table 19: SIM electronic characteristics in 1.8V mode (SIM_PWR=1.8V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SIM_VDD	Power supply for SIM card	1.65	1.8	1.95	V
V_{IH}	High-level input voltage	1.26	-	1.95	V
V_{IL}	Low-level input voltage	0	-	0.36	V
V_{OH}	High-level output voltage	1.44	-	1.8	V
V_{OL}	Low-level output voltage	0	-	0.4	V

Table 20: SIM electronic characteristics 3.0V mode (SIM_PWR=3.0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SIM_VDD	Power supply for SIM card	2.7	3.0	3.05	V
V_{IH}	High-level input voltage	2.1	-	3.05	V
V_{IL}	Low-level input voltage	0	-	0.6	V
V_{OH}	High-level output voltage	2.4	-	3.0	V
V_{OL}	Low-level output voltage	0	-	0.4	V

The module supports SIM card hot-swap function through the SIM_DET pin, which is a level trigger pin. The SIM_DET pin requires pull up externally.

The following figure shows SIM card reference circuit.

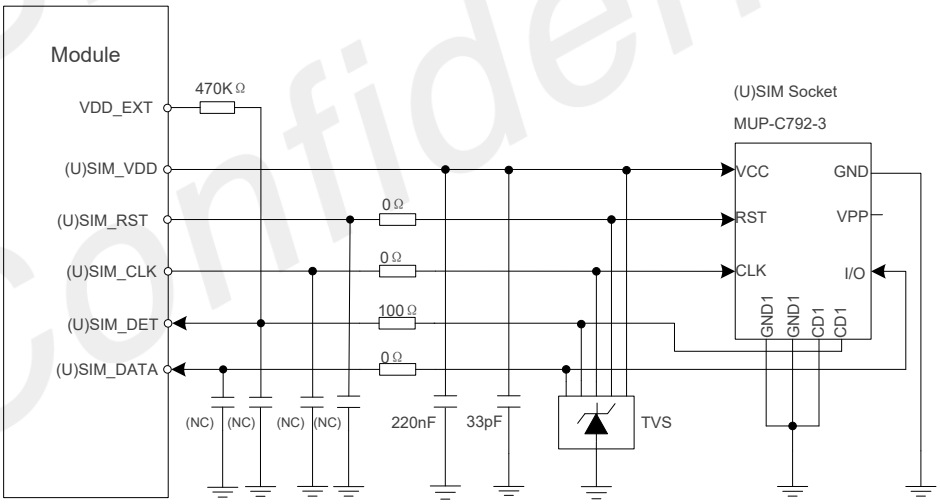

Figure 19: SIM interface reference circuit

After inserting SIM card, the SIM_DET pin will change from low to high level. The rising edge will indicate that the SIM card has been inserted. After removing the SIM card, the SIM_DET pin will change from high to low level. This falling edge will indicate the removal of the SIM card.

Using “AT+UIMHOTSWAPON=0 or 1” and “AT+UIMHOTSWAPLEVEL=0 or 1”AT command to set module SIM card hot swap function enable and SIM card detection level, for more details, please refer to SIM7912&SIM7906 Series AT Command Manual document.

Using “AT+SMSIMCFG=1,1” and “AT+SMSIMCFG=1,2” AT command to switch SIM1 and SIM2 function, for more details, please refer to Document [1] in the appendix.

The following table shows recommended TVS of ESD protect and SIM socket.

Table 21: Recommended TVS and SIM socket list

Name	Manufacturer	Model
TVS	ST	ESDA6V1-5W6
SIM socket	MUP	MUP-C792-3

If the SIM card hot-swap function is not used, customers should keep the SIM_DET pin open.

NOTE

1. The recommended SIM socket is normal close, which makes SIM_DET is active high. If the active low of SIM_DET is required, SIM socket should be normal open.
2. AT command “AT+UIMHOTSWAPLEVEL” could change the SIM_DET detection level and the default value is 1, which is active high, for more details, please refer to Document [1] in the appendix.

The SIM card layout guidelines:

- Make sure that the SIM card socket should be far away from the antennas.
- SIM traces should be away from RF, VBAT and high-speed signals.
- The traces should be as short as possible.
- Keep SIM socket’s GND pins directly connect to the main ground.
- Shielding the SIM card signals by ground.
- Recommended to place a 33pF～1uF capacitor on SIM_VDD net and place close to the holder.
- The rise/fall time of SIM_CLK should not exceed 40ns.
- The parasitic capacitance of TVS should not exceed 60pF, and the TVS should be placed close to the SIM socket.

3.9 PCM and I2S Interface

Module supports one I2S/PCM interface for external codec, which meets the requirements in the Phillips I2S bus specification.

The PCM interface is multiplexing with I2S interface. The default audio interface of the module is I2S.

Table 22: The PCM interface is multiplexing with I2S interface

Pin name	Pin no.	I/O	Functional description	Comment
PCM_OUT	68	DO	PCM data output. It can also be multiplexed as I2S_D1.	1.8V power domain. If unused, please keep open.
PCM_IN	66	DI	PCM data input. It can also be multiplexed as I2S_D0.	1.8V power domain. If unused, keep it open.
PCM_CLK	67	DO	PCM data clock. It can also be multiplexed as I2S_CLK.	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_SYNC	65	DIO	PCM data frame synchronization signal. It can also be multiplexed as I2S_WS.	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
I2S_MCLK	152	DO	Clock output	Provide a digital clock output for an external audio codec. If unused, keep it open.

Table 23: PCM / I2S format

Characteristics	Specification
Line interface format	Linear(fixed)
Data length	16bits(fixed)
I2S flock/sync source	Master mode(fixed)
I2S clock rate	1.536 MHz (default)
I2S MCLK rate	12.288MHz (default)
Data ordering	MSB

NOTE

For more details about PCM/I2S AT commands, please refer to Document [1] in the appendix.

3.9.1 I2S Timing

The module supports I2S sampling rate of 48 KHz and 32bit coding signal (16bit length), the timing sequence is shown in the following figure.

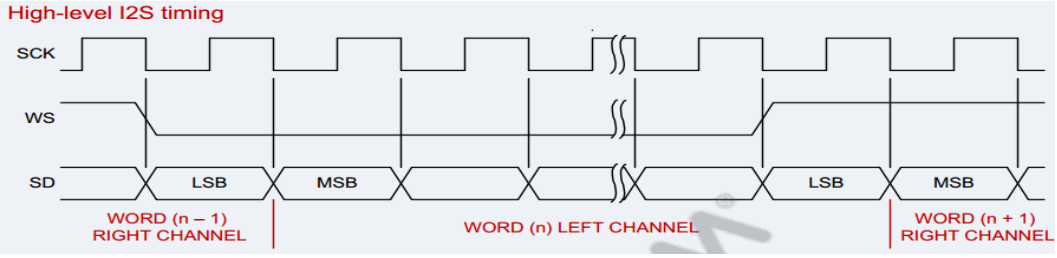

Figure 20: I2S timing

Table 24: I2S timing parameters

Signal	Parameter	Description	Min.	Typ.	Max.	Unit
I2S_MCLK	Frequency	Frequency	–	12.288	12.288	MHz
	T	Clock period	81.380	81.380	–	ns
	t(HC)	Clock high	0.45T	–	0.55T	ns
	t(LC)	Clock low	0.45T	–	0.55T	ns
I2S_CLK	Frequency	Frequency	-	1.536	-	MHz
	T	Clock period	-	651.04	-	ns
	t(HC)	Clock high	0.45T	–	0.55T	ns
	t(LC)	Clock low	0.45T	–	0.55T	ns
I2S_WS	t(sr)	DIN/DOUT and WS input setup time	16.276	–	–	ns
	t(hr)	DIN/DOUT and WS input hold time	0	–	–	ns
	t(dtr)	DIN/DOUT and WS output delay	–	–	65.10	ns
	t(htr)	DIN/DOUT and WS output hold time	0	–	–	ns

3.9.2 I2S Reference Circuit

The following figure shows the external codec reference design.

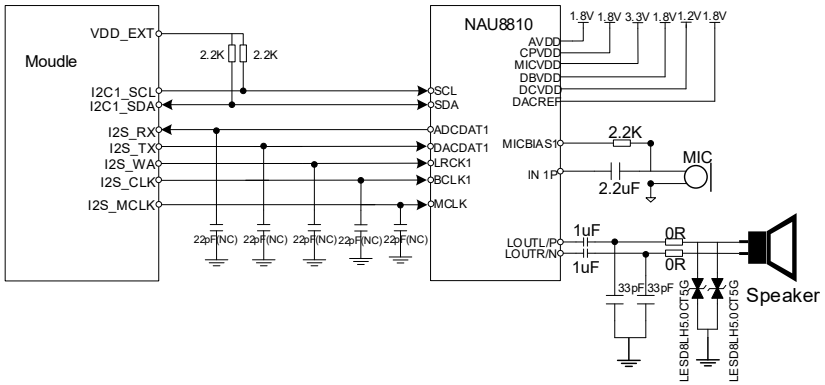

Figure 21: Audio codec reference circuit

Audio layout guidelines：

Analog input:

- 0.2mm trace widths; 0.2mm spacing between traces.
- Pseudo differential route for MIC.
- Isolate from noise sources, such as antenna, RF signals, SMPS, clocks, and other high-speed signals.

Analog output:

- Isolate from noise sources such as antenna, RF signals, SMPS, clocks, and other digital signals with fast transients.
- Speaker output signal – route as differential pair with 0.5mm trace widths.

3.10 I2C Interface

Module supports one I2C interfaces, meet I2C specification version 5.0, and data rate up to 400 Kbps.

The following figure shows the I2C bus reference circuit.

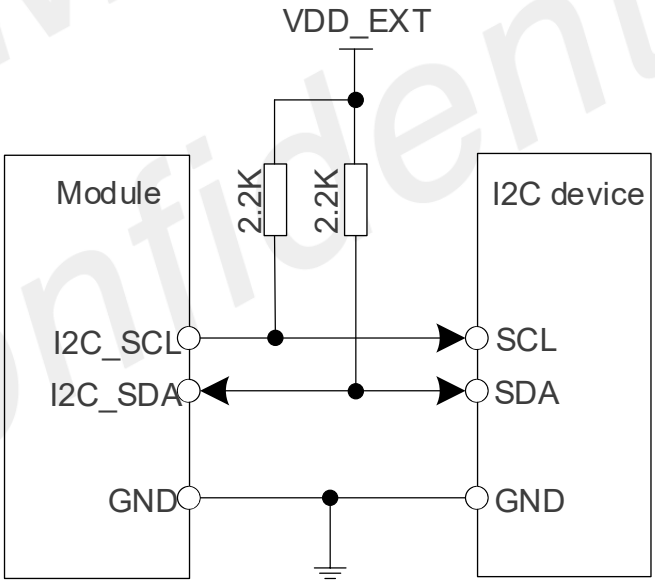

Figure 22: I2C reference circuit

Table 25: Definition of I2C interface

Pin name	Pin no.	I/O	Functional description	Comment
I2C_SCL	43	OD	I2C serial clock	I2C default use for codec Pull up to VDD_EXT externally If unused, keep it open.
I2C_SDA	42	OD	I2C serial data	

NOTE

1. SDA and SCL need to pull up to VDD_EXT by a 2.2K resistor externally.
2. For more details about AT commands please refer to Document [1] in the appendix.

3.11 UART Interface

The module provides three UART interfaces: main UART interface, debug UART interface, and BT UART interface. Features of these interfaces are shown as below:

- Main UART interface supports 4800bps, 9600bps, 19200bps, 38400bps, 57600bps, 115200bps (default), 230400bps, 460800bps, 921600bps and up to 4M bps baud rates. This interface is used for data transmission and AT command communication.
- Debug UART interface supports 115200bps baud rate. It is used for Linux console and log output.
- BT UART interface supports 115200bps baud rate. It is used for BT communication and can be multiplexed into SPI interface*.

Table 26: Definition of UART interface

Pin name	Pin no.	I/O	Functional description	Comment
CTS	56	DO	Clear to send	1.8V power domain Default use for AT command.
RTS	57	DI	Request to send	
TXD	60	DO	Transmit data	
RXD	58	DI	Receive data	
DCD	59	DO	Carrier detect	
RI	61	DO	Ring indicator	
DTR	62	DI	Data terminal ready sleep mode control	
DBG _TXD	137	DO	Transmit data	1.8V power domain. Used for debug only.
DBG _RXD	136	DI	Receive data	
BT_CTS	164	DO	Clear to send	Default use for BT 1.8V power domain If unused, keep it open.
BT_ RTS	166	DI	Request to send	
BT_ TXD	163	DO	Transmit data	
BT_ RXD	165	DI	Receive data	
BT_EN	3	DO	BT function enable control	

All the UART level of module is 1.8V. If it communicates with the 3.3V serial port level, a level conversion

chip needs to be added in the middle. It is recommended to use TI's TXS0104EPWR level shift, the reference circuit is as follows.

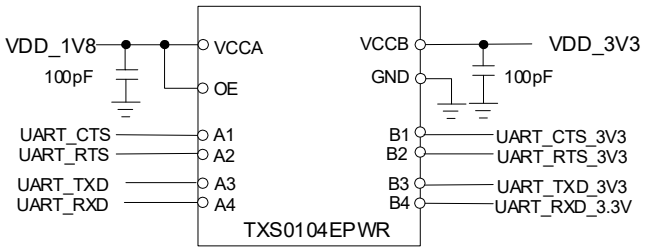

Figure 23: UART level conversion circuit

The following level shifting circuits can also be used:

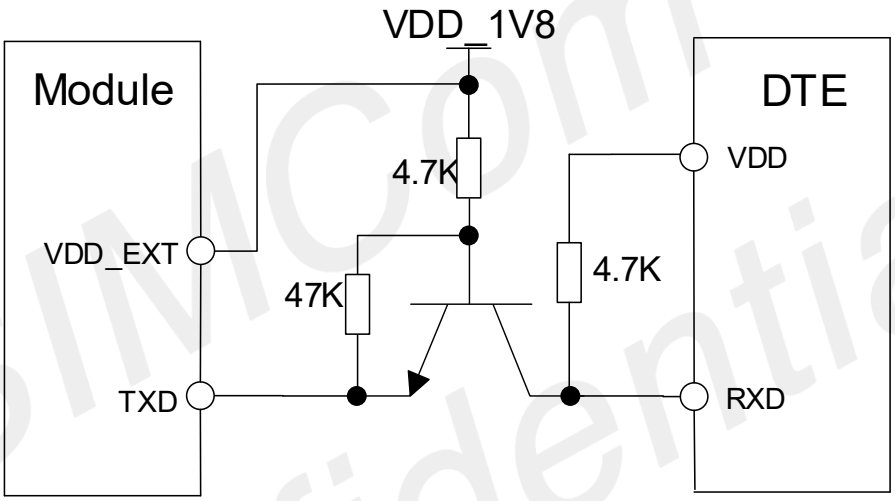

Figure 24: UART TX level conversion circuit

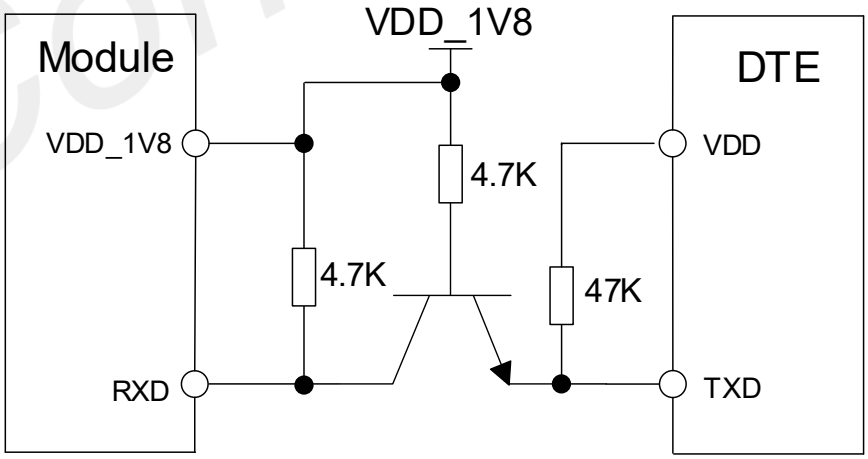

Figure 25: UART RX level conversion circuit

3.12 SPI Interface

Module provides one SPI interface multiplexed from BT UART interface. The interface only supports master mode with a maximum clock frequency up to 50MHz.

The following table shows the pin definition of SPI interface.

Table 27: Definition of SPI interface

Pin name	Pin no.	I/O	Functional description	Comment
BT_CTS	164	DO	Can be multiplexed into SPI_CLK.	1.8V power domain
BT_ RTS	166	DI	Can be multiplexed into SPI_CS.	
BT_ TXD	163	DO	Can be multiplexed into SPI_MOSI.	
BT_ RXD	165	DI	Can be multiplexed into SPI_MISO.	

The following figure shows the reference circuit of SPI interface.

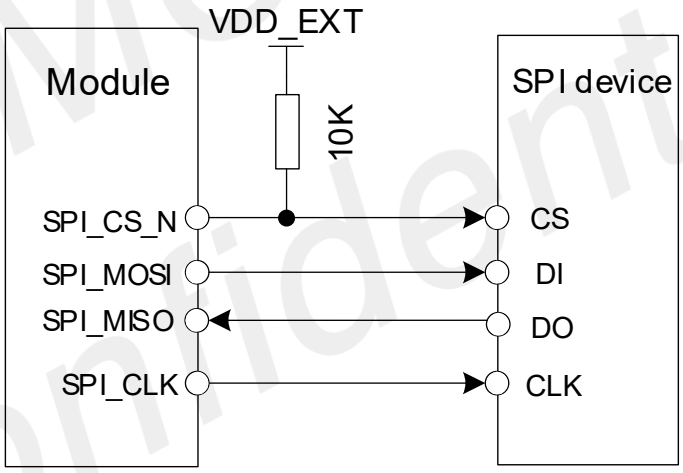

Figure 26: SPI reference circuit

3.13 ADC Interface

Module supports two 15bits ADC interfaces. Its performance parameters are shown as follow:

Table 28: Definition of ADC interface

Pin name	Pin no.	I/O	Functional description	Comment
ADC0	173	AI	Input Voltage Range: 0~1.875V	General purpose analog to digital converter interface.

				If unused, keep it open.
ADC1	175	AI	Input Voltage Range: 0~1.875V	General purpose analog to digital converter interface If unused, keep it open.

NOTE

1. The input voltage of ADC should not exceed 1.875V
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.

3.14 GPIOs Interface

The follow pins of module can be used as GPIO function, if the customer does not use the default functions. In addition, these pins support alternate function by software configure according to the customer's requirements.

Table 29: GPIO list

Pin name	Pin no.	I/O	Functional description	Comment
GPIO_1	138	IO	General purpose input/output ports. These four GPIOs can also be multiplexed into a group of PCM or I2S for BT.	1.8V power domain. If unused, keep it open.
GPIO_2	139	IO		
GPIO_3	159	IO		
GPIO_4	161	IO		
GPIO_5	172	IO	General purpose input/output ports. This GPIO can also be multiplexed into 1PPS for GNSS.	

3.15 Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The following tables describe pin definition and logic level changes in different network status.

Table 30: Definition of network indication pins

Pin name	Pin no.	I/O	Functional description	Comment
NET_STATUS	170	DO	Indicate the module's network activity status.	1.8V power domain. If unused, keep it open
NET_MODE	147	DO	Indicate the module's network registration mode.	1.8V power domain. If unused, keep it open

The timing parameters are shown in the following table.

Table 31: NET_STATUS pin status

Pin Name	Status	Description
NET_MODE	Always High	Registered on network
	Always Low	Others
NET_STATUS	Flicker slowly (200ms High/1800ms Low)	Network searching
	Flicker slowly (1800ms High/200ms Low)	Idle
	Flicker quickly (125ms High/125ms Low)	Data transfer ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

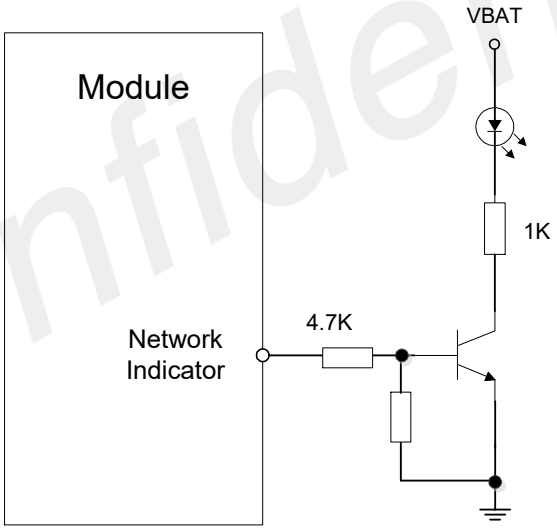

Figure 27: Network Indicator reference circuit

3.16 Status Indication

The STATUS pin is set as the module status indicator. It outputs high level voltage when the module is turned on.

The following table describes pin definition of STATUS.

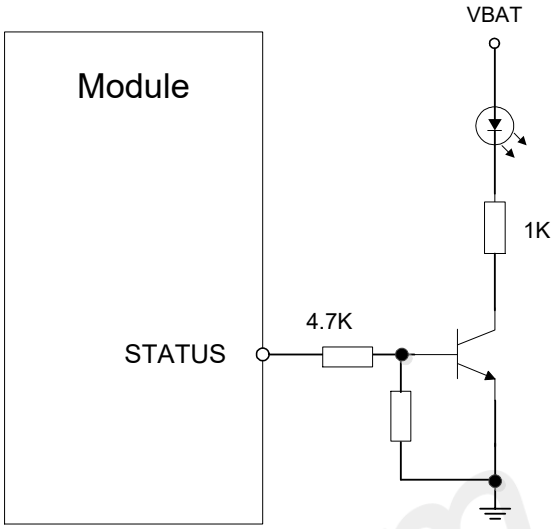

Figure 28: Reference Circuits of STATUS

3.17 Flight Mode Control

The W_DISABLE pin can be used to control module to enter or exit the flight mode. In flight mode, the RF circuit is closed to prevent interference with other equipment's and minimize current consumption. Its reference circuit is shown in the following figure.

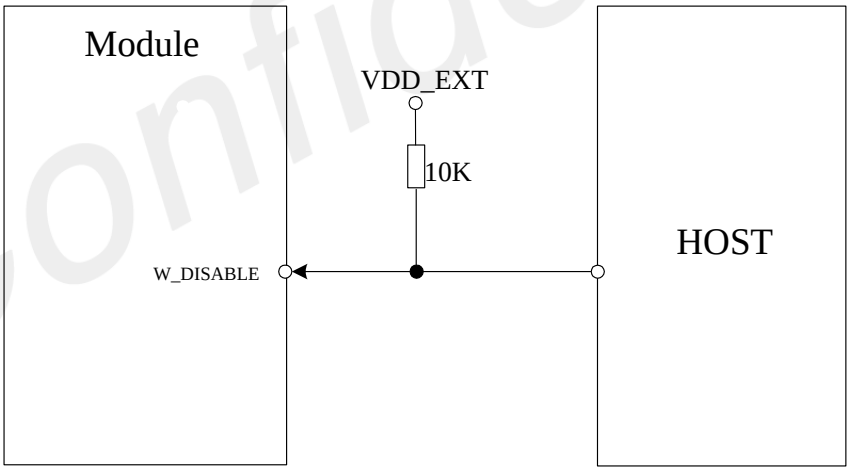

Figure 29: W_DISABLE# pin reference circuit

Table 32: Definition of W_DISABLE pin

Pin name	Pin no.	I/O	Functional description	Comment
W_DISABLE#	151	DI	Flight mode control input active low	

Table 33: W_DISABLE pin status

W_DISABLE pin status	Module operation
Input low level	Flight mode: RF is disabled
Input high level	AT+CFUN=4: Flight mode AT+CFUN=1: RF is enabled (Default)

3.18 USB_BOOT Interface

Module provides a USB_BOOT pin. Pulling up USB_BOOT to VDD_EXT before power-on will make the module enter emergency download mode when powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 34: Pin Definition of USB_BOOT Interface

Pin name	Pin no.	I/O	Functional description	Comment
USB_BOOT	140	DI	Force the module into emergency download mode	1.8V power domain. Active high. If unused, keep it open.

The following figure shows a reference circuit of USB_BOOT.

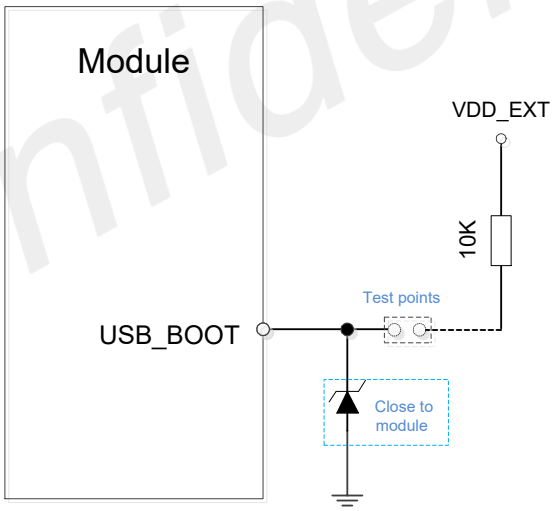

Figure 30: Reference Circuit of USB_BOOT

3.19 Antenna Tuner Control Interface*

The module supports external antenna tuner control through either RFFE interface or dedicated GPIO interfaces. Customers can choose either one according to their tuner design. The following are the pin definitions of the RFFE and dedicated GPIO interfaces.

Table 35: PIN Definition of RFFE Interface for Antenna Tuner Control

Pin name	Pin no.	I/O	Functional description	Comment
RFFE_CLK	71	DO	RFFE serial interface for external tuner control.	1.8V voltage domain. If unused, please keep open
RFFE_DATA	73	DIO		
VDD_RF	162	PO	Provide 2.85V for external RF circuit.	

NOTE

1. “*” means under development, for details please contact SIMCom support teams.

4 Antenna Interfaces

Module provides five antennas for 3G/4G and GNSS. The antenna ports have an RF impedance of 50Ω.

4.1 Antenna Definitions

For detailed designs about antenna, please refer to the antenna design guide Document [14] "SIM7912&SIM7906_LGA Antenna Port Mapping and Design Guide" in the appendix.

Table 36: Antenna port definitions

FUNCTIONS	ANT_MAIN	ANT_DIV	ANT_MIMO1	ANT_MIMO2	ANT_GNSS
3G/4G LB/MHB TRX	✓				
3G/4G LB/MHB DIV		✓			
DL-MIMO1 (B1/B3/B7/B38/B41/43/48/46 for SIM7912E) (B2/B4/B25/B66/B7/B41/43/48/46 For SIM7912A)			✓*		
DL-MIMO2 (B1/B3/B7/B38/B41/43/48/46 for SIM7912E) (B2/B4/B25/B66/B7/B41/43/48/46 For SIM7912A)				✓*	
GNSS					✓

NOTE

1. ANT_MIMO1 and ANT_MIMO2 are optional for SIM7906E and SIM7906A.

4.1.1 3G/4G Operating Frequency

Table 37: SIM7912 operating frequencies

Frequency	Uplink (UL)	Downlink (DL)	Duplex

band			mode
WCDMA B1	1920 MHz ~ 1980 MHz	2110 MHz ~ 2170 MHz	FDD
WCDMA B2	1850 MHz ~1910 MHz	1930 MHz ~ 1990 MHz	FDD
WCDMA B3	1710 MHz ~ 1785 MHz	1805 MHz ~ 1880 MHz	FDD
WCDMA B4	1710 MHz ~ 1755 MHz	2110 MHz ~ 2155 MHz	FDD
WCDMA B5	824 MHz ~ 849 MHz	869 MHz ~ 894MHz	FDD
WCDMA B8	880 MHz ~ 915 MHz	925 MHz ~ 960 MHz	FDD
LTE B1	1920 MHz ~ 1980 MHz	2110 MHz ~ 2170 MHz	FDD
LTE B2	1850 MHz ~ 1910MHz	1930 MHz ~ 1990MHz	FDD
LTE B3	1710 MHz ~ 1785 MHz	1805 MHz ~ 1880 MHz	FDD
LTE B4	1710 MHz ~ 1755MHz	2110 MHz ~ 2155MHz	FDD
LTE B5	824 MHz ~ 849 MHz	869 MHz ~ 894MHz	FDD
LTE B7	2500 MHz ~ 2570MHz	2620 MHz ~ 2690MHz	FDD
LTE B8	880 MHz ~ 915 MHz	925 MHz ~ 960 MHz	FDD
LTE B12	698 MHz ~ 716MHz	728 MHz ~ 746MHz	FDD
LTE B13	777 MHz ~787MHz	746 MHz ~ 756MHz	FDD
LTE B14	788 MHz ~ 798MHz	758 MHz ~ 768MHz	FDD
LTE B17	704 MHz ~ 716MHz	734 MHz ~ 746MHz	FDD
LTE B18	815 MHz ~ 830MHz	860 MHz ~ 875MHz	FDD
LTE B19	830 MHz ~ 845MHz	875 MHz ~ 890MHz	FDD
LTE B20	832 MHz ~ 862MHz	791 MHz ~ 821MHz	FDD
LTE B25	1850 MHz ~ 1915MHz	1930 MHz ~ 1995MHz	FDD
LTE B26	814 MHz ~849MHz	859 MHz ~ 894MHz	FDD
LTE B28	703 MHz ~ 748MHz	758 MHz ~ 803MHz	FDD
LTE B32	/	1452 MHz ~ 1496MHz	FDD
LTE B34	2010 MHz ~ 2025MHz	2010 MHz ~ 2025MHz	TDD
LTE B38	2570 MHz ~ 2620 MHz	2570 MHz ~ 2620 MHz	TDD
LTE B39	1880 MHz ~ 1920MHz	1880 MHz ~ 1920MHz	TDD
LTE B40	2300 MHz ~ 2400 MHz	2300 MHz ~ 2400 MHz	TDD
LTE B41	2496 MHz ~ 2690 MHz	2496 MHz ~ 2690 MHz	TDD
LTE B43	3600MHz ~ 3800MHz	3600 MHz ~ 3800MHz	TDD
LTE B48	3550 MHz ~ 3700MHz	3550 MHz ~ 3700MHz	TDD
LTE B66	1710 MHz ~ 1780MHz	2110 MHz ~ 2180MHz	FDD
LTE B71	663 MHz ~ 698MHz	617MHz ~ 652MHz	FDD

Table 38: SIM7906 operating frequencies

Frequency band	Uplink (UL)	Downlink (DL)	Duplex mode
WCDMA B1	1920 MHz ~ 1980 MHz	2110 MHz ~ 2170 MHz	FDD

WCDMA B2	1850 MHz ~1910 MHz	1930 MHz ~ 1990 MHz	FDD
WCDMA B3	1710 MHz ~ 1785 MHz	1805 MHz ~ 1880 MHz	FDD
WCDMA B4	1710 MHz ~ 1755 MHz	2110 MHz ~ 2155 MHz	FDD
WCDMA B5	824 MHz ~ 849 MHz	869 MHz ~ 894MHz	FDD
WCDMA B8	880 MHz ~ 915 MHz	925 MHz ~ 960 MHz	FDD
LTE B1	1920 MHz ~ 1980 MHz	2110 MHz ~ 2170 MHz	FDD
LTE B2	1850 MHz ~ 1910MHz	1930 MHz ~ 1990MHz	FDD
LTE B3	1710 MHz ~ 1785 MHz	1805 MHz ~ 1880 MHz	FDD
LTE B4	1710 MHz ~ 1755MHz	2110 MHz ~ 2155MHz	FDD
LTE B5	824 MHz ~ 849 MHz	869 MHz ~ 894MHz	FDD
LTE B7	2500 MHz ~ 2570MHz	2620 MHz ~ 2690MHz	FDD
LTE B8	880 MHz ~ 915 MHz	925 MHz ~ 960 MHz	FDD
LTE B12	698 MHz ~ 716MHz	728 MHz ~ 746MHz	FDD
LTE B13	777 MHz ~787MHz	746 MHz ~ 756MHz	FDD
LTE B14	788 MHz ~ 798MHz	758 MHz ~ 768MHz	FDD
LTE B17	704 MHz ~ 716MHz	734 MHz ~ 746MHz	FDD
LTE B18	815 MHz ~ 830MHz	860 MHz ~ 875MHz	FDD
LTE B19	830 MHz ~ 845MHz	875 MHz ~ 890MHz	FDD
LTE B20	832 MHz ~ 862MHz	791 MHz ~ 821MHz	FDD
LTE B25	1850 MHz ~ 1915MHz	1930 MHz ~ 1995MHz	FDD
LTE B26	814 MHz ~849MHz	859 MHz ~ 894MHz	FDD
LTE B28	703 MHz ~ 748MHz	758 MHz ~ 803MHz	FDD
LTE B32	/	1452 MHz ~ 1496MHz	FDD
LTE B34	2010 MHz ~ 2025MHz	2010 MHz ~ 2025MHz	TDD
LTE B38	2570 MHz ~ 2620 MHz	2570 MHz ~ 2620 MHz	TDD
LTE B39	1880 MHz ~ 1920MHz	1880 MHz ~ 1920MHz	TDD
LTE B40	2300 MHz ~ 2400 MHz	2300 MHz ~ 2400 MHz	TDD
LTE B41	2496 MHz ~ 2690 MHz	2496 MHz ~ 2690 MHz	TDD
LTE B43	3600MHz ~ 3800MHz	3600 MHz ~ 3800MHz	TDD
LTE B48	3550 MHz ~ 3700MHz	3550 MHz ~ 3700MHz	TDD
LTE B66	1710 MHz ~ 1780MHz	2110 MHz ~ 2180MHz	FDD
LTE B71	663 MHz ~ 698MHz	617MHz ~ 652MHz	FDD

NOTE

2. LTE-FDD B32 support Rx only and are only for secondary component carrier.

4.1.2 GNSS Frequency

The following table shows frequency specification of GNSS antenna interface.

Table 39: GNSS frequency

Type	Frequecy
GPS L1/Galileo/QZSS	1575.42±1.023MHz
GPS L5	1176.45±10.23MHz
GLONASS	1597.5~1605.8MHz
BeiDou/Compass	1561.098±2.046MHz

4.2 Antenna Installation

4.2.1 PCB Layout Guidelines

To avoid interference, minimalize the insertion loss of the RF trace, the PCB should follow below rules:

(1) The coaxial cable PCB pads, RF antenna connector and other connectors which used to test contact performance of module should place as close as to the module antenna pads.
(2) The antenna matching network should place to antenna feed port.
(3) The RF trace should be as short and straight as possible, and do not routing as perpendicular line, we recommend do it as 45° corner trace.
(4) And the RF trace ground should be complete;
(5) RF device should place ground to the nearest ground plane;
(6) Between RF trace and below should avoid other signal trace or parallel trace to the RF signal.
(7) Recommend to more ground vias near the RF traces.

4.2.2 Antenna Tuner

When end device needs to support 700MHz low frequency(B12\B13\B28), it is recommended to add anten na tuner to improve RF performance. Antenna tuner contains antenna aperture tuner, antenna impedance tuner and hybrid tuner of the two. Aperture tuner optimizes the total antenna efficiency from the free space of the antenna terminal, and can optimize antenna efficiency across multiple frequency bands. Impedance tuner adjusts the mismatch between the RF front end and the antenna to achieve maximum transmission power. Hybrid tuner combines the advantages of both to maximize antenna RF performance. Customers c an choose according to specific needs, according to the recommendations from the antenna vendor.

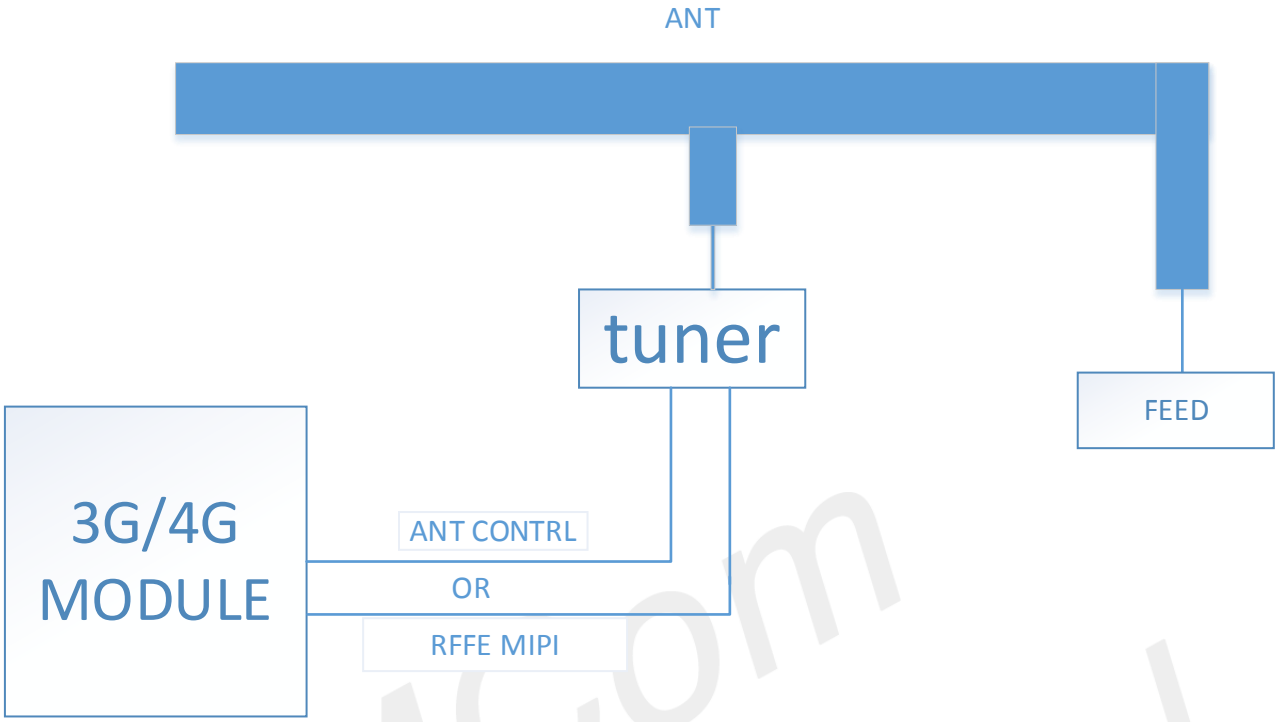

Figure 31: Aperture tuner reference block diagram

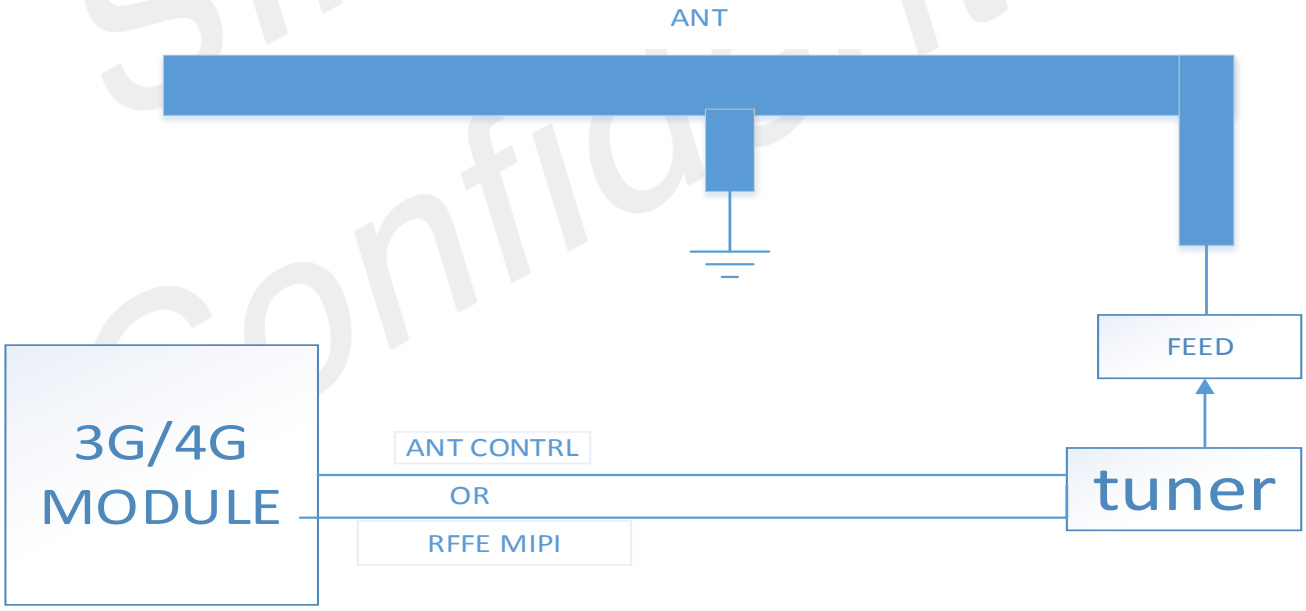

Figure 32: Impedance tuner reference block diagram

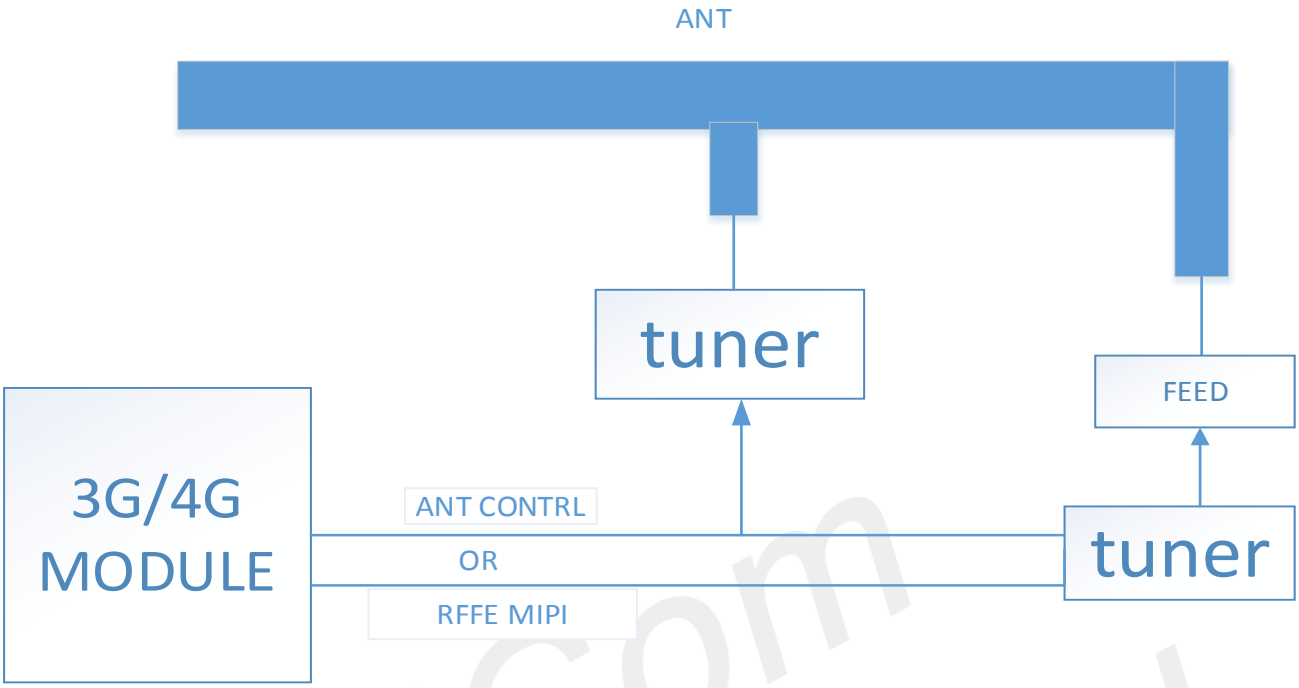

Figure 33: Hybrid tuner reference block diagram

The antenna control Tuner mipi interface of different package modules is as follows.

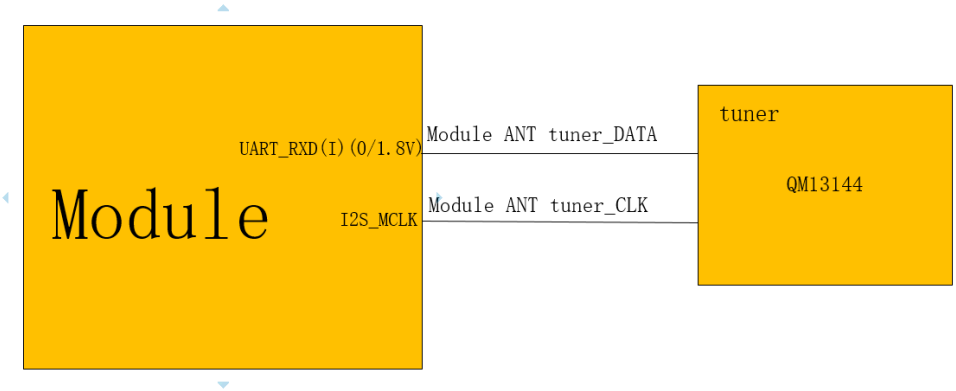

Figure 34: M.2 package Tuner mipi interface

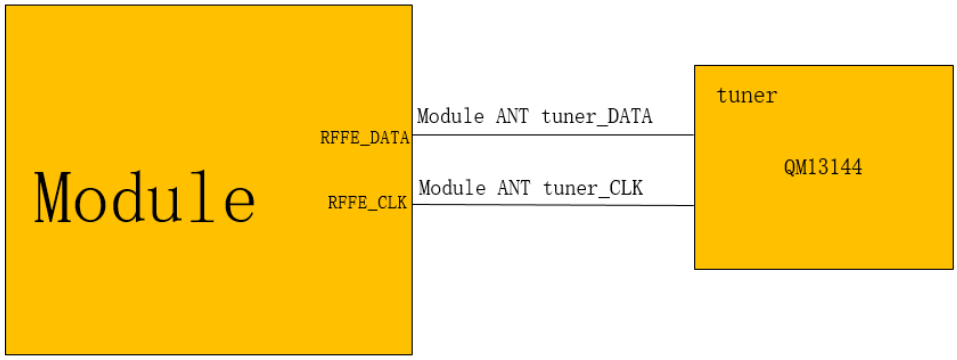

Figure 35: LGA package Tuner mipi interface

NOTE

1. When multiple Tuners are needed, pay attention to the distinction of the same device USID under the same group of mipi;
2. For details please refer to the Antenna Tuner Reference Design document and contact SIMCom support teams.

4.2.3 Antenna Requirements

The following table shows the requirements on 3G/4G antennas and GNSS antenna.

Table 40: 3G/4G/GNSS antennas

Parameter	Requirement
Operating Frequency	See **Table 37: SIM7912 operating frequencies** for each antenna
Direction	Omni Directional
Gain	> -3dBi (Avg)
Impedance	50 Ω
Efficiency	> 50 %
Max. Input Power	50W
VSWR	< 2
Isolation	20dB is preferred
Cable Insertion Loss <1GHz	<1dB
Cable Insertion Loss 1GHz~2.2GHz	<1.5dB
Cable Insertion Loss 2.3GHz~2.7GHz	<2dB
Cable Insertion Loss 3.3GHz~6GHz	<2.5dB

Table 41: GNSS antenna (for dedicated GNSS antenna only)*

Parameter	Requirement
Operating Frequency	L1: 1559~1609MHZ L5: 1166~1187MHz
Direction	Hemisphere, face to sky
Antenna Gain	> 2 dB_{ic}
Impedance	50 Ω
Efficiency	> 50 %
Max. Input Power	50W
VSWR	< 2
Polarization	RHCP or Linear
Noise Figure for Active Antenna	< 1.5
Total Gain for Active Antenna	< 17 dB
Cable Insertion Loss	<1.5dB

NOTE

*: These recommendations are for dedicated GNSS antenna which the application need best of class GNSS tracking performance.

5 Electrical Specifications

5.1 Absolute Maximum Ratings

Absolute maximum rating for digital and analog pins of module are listed in the following table:

Table 42: Absolute maximum ratings

Parameter	Min.	Typ.	Max.	Unit
Voltage at VBAT[1] pins	-	-	4.7	V
Voltage at USB_VBUS	-	-	5.5	V
Voltage at PWRKEY	-	-	2.1	V
Voltage at RESIN_N	-	-	1.9	V
Voltage at digital pins (GPIO, I2C, UART, I2S)	-	-	2.1	V
Voltage at digital pins SIM	-	-	3.05	V

NOTE

1. The VBAT include VBAT_BB and VBAT_RF pins.

5.2 Operating Conditions

Table 43: VBAT recommended operating ratings

Parameter	Min.	Typ.	Max.	Unit
Voltage at VBAT[1] pins	3.3	3.8	4.3	V
USB_VBUS	3.3	5.0	5.25	V

NOTE

1. The VBAT include VBAT_BB and VBAT_RF pins.

Table 44: 1.8V digital I/O characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage	1.17	-	2.1	V
V_{IL}	Low-level input voltage	0	-	0.63	V
V_{OH}	High-level output voltage	1.35	-	1.8	V
V_{OL}	Low-level output voltage	0	-	0.45	V

NOTE

These parameters are for digital interface pins, such as UART, I2C, I2S, SPI, and GPIOs (SIM_DET, SD_DET).

Table 45: Operating temperature

Parameter	Min.	Typ.	Max.	Unit
Normal operation temperature (3GPP compliant)	-30	+25	+75	℃
Extended operation temperature	-40	-	+85	℃
Storage temperature	-40	-	+90	℃

5.3 Operating Mode

5.3.1 Operating Mode Definition

The table below summarizes the various operating modes of module.

Table 46: Operating mode definition

Mode		Function
Normal operation	Sleep	AT command “AT+CSCLK=1” can be used to set the module to a sleep mode. In this case, the current consumption of module will be reduced to a very low level and the module can still receive paging message and SMS.
	Idle	Software is active. Module is registered to the network and ready to

		communicate.
	Talk	Connection between two subscribers is in progress. In this case, the power consumption depends on network settings such as DTX off/on, FR/EFR/HR, hopping sequences and antenna.
	Standby	Module is ready for data transmission, but no data is currently sent or received. In this case, power consumption depends on network settings.
	Data transmission	There is data transmission in progress. In this case, power consumption is related to network settings (e.g. power control level); uplink/downlink data rates, etc.
Minimum functionality mode		AT command “AT+CFUN=0” can be used to set the Module to a minimum functionality mode without removing the power supply. In this mode, the RF part of the Module will not work and the SIM card will not be accessible, but the serial port and USB port are still accessible. The power consumption in this mode is lower than normal mode.
Flight mode		AT command “AT+CFUN=4” or pulling down the W_disable1# pin can be used to set the Module to flight mode without removing the power supply. In this mode, the RF part of the Module will not work, but the serial port and USB port are still accessible. The power consumption in this mode is lower than normal mode.
Power off		Normally module will go into power off mode by sending the AT command “AT+CPOF” or pull down the FUL_CARD_POWER_OFF# pin. In this mode the power management unit shuts down the power supply, and software is not active. The serial port and USB are is not accessible.

5.3.2 Sleep Mode

In sleep mode, the current consumption of module will be reduced to a very low level.

Several hardware and software conditions must be satisfied in order to let module enter into sleep mode:

- UART condition
- USB condition
- Software condition

NOTE

Before designing, pay attention to how to realize sleeping/waking function.

5.3.3 Minimum Functionality Mode and Flight Mode

Minimum functionality mode ceases a majority function of Module, in order to minimizing the power consumption. This mode is set by the AT command which provides a choice of 3 different functionality levels.

- AT+CFUN=0: Minimum functionality
- AT+CFUN=1: Full functionality (Default)
- AT+CFUN=4: Flight mode

If module has been set to minimum functionality mode, the RF SIM card function will be closed while the serial port and USB are still available.

If module has been set to flight mode, the RF function will be closed, while the SIM card, the serial port and USB are still available.

When module is in minimum functionality or flight mode, it can return to full functionality by the AT command "AT+CFUN=1".

5.4 Current Consumption

The current consumptions are listed in the follows table.

Table 47: Current consumption on VBAT pins (VBAT=3.8V)

Description	Condition.	Typical	Unit
Power off mode	Power off	20	uA
GNSS mode	DPO	15	mA
Sleep mode (GNSS off, without connection USB)	WCDMA(AT+CFUN=0)	0.818	mA
	WCDMA DRX=1.28s	1.472	mA
	WCDMA DRX=2.56s	1.025	mA
	LTE-FDD(AT+CFUN=0)	0.698	mA
	LTE-FDD DRX=0.32s	3.243	mA
	LTE-FDD DRX=0.64s	2.106	mA
	LTE-FDD DRX=1.28s	1.617	mA
	LTE-FDD DRX=2.56s	1.041	mA
	LTE-TDD(AT+CFUN=0)	0.702	mA
	LTE-TDD DRX=0.32s	3.421	mA
	LTE-TDD DRX=0.64s	2.225	mA
	LTE-TDD DRX=1.28s	1.425	mA
	LTE-TDD DRX=2.56s	1.212	mA
Idle mode	WCDMA	12.504	mA

(GNSS off, without connection USB)	LTE FDD	15.465	mA
	LTE TDD	9.25	mA
HSDPA data			
WCDMA B2	@Power 22.30dBm Typical: 536 mA		
WCDMA B4	@Power 22.28dBm Typical: 586 mA		
WCDMA B5	@Power 23.05dBm Typical: 553 mA		
LTE data			
LTE-FDD B2	@5MHz 21.31dBm Typical : 528 mA @10MHz 21.25dBm Typical : 547 mA @20MHz 21.32dBm Typical : 546 mA		
LTE-FDD B4	@5MHz 23.12dBm Typical : 608 mA @10MHz 23.19dBm Typical : 632 mA @20MHz 22.81dBm Typical : 609 mA		
LTE-FDD B5	@5MHz 22.81dBm Typical : 541 mA @10MHz 22.98dBm Typical : 548 mA		
LTE-FDD B7	@5MHz 22.38dBm Typical : 696 mA @10MHz 22.95dBm Typical : 720 mA @20MHz 22.92dBm Typical : 785 mA		
LTE-FDD B12	@5MHz 22.07dBm Typical : 542 mA @10MHz 22.09dBm Typical : 552 mA		
LTE-FDD B13	@5MHz 22.70dBm Typical : 538 mA @10MHz 22.60dBm Typical : 522 mA		
LTE-FDD B14	@5MHz 22.89dBm Typical : 528 mA @10MHz 23.05dBm Typical : 536 mA		
LTE-FDD B17	@5MHz 22.54dBm Typical : 526 mA @10MHz 22.50dBm Typical : 531 mA		
LTE-FDD B25	@5MHz 23.89dBm Typical : 602 mA @10MHz 23.76dBm Typical : 645 mA @20MHz 23.78dBm Typical : 744 mA		
LTE-FDD B26	@5MHz 22.96dBm Typical : 607 mA @10MHz 22.83dBm Typical : 598 mA		
LTE-TDD B41	@5MHz 22.63dBm Typical : 711 mA @10MHz 22.59dBm Typical : 720 mA @20MHz 22.49dBm Typical : 714 mA		
LTE-FDD B48	@5MHz 22.77dBm Typical : 683 mA @10MHz 22.23dBm Typical : 688 mA @20MHz 20.86dBm Typical : 676 mA		
LTE-FDD B66	@5MHz 22.43dBm Typical : 737 mA @10MHz 22.39dBm Typical : 762 mA @20MHz 22.23dBm Typical: 780 mA		
LTE-TDD B71	@5MHz 22.18dBm Typical : 524 mA @10MHz 22.10dBm Typical : 520 mA @20MHz 22.25dBm Typical : 517 mA		

NOTE

1. The VBAT include VBAT_BB and VBAT_RF pins.
2. The current consumption of Table 47: **Current consumption on VBAT pins (VBAT=3.8V)** based on SIM7912E and it is only for reference, please refer to actual current consumption.

5.5 RF Output Power

The RF output power is shown in the following table.

Table 48: Conducted output power

Frequency	Max	Min
WCDMA Bands	24dBm + 1/-3dB	< -50dBm
LTE-FDD Bands	23dBm + 2/-2dB	< -40dBm
LTE-TDD Bands	23dBm + 2/-2dB	< -40dBm

5.6 Conducted Receive Sensitivity

Module conducted RF receiving sensitivity is fully meet 3GPP specification. Customers can get more details by check 3GPP official website http://www.3gpp.org/.

5.7 Thermal Design

Make sure that the module can reach maximum work performance under extended temperature or extreme conditions for a long time, thermal dissipation design is very important.

There are some design rules to enhance thermal dissipation performance:

- Keep the module away from other heat sources such as battery, power, AP, etc.
- All the GND pins of the module should be connected.
- Add enough through GND via on the main PCB. Via material is very important solid copper and stacked via is better.
- Make sure maximize airflow around the module.
- Recommend use heat dissipation material connect to the customers' device on the top side of the module to enhance the heat dissipation. Large heat dissipation area is better.
- Chose a high effective heat dissipation material is better such as heat pipe, graphite sheets.

5.8 ESD

Module is sensitive to ESD in the process of storage, transporting, and assembling. When module is mounted on the customers' main board, the ESD components should be placed closed to the connectors which human body may touch, such as SIM card socket, SD card socket, audio jacks, switches, USB interface, etc. The following table shows the module ESD measurement performance.

Table 49: The ESD performance measurement table (temperature: 25℃, humidity: 45%)

Part	Contact discharge(kV)	Air discharge(kV)
VBAT, GND	±4	±8
Antenna Interfaces	±4	±8
Other PADs	±2	±4

NOTE

Test conditions:
1. The external of the module has surge protection diodes and ESD protection diodes.

2. The data in Table 49: **The ESD performance measurement table (temperature: 25℃, humidity: 45%)** were tested using SIMCom EVB.

6 Manufacturing

6.1 Top and Bottom View of Module

Figure 36: Top and bottom view of Module

6.2 Label Description Information

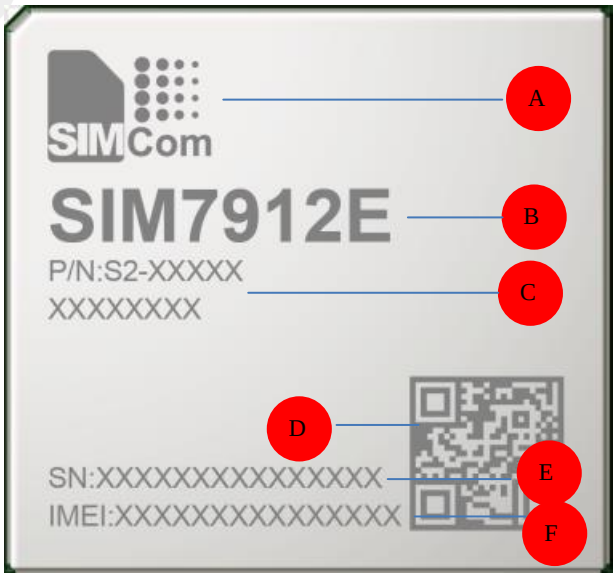

Figure 37: Label description of module

Table 50: Label description of module information

No.	Description
A	LOGO
B	Project name
C	Product code
D	QR code
E	Serial number
F	International mobile equipment identity

NOTE

Figure 36: Top and bottom view of and Figure 37: Label description of module are the effect diagrams of the module, for reference only. Please refer to the actual product for appearance.

6.3 Recommended PCB Footprint

The following figure shows the PCB footprint of SIM7912&SIM7906.

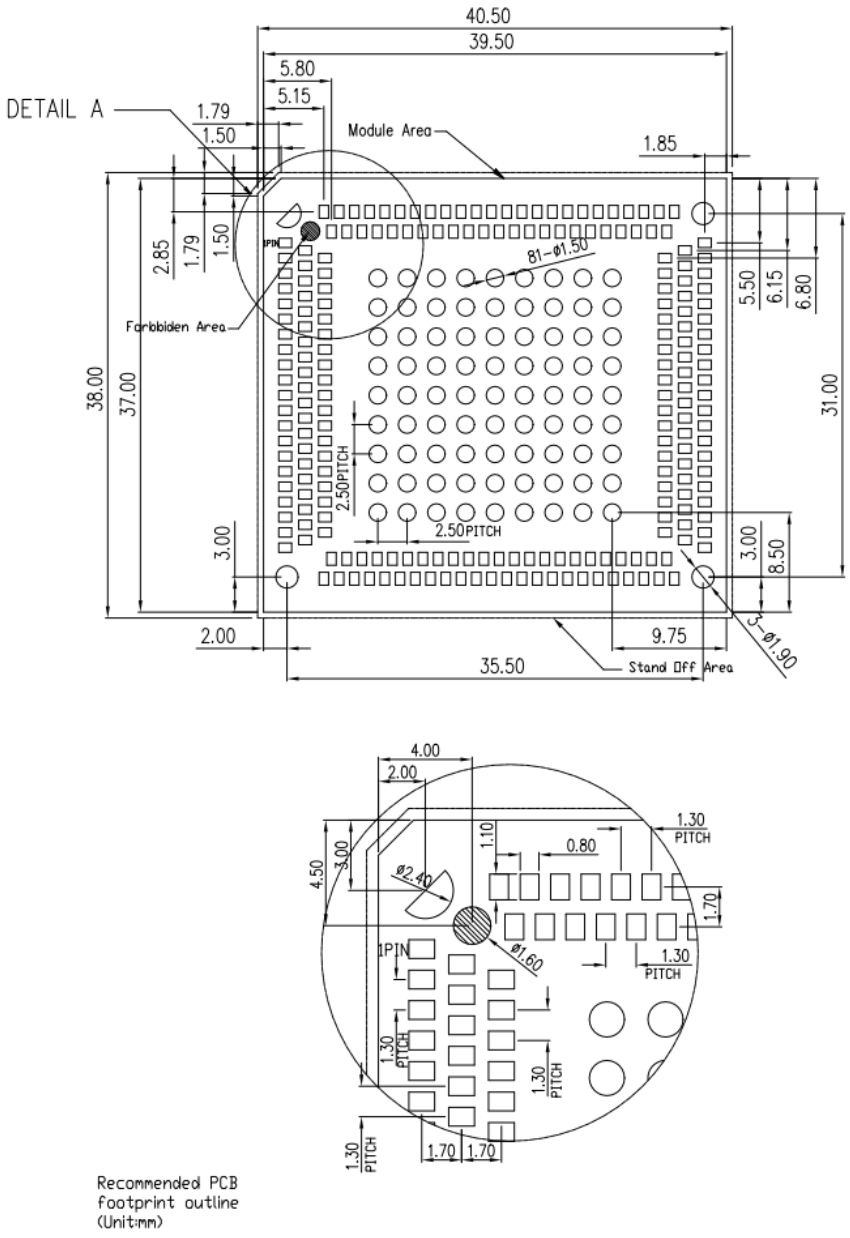

Figure 38: Recommended PCB footprint

6.4 Recommended SMT Stencil

The following figure shows the SMT stencil of SIM7912&SIM7906.

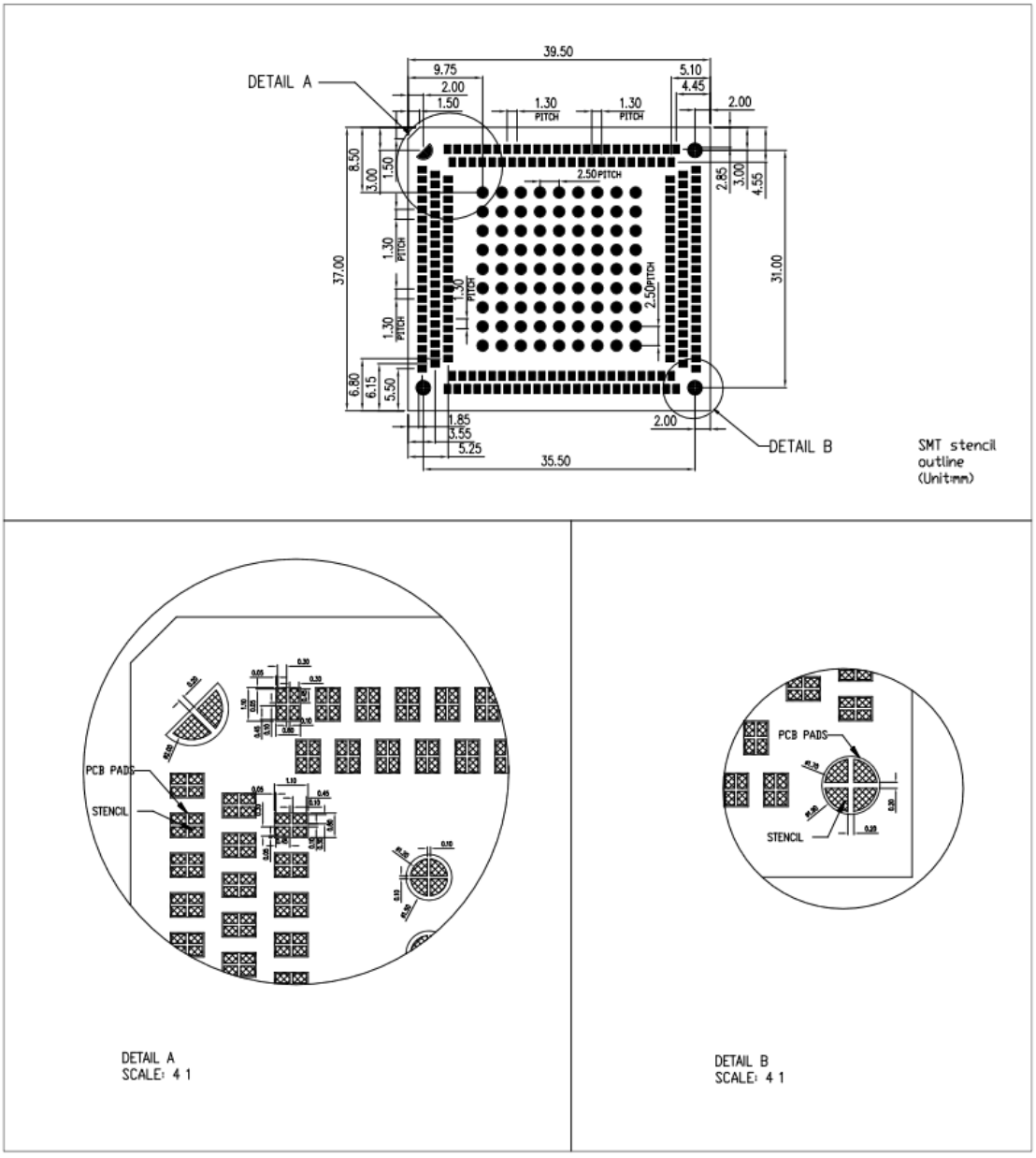

Figure 39: Recommended SMT stencil

6.5 Recommended SMT Reflow Profile

The following figure shows the SMT reflow profile of SIM7912&SIM7906.

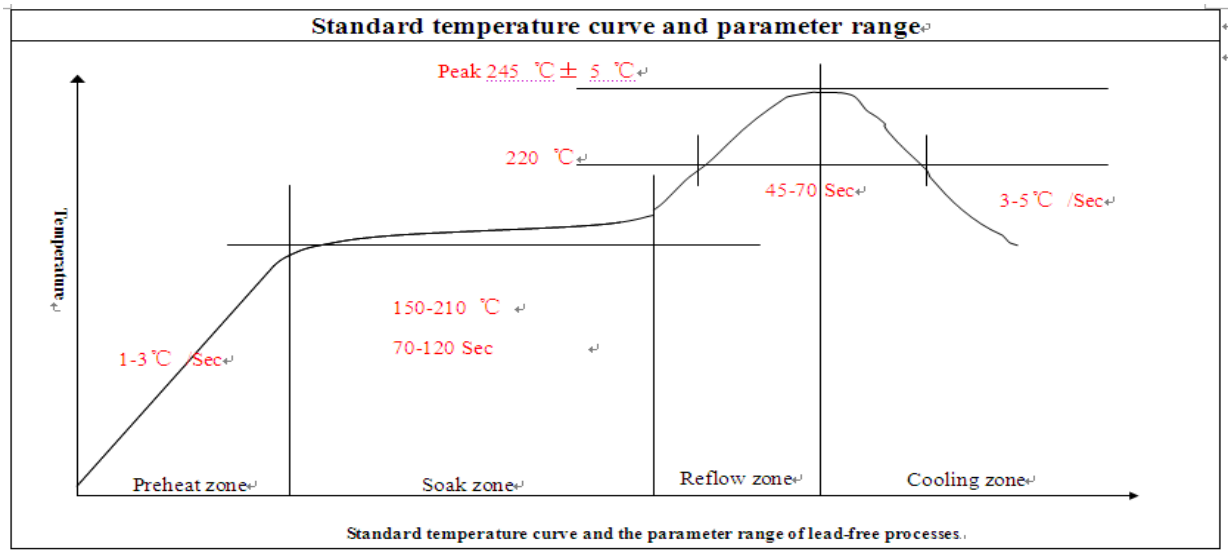

Figure 40: Recommended SMT reflow profile

NOTE

Refer to “Module secondary-SMT-UGD” for more information about the module shipping and manufacturing.

6.6 Moisture Sensitivity Level (MSL)

Module is susceptible to damage induced by absorbed moisture and high temperature. A package's moisture-sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 51.

Table 51: MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤+30℃/85% RH
2	1 year	≤+30℃/60% RH
2a	4 weeks	≤+30℃/60% RH
3	168 hours	≤+30℃/60% RH
4	72 hours	≤+30℃/60% RH
5	48 hours	≤+30℃/60% RH
5a	24 hours	≤+30℃/60% RH
6	Mandatory bake before use. After bake, it must be reflowed within the time limit specified on the label.	≤+30℃/60% RH

The device samples are currently classified as MSL3 at 255 (+5, -0)°C, following the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

6.7 Baking Requirements

It is necessary to bake modules if the prescribed time limit has been exceeded. The baking conditions are specified in Table 52. Note that if baking is required, the devices must be transferred into trays that can be baked to at least 125°C.

Table 52: Baking requirements

Baking conditions options	Duration
40°C±5°C, <5% RH	192 hours
120°C±5°C, <5% RH	4 hours

7 Packaging

Module supports tray packaging. The packaging process is shown in the following figures.

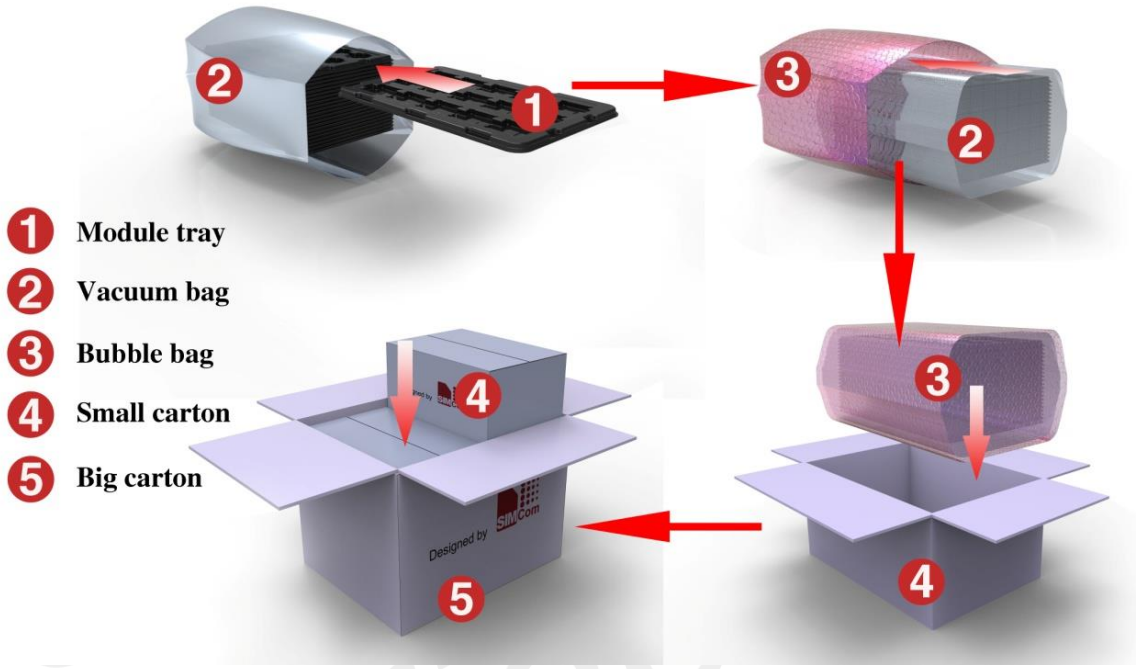

Figure 41: Packaging process

Module tray drawing：

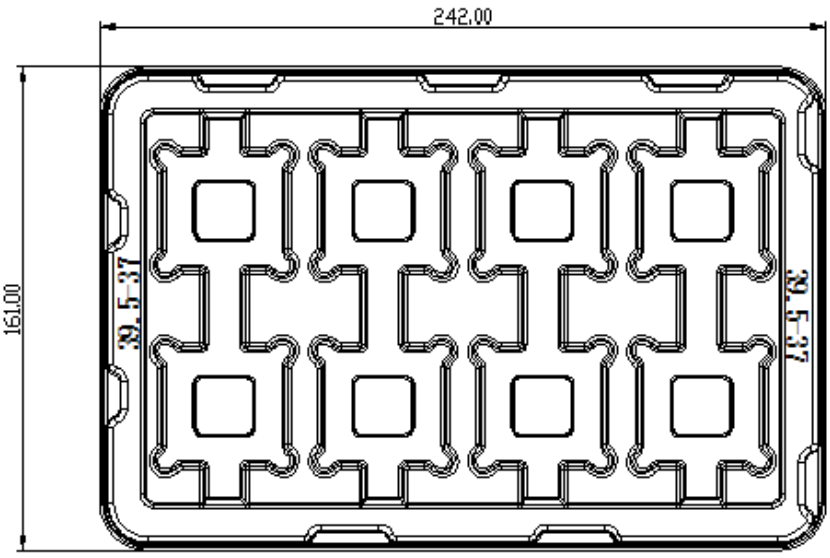

Figure 42: Module tray drawing

Table 53: Tray size

Length（±3mm）	Width（±3mm）	Number
242.0	161.0	8

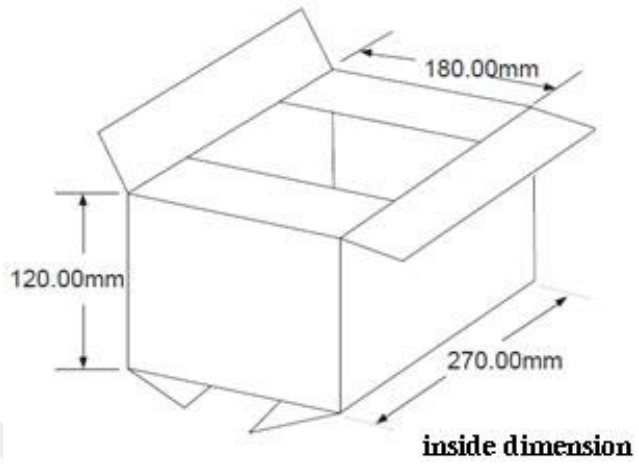

Figure 43: Small carton drawing

Table 54: Small carton size

Length（±10mm）	Width（±10mm）	Height（±10mm）	Number
270	180	120	8*19-2=150

Big carton drawing：

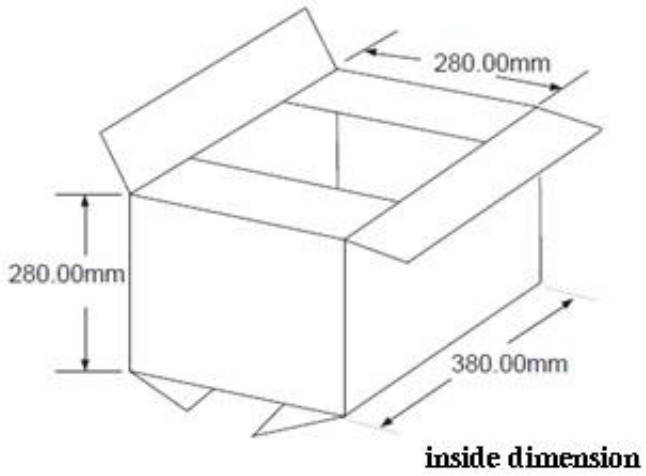

Figure 44: Big carton drawing

Table 55: Big carton size

Length（±10mm）	Width（±10mm）	Height（±10mm）	Number
380	280	280	150*4=600

8 Appendix

8.1 Coding Schemes and Maximum Net Data Rates over Air Interface

Table 56: Coding schemes and maximum net data rates over air interface

HSDPA device category	Max data rate（peak）	Modulation type
Category 1	1.2Mbps	16QAM,QPSK
Category 2	1.2Mbps	16QAM,QPSK
Category 3	1.8Mbps	16QAM,QPSK
Category 4	1.8Mbps	16QAM,QPSK
Category 5	3.6Mbps	16QAM,QPSK
Category 6	3.6Mbps	16QAM,QPSK
Category 7	7.2Mbps	16QAM,QPSK
Category 8	7.2Mbps	16QAM,QPSK
Category 9	10.2Mbps	16QAM,QPSK
Category 10	14.4Mbps	16QAM,QPSK
Category 11	0.9Mbps	QPSK
Category 12	1.8Mbps	QPSK
Category 13	17.6Mbps	64QAM
Category 14	21.1Mbps	64QAM
Category 15	23.4Mbps	16QAM
Category 16	28Mbps	16QAM
Category 17	23.4Mbps	64QAM
Category 18	28Mbps	64QAM
Category 19	35.5Mbps	64QAM
Category 20	42Mbps	64QAM
Category 21	23.4Mbps	16QAM
Category 22	28Mbps	16QAM
Category 23	35.5Mbps	64QAM
Category 24	42.2Mbps	64QAM
HSUPA device category	**Max data rate（peak）**	**Modulation type**
Category 1	0.96Mbps	QPSK
Category 2	1.92Mbps	QPSK
Category 3	1.92Mbps	QPSK

Category 4	3.84Mbps	QPSK
Category 5	3.84Mbps	QPSK
Category 6	5.76Mbps	QPSK
LTE-FDD device category (Downlink)	**Max data rate（peak）**	**Modulation type**
Category 1	10Mbps	QPSK/16QAM/64QAM
Category 2	50Mbps	QPSK/16QAM/64QAM
Category 3	100Mbps	QPSK/16QAM/64QAM
Category 4	150Mbps	QPSK/16QAM/64QAM
Category 5	300Mbps	QPSK/16QAM/64QAM
Category 6	300Mbps	QPSK/16QAM/64QAM
Category 12	600Mbps	QPSK/16QAM/64QAM/256QAM
LTE-FDD device category (Uplink)	**Max data rate（peak）**	**Modulation type**
Category 1	5Mbps	QPSK/16QAM
Category 2	25Mbps	QPSK/16QAM
Category 3	50Mbps	QPSK/16QAM
Category 4	50Mbps	QPSK/16QAM
Category 5	75Mbps	QPSK/16QAM/64QAM
Category 6	50Mbps	QPSK/16QAM
Category 12	100 Mbps	QPSK/16QAM/64QAM

8.2 Related Documents

Table 57: Related documents

NO.	Title	Description
[1]	SIM7912&SIM7906 Series AT Command Manual	AT Command Manual
[2]	ITU-T Draft new ecommendation.25ter	Serial asynchronous automatic dialing and control
[3]	3GPP TS 51.010-1	Digital cellular telecommunications system (Release 5); Mobile Station (MS) conformance specification
[4]	3GPP TS 34.124	Electromagnetic Compatibility (EMC) for mobile terminals and ancillary equipment.
[5]	3GPP TS 34.121	Electromagnetic Compatibility (EMC) for mobile terminals and ancillary equipment.
[6]	3GPP TS 34.123-1	Technical Specification Group Radio Access Network; Terminal conformance specification; Radio transmission and reception (FDD)
[7]	3GPP TS 34.123-3	User Equipment (UE) conformance specification; Part 3: Abstract Test Suites.
[8]	EN 301 908-02 V2.2.1	Electromagnetic compatibility and Radio Spectrum Matters (ERM); Base Stations (BS) and User Equipment (UE) for IMT-2000. Third Generation cellular networks; Part 2: Harmonized EN for IMT-2000, CDMA Direct Spread (UTRA FDD) (UE) covering essential requirements of article 3.2 of the R&TTE Directive
[9]	EN 301 489-24 V1.2.1	Electromagnetic compatibility and Radio Spectrum Matters (ERM); Electromagnetic Compatibility (EMC) standard for radio equipment and services; Part 24: Specific conditions for IMT-2000 CDMA Direct Spread (UTRA) for Mobile and portable (UE) radio and ancillary equipment
[10]	IEC/EN60950-1(2001)	Safety of information technology equipment (2000)
[11]	3GPP TS 51.010-1	Digital cellular telecommunications system (Release 5); Mobile Station (MS) conformance specification
[12]	GCF-CC V3.23.1	Global Certification Forum – Certification Criteria
[13]	2002/95/EC	Directive of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS)
[14]	SIM7912&SIM7906_LGA Antenna Port Mapping and Deign Guide	Antenna design guidelines for diversity receiver system

[15]	SIM7912&SIM7906_CA COMBO list	CA list for SIM7912 and SIM7906
[16]	Antenna Tuner reference design	Antenna tuning method and antenna tuning reference design example

8.3 Terms and Abbreviations

Table 58: Terms and abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
CS	Coding Scheme
CTS	Clear to Send
DRX	Discontinuous Reception
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FDD	Frequency Division Dual
FR	Full Rate
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
HR	Half Rate
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IMEI	International Mobile Equipment Identity
LTE	Long Term Evolution
MDIO	Management Data Input/Output
MMD	MDIO manageable device
MO	Mobile Originated
MSB	Most Significant Bit
PCB	Printed Circuit Board
PCIe	Peripheral Component Interface Express
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
SDIO	Secure Digital Input and Output
SIM	Subscriber Identification Module
SMS	Short Message Service
SPI	serial peripheral interface
TDD	Time Division Dual
TX	Transmit Direction
UART	Universal Asynchronous Receiver & Transmitter
VSWR	Voltage Standing Wave Ratio
SM	SIM phonebook

HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
WCDMA	Wideband Code Division Multiple Access
SIM	Universal subscriber identity module
UMTS	Universal mobile telecommunications system
UART	Universal asynchronous receiver transmitter
LB	Low Frequency Band
MHB	Middle and High Frequency Band
UHB	Ultra High Frequency Band
LAA	Limited Access Authorization
TRX	Transmit and Receive signal
UL-MIMO	Uplink- Multiple Input Multiple Output
DL-MIMO	Downlink- Multiple Input Multiple Output

8.4 Safety Caution

Table 59: Safety caution

Marks	Requirements
	When in a hospital or other health care facility, observe the restrictions about the mobiles. Switch the cellular terminal or mobile off, medical equipment may be sensiti not operate normally due to RF energy interference.
	Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it is sv off. The operation of wireless appliances in an aircraft is forbidden to prevent interferen communication systems. Forgetting to think much of these instructions may impact th safety, or offend local legal action, or both.
	Do not operate the cellular terminal or mobile in the presence of flammable gases or Switch off the cellular terminal when you are near petrol stations, fuel depots, chemica or where blasting operations are in progress. Operation of any electrical equipn potentially explosive atmospheres can constitute a safety hazard.
	Your cellular terminal or mobile receives and transmits radio frequency energy while sv on. RF interference can occur if it is used close to TV sets, radios, computers or other equipment.
	Road safety comes first! Do not use a hand-held cellular terminal or mobile when dr vehicle, unless it is securely mounted in a holder for hands free operation. Before ma call with a hand-held terminal or mobile, park the vehicle.
	Mobiles operate over radio frequency signals and cellular networks and cannot be guar to connect in all conditions, especially with a mobile fee or an invalid SIM card. While y in this condition and need emergent help, please remember to use emergency calls. I to make or receive calls, the cellular terminal or mobile must be switched on and in a area with adequate cellular signal strength. Some networks do not allow for emergency call if certain network services or phone fe are in use (e.g. lock functions, fixed dialing etc.). You may have to deactivate those fe before you can make an emergency call. Also, some networks require that a valid SIM card be properly inserted in the cellular t or mobile.

FCC Caution.

§ 15.19 Labelling requirements.

This device complies with part 15 of the FCC Rules. Operation is subject to the condition that this device does not cause harmful interference.

§ 15.21 Information to user.

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

§ 15.105 Information to the user.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-Reorient or relocate the receiving antenna.

-Increase the separation between the equipment and receiver.

-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-Consult the dealer or an experienced radio/TV technician for help. Body-worn Operation

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated withmini mum distance 20cm between the radiator & your body

This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this Modular, including any applicable source-based time averaging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.

if the host is marketed so that end users do not have straight forward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: Contains Transmitter Module FCC ID: 2AJYU-8XM0001 or Contains FCC ID: 2AJYU-8XM0001 must be used.