SIM7600G/G-H_Hardware Design_V1.01

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FCC Caution:

(1)Exposure to Radio Frequency Radiation. This equipment must be installed and operated in accordance with provided instructions and the antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be collocated or operating in conjunction with any other antenna or transmitter. End-users and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance.

(2) Any changes or modifications not expressly approved by the grantee of this device could void the user's authority to operate the equipment.

(3) This Transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

(4) Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user authority to operate the equipment.

(6) Labelling requirements:This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

(6) if the host is marketed so that end users do not have straight forward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: Contains Transmitter Module FCC ID: 2AJYU-8PYA004 or Contains FCC ID: 2AJYU-8PYA004 must be used.

This product is suitable for collocation internal and external antenna.Gain the scope of the reference is as follows:

Frequency Band	Antenna Gain(dBi)
GSM850	-1
GSM1900	6
GPRS850 4TS	-1
GPRS1900 4TS	6
WCDMA Band2	10
WCDMA Band4	9
WCDMA Band5	7
LTE Band2	10
LTE Band4	11
LTE Band5	7
LTE Band7	10
LTE Band12	6
LTE Band13	6
LTE Band25	10
LTE Band26	8
LTE Band41	9
LTE Band66	9

Contents

1 Introduction

This document describes the electronic specifications, RF specifications, interfaces, mechanical characteristics and testing results of the SIMCom MODULE. With the help of this document and other software application notes/user guides, users can understand and use MODULE to design and develop applications quickly.

1.1 Product Outline

Aimed at the global market, the MODULE support GSM, WCDMA, LTE-TDD and LTE-FDD. Users can choose the MODULE according to the wireless network configuration. The supported radio frequency bands are described in the following table.

Table 1: Module frequency bands

Standard	Frequency	SIM7600G	SIM7600G-H
GSM	850MHz	√	√
	900MHz	√	√
	1800M Hz	√	√
	1900M Hz	√	√
WCDMA	B1	√	√
	B2	√	√
	B4	√	√
	B5	√	√
	B6	√	√
	B8	√	√
	B19	√	√
LTE	FDD B1	√	√
	FDD B2	√	√
	FDD B3	√	√
	FDD B4	√	√
	FDD B5	√	√
	FDD B7	√	√
	FDD B8	√	√
	FDD B12	√	√
	FDD B13	√	√
	FDD B18	√	√
	FDD B19	√	√
	FDD B20	√	√
	FDD B25	√	√

	FDD B26	√	√
	FDD B28	√	√
	FDD B66	√	√
	TDD B34	√	√
	TDD B38	√	√
	TDD B39	√	√
	TDD B40	√	√
	TDD B41	√	√
Category		CAT1	CAT4

With a small physical dimension of 30*30*2.9 mm and with the functions integrated, the MODULE can meet almost any space requirement in users' applications, such as smart phone, PDA, industrial handheld, machine-to-machine and vehicle application, etc.

1.2 Hardware Interface Overview

The interfaces are described in detail in the next chapters include:

- Power Supply
- USB2.0 Interface
- UART Interface
- MMC/SD Interface
- SDIO Interface
- USIM Interface
- SPI Interface
- GPIO
- ADC
- LDO Power Output
- Current Sink Source
- PCM Interface
- SPI Interface
- I2C Interface
- HSIC Interface
- SGMII Interface

1.3 Hardware Block Diagram

The block diagram of the MODULE is shown in the figure below.

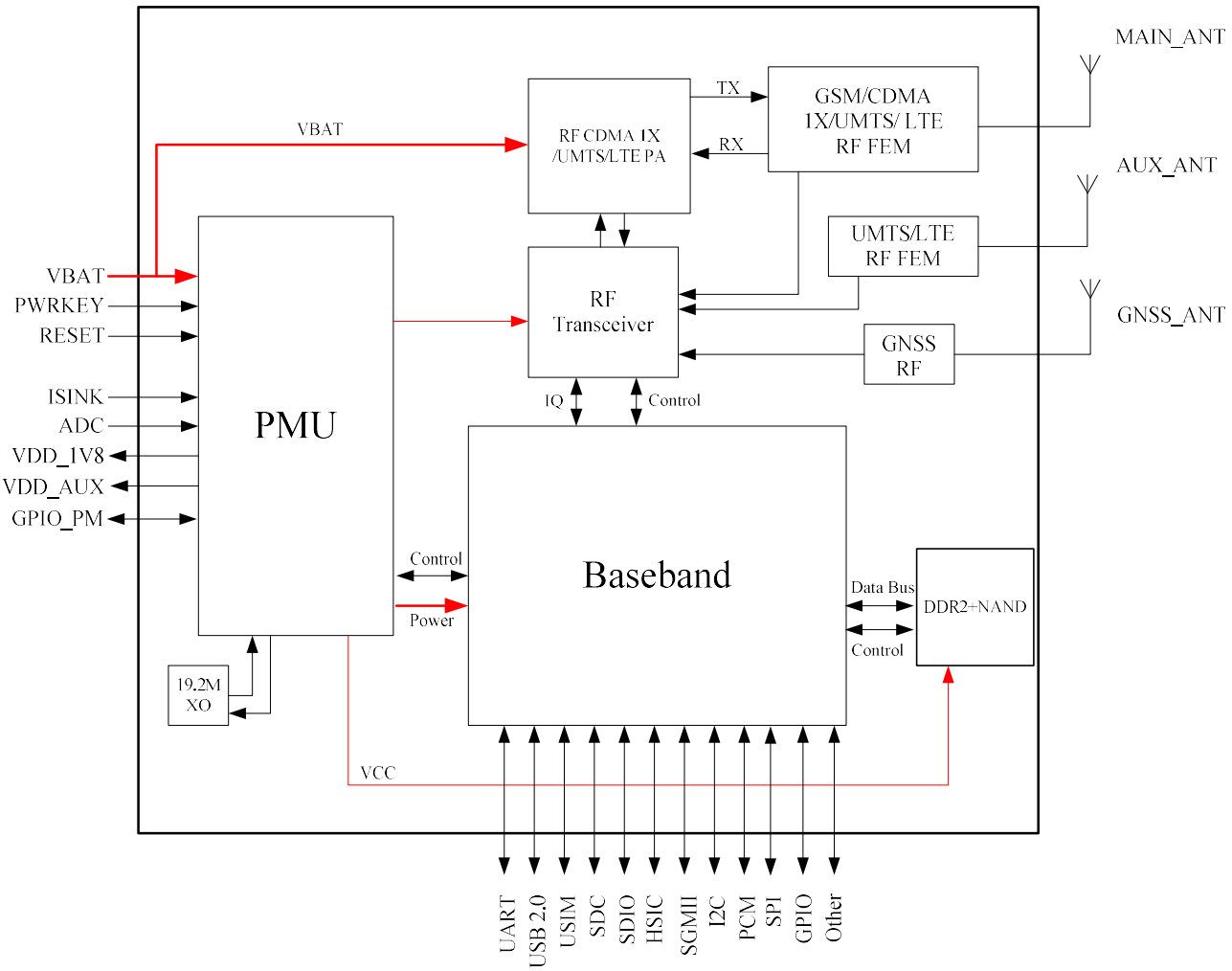


Figure 1: MODULE block diagram

1.4 Functional Overview

Table 2: General features

Feature	Implementation
Power supply	Single supply voltage 3.4～4.2V, Recommend supply voltage 3.8V
Power saving	Current in sleep mode : <5mA
Radio frequency bands	Please refer to the table 1
Transmitting power	GSM/GPRS power class: --GSM850: 4 (2W) --EGSM900: 4 (2W) --DCS1800: 1 (1W) --PCS1900: 1 (1W) EDGE power class: --GSM850: E2 (0.5W) --EGSM900: E2 (0.5W) --DCS1800: E1 (0.4W) --PCS1900: E1 (0.4W) UMTS power class: --WCDMA :3 (0.25W) LTE power class: 3 (0.25W)
Data Transmission Throughput	GPRS multi-slot class 12 EDGE multi-slot class 12 UMTS R99 speed: 384 kbps DL/UL HSPA+: 5.76 Mbps(UL), 42 Mbps(DL) HSDPA/HSUPA: 2.2 Mbps(UL), 2.8 Mbps(DL) LTE CAT 1: 10 Mbps(DL) 5 Mbps(UL) LTE CAT 4 :150 Mbps (DL) 50 Mbps (UL)
Antenna	GSM/UMTS/LTE main antenna. UMTS/LTE auxiliary antenna GNSS antenna
GNSS	GNSS engine (GPS,GLONASS and BD) Protocol: NMEA 0183
SMS	MT, MO, CB, Text and PDU mode SMS storage: USIM card or ME(default) Transmission of SMS alternatively over CS or PS.
USIM interface	Support identity card: 1.8V/ 3V
USIM application toolkit	Support SAT class 3, GSM 11.14 Release 98 Support USAT
Phonebook management	Support phonebook types: DC,MC,RC,SM,ME,FD,ON,LD,EN

Audio feature	Support PCM interface Only support PCM master mode and short frame sync, 16-bit linear data formats
UART interface	A full modem serial port by default Baud rate: 300bps to 4Mbps(default:115200bps) Autobauding baud rate: 9600,19200,38400,57600,115200bps Can be used as the AT commands or data stream channel Support RTS/CTS hardware handshake Multiplex ability according to GSM 07.10 Multiplexer Protocol
MMC/SD	Support MMC and SD cards with 2.85 V on SD port
SDIO	Support SDIO with 1.8 V only on SDIO port
USB	USB 2.0 high speed interface, Can used be send AT command, Software update, GNSS NMEA,USB voice function etc.
Firmware upgrade	Firmware upgrade over USB interface or FOTA
Physical characteristics	Size:30*30*2.9m Weight:5.7 g
Temperature range	Normal operation temperature: -30°C to +80°C Extended operation temperature: -40°C to +85°C* Storage temperature -45°C to +90°C

Note: Module is able to make and receive voice calls, data calls, SMS and make GPRS/UMTS/HSPA+/LTE traffic in -40℃ ~ +85℃. The performance will be reduced slightly from the 3GPP specifications if the temperature is outside the normal operating temperature range and still within the extreme operating temperature range.

2 Package Information

2.1 Pin Assignment Overview

All functions of the MODULE will be provided through 135 pads that will be connected to the users' platform. The following Figure is a high-level view of the pin assignment of the MODULE.

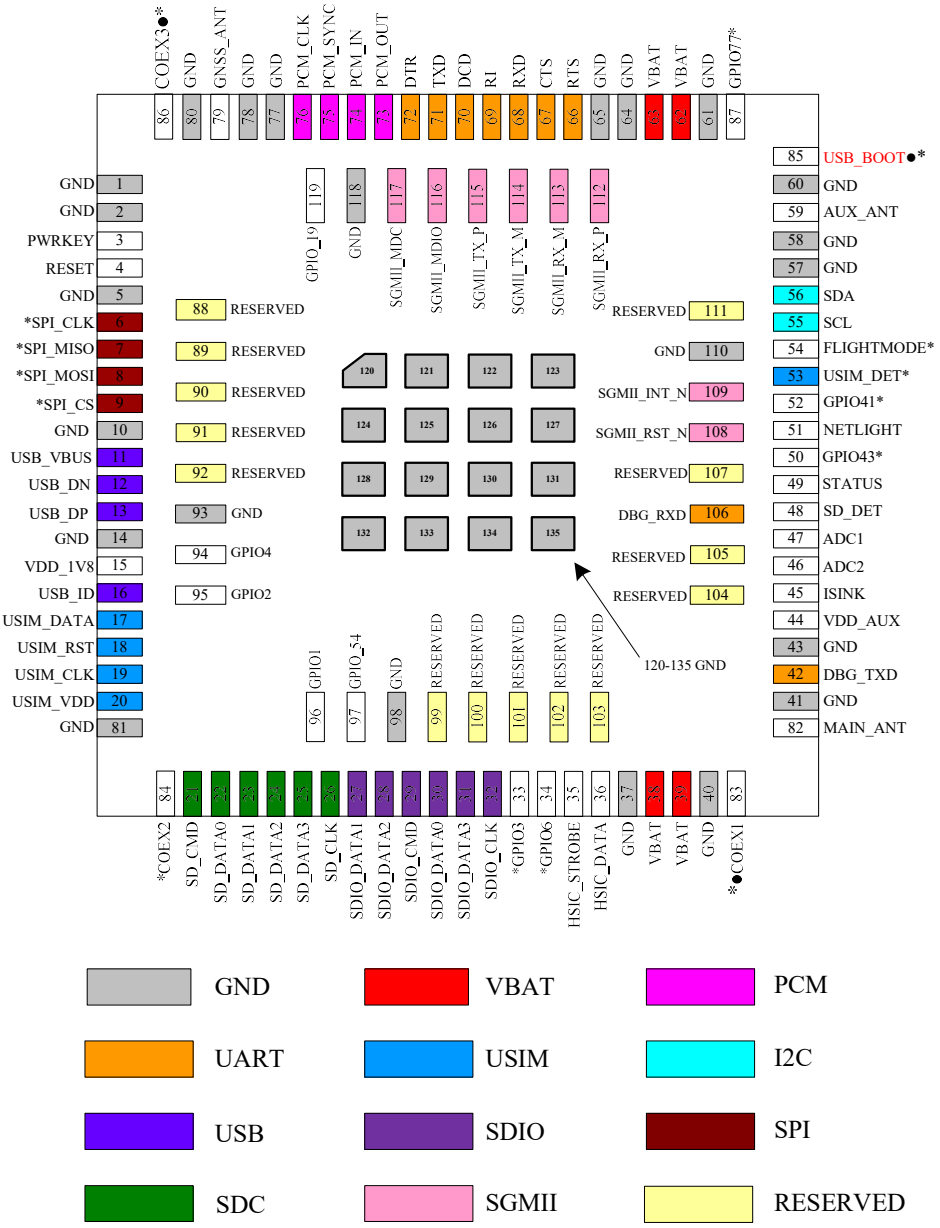


Figure 2: Pin assignment overview

Table 3: Pin definition

Pin No.	Pin name	Pin No.	Pin name
1	GND	2	GND
3	PWRKEY	4	RESET
5	GND	6	SPI_CLK*
7	SPI_MISO*	8	SPI_MOSI*
9	SPI_CS*	10	GND
11	USB_VBUS	12	USB_DN
13	USB_DP	14	GND
15	VDD_1V8	16	USB_ID
17	USIM_DATA	18	USIM_RST
19	USIM_CLK	20	USIM_VDD
21	SD_CMD	22	SD_DATA0
23	SD_DATA1	24	SD_DATA2
25	SD_DATA3	26	SD_CLK
27	SDIO_DATA1	28	SDIO_DATA2
29	SDIO_CMD	30	SDIO_DATA0
31	SDIO_DATA3	32	SDIO_CLK
33	GPIO3*	34	GPIO6*
35	HSIC_STROBE	36	HSIC_DATA
37	GND	38	VBAT
39	VBAT	40	GND
41	GND	42	DBG_TXD
43	GND	44	VDD_AUX
45	ISINK	46	ADC2
47	ADC1	48	SD_DET
49	STATUS	50	GPIO43*
51	NETLIGHT	52	GPIO41*
53	USIM_DET*	54	FLIGHTMODE*
55	SCL	56	SDA
57	GND	58	GND
59	AUX_ANT	60	GND
61	GND	62	VBAT
63	VBAT	64	GND
65	GND	66	RTS
67	CTS	68	RXD

69	RI	70	DCD
71	TXD	72	DTR
73	PCM_OUT	74	PCM_IN
75	PCM_SYNC	76	PCM_CLK
77	GND	78	GND
79	GNSS_ANT	80	GND
81	GND	82	MAIN_ANT
83	COEX1●*	84	COEX2*
85	BOOT_CFG0●*	86	COEX3●*
87	GPIO77	88	RESERVED
89	RESERVED	90	RESERVED
91	RESERVED	92	RESERVED
93	GND	94	GPIO4
95	GPIO2	96	GPIO1
97	GPIO_54	98	GND
99	RESERVED	100	RESERVED
101	RESERVED	102	RESERVED
103	RESERVED	104	RESERVED
105	RESERVED	106	DBG_ RXD
107	RESERVED	108	SGMII_RST_N
109	SGMII_INT_N	110	GND
111	RESERVED	112	SGMII_RX_P
113	SGMII_RX_M	114	SGMII_TX_M
115	SGMII_TX_P	116	SGMII_MDIO
117	SGMII_MDC	118	GND
119	GPIO_19	120	GND
121	GND	122	GND
123	GND	124	GND
125	GND	126	GND
127	GND	128	GND
129	GND	130	GND
131	GND	132	GND
133	GND	134	GND
135	GND		

NOTE: ● Means Before the normal power up, COEX1, COEX3 or BOOT_CFG0 cannot be pulled up, otherwise module will not be powered up normally.

**** Means that pins has MUX function.***

2.2 Pin Description

Table 4: IO parameters definition

Pin type	Description
PI	Power input
PO	Power output
AI	Analog input
AIO	Analog input/output
I/O	Bidirectional input /output
DI	Digital input
DO	Digital output
DOH	Digital output with high level
DOL	Digital output with low level
PU	Pull up
PD	Pull down

Table 5: Pin description

Pin name	Pin No.	Default status	Description	Comment
Power supply				
VBAT	38,39, 62,63	PI	Power supply, voltage range: 3.4～4.2V.	
VDD_AUX	44	PO	LDO power output for other external circuits with Max 150mA current output. Its output voltage is 2.85V by default.（The voltage can be configured from 1.7V to 3.05V by AT command）.	If used SGMII function ,this pin used for SGMII function. If unused, keep it open.
VDD_1V8	15	PO	1.8 output with Max 50mA current output for external circuit, such as level shift circuit.	If unused, keep it open.
GND	1,2,5, 10,14,37 ,40,41,4 3,57,58, 60,61,64 ,65,77,7 8,80,81, 93,96,11 0,118,12 0,121,12 2,123,12 4,125,12 6,127,12 8,129,13		Ground	

	0,131,132,133,134135			
System Control				
PWRKEY	3	DI,PU	System power on/off control input, active low.	The high voltage is 0.8V;
RESET	4	DI, PU	System reset control input, active low.	RESET has been pulled up to 1.8V via 40Kohm resistor internally.
SD interface				
SD_CMD	21	I/O,PD	SDIO command	If unused, keep them open.
SD_DATA0	22	I/O,PD	SDIO data	
SD_DATA1	23	I/O,PD		
SD_DATA2	24	I/O,PD		
SD_DATA3	25	I/O,PD		
SD_CLK	26	DO	SDIO clock	
SD_DET	48	DI,PU	SD card insertion detect H: SD card is removed L: SD card is inserted	
USIM interface				
USIM_DATA	17	I/O,PU	USIM Card data I/O, which has been pulled up via a 10KR resistor to USIM_VDD internally. Do not pull it up or down externally.	All lines of USIM interface should be protected against ESD.
USIM_RST	18	DO,PD	USIM Reset	
USIM_CLK	19	DO,PD	USIM clock	
USIM_VDD	20	PO,PD	Power output for USIM card, its output Voltage depends on USIM card type automatically. Its output current is up to 50mA.	
SPI interface				
SPI_CLK*	6	DO	SPI clock output	Default SPI Optional: BT uart function
SPI_MISO*	7	DI	SPI master in/slave out data	
SPI_MOSI*	8	DO	SPI master out/slave in data	
SPI_CS*	9	DO	SPI chip-select output	
USB				
USB_VBUS	11	AI	Valid USB detection input with 3.0~5.25V detection voltage	
USB_DN	12	AI, AO	Negative line of the differential, bi-directional USB signal.	

USB_DP	13	AI, AO	Positive line of the differential, bi-directional USB signal.	
USB_ID	16	AI	High-speed USB ID input	Keep it open.
SGMII interface				
SGMII_RX_P	112	AI	SGMII receive – positive	If unused, keep them open.
SGMII_RX_M	113	AI	SGMII receive - negative	
SGMII_TX_M	114	AO	SGMII transmit - negative	
SGMII_TX_P	115	AO	SGMII transmit– positive	
SGMII_RST_N	108	DO	Ethernet PHY reset	External 1.5K pull-up resistor from 3.3V/2.5V to MDIO_DATA and 10K pull-up resistor from VDD_1V8 to ETH_INT_N are needed when the Ethernet PHY is connected. If unused, please keep them open.
SGMII_INT_N	109	DI,PU	Ethernet PHY interrupt	
SGMII_MDIO	116	DIO	Management data input/output-data	
SGMII_MDC	117	DO	Management data input/output-clock	
UART interface				
RTS	66	DOH	Request to send	If unused, keep them open.
CTS	67	DI	Clear to Send	
RXD	68	DI	Receive Data	
RI	69	DOH	Ring Indicator	
DCD	70	DOH	Carrier detects	
TXD	71	DOH	Transmit Data	
DTR	72	DI,PU	DTE get ready	
DBG_UART				
DBG_TXD	42	DO	Log output	If unused, keep them open.
DBG_RXD	106	DI	Log input	
I2C interface				
SCL	55	OD	I2C clock output	If unused, keep open, or else pull them up via 2.2KΩ resistors to 1.8V.
SDA	56	OD	I2C data input/output	
SDIO interface				
SDIO_DATA1	27	I/O	SDIO data1	It can be used for WLAN function. If unused, please
SDIO_DATA2	28	I/O	SDIO data2	
SDIO_CMD	29	I/O	SDIO command	

SDIO_DATA0	30	I/O	SDIO data0	keep them open.
SDIO_DATA3	31	I/O	SDIO data3	
SDIO_CLK	32	DO	SDIO clock	
HSIC interface				
HSIC_STROBE	35	I/O	HSIC strobe wakeup	***If use, please refer to document [27]*** Otherwise please keep them open.
HSIC_DATA	36	I/O	HSIC data	
PCM interface				
PCM_OUT	73	DO,PD	PCM data output.	If unused, please keep them open.
PCM_IN	74	DI,PD	PCM data input.	
PCM_SYNC	75	I/O,PD	PCM data frame sync signal.	
PCM_CLK	76	I/O,PU	PCM data bit clock.	
GPIO				
NETLIGHT	51	DO,PU	LED control output as network status indication.	If unused, keep them open.
STATUS	49	DO,PU	Operating status output. High level: Power on and firmware ready Low level: Power off	
GPIO4	94	IO,PD	Default: GPIO	
GPIO2	95	IO,PD	Default: GPIO	
GPIO1	96	IO,PD	Default: GPIO	
GPIO_54	97	IO,PD	Default: GPIO	
GPIO_19	119	IO,PD	Default: GPIO	
RF interface				
MAIN _ANT	82	AIO	MAIN antenna soldering pad	
GNSS_ANT	79	AI	GNSS antenna soldering pad	
AUX_ANT	59	AI	Auxiliary antenna soldering pad	
Other interface				
ISINK	45	PI	Ground-referenced current sink.	If unused, please keep them open.
ADC1	47	AI	Analog-digital converter input 1	
ADC2	46	AI	Analog-digital converter input 2	
RESERVED	88,89,90,91,92,99,100,101,102,103,104,105,107,111		Reserved for future use	Please keep them open.
Mux function interface				
COEX1●*	83	I/O	RF synchronizing between Wi-Fi and LTE.	Default:COEX1●* Option:WLAN_EN●

COEX2*	84	I/O	RFsynchronizing between Wi-Fi and LTE.	Default:COEX2* Option: WoWWAN●
COEX3●*	86	I/O	RF synchronizing between Wi-Fi and LTE.	Default:COEX3* Option:BT_PCM_CLK●
BOOT_CFG0●*	85	DI,PD	Boot configuration input. Module will be forced into USB download mode by connect 85 pin to VDD_1V8 during power up.	Default: BOOT_CFG0●* Option:COEX_RXD● Do place 2 test points for debug. ***DO NOT PULL UP BOOT_CFG0 DURING NORMAL POWER UP!***
FLIGHTMODE*	54	DI,PU	Flight Mode control input. High level(or open): Normal Mode Low level: Flight Mode	Default: FLIGHTMODE* Option:BT_PCM_IN●
GPIO3*	33	IO	GPIO	Default:GPIO3* Option:WL_PWR_EN●
GPIO6*	34	IO	GPIO	Default:GPIO6* Option:WL_SLP_CLK●
USIM_DET*	53	IO	Default: GPIO Optional: USIM card detecting input. H: USIM is removed L: USIM is inserted	Default:USIM_DET* Option:BT_EN●
GPIO77*	87	IO	GPIO	Default:GPIO77* Option:BT_PCM_OUT●
GPIO43*	50	I/O,PD	GPIO	Default:GPIO43* Option:COEX_TXD●
GPIO41*	52	I/O,PD	GPIO	Default:GPIO41* Option:BT_PCM_SYNC●

2.3 Mechanical Information

The following figure shows the package outline drawing of MODULE.

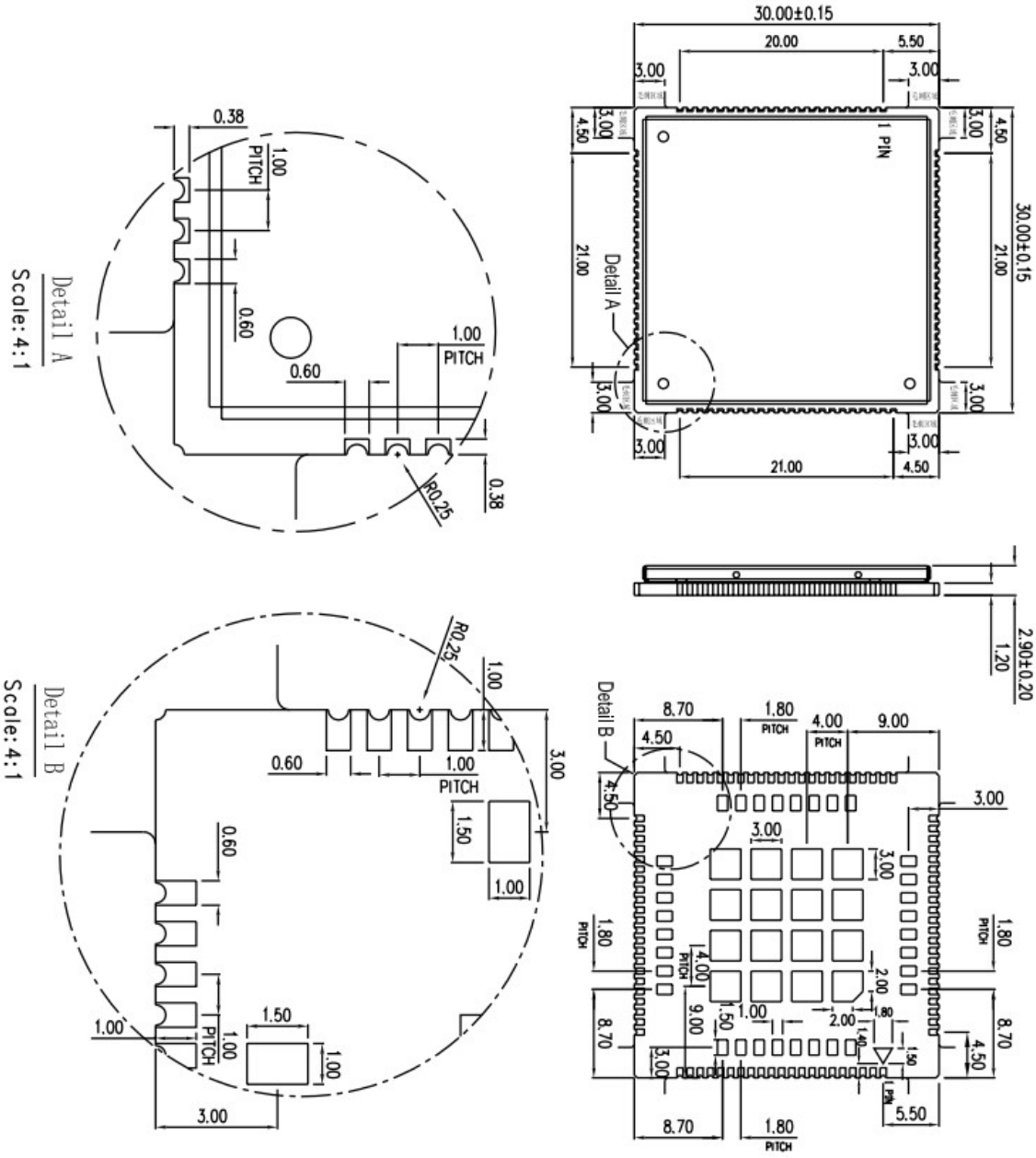


Figure 3: Dimensions (Unit: mm)

2.4 Footprint Recommendation

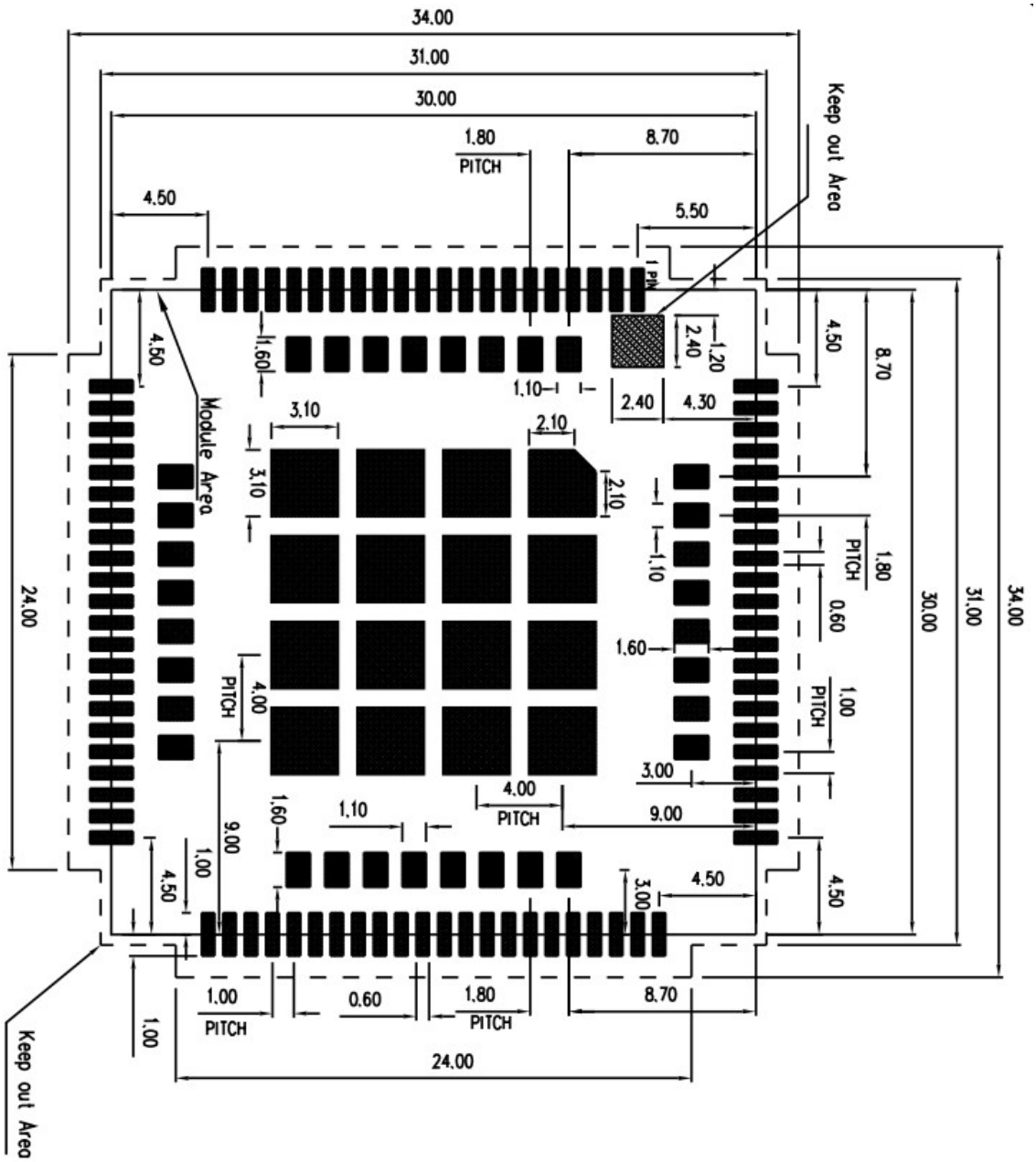


Figure 4: Footprint recommendation (Unit: mm)

3 Interface Application

3.1 Power Supply

The power supply pins of MODULE include 4 pins (pin 62&63, pin 38&39) named VBAT.
The 4 VBAT pads supply the power to RF and baseband circuits directly. On VBAT pads, the ripple current up to 2A typically, due to GSM/GPRS emission burst (every 4.615ms), may cause voltage drop. So the power supply for these pads must be able to provide sufficient current up to more than 2A in order to avoid the voltage drop is more than 300mV.
The following figure shows the VBAT voltage ripple wave at the maximum power transmit phase.

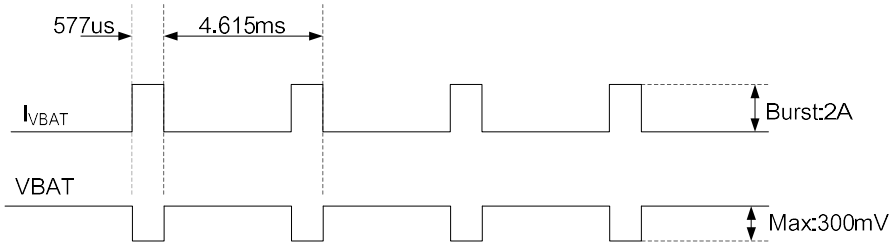


Figure 5: VBAT voltage drop during burst emission (GSM/GPRS)

Note: The test condition: The voltage of power supply for VBAT is 3.8V, Cd=100 µF tantalum capacitor (ESR=0.7Ω) and Cf=100nF (Please refer to Figure 6—Application circuit).

Table 6: VBAT pins electronic characteristic

Symbol	Description	Min.	Typ.	Max.	Unit
VBAT	Module power voltage	3.4	3.8	4.2	V
$I_{VBAT(peak)}$	Module power peak current in normal mode.	-	2	-	A
$I_{VBAT(average)}$	Module power average current in normal mode	Please refer to the table 34			
$I_{VBAT(sleep)}$	Power supply current in sleep mode				
$I_{VBAT(power-off)}$	Module power current in power off mode.	-	-	20	uA

3.1.1 Power Supply Design Guide

Make sure that the voltage on the VBAT pins will never drop below 3.4V, even during a transmit burst, when current consumption may rise up to 2A. If the voltage drops below 3.4V, the RF performance may be affected.

Note: If the power supply for VBAT pins can support up to 2A, more than 300uF capacitors are recommended .Otherwise users must use a total of 1000uF capacitors typically, in order to avoid of the voltage drop more than 300mV.

Some multi-layer ceramic chip (MLCC) capacitors (0.1/1uF) with low ESR in high frequency band can be used for EMC.

These capacitors should be put as close as possible to VBAT pads. Also, users should keep VBAT trace on circuit board wider than 2 mm to minimize PCB trace impedance. The following figure shows the recommended circuit.

Recommend Bead for vbat filter are BLM21PG300SN1D and MPZ2012S221A。

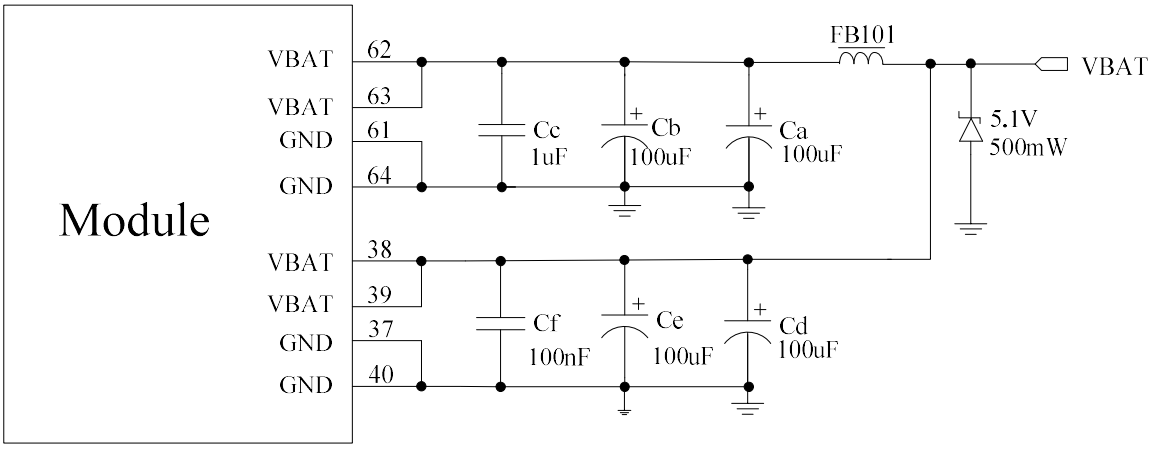


Figure 6: Power supply application circuit

In addition, in order to guard for over voltage protection, it is suggested to use TVS.

Note: user could only power pin 62, 63 or only power pin 38, 39, for these pins are connected inside the MODULE.

Table 7: Recommended TVS list

No.	Manufacturer	Part Number	Power dissipation	Package
1	JCET	ESDBW5V0A1	5V	DFN1006-2L
2	WAYON	WS05DPF-B	5V	DFN1006-2L
3	WILLSEMI	ESD5611N	5V	DFN1006-2L
4	WILLSEMI	ESD56151W05	5V	SOD-323
5*	PRISEMI	PESDHC2FD4V5BH	4.5V	DFN1006-2L
6*	WAYON	WS4.5DPV	4.5V	DFN1610-2L

Note: If user chooses TVS, please pay attention to Clamping Voltage in your datasheet . For example when the surge input is 100V,the Clamping Voltage is less than 10V.

*If vbat is higher than 3.8V, do not choose 5 and 6.

3.1.2 Recommended Power Supply Circuit

It is recommended that a switching mode power supply or a linear regulator power supply is used. It is important to make sure that all the components used in the power supply circuit can resist a peak current up to 2A.

The following figure shows the linear regulator reference circuit with 5V input and 3.8V output.

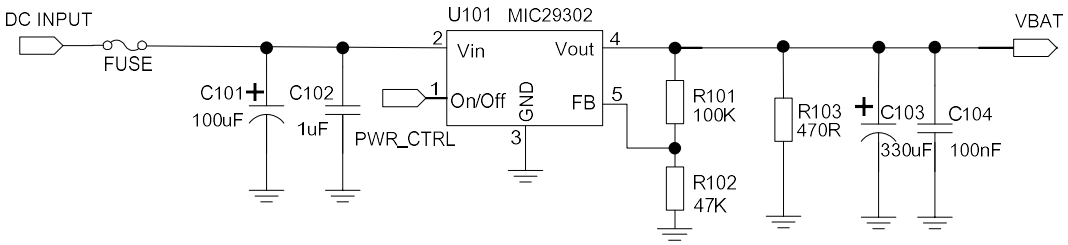


Figure 7: Linear regulator reference circuit

If there is a big voltage difference between input and output for VBAT power supply, or the efficiency is extremely important, then a switching mode power supply will be preferable. The following figure shows the switching mode power supply reference circuit.

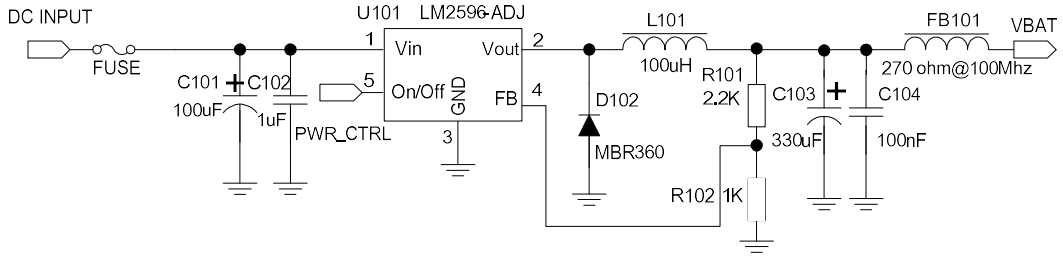


Figure 8: Switching mode power supply reference circuit

Note: The Switching Mode power supply solution for VBAT must be chosen carefully against Electro Magnetic Interference and ripple current from depraving RF performance.

3.1.3 Voltage Monitor

To monitor the VBAT voltage, the AT command “AT+CBC” can be used.

For monitoring the VBAT voltage outside or within a special range, the AT command “AT+CVALARM” can be used to enable the under-voltage warning function.

If users need to power off MODULE, when the VBAT voltage is out of a range, the AT command “AT+CPMVT” can be used to enable under-voltage power-off function.

Note: Under-voltage warning function and under-voltage power-off function are disabled by default. For more information about these AT commands, please refer to Document [1].

3.2 Power on/Power off/Reset Function

3.2.1 Power on

MODULE can be powered on by pulling the PWRKEY pin down to ground.
The PWRKEY pin has been pulled up with a diode to 1.8V internally, so it does not need to be pulled up externally. It is strongly recommended to put a100nF capacitor, an ESD protection diode, close to the PWRKEY pin as it would strongly enhance the ESD performance of PWRKEY pin. Please refer to the following figure for the recommended reference circuit.

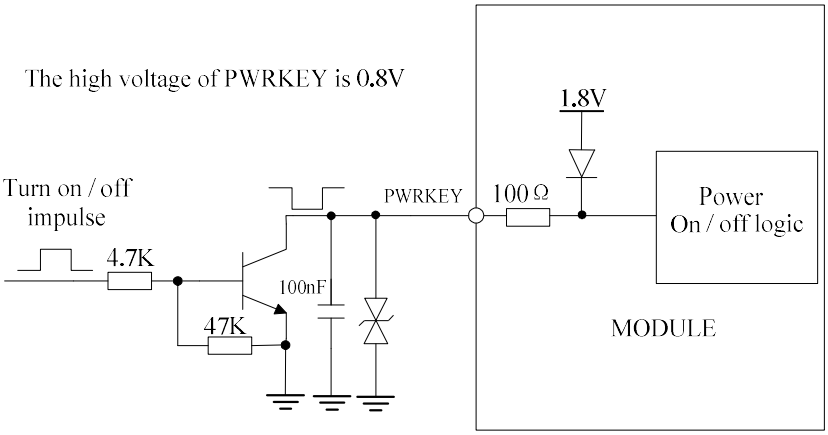


Figure 9: Reference power on/off circuit

Note: Module could be automatically power on by connecting PWRKEY pin to ground via 0R resistor directly.

The power-on scenarios are illustrated in the following figure.

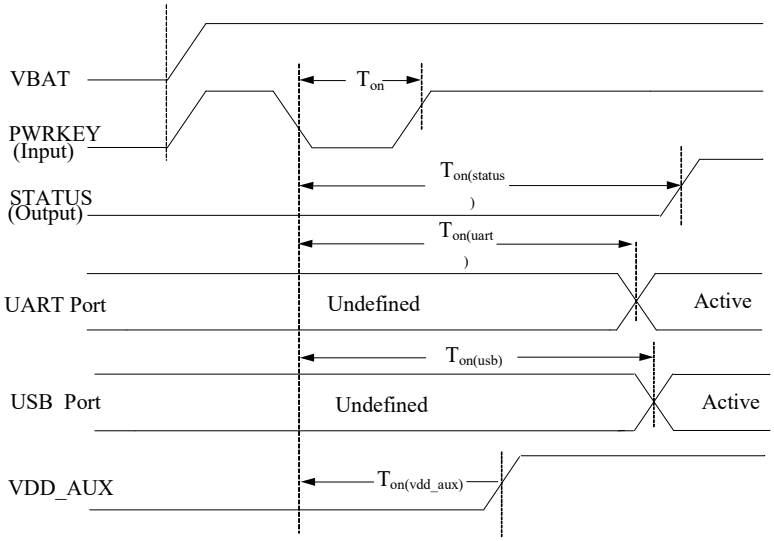


Figure 10: Power on timing sequence

Table 8: Power on timing and electronic characteristic

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{on}	The time of active low level impulse of PWRKEY pin to power on MODULE	100	500	-	ms
$T_{on(status)}$	The time from power-on issue to STATUS pin output high level(indicating power up ready)	15	16	-	s
$T_{on(uart)}$	The time from power-on issue to UART port ready	13	14	-	s
$T_{on(vdd\_aux)}$	The time from power-on issue to VDD_AUX ready		2.5	-	s
$T_{on(usb)}$	The time from power-on issue to USB port ready	11	12	-	s
V_{IH}	Input high level voltage on PWRKEY pin	0.6	0.8	1.8	V
V_{IL}	Input low level voltage on PWRKEY pin	-0.3	0	0.5	V

3.2.2 Power off

The following methods can be used to power off MODULE.

- Method 1: Power off MODULE by pulling the PWRKEY pin down to ground.
- Method 2: Power off MODULE by AT command “AT+CPOF”.
- Method 3: over-voltage or under-voltage automatic power off. The voltage range can be set by AT command “AT+CPMVT”.
- Method 4: over-temperature or under-temperature automatic power off.

Note: If the temperature is outside the range of -30~+80℃, some warning will be reported via AT port. If the temperature is outside the range of -40~+85℃, MODULE will be powered off automatically.

For details about “AT+CPOF” and “AT+CPMVT”, please refer to Document [1].

These procedures will make MODULE disconnect from the network and allow the software to enter a safe state, and save data before MODULE be powered off completely.
The power off scenario by pulling down the PWRKEY pin is illustrated in the following figure.

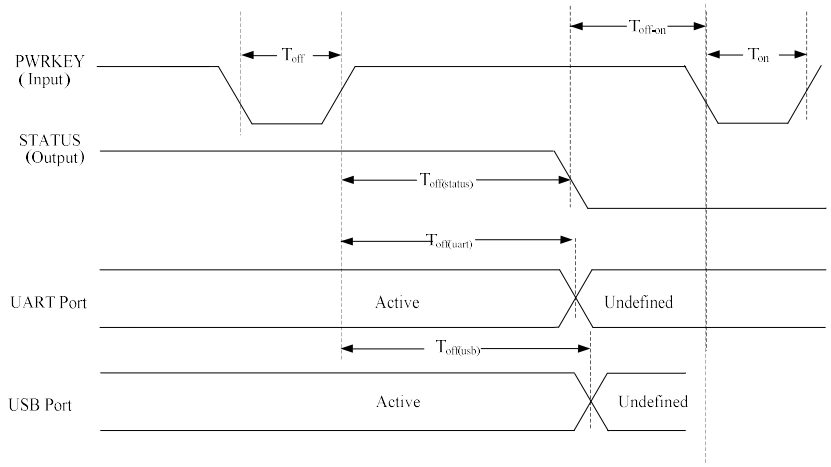


Figure 11: Power off timing sequence

Table 9: Power off timing and electronic characteristic

Symbol	Parameter	Time value			Unit
		Min.	Typ.	Max.	
T_{off}	The active low level time pulse on PWRKEY pin to power off MODULE	--	2.5	--	s
$T_{off(status)}$	The time from power-off issue to STATUS pin output low level(indicating power off)*	25	26	-	s
$T_{off(uart)}$	The time from power-off issue to UART port off	14	15	-	s
$T_{off(usb)}$	The time from power-off issue to USB port off	27	28	-	s
T_{off-on}	The buffer time from power-off issue to power-on issue	0	-	-	s

Note: The STATUS pin can be used to detect whether MODULE is powered on or not. When MODULE has been powered on and firmware goes ready, STATUS will be high level, or else STATUS will still low level.

3.2.3 Reset Function

MODULE can be reset by pulling the RESET pin down to ground.

Note: This function is only used as an emergency reset, when AT command "AT+CPOF" and the PWRKEY pin all have lost efficacy.

The RESET pin has been pulled up with a 40KΩ resistor to 1.8V internally, so it does not need to be pulled up externally. It is strongly recommended to put a100nF capacitor and an ESD protection diode close to the RESET pin. Please refer to the following figure for the recommended reference circuit.

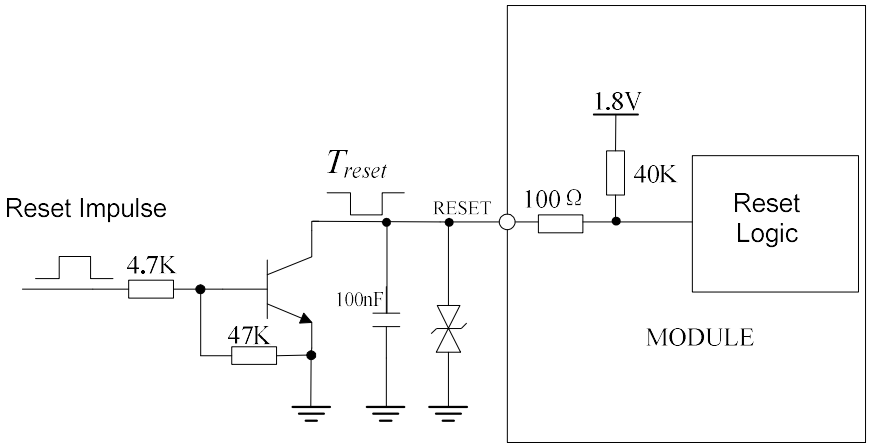


Figure 12: Reference reset circuit

Table 10: RESET pin electronic characteristic

Symbol	Description	Min.	Typ.	Max.	Unit
T_{reset}	The active low level time impulse on RESET pin to reset MODULE	100	200	500	ms
V_{IH}	Input high level voltage	1.17	1.8	2.1	V
V_{IL}	Input low level voltage	-0.3	0	0.8	V

3.3 UART Interface

MODULE provides a 7-wire UART (universal asynchronous serial transmission) interface as DCE (Data Communication Equipment). AT commands and data transmission can be performed through UART interface.

3.3.1 UART Design Guide

The following figures show the reference design.

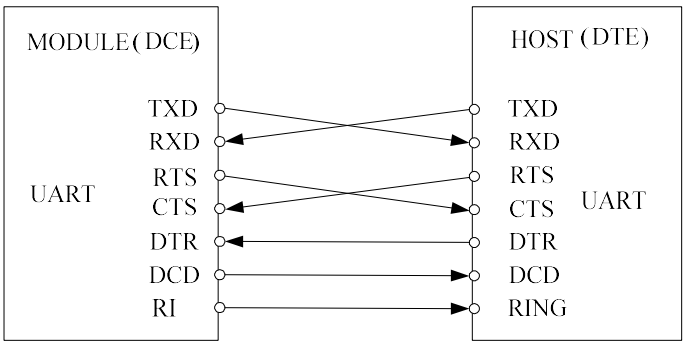


Figure 13: UART full modem

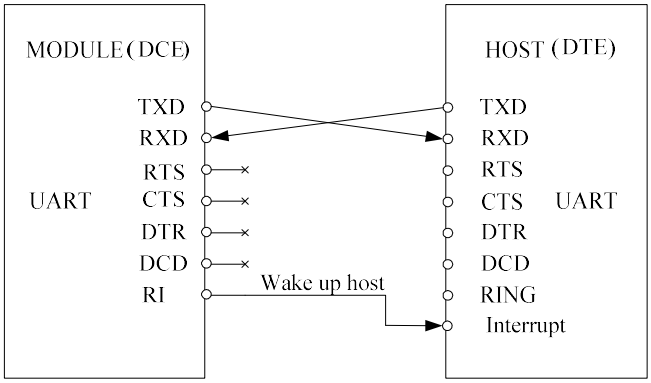


Figure 14: UART null modem

The MODULE UART is 1.8V voltage interface. If user's UART application circuit is 3.3V voltage interface, the level shifter circuits should be used for voltage matching. The TXB0108RGYR provided by Texas Instruments is recommended. The following figure shows the voltage matching reference design.

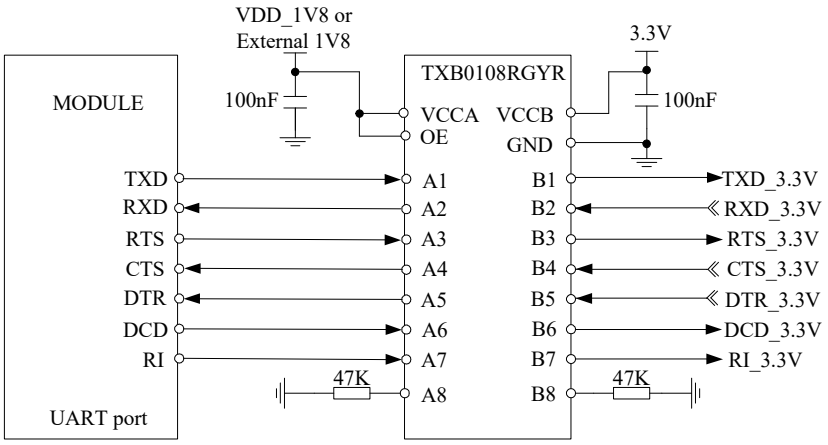


Figure 15: Reference circuit of level shift

User can use another level shifter circuits as follow

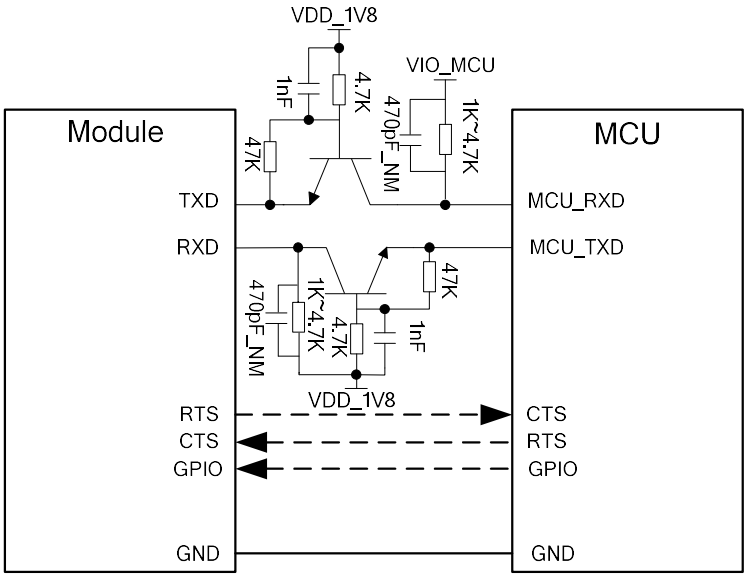


Figure 16: level matching circuit

To comply with RS-232-C protocol, the RS-232-C level shifter chip should be used to connect MODULE to the RS-232-C interface, for example SP3238ECA, etc.

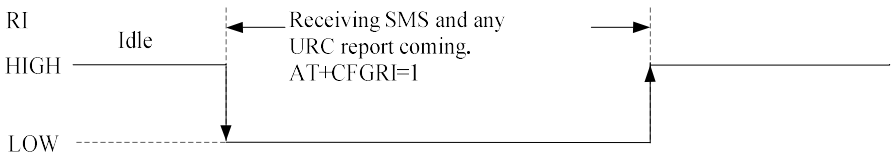
Note1: User needs to use high speed transistors such as MMBT3904.

Note2: MODULE supports the following baud rates: 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600, 3200000, 3686400, 4000000bps. The default band rate is 115200bps.

3.3.2 RI and DTR Behavior

The RI pin can be used to interrupt output signal to inform the host controller such as application CPU.

Normally RI will keep high level until certain conditions such as receiving SMS, or a URC report coming, and then it will change to low level.



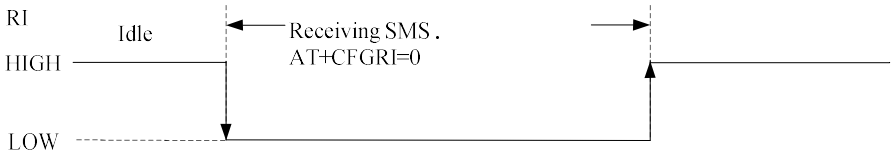


Figure 177: RI behaviour（SMS and URC report）

Normally RI will be kept at a high level until a voice call, then it will output periodic rectangular wave with 5900ms low level and 100ms high level. It will output this kind of periodic rectangular wave until the call is answered or hung up.

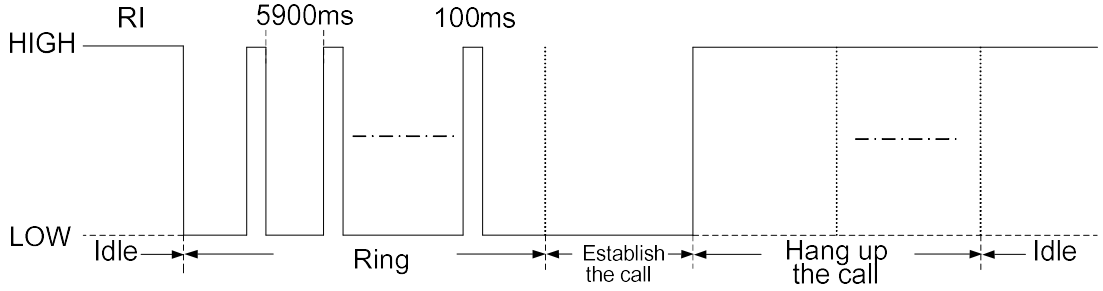


Figure 188 : RI behaviour（voice call）

Note: For more details of AT commands about UART, please refer to document [1] and [22].

DTR pin can be used to wake MODULE from sleep. When MODULE enters sleep mode, pulling down DTR can wake MODULE.

3.4 USB Interface

The MODULE contains a USB interface compliant with the USB2.0 specification as a peripheral, but the USB charging function is not supported.

MODULE can be used as a USB device. MODULE supports the USB suspend and resume mechanism which can reduce power consumption. If there is no data transmission on the USB bus, MODULE will enter suspend mode automatically, and will be resumed by some events such as voice call, receiving SMS, etc.

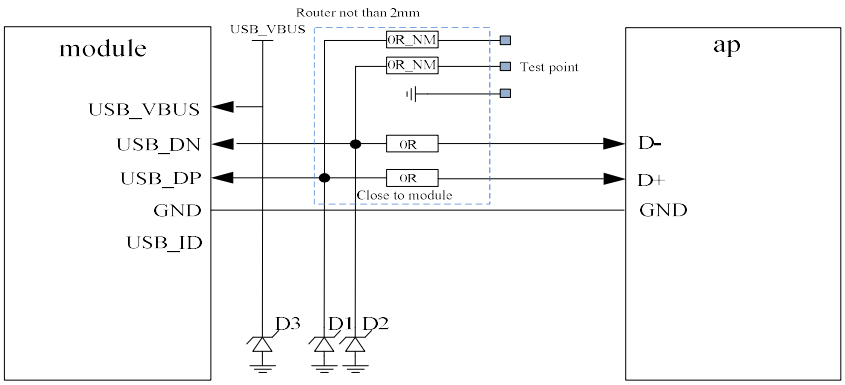


Figure19: USB reference circuit

Because of the high bit rate on USB bus, more attention should be paid to the influence of the junction capacitance of the ESD component on USB data lines. Typically, the capacitance should be less than 1pF. It is recommended to use an ESD protection component such as ESD9L5.0ST5G provided by On Semiconductor (www.onsemi.com).

D3 is suggested to select the diode with anti-ESD and voltage surge function, or user could add a TVS for surge clamping. The recommend TVS please refer to table 7.

Note：The USB_DN and USB_DP nets must be traced by 90Ohm+/-10% differential impedance.

3.5 HSIC interface

HSIC is a 2-signal source synchronous serial interface which uses 240MHz DDR signaling to provide High-Speed 480Mbps USB transfers which are 100% host driver compatible with traditional USB cable-connected topologies. Full-Speed (FS) and Low-Speed (LS) USB transfers are not directly supported by the HSIC interface (a HSIC enabled hub can provide FS and LS support, as well as IC_USB support)

The differences between HSIC and USB2.0 are listed below:

Table 11: Key differences between HSIC and HS-USB

HSIC	USB2.0
Signal-ended signaling at 1.2 V	Differential signaling
Two signals – STROBE, DATA	Four wires – Ground, D+, D-, VBUS
Double data rate signaling	Data inferred from differential signaling
HS-USB 480 Mbps only	HS/FS/LS support
Maximum trace length of 10 cm	Maximum cable length of 5 m
No HS chirp protocol	HS chirp protocol
Lower power consumption (digital)	Higher power consumption (analog)
No concept of disconnect	Hot plug/play support

module implements a HSIC interface compliant with the HSIC1.0 specification which can be used to connect to the external IC.

Note: The module HSIC default work as HSIC to LAN function, if user have any other questions , please contact simcom for more details.

3.6 SGMII Interface

MODULE provides a SGMII interface with an Ethernet MAC embedded, users could add a PHY to connect to the Ethernet, and the PHY device could be controlled by the MDIO interface and other dedicated signals.

Two Ethernet PHY are supported: AR8031/AR8033 (Qualcomm) and BCM89820 (Broadcom). The AR8031/AR8033 is used for the industrial field and the BCM89820 is dedicated for the automotive field.

Main features of SGMII:

- Ethernet Mac integrated in the module
- IEEE 802.3 Ethernet 10/100/1000Mbps, SGMII IF
- Supports IEEE 1588, Precision Time Protocol (PTP)
- Full duplex rated to 1 Gbps
- Half/full duplex for 10/100 Mbps
- Can be connected to external Ethernet PHY like AR8031/AR8033(industrial 10/100/1000Mbps), BCM89820(automotive 10/100Mbps)
- Uses 8B10B encoding of data with effective baud data rate of 1 Gbps, data rate is always 1.25 Gbps (or DDR clock is always at 625 MHz)

Main features of MDIO:

- Host mode only
- Dual voltage: 1.8 V or 2.85 V operation
- Default signal frequency: 6.25MHz
- MDIO_DATA is OD-gate, and requires an external 1.5 kΩ pull-up resistor to VMDIO.

For the AR8031/AR8033, User should provide 3.3V to power the external Ethernet PHY system and the current should be more than 200mA.

3.6.1 Reference schematic with AR8033

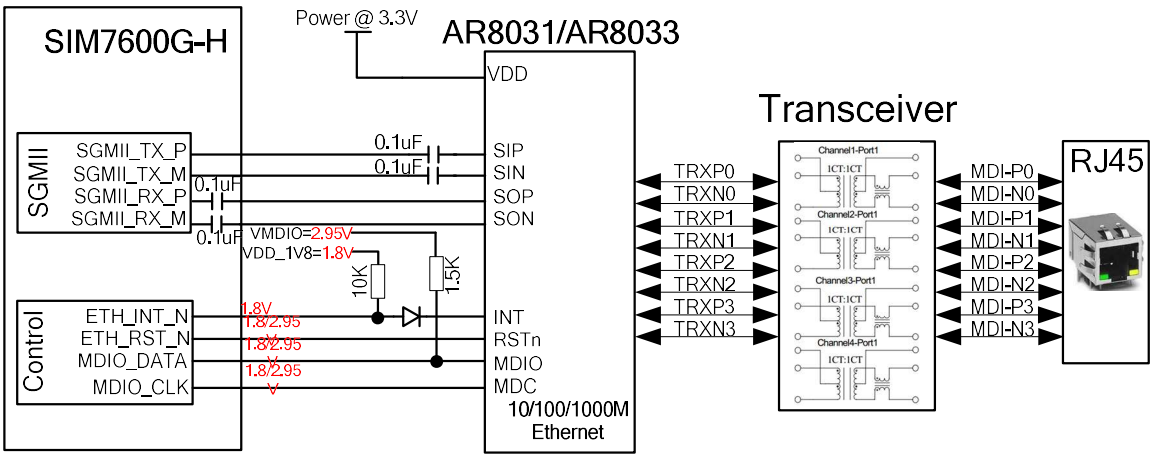


Figure20: Reference SGMII circuit with AR8033

For the BCM89820, Users should provide 3.3V and 1.2V to power the external Ethernet PHY system and the data interface of PHY. The current of 3.3V and 1.2V should be more than 100mA and 150mA.

3.6.2 Reference schematic with BCM89820

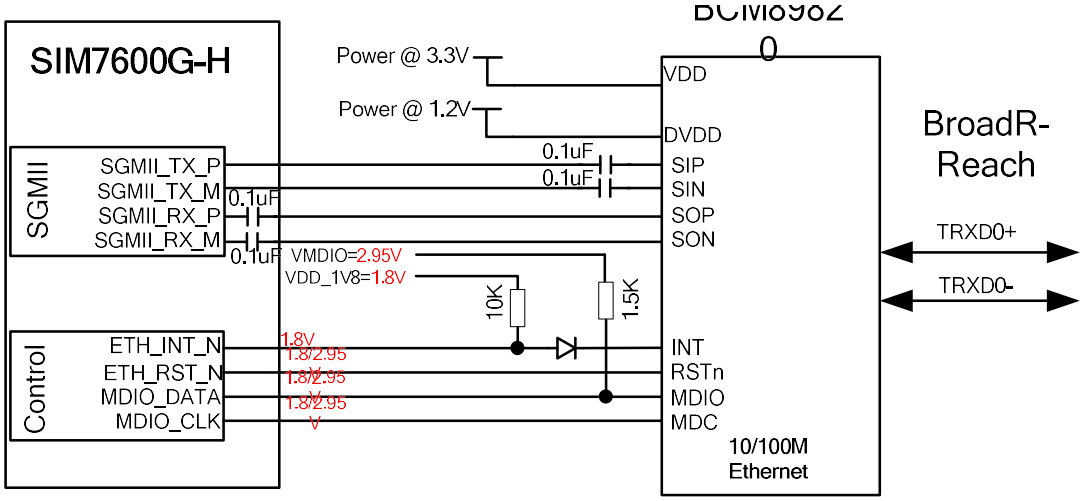


Figure21: Reference SGMII circuit with BCM89820

Note: The module SGMII function default closed. If user need, please contact SIMCom for more details or refer to document [28]

3.7 USIM Interface

MODULE supports both 1.8V and 3.0V USIM Cards.

Table 12: USIM electronic characteristic in 1.8V mode (USIM_VDD=1.8V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
USIM_VDD	LDO power output voltage	1.75	1.8	1.95	V
V_{IH}	High-level input voltage	0.65*USIM_VDD	-	USIM_VDD +0.3	V
V_{IL}	Low-level input voltage	-0.3	0	0.35*USIM_VDD	V
V_{OH}	High-level output voltage	USIM_VDD -0.45	-	USIM_VDD	V
V_{OL}	Low-level output voltage	0	0	0.45	V

Table 123: USIM electronic characteristic 3.0V mode (USIM_VDD=2.95V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
USIM_VDD	LDO power output voltage	2.75	2.95	3.05	V
V_{IH}	High-level input voltage	0.65*USIM_VDD	-	USIM_VDD +0.3	V
V_{IL}	Low-level input voltage	-0.3	0	0.25*USIM_VDD	V
V_{OH}	High-level output voltage	USIM_VDD -0.45	-	USIM_VDD	V
V_{OL}	Low-level output voltage	0	0	0.45	V

3.7.1 USIM Application Guide

It is recommended to use an ESD protection component such as ESDA6V1W5 produced by ST (www.st.com) or SMF15C produced by ON SEMI (www.onsemi.com). Note that the USIM peripheral circuit should be close to the USIM card socket. The following figure shows the 6-pin SIM card holder reference circuit.

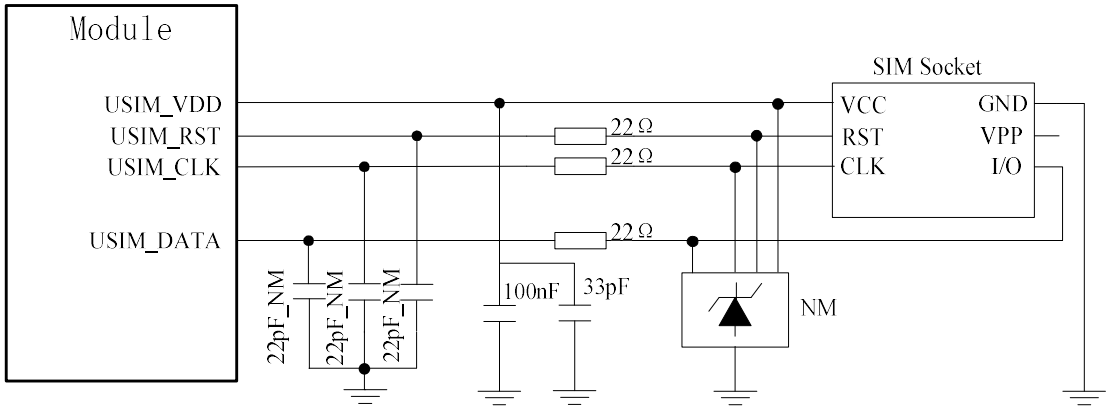


Figure 192: USIM interface reference circuit

Note: USIM_DATA has been pulled up with a 10KΩ resistor to USIM_VDD in MODULE. A 100nF capacitor on USIM_VDD is used to reduce interference. For more details of AT commands about USIM, please refer to document [1].USIM_CLK is very important signal, the rise time and fall time of USIM_CLK should be less than 40ns, otherwise the USIM card might not be initialized correctly.

The USIM_DET pin is used for detection of the USIM card hot plug in. User can select the 8-pin USIM card holder to implement USIM card detection function.

The following figure shows the 8-pin SIM card holder reference circuit.

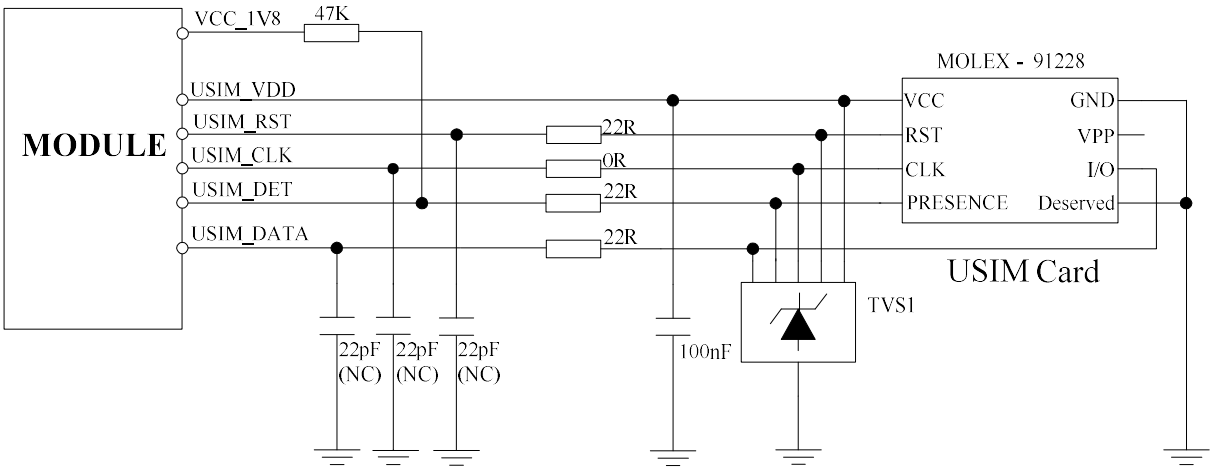


Figure 203: USIM interface reference circuit with USIM_DET

If the USIM card detection function is not used, user can keep the USIM_DET pin open.

SIM card circuit is susceptible, the interference may cause the SIM card failures or some other situations, so it is strongly recommended to follow these guidelines while designing:

- Make sure that the SIM card holder should be far away from the antenna while in PCB layout.
- SIM traces should keep away from RF lines, VBAT and high-speed signal lines.
- The traces should be as short as possible.
- Keep SIM holder's GND connect to main ground directly.
- Shielding the SIM card signal by ground.
- Recommended to place a 0.1～1uF capacitor on USIM_VDD line and keep close to the holder.
- The rise/fall time of USIM_CLK should not be more than 40ns.
- Add some TVS and the parasitic capacitance should not exceed 60pF.

Recommended USIM Card Holder

It is recommended to use the 6-pin USIM socket such as C707 10M006 512 produced by Amphenol. User can visit http://www.amphenol.com for more information about the holder.

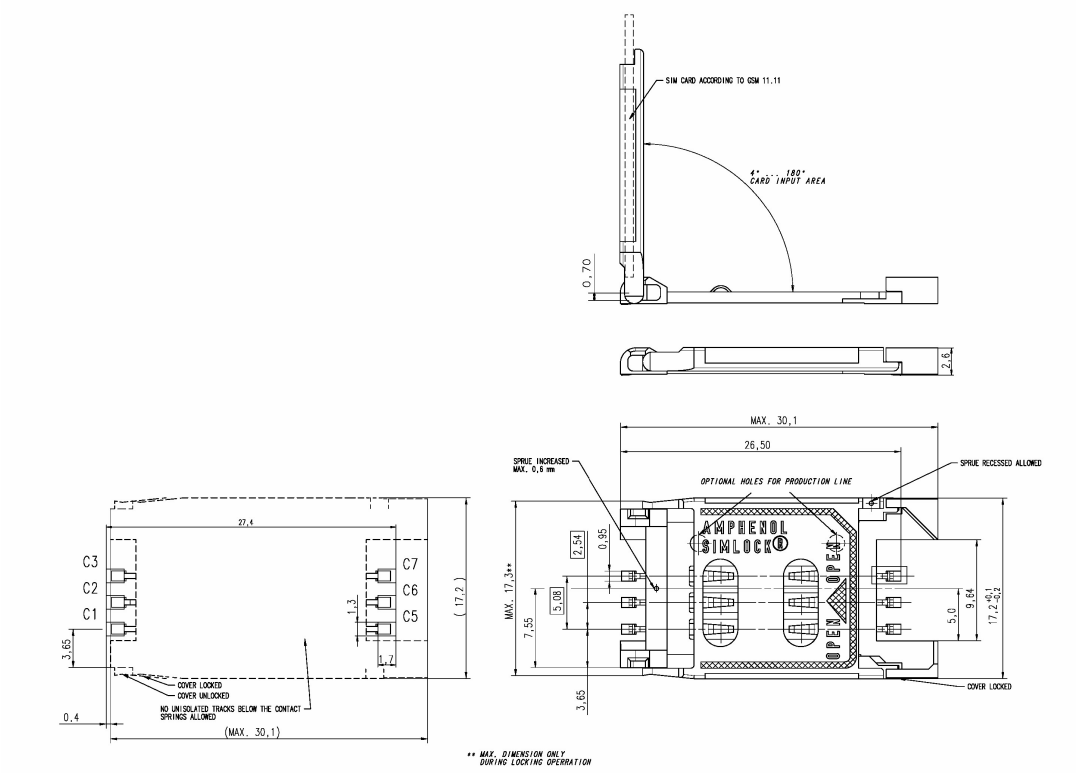


Figure 214: Amphenol SIM card socket

Table 134: Amphenol USIM socket pin description

Pin	Signal	Description
C1	USIM_VDD	USIM Card Power supply.
C2	USIM_RST	USIM Card Reset.
C3	USIM_CLK	USIM Card Clock.
C5	GND	Connect to GND.
C6	VPP	NC
C7	USIM_DATA	USIM Card data I/O.

3.8 PCM Interface

MODULE provides a PCM interface for external codec, which can be used in master mode with short sync and 16 bits linear format.

Table 145: PCM format

Characteristics	Specification
Line Interface Format	Linear(Fixed)
Data length	16bits(Fixed)
PCM Clock/Sync Source	Master Mode(Fixed)
PCM Clock Rate	2048 KHz (Fixed)
PCM Sync Format	Short sync(Fixed)
Data Ordering	MSB

Note: For more details about PCM AT commands, please refer to document [1].

3.8.1 PCM timing

MODULE supports 2.048 MHz PCM data and sync timing for 16 bits linear format codec.

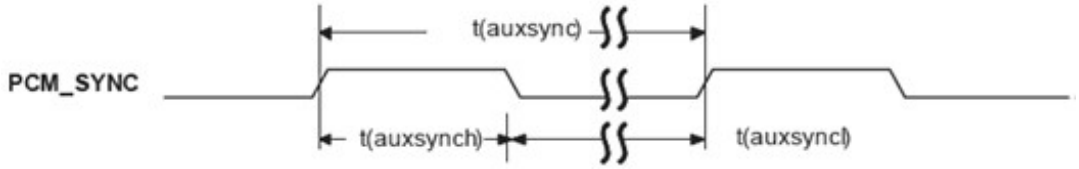


Figure 225: PCM_SYNC timing

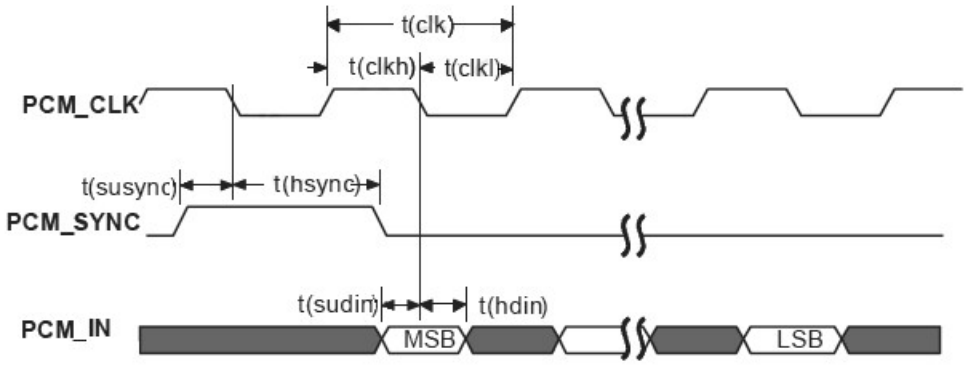


Figure 236: EXT codec to MODULE timing

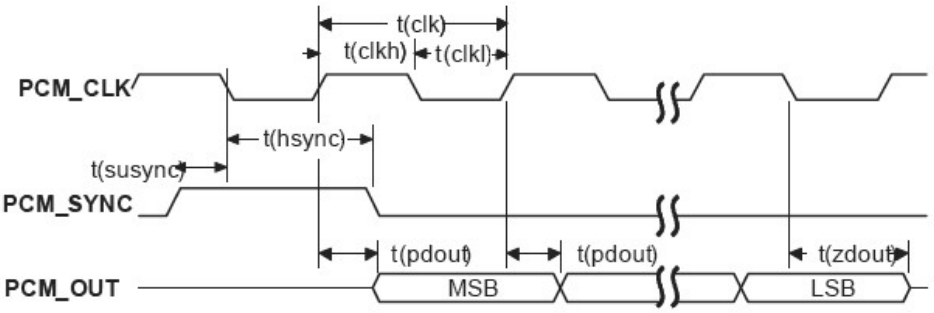


Figure 247: Module to EXT codec timing

Table 16: PCM timing parameters

Parameter	Description	Min.	Typ.	Max.	Unit
T(sync)	PCM_SYNC cycle time	–	125	–	µs
T(synch)	PCM_SYNC high level time	–	488	–	ns
T(syncl)	PCM_SYNC low level time	–	124.5	–	µs
T(clk)	PCM_CLK cycle time	–	488	–	ns
T(clkh)	PCM_CLK high level time	–	244	–	ns
T(clkl)	PCM_CLK low level time	–	244	–	ns
T(susync)	PCM_SYNC setup time high before falling edge of PCM_CLK	–	244	–	ns
T(hsync)	PCM_SYNC hold time after falling edge of PCM_CLK	–	244	–	ns
T(sudin)	PCM_IN setup time before falling edge of PCM_CLK	60	–	–	ns
T(hdin)	PCM_IN hold time after falling edge of PCM_CLK	10	–	–	ns
T(pdout)	Delay from PCM_CLK rising to PCM_OUT valid	–	–	60	ns
T(zdout)	Delay from PCM_CLK falling to PCM_OUT HIGH-Z	–	160	-	ns

3.8.2 PCM Application Guide

The following figure shows the external codec reference design.

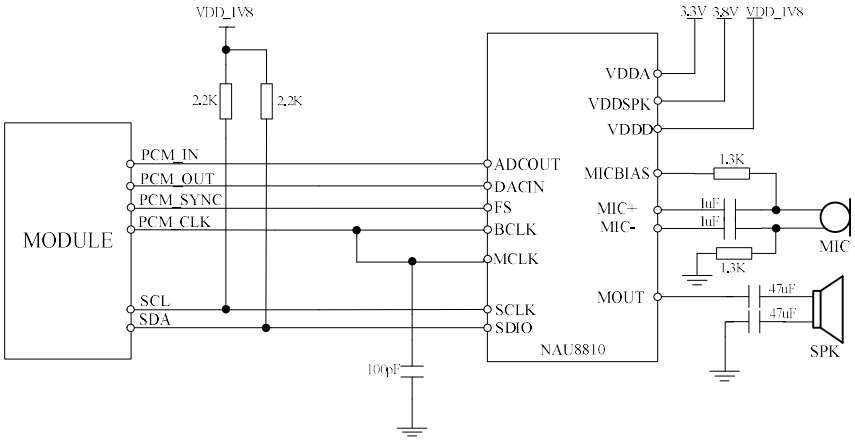


Figure 258: Audio codec reference circuit

3.9 SD Interface

MODULE provides a 4-bit SD/MMC/eMMC interface with clock rate up to 200 MHz.

When connected to a SD or MMC card, the voltage of SD interface is 1.8/2.85V, which is compatible with Secure Digital Physical Layer Specification version 3.0 and SDIO Card Specification version 3.0.It supports up to 128GB SD cards.

When connected to a eMMC card, the interface voltage will be a single 1.8V, which is compatible with eMMC Specification, version 4.5. It supports up to 128GB eMMC cards.

Table 17: SD/MMC electronic characteristic as 2.85V (SD_DATA0-3，SD_CLK and SD_CMD)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage	0.65*2.85	-	2.85+0.3	V
V_{IL}	Low-level input voltage	-0.3	0	0.25*2.85	V
V_{OH}	High-level output voltage	0.75*2.85	2.85	2.85	V
V_{OL}	Low-level output voltage	0	0	0.15*2.85	V

Table 158: SD/MMC/eMMC electronic characteristic as 1.8V (SD_DATA0-3，SD_CLK and SD_CMD)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage	0.7*1.8	-	1.8+0.2	V
V_{IL}	Low-level input voltage	-0.3	0	0.3*1.8	V
V_{OH}	High-level output voltage	1.8-0.4	1.8	1.8	V
V_{OL}	Low-level output voltage	0	0	0.45	V

Users should provide 2.85V to power SD card system and the current should more than 350mA, which is showed below as VCC_SD. ESD/EMI components should be arranged beside SD card socket. Refer to the following application circuit.

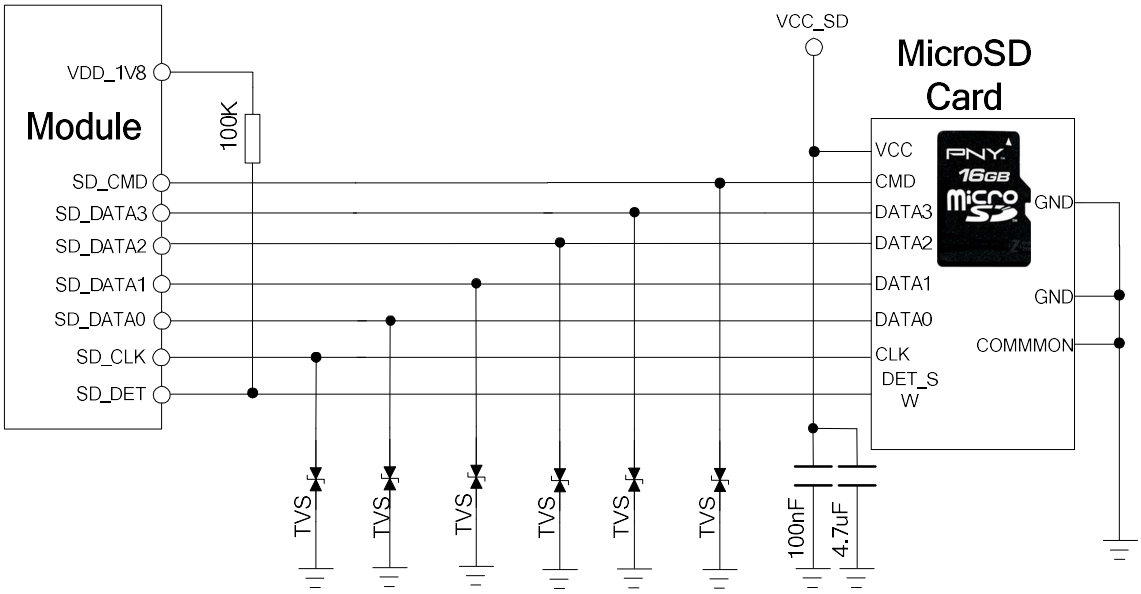


Figure29: SD reference circuit

Users should provide 2.85V to power eMMC card system and 1.8V to power the SDIO_DATA/CMD/CLK signals. The source of 2.85V should be able to provide more than 500mA* which showed below as VCC_eMMC, as the source of 1.8V should be able to provide more than 300mA* which showed below as VCCQ_1V8. ESD/EMI components should be arranged close to the eMMC card. Refer to the following application circuit.

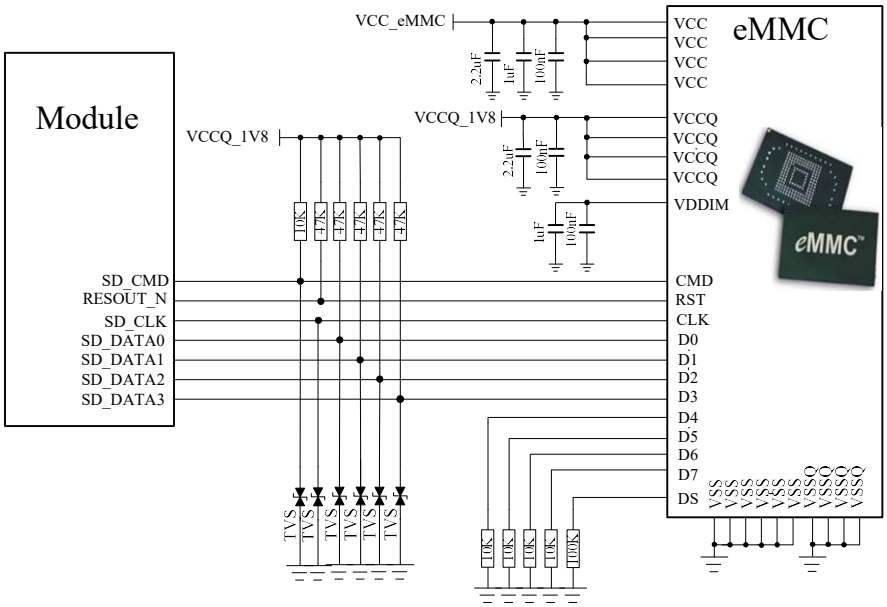


Figure 30: eMMC reference circuit

NOTE: For the current of VCC_eMMC and VCCQ_1V8, users should better refer to the related datasheet of eMMC which is used. The listed current of 500mA and 300mA are just for your reference.

SD/MMC/eMMC card layout guide lines:

- Protect SD card signals from noisy signals (clocks, SMPS, etc.).
- Up to 200 MHz clock rate, 50 Ω nominal, ±10% trace impedance
- CLK to DATA/CMD length matching < 1 mm
- Total routing length < 50 mm
- Spacing to all other signals = 2x line width
- Bus capacitance < 10 pF

3.10 I2C Interface

MODULE provides a I2C interface compatible with I2C specification, version 5.0, with clock rate up to 400 kbps. Its operation voltage is 1.8V.

The following figure shows the I2C bus reference design.

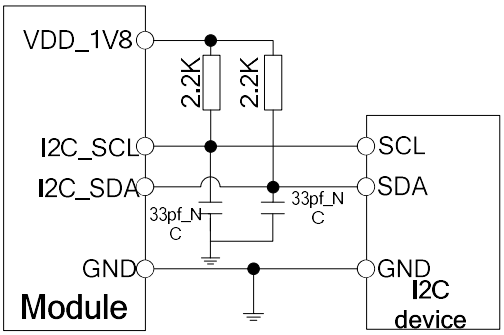


Figure31: I2C reference circuit

Note：SDA and SCL do not have pull-up resistors in MODULE. So, 2 external pull up resistors are needed in application circuit.

"AT+CRIIC and AT+CWIIC" AT commands could be used to read/write register values of the I2C peripheral devices. For more details about AT commands please refer to document [1].

3.11 SDIO Interface

MODULE provides a 4 bit 1.8V SDIO interface for WLAN solution with W58 module.
The SDIO interface can be used for WLAN solution.
Note: Special software version for CAT4 MODULEs supports this function.

3.12 SPI Interface

SIM7600G provides a SPI interface as a master only. It provides a duplex, synchronous, serial

communication link with peripheral devices. Its operation voltage is 1.8V, with clock rates up to 50 MHz

Note：For more details of the AT commands about the SPI, please refer to document [1].

3.13 Network status

The NETLIGHT pin is used to control Network Status LED, its reference circuit is shown in the following figure.

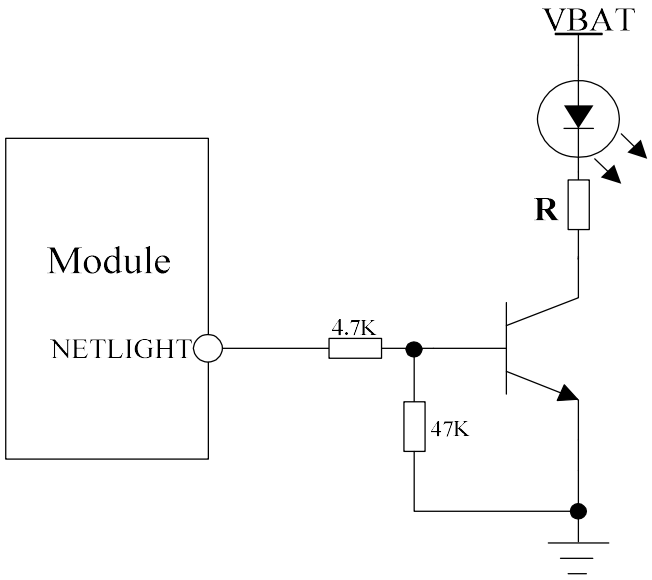


Figure32: NETLIGHT reference circuit

Note: The value of the resistor named "R" depends on the LED characteristic.

Table 19: NETLIGHT pin status

NETLIGHT pin status	Module status
Always On	Searching Network; Call Connect(include VOLTE,SRLTE)
200ms ON, 200ms OFF	Data Transmit; 4G registered;
800ms ON, 800ms OFF	2G/3G registered network
OFF	Power off ;Sleep

Note: NETLIGHT output low level as "OFF", and high level as "ON".

3.14 Flight Mode Control

The FLIGHTMODE pin can be used to control MODULE to enter or exit the Flight mode. In Flight mode, the RF circuit is closed to prevent interference with other equipments and minimize

current consumption. Bidirectional ESD protection component is suggested to add on FLIGHTMODE pin, its reference circuit is shown in the following figure.

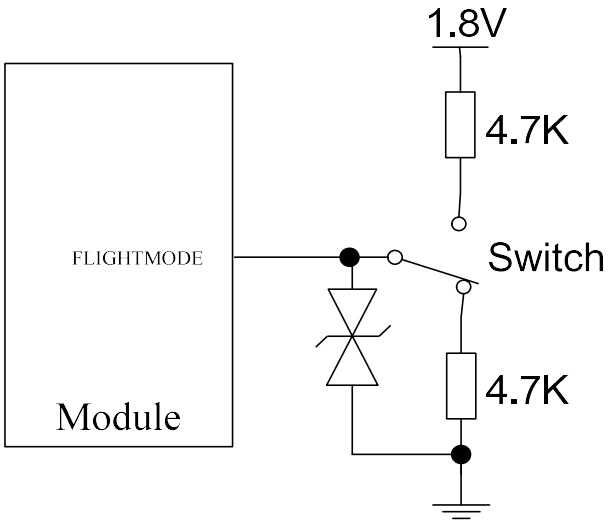


Figure 33: Flight mode switch reference circuit

Table 20: FLIGHTMODE pin status

FLIGHTMODE pin status	Module operation
Input Low Level	Flight Mode: RF is closed
Input High Level	AT+CFUN=0: RF is closed AT+CFUN=1:RF is working

3.15 Other interface

3.15.1 Sink Current Source

The ISINK pin is VBAT tolerant and intended to drive some passive devices, such as LCD backlight and white LED, etc. Its output current can be up to 40mA and be set by the AT command "AT+ CLEDITST".

Table 21: Sink current electronic characteristic

Symbol	Description	Min.	Typ.	Max.	Unit
V_{ISINK}	Voltage tolerant	0.5	-	VBAT	V
I_{ISINK}	Current tolerant	0	-	40	mA

ISINK is a ground-referenced current sink. The following figure shows its reference circuit.

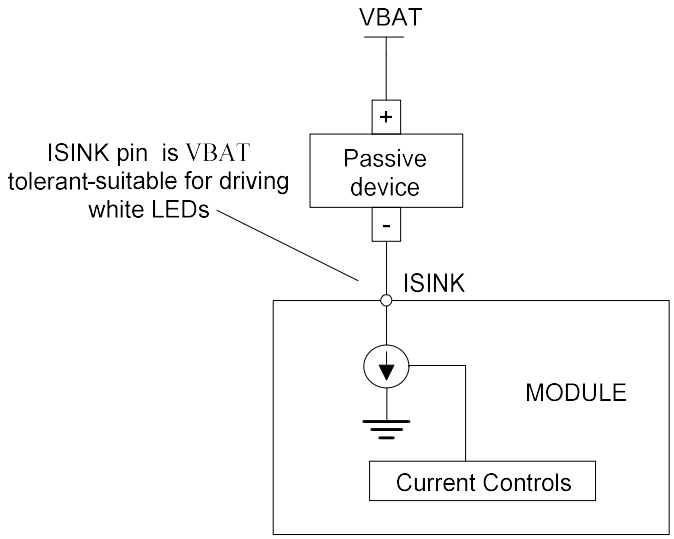


Figure34: ISINK reference circuit

Note: The sinking current can be adjusted to meet the design requirement through the AT command "AT+ CLEDITST =<0>, <value>".The "value" ranges from 0 to 8, on behalf of the current from 0mA to 40mA by 5mA step.

3.15.2 ADC

MODULE has 2 dedicated ADC pins named ADC1 and ADC2.They are available for digitizing analog signals such as battery voltage and so on. These electronic specifications are shown in the following table.

Table 22: ADC1 and ADC2 electronic characteristics

Characteristics	Min.	Typ.	Max.	Unit
Resolution	–	15	–	Bits
Conversion time	–	442	–	ms
Input Range	0.1		1.7	V
Input serial resistance	1	–	–	MΩ

Note: "AT+CADC" and "AT+CADC2" can be used to read the voltage of the ADC1 and ADC2 pins, for more details, please refer to document [1].

3.15.3 LDO

MODULE has a LDO power output, named VDD_AUX. its output voltage is 2.85V by default, Users can switch the LDO on or off by the AT command "AT+CVAUXS" and configure its output voltage by the AT command "AT+CVAUXV".

Table 23: Electronic characteristic

Symbol	Description	Min.	Typ.	Max.	Unit
V_{VDD_AUX}	Output voltage	1.7	2.85	3.05	V
I_O	Output current	-	-	150	mA

Note：For more details of AT commands about VDD_AUX, please refer to document [1].

4 RF Specifications

4.1 GSM/UMTS/LTE RF Specifications

Table 16: Conducted transmission power

Technology/Band	Mode	Target Power and Tolerance (dBm)
GSM 850	GMSK(1TS)	34±1
	8PSK(1TS)	28±1
GSM 1900	GMSK(1TS)	29±1
	8PSK(1TS)	25±1
WCDMA Band 2	QPSK/16QAM	21±1
WCDMA Band 4	QPSK/16QAM	21±1
WCDMA Band 5	QPSK/16QAM	22±1
LTE Band 2	QPSK/16QAM	21±1
LTE Band 4	QPSK/16QAM	21±1
LTE Band 5	QPSK/16QAM	22±1
LTE Band 7	QPSK	22±1
	16QAM	21±1.5
LTE Band 12	QPSK/16QAM	22±1.5
LTE Band 13	QPSK	23±1
	16QAM	22±1.7
LTE Band 25	QPSK	22±1
	16QAM	21±1.7
LTE Band 26	QPSK/16QAM	22±2
LTE Band 41	QPSK	23±1
	16QAM	22±2
LTE Band 66	QPSK	22±1.5
	16QAM	21±2

Table 17: Operating frequencies

Frequency	Receiving	Transmission
GSM850	869～894MHz	824～849 MHz
EGSM900	925～960MHz	880～915 MHz

DCS1800	1805～1880 MHz	1710～1785 MHz
PCS1900	1930~1990 MHz	1850~1910 MHz
WCDMA B1	2110～2170 MHz	1920～1980 MHz
WCDMA B2	1930~1990 MHz	1850~1910 MHz
WCDMA B4	2110~2155MHz	1710~1755MHz
WCDMA B5	869～894 MHz	824～849 MHz
WCDMA B6	877~882MHz	832~837MHz
WCDMA B8	925～960 MHz	880～915 MHz
WCDMA B19	875~890MHz	835~845MHz
The LTE Operating frequencies are shown in the following table 24. Note: Operating frequencies of LTE TDD B41 for the MODULE is 100MHz BW, 2555～2655 MHz		
GPS	1574.4 ～1576.44 MHz	-
GLONASS	1598 ～1606 MHz	-
BD	1559 ～1563 MHz	

Table 2418: E-UTRA operating bands

E-UTRA Operating Band	Uplink (UL) operating band	Downlink (DL) operating band	Duplex Mode
1	1920 ~1980 MHz	2110 ~2170 MHz	FDD
2	1850~1910 MHz	1930~1990 MHz	FDD
3	1710 ~1785 MHz	1805 ~1880 MHz	FDD
4	1710~1755MHz	2110~2155MHz	FDD
5	824～849 MHz	869～894MHz	FDD
7	2500~2570MHz	2620~2690MHz	FDD
8	880 ~915 MHz	925 ~960 MHz	FDD
12	699~716MHz	728~746MHz	FDD
13	777~787MHz	746~757MHz	FDD
18	815~830MHz	860~875MHz	FDD
19	830~845MHz	875~890MHz	FDD
20	832~862MHz	791~ 821MHz	FDD
25	1850~1915MHz	1930~1995MHz	FDD
26	814~849MHz	859~894MHz	FDD
28	703~748MHz	758~803MHz	FDD
66	1710~1780MHz	2110~2200MHz	FDD
34	2010~2025MHz	2010~2025MHz	TDD
38	2570 ~2620 MHz	2570 ~2620 MHz	TDD
39	1880~1920MHz	1880~1920MHz	TDD
40	2300 ~2400 MHz	2300 ~2400 MHz	TDD
41	2496~2696 MHz	2496~2696 MHz	TDD

Table 19: Conducted receive sensitivity

Frequency	Receive sensitivity(Typical)	Receive sensitivity(MAX)
GSM850	< -109dBm	3GPP
EGSM900	< -109dBm	3GPP
DCS1800	< -109dBm	3GPP
PCS1900	< -109dBm	3GPP
WCDMA B1	< -110dBm	3GPP
WCDMA B2	< -110dBm	3GPP
WCDMA B4	< -110dBm	3GPP
WCDMA B5	< -110dBm	3GPP
WCDMA B6	< -110dBm	3GPP
WCDMA B8	< -110dBm	3GPP
WCDMA B19	< -110dBm	3GPP
LTE FDD/TDD	See table 26.	3GPP

Table 2620: Reference sensitivity (QPSK)

E-UTRA band	1.4 MHz Standard	3 MHz Standard	5 MHz Standard	10 MHz Standard	15 MHz Standard	20 MHz Standard	Duplex Mode
1	-	-	-100	-97	-95.2	-94	FDD
2	-102.7	-99.7	-98	-95	-93.2	-92	FDD
3	-101.7	-98.7	-97	-94	-92.2	-91	FDD
4	-104.7	-101.7	-100	-97	-95.2	-94	FDD
5	-103.2	-100.2	-98	-95			FDD
7			-98	-95	-93.2	-92	FDD
8	-102.2	-99.2	-97	-94			FDD
12	-101.7	-98.7	-97	-94			FDD
13			-97	-94			FDD
18			-100	-97	-95.2		FDD
19			-100	-97	-95.2		FDD
20			-97	-94	-91.2	-90	FDD
25	-101.2	-98.2	-96.5	-93.5	-91.7	-90.5	FDD
26	-102.7	-99.7	-97.5	-94.5	-92.7		FDD
28		-100.2	-98.5	-95.5	-93.7	-91	FDD
66	-104.7	-101.7	-100	-97	-95.2	-94	FDD
34			-100	-97	-95.2		TDD
38	-	-	-100	-97	-95.2	-94	TDD
39			-100	-97	-95.2		TDD
40	-	-	-100	-97	-95.2	-94	TDD
41	-	-	-99	-96	-94.2	-93	TDD

4.2 GSM /UMTS/LTE Antenna Design Guide

Users should connect antennas to MODULE's antenna pads through micro-strip line or other types of RF trace and the trace impedance must be controlled in 50Ω. SIMCom recommends that the total insertion loss between the antenna pads and antennas should meet the following requirements:

Table 21: Trace loss

Frequency	Loss
700MHz-960MHz	<0.5dB
1710MHz-2170MHz	<0.9dB
2300MHz-2650MHz	<1.2dB

To facilitate the antenna tuning and certification test, a RF connector and an antenna matching circuit should be added. The following figure is the recommended circuit.

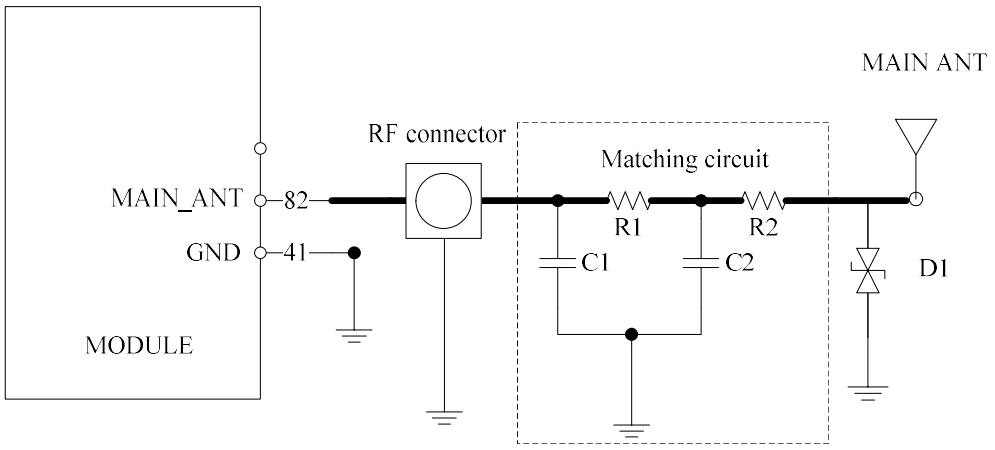


Figure35: Antenna matching circuit (MAIN_ANT)

In above figure, the components R1, C1, C2 and R2 are used for antenna matching, the values of components can only be achieved after the antenna tuning and usually provided by antenna vendor. By default, the R1, R2 are 0Ω resistors, and the C1, C2 are reserved for tuning. The component D1 is a TVS for ESD protection, and it is optional for users according to application environment.
The RF test connector is used for the conducted RF performance test, and should be placed as close as to the MODULE's MAIN_ANT pin. The traces impedance between MODULE and antenna must be controlled in 50Ω.