# Specification

## Remote control module

## HJC0

**(2.4GHz)**

# Revision History

| Rev. No. | History | Issue Date | Remark |
|---|---|---|---|
| 0.0 | Initial issue. | Dec 27th, 2007 | Preliminary |
| 0.1 | Modified specification and add section for TX power setting | Feb 20th, 2008 | Preliminary |
| 0.2 | Add top marking info., reflow profile, Carry tape & reel dimensions | Oct. 9th, 2008 | Preliminary |
| 0.3 | Modify description of state machine and FIFO mode<br>Rename IRQS1/IRQS2 to GIO1S/GIO2S<br>Rename GPIO1/GPIO2 to GIO1/GIO2<br>Add Easy FIFO mode, Segment FIFO mode<br>Delete thermal sensor function / external voltage measurement<br>Delete TWWS function<br>Add State diagram of quick/normal/power saving FIFO mode<br>Add State diagram of Direct mode<br>Rename Master Clock $F_{CSCK}$ to $F_{MCLK}$<br>Modify data rate support from 1K~500K to 2K ~ 500K | Jan. 7th, 2009 | Preliminary |
| 1.0 | Revise description of state machine and FIFO mode<br>Remove un-necessary components of application circuit<br>Add RSSI curve<br>Add layout guidance | August, 2009 | Full Production |
| 1.1 | Revise min. operation voltage from 1.9V to 2.0V<br>Revise typical TX current (0dBm) from 19mA to 20mA | Feb., 2010 | Full Production |
| 1.2 | Add note 9 in chapter 8, specification.<br>Fix typo in below pages (51, 52, 57, 62, 66, 78, 79). | Nov., 2010 | Full Production |
| 1.3 | Change English Company Name | Nov. 30, 2010 | Full Production |
| 1.4 | Revise pin description of VDA1, VDA2, VDA3 in Ch5. | Jan., 2011 | Full Production |
| 1.5 | Update block diagram and Ch19.<br>Correct typo of Ch9, 18h. | Feb., 2012 | Full Production |

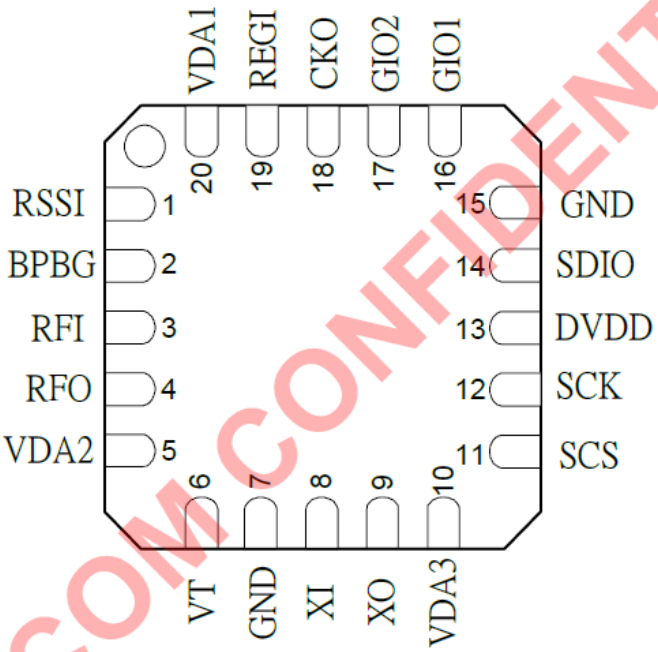
## 2. Typical Applications

- Wireless keyboard and mice
- Remote control
- Helicopter and airplane radio controller
- 2400 ~ 2483.5 MHz ISM system
- Wireless metering and building automation
- Wireless toys and game controllers

## 3. Feature

- Small size (QFN4 X4, 20 pins).
- Frequency band: 2400 ~ 2483.5MHz.
- FSK or GFSK modulation
- Low current consumption: RX 16mA, TX 20mA (at 0dBm output power).
- Low sleep current (1.5 uA).
- On chip regulator, support input voltage 2.0 ~ 3.6 V.
- Programmable data rate from 2Kbps to 500Kbps.
- Programmable TX power level from – 20 dBm to 1 dBm.
- Ultra High sensitivity:
  - -95dBm at 500Kbps on-air data rate.
  - -97dBm at 250Kbps on-air data rate
  - -104dBm at 25Kbps on-air data rate
  - -107dBm at 2Kbps on-air data rate
- Fast settling time (130 us) synthesizer for frequency hopping system.
- Built-in Battery Detector.
- Support low cost crystal (6 / 8 /12 / 16 / 20 / 24MHz).
- Support crystal sharing, (1 / 2 / 4 / 8MHz) to MCU.
- Support Frequency Compensation.
- Easy to use.
  - Support 3-wire or 4-wire SPI.
  - Unique Strobe command via SPI.
  - ONE register setting for new channel frequency.
  - 8-bits Digital RSSI for clear channel indication.
  - Fast exchange mode during TRX role switching.
  - Auto RSSI measurement.
  - Auto Calibrations.
  - Auto IF function.
  - Auto CRC Check.
  - Auto FEC by (7, 4) Hamming code (1 bit error correction / code word).
  - Data Whitening for encryption and decryption.
  - Separated 64 bytes RX and TX FIFO.
  - Easy FIFO / Segment FIFO / FIFO Extension (up to 256 bytes).
  - Support direct mode with recovery clock output to MCU.
  - Support FIF mode with frame sync signal to MCU.

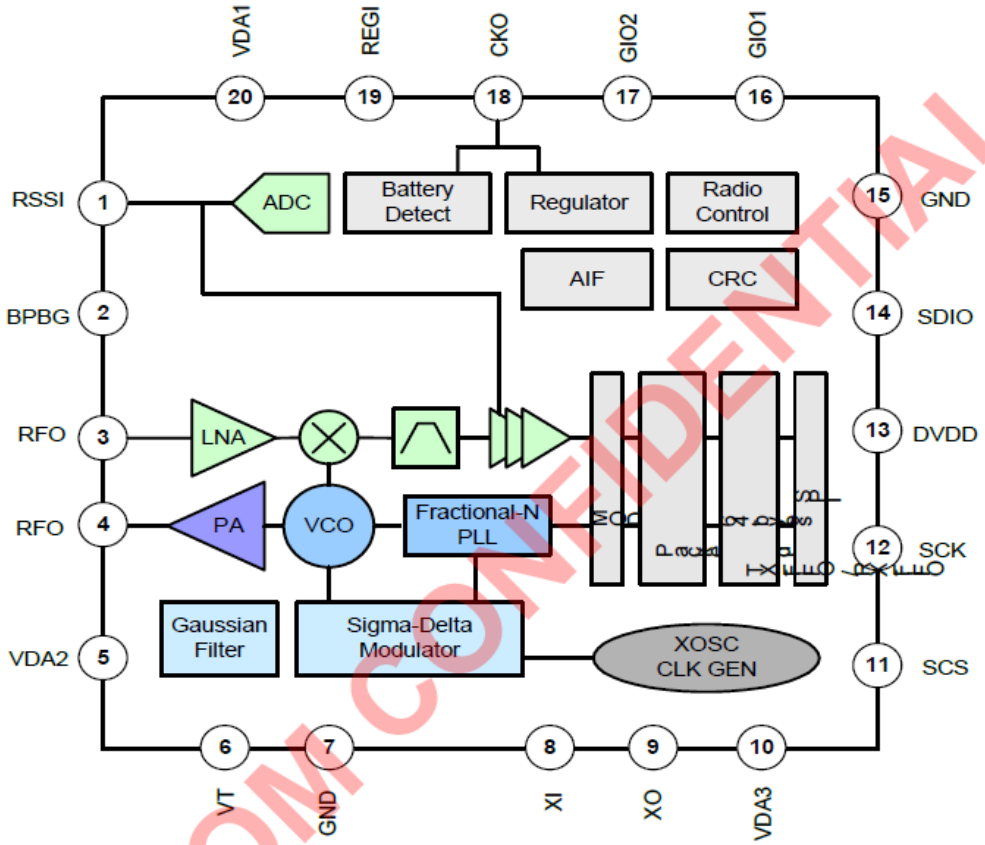
## 4. Pin Configurations




## 5. Pin Description (I: input; O: output, I/O: input or output)

| Pin No. | Symbol | I/O | Function Description |
|---|---|---|---|
| 1 | RSSI | O | Connected to a bypass capacitor for RSSI reading. |
| 2 | BPBG | O | Connected to a bypass capacitor for internal Regulator bias point |
| 3 | RFI | I | Low noise amplifier input. |
| 4 | RFO | O | Power amplifier output. (powered by VDA1) |
| 5 | VDA2 | I/O | TRX Voltage supply **(from IC internal analog regulator)**, connected to a bypass capacitor. |
| 6 | VT | I | VCO frequency control input, internal connected to PLL charge pump. |
| 7 | GND | G | Ground |
| 8 | XI | I | Crystal oscillator input node |
| 9 | XO | O | Crystal oscillator output node |
| 10 | VDA3 | I | Voltage supply **(from VDA1, pin 20)** for PLL part |
| 11 | SCS | I | 3 wire SPI chip select. |
| 12 | SCK | I | 3 wire SPI clock input pin. |
| 13 | DVDD | I | TRX Voltage supply **(from IC internal digital regulator)**, Connected to a bypass capacitor. |
| 14 | SDIO | I/O | 3 wire SPI read/write data pin. |
| 15 | GND | G | Ground |
| 16 | GIO1 | I/O | Multi-function GIO1 / 4-wire SPI data output. |
| 17 | GIO2 | I/O | Multi-function GIO2 / 4-wire SPI data output. |
| 18 | CKO | O | Multi-function clock output. |
| 19 | REGI | I | Internal Regulator input **(External Power Input)** |
| 20 | VDA1 | I/O | Internal Analog Regulator output to supply **RFO (pin 4) and VDA3 (pin 10).** |
| | **Back side plate** | G | Ground.<br>Back side plate shall be well-solder to ground; otherwise, it will impact RF performance. |

## 6. Chip Block Diagram




## 7. Absolute Maximum Ratings

| Parameter | With respect to | Rating | Unit |
|---|---|---|---|
| Supply voltage range (VDD) | GND | -0.3 ~ 3.6 | V |
| Digital IO pins range | GND | -0.3 ~ VDD+0.3 | V |
| Voltage on the analog pins range | GND | -0.3 ~ 2.1 | V |
| Input RF level | | 5 | dBm |
| Storage Temperature range | | -55 ~ 125 | °C |
| ESD Rating | HBM | ± 2K | V |
| | MM | ± 100 | V |

*Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*Device is ESD sensitive. Use appropriate ESD precautions. HBM (Human Body Mode) is tested under MIL-STD-883F Method 3015.7. MM (Machine Mode) is tested under JEDEC EIA/JESD22-A115-A.
*Device is Moisture Sensitivity Level III (MSL 3).

## 8. Electrical Specification

(Ta=25℃, VDD=3.0V, data rate= 500Kbps, IF bandwidth = 500KHz, $F_{XTAL}$ =16MHz, with Match Networking and low pass filter, On Chip Regulator = 2.1V, unless otherwise noted.)

| Parameter | Description | Min. | Type | Max. | Unit |
|---|---|---|---|---|---|
| **General** | | | | | |
| Operating Temperature | | -40 | | 85 | °C |
| Supply Voltage (VDD) | with internal regulator | 2.0 | | 3.6 | V |
| Current Consumption | Sleep mode (RC OSC off) | | 1.5*[1] | | μA |
| | Idle Mode (Regulator on) | | 0.3*[1] | | mA |
| | Standby Mode (XOSC on,clock generator on) | | 1.9 | | mA |
| | PLL mode | | 9 | | mA |
| | RX Mode | | 16 | | mA |
| | TX Mode (@0dBm output) | | 20 | | mA |
| | TX Mode (@-3dBm output) | | 16 | | mA |
| | TX Mode (@-6dBm output) | | 14.5 | | mA |
| | TX Mode (@-11dBm output) | | 13.9 | | mA |
| | TX Mode (@-20dBm output) | | 12.5 | | mA |
| **PLL block** | | | | | |
| Crystal start up time*[2] | | | 0.6 | | ms |
| Crystal frequency | | | 6, 8, 12, **16**, 20, 24 | | MHz |
| Crystal tolerance | without FW FC | | ±10 | | ppm |
| | with FW FC | | ±20 | | ppm |
| Crystal ESR | | | | 80 | ohm |
| VCO Operation Frequency | | 2400 | | 2483.5 | MHz |
| PLL phase noise | Offset 10k<br>Offset 100K<br>Offset 1M | | 80<br>85<br>90 | | dBc |
| PLL settling time *[3] | @Loop BW = 500Khz | | 70 | | μS |
| **Transmitter** | | | | | |
| Output power range | | -20 | 0 | | dBm |
| Out Band Spurious Emission *[4] | 30MHz~1GHz | | | -36 | dBm |
| | 1GHz~12.75GHz | | | -30 | dBm |
| | 1.8GHz~ 1.9GHz | | | -47 | dBm |
| | 5.15GHz~ 5.3GHz | | | -47 | dBm |
| Frequency deviation*[5] | Data rate > 50Kbps | | 186K | | Hz |
| | Date rate <=50Kbps | | 124K | | Hz |
| Data rate | | 2K | | 500K | Bps |
| TX ready time*[6] (PLL to WPLL + WPLL to TX) | @Loop BW = 500 KHz, LO fixed | | 10+60 | | μS |
| | @Loop BW = 500 KHz, Hopping | | 70+60 | | μS |
| **Receiver** | | | | | |
| Receiver sensitivity @ BER = 0.1% | Data rate 500K ($F_{IF}$ = 500KHz) | | -95 | | dBm |
| | Data rate 250K ($F_{IF}$ = 500KHz) | | -97 | | dBm |

| | | | | | |
|---|---|---|---|---|---|
| | Data rate 25K ($F_{IF}$ = 500KHz) | | -104 | | dBm |
| | Data rate 2K ($F_{IF}$ = 500KHz) | | -107 | | dBm |
| IF frequency bandwidth | | | 250/500 | | KHz |
| IF center frequency | | | 250/500 | | KHz |
| Interference *7 | Co-Channel ($C/I_0$) | | 11 | | dB |
| | ±1MHz Adjacent Channel | | - 20 | | dB |
| | ±2MHz Adjacent Channel | | - 30 | | dB |
| | > ±5MHz Adjacent Channel | | - 40 | | dB |
| | Image ($C/I_{IM}$) | | - 12 | | dB |
| Maximum Operating Input Power | @RF input (BER=0.1%) | | | 0 | dBm |
| Spurious Emission *4 | 30MHz~1GHz | | | -57 | dBm |
| | 1GHz~12.75GHz | | | -47 | |
| RSSI Range | @RF input | -105 | | -50 | dBm |
| RX Ready Time*8 (PLL to WPLL + WPLL to RX) | LO fixed, Data rate < = 125 Kbps | | 10+40 | | µs |
| | LO fixed, Data rate = 250 Kbps | | 10+100 | | µs |
| | LO fixed, Data rate = 500 Kbps | | 10+60 | | µs |
| | Hopping, Data rate < = 125 Kbps | | 70+40 | | µs |
| | Hopping, Data rate = 250 Kbps | | 70+100 | | µs |
| | Hopping, Data rate = 500 Kbps | | 70+60 | | µs |
| RX Spurious Emission | above 1GHz | | | -47 | dBm |
| **Regulator** | | | | | |
| Regulator settling time | Pin 2 connected to 1.5 nF | | 500*9 | | µs |
| Band-gap reference voltage | | | 1.23 | | V |
| Regulator output voltage | | 1.8 | 2.1 | 2.3 | V |
| Line regulation | Load current 30mA | 35 | 40 | | dBc |
| **Digital IO DC characteristics** | | | | | |
| High Level Input Voltage ($V_{IH}$) | | 0.8*VDD | | VDD | V |
| Low Level Input Voltage ($V_{IL}$) | | 0 | | 0.2*VDD | V |
| High Level Output Voltage ($V_{OH}$) | @$I_{OH}$= -0.5mA | VDD-0.4 | | VDD | V |
| Low Level Output Voltage ($V_{OL}$) | @$I_{OL}$= 0.5mA | 0 | | 0.4 | V |

Note 1: When digital I/O pins are configured as input, those pins shall NOT be floating but pull either high or low (SCS shall be pulled high only); otherwise, leakage current will be induced.
Note 2: Refer to Delay Register II (17h) to set up crystal settling delay.
Note 3: Refer to Delay Register I (17h) to set up PDL (PLL settling delay).
Note 4: With external RF filter that provides minimum 17dB of attenuation in the band: 30MHz ~ 2GHz and 3GHz ~12.75GHz.
Note 5: Refer to TX Register II (15h) to set up FD [4:0].
Note 6: Refer to Delay Register I (17h) to set up PDL and TDL delay.
Note 7: The power level of wanted signal is set at sensitivity level +3dB. The modulation data for wanted signal and interferer are PN9 and PN15, respectively. Channel spacing is 500KHz.
Note 8: For 250K/500Kbps, set DCM[1:0]= [10b] by ID, (29h). For <= 125Kbps, set DCM[1:0]= [01b] by Preamble, (29h).
Note 9: When VDD < 2.1V and temperature < -30 degree C, the regulator settling time will arise up to **20ms**.

## 9. Control Register

A7105 contains 51 x 8-bit control registers. MCU can access those control registers via 3-wire (SCS, SCK, SDIO) or 4-wire (SCS, SCK, SDIO, GIO1/GIO2) SPI interface (support max. SPI data rate up to 10 Mbps). User can refer to chapter 10 for details of SPI timing. A7105 is simply controlled by registers and outputs its status to MCU by GIO1 and GIO2 pins.

### 9.1 Control register table

| Address / Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 00h Mode | W | RESETN | RESETN | RESETN | RESETN | RESETN | RESETN | RESETN | RESETN |
| | R | -- | FECF | CRCF | CER | XER | PLLER | TRSR | TRER |
| 01h Mode control | W | DDPC | ARSSI | AIF | DFCD | WWSE | FMT | FMS | ADCM |
| | R | DDPC | ARSSI | AIF | CD | WWSE | FMT | FMS | ADCM |
| 02h Calc | R/W | -- | -- | -- | -- | -- | VCC | VBC | FBC |
| 03h FIFO I | W | FEP7 | FEP6 | FEP5 | FEP4 | FEP3 | FEP2 | FEP1 | FEP0 |
| 04h FIFO II | W | FPM1 | FPM0 | PSA5 | PSA4 | PSA3 | PSA2 | PSA1 | PSA0 |
| 05h FIFO Data | R/W | FIFO7 | FIFO6 | FIFO5 | FIFO4 | FIFO3 | FIFO2 | FIFO1 | FIFO0 |
| 06h ID Data | R/W | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| 07h RC OSC I | W | WWS_SL7 | WWS_SL6 | WWS_SL5 | WWS_SL4 | WWS_SL3 | WWS_SL2 | WWS_SL1 | WWS_SL0 |
| | R | -- | -- | RCOC5 | RCOC4 | RCOC3 | RCOC2 | RCOC1 | RCOC0 |
| 08h RC OSC II | W | WWS_SL9 | WWS_SL8 | WWS_AC5 | WWS_AC4 | WWS_AC3 | WWS_AC2 | WWS_AC1 | WWS_AC0 |
| 09h RC OSC III | W | BBCKS1 | BBCKS0 | -- | -- | -- | RCOSC_E | TSEL | TWWS_E |
| 0Ah CKO Pin | W | ECKOE | CKOS3 | CKOS2 | CKOS1 | CKOS0 | CKOI | CKOE | SCKI |
| 0Bh GPIO1 Pin I | W | -- | -- | GIO1S3 | GIO1S2 | GIO1S1 | GIO1S0 | GIO1I | GIO1OE |
| 0Ch GPIO2 Pin II | W | -- | -- | GIO2S3 | GIO2S2 | GIO2S1 | GIO2S0 | GIO2I | GIO2OE |
| 0Dh Clock | R/W | GRC3 | GRC2 | GRC1 | GRC0 | CSC1 | CSC0 | CGS | XS |
| 0Eh Data rate | R/W | SDR7 | SDR6 | SDR5 | SDR4 | SDR3 | SDR2 | SDR1 | SDR0 |
| 0Fh PLL I | R/W | CHN7 | CHN6 | CHN5 | CHN4 | CHN3 | CHN2 | CHN1 | CHN0 |
| 10h PLL II | R/W | DBL | RRC1 | RRC0 | CHR3 | CHR2 | CHR1 | CHR0 | IP8 |
| 11h PLL III | R/W | IP7 | IP6 | IP5 | IP4 | IP3 | IP2 | IP1 | IP0 |
| 12h PLL IV | W | FP15 | FP14 | FP13 | FP12 | FP11 | FP10 | FP9 | FP8 |
| | R | -- | AC14 | AC13 | AC12 | AC11 | AC10 | AC9 | AC8 |
| 13h PLL V | W | FP7 | FP6 | FP5 | FP4 | FP3 | FP2 | FP1 | FP0 |
| | R | AC7 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |
| 14h TX I | W | TXSM1 | TXSM0 | TXDI | TME | FS | FDP2 | FDP1 | FDP0 |
| 15h TX II | W | -- | PDV1 | PDV0 | FD4 | FD3 | FD2 | FD1 | FD0 |
| 16h Delay I | W | DPR2 | DPR1 | DPR0 | TDL1 | TDL0 | PDL2 | PDL1 | PDL0 |
| 17h Delay II | W | WSEL2 | WSEL1 | WSEL0 | AGC_D1 | AGC_D0 | RS_DLY2 | RS_DLY1 | RS_DLY0 |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 18h RX | W | -- | RXSM1 | RXSM0 | FC | RXDI | DMG | BWS | ULS |
| 19h RX Gain I | R/W | MVGS | -- | IGC | MGC1 | MGC0 | LGC2 | LGC1 | LGC0 |
| 1Ah RX Gain II | W | RH7 | RH6 | RH5 | RH4 | RH3 | RH2 | RH1 | RH0 |
| 1Bh RX Gain III | W | RL7 | RL6 | RL5 | RL4 | RL3 | RL2 | RL1 | RL0 |
| 1Ch RX Gain IV | W | ENGC | -- | -- | -- | MHC | LHC1 | LHC0 | VGCE |
| 1Dh RSSI Threshold | W | RTH7 | RTH6 | RTH5 | RTH4 | RTH3 | RTH2 | RTH1 | RTH0 |
| | R | ADC7 | ADC6 | ADC5 | ADC4 | ADC3 | ADC2 | ADC1 | ADC0 |
| 1Eh ADC | W | RSM1 | RSM0 | ERSS | FSARS | -- | XADS | RSS | CDM |
| 1Fh Code I | W | -- | MCS | WHTS | FECS | CRCS | IDL | PML1 | PML0 |
| 20h Code II | W | -- | DCL2 | DCL1 | DCL0 | ETH1 | ETH0 | PMD1 | PMD0 |
| 21h Code III | W | -- | WS6 | WS5 | WS4 | WS3 | WS2 | WS1 | WS0 |
| 22h IF Calibration I | W | -- | -- | -- | MFBS | MFB3 | MFB2 | MFB1 | MFB0 |
| | R | -- | -- | -- | FBCF | FB3 | FB2 | FB1 | FB0 |
| 23h IF Calibration II | R | -- | -- | -- | FCD4 | FCD3 | FCD2 | FCD1 | FCD0 |
| 24h VCO current Calibration | W | -- | -- | VCCS | MVCS | VCOC3 | VCOC2 | VCOC1 | VCOC0 |
| | R | -- | -- | -- | FVCC | VCB3 | VCB2 | VCB1 | VCB0 |
| 25h VCO Single band Calibration I | W | -- | -- | -- | -- | MVBS | MVB2 | MVB1 | MVB0 |
| | R | -- | -- | DVT1 | DVT0 | VBCF | VB2 | VB1 | VB0 |
| 26h VCO Single band Calibration II | W | -- | -- | VTH2 | VTH1 | VTH0 | VTL2 | VTL1 | VTL0 |
| 27h Battery detect | W | RGS | RGV1 | RGV0 | -- | BVT2 | BVT1 | BVT0 | BDS |
| | R | RGS | RGV1 | RGV0 | BDF | BVT2 | BVT1 | BVT0 | BDS |
| 28h TX test | W | -- | -- | TXCS | PAC1 | PAC0 | TBG2 | TBG1 | TBG0 |
| 29h Rx DEM test I | W | DMT | DCM1 | DCM0 | MLP1 | MLP0 | SLF2 | SLF1 | SLF0 |
| 2Ah Rx DEM test II | W | DCV7 | DCV6 | DCV5 | DCV4 | DCV3 | DCV2 | DCV1 | DCV0 |
| 2Bh CPC | W | -- | -- | -- | -- | -- | -- | CPC1 | CPC0 |
| 2Ch Crystal test | W | -- | -- | -- | -- | DBD | XCC | XCP1 | XCP0 |
| 2Dh PLL test | W | -- | PMPE | PRRC1 | PRRC0 | PRIC1 | PRIC0 | SDPW | NSDO |
| 2Eh VCO test I | W | -- | -- | -- | TLB | TLB | RLB | RLB | VCBS |
| 2Fh VCO test II | W | -- | -- | -- | -- | RFT3 | RFT2 | RFT1 | RFT0 |
| 30h IFAT | W | IGFI2 | IGFI1 | IGFI0 | IGFQ2 | IGFQ1 | IGFQ0 | IFBC | LIMC |
| 31h RScale | R/W | RSC7 | RSC6 | RSC5 | RSC4 | RSC3 | RSC2 | RSC1 | RSC0 |
| 32h Filter test | W | FT7 | FT6 | FT5 | FT4 | FT3 | FT2 | FT1 | FT0 |

Legend: -- = unimplemented

# Warning

## Caution:

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
-Reorient or relocate the receiving antenna.
-Increase the separation between the equipment and receiver.
-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
-Consult the dealer or an experienced radio/TV technician for help.

## MPE Reminding

To satisfy FCC RF exposure requirements, a separation distance of 20 cm or more should be maintained between the antenna of this device and persons during device operation. To ensure compliance, operations at closer than this distance is not recommended.

## Region Selection

Limited by local law regulations, version for North America does not have region selection option.

## Information for the OEM Integrators

This device is intended for OEM integrators only. Please see the full grant of equipment document for restrictions.

## Label Information to the End User by the OEM or Integrators

If the FCC ID of this module is not visible when it is installed inside another device, then the outside of the device into which the module is into which the module is installed must be label with "Contains FCC ID: FCC ID: 2AJJGHJC0".