
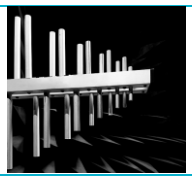
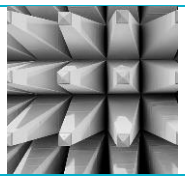

CTC advanced
member of RWTÜV group

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BNetzA-CAB-02/21-102

ilac-MRA DAkkS Deutsche Akkreditierungsstelle D-PL-12076-01-04

SAR Test exclusion documentation according to FCC KDB 447498

Report identification number: 1-2507/21-01-09 Exclusion (FCC)

Certification numbers and labeling requirements	
FCC ID	2AJ58-14

This test report is electronically signed and valid without handwritten signature. For verification of the electronic signatures, the public keys can be requested at the testing laboratory.

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EUT technologies:

Technologies:	Max. cond. Power*
NFC 13.56 MHz	23.01 dBm

)* total power dissipation max. 200 mW (see Annex A: MFRC522 datasheet)

SAR test exclusion according to KDB447498 (General RF Exposure Guidance)

Equations from Chapter 4.3.1: Standalone SAR test exclusion considerations page 11 and ff. and tables in Annex C

(c) (2) Standalone SAR test exclusion below 100 MHz < 50mm

$0.5 \times (\text{Threshold}_{100MHz}) \times (1+\log(100/f))$

where

$\text{Threshold}_{1\text{-g;}10\text{-g}}$	is 3 for 1-g; 7.5 for 10-g
f	is the RF channel transmit frequency
$\text{Threshold}_{100MHz,50mm}$	is $\text{Threshold}_{1\text{-g;}10\text{-g}} \times d / f^{0.5}$; with f = 100MHz and d=50mm

The table below gives the calculated maximal power that could be used for source based time averaged conducted power, adjusted for tune up tolerance. If this is below the calculated value SAR testing is excluded.

frequency [MHz]	Threshold1-g;10-g	$\text{Threshold}_{100MHz,50mm}$	Powerlimit [mW]	$P_{max\text{-}declared}$		Exclusion
				[dBm]	[mW]	
13.56	3	474.34	442.97	23.01	200.0	yes

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Annex A: MFRC522 datasheet:

11. Limiting values

Table 150. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	analog supply voltage		–0.5	+4.0	V
V_{DDD}	digital supply voltage		–0.5	+4.0	V
$V_{DD(PVDD)}$	PVDD supply voltage		–0.5	+4.0	V
$V_{DD(TVDD)}$	TVDD supply voltage		–0.5	+4.0	V
$V_{DD(SVDD)}$	SVDD supply voltage		–0.5	+4.0	V
V_I	input voltage	all input pins except pins MFIN and RX	$V_{SS(PVSS)}$ – 0.5	$V_{DD(PVDD)}$ + 0.5	V
		pin MFIN	$V_{SS(PVSS)}$ – 0.5	$V_{DD(SVDD)}$ + 0.5	V
P_{tot}	total power dissipation	per package; and V_{DDD} in shortcut mode	-	200	mW
T_j	junction temperature		-	100	°C
V_{ESD}	electrostatic discharge voltage	HBM; 1500 Ω, 100 pF; JESD22-A114-B	-	2000	V
		MM; 0.75 µH, 200 pF; JESD22-A114-A	-	200	V
		Charged device model; JESD22-C101-A			
		on all pins	-	200	V
		on all pins except SVDD in TFBGA64 package	-	500	V