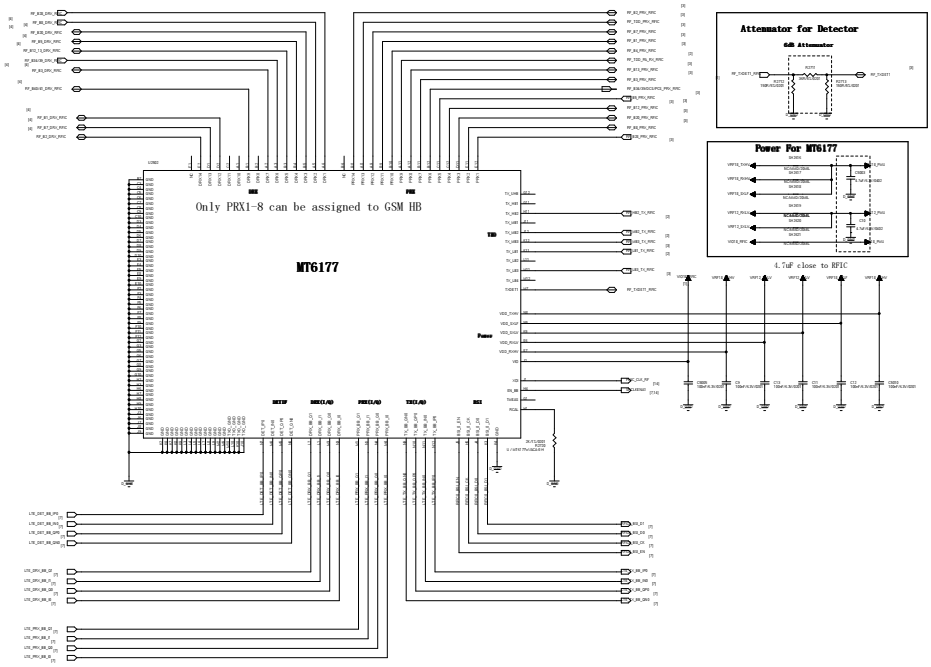
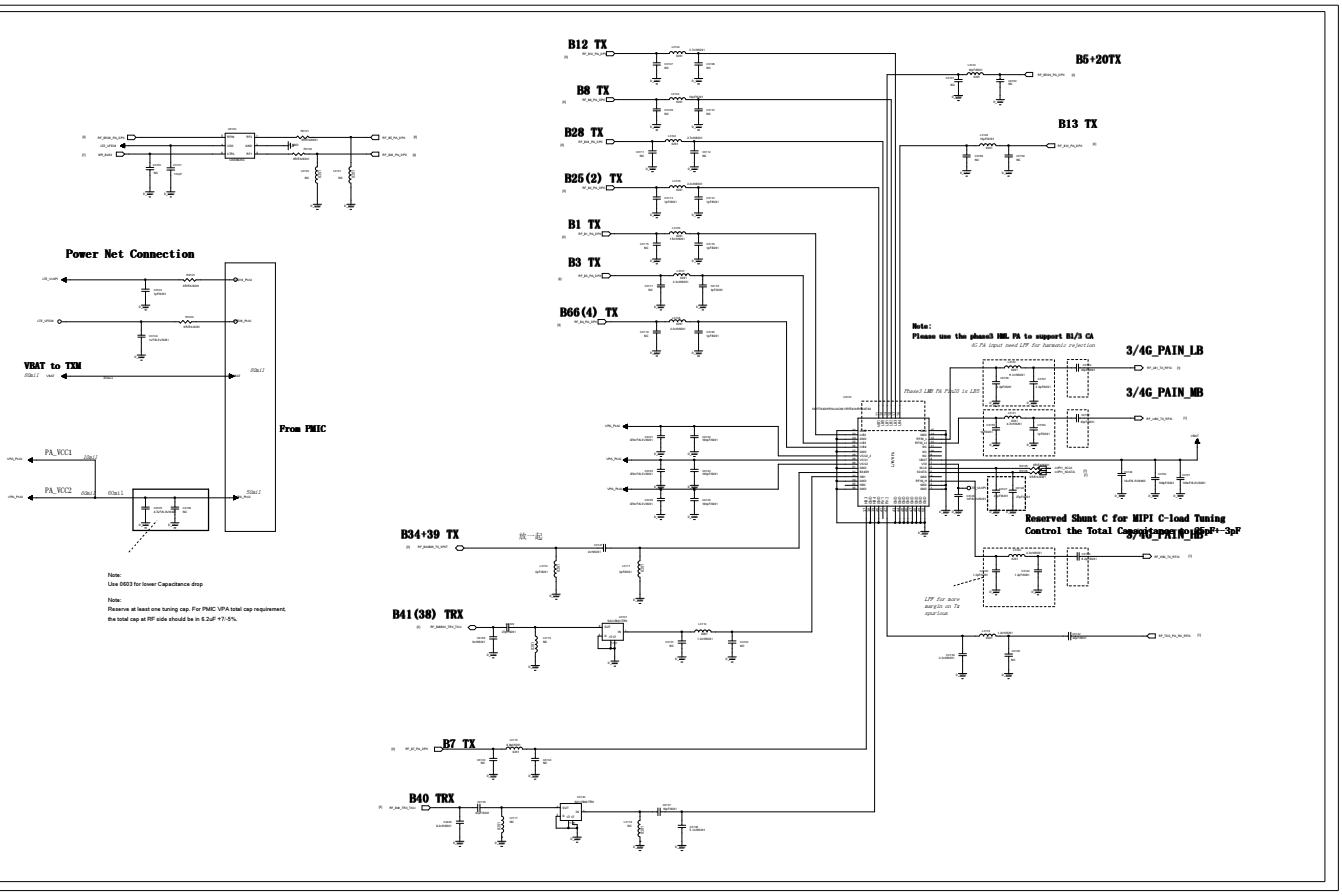
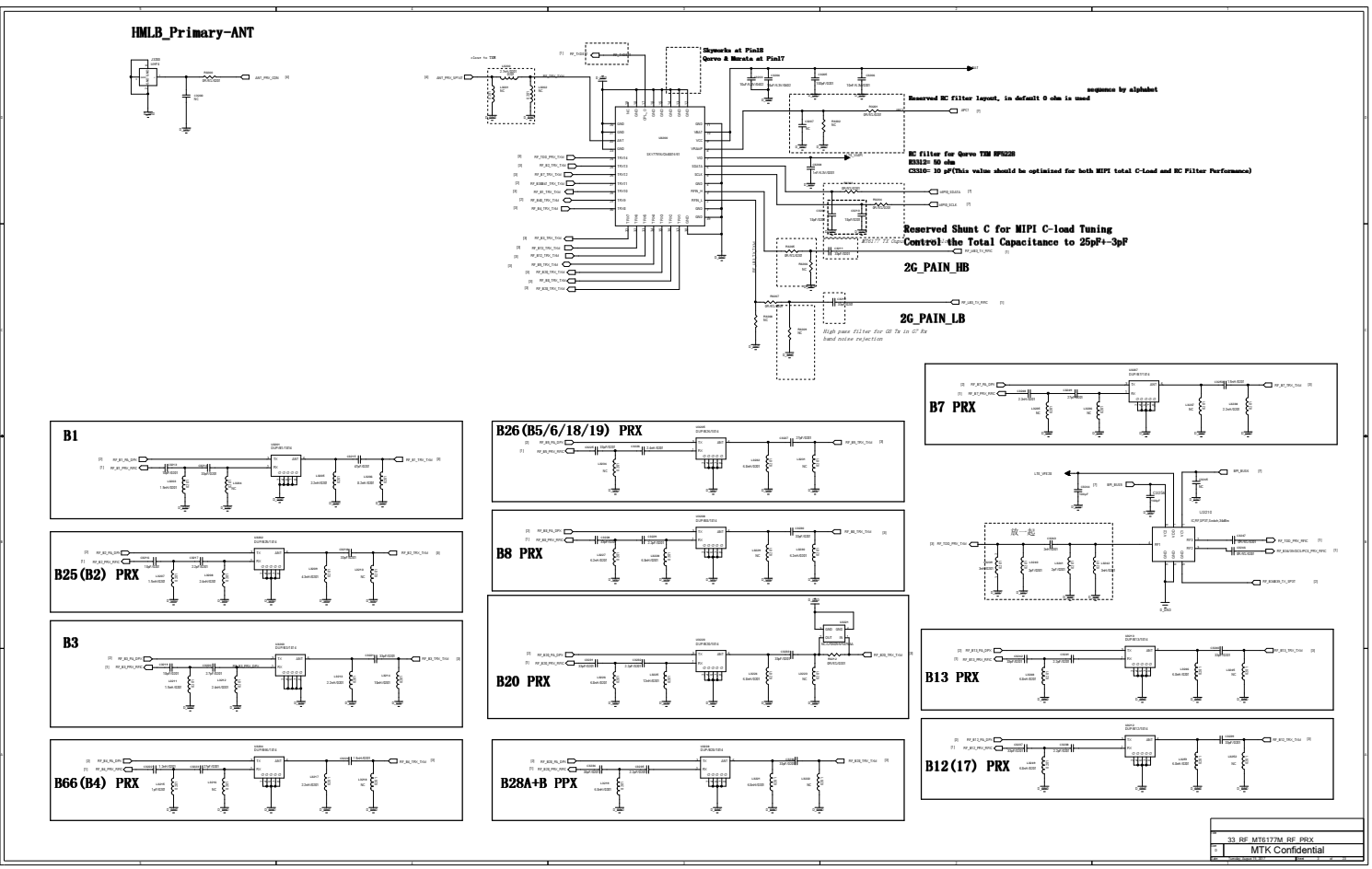

Attenuator for Detector
6db Attenuator
Power For MT6177
Only PRX1-8 can be assigned to GSM HB
MT6177
4.7uF close to RFIC

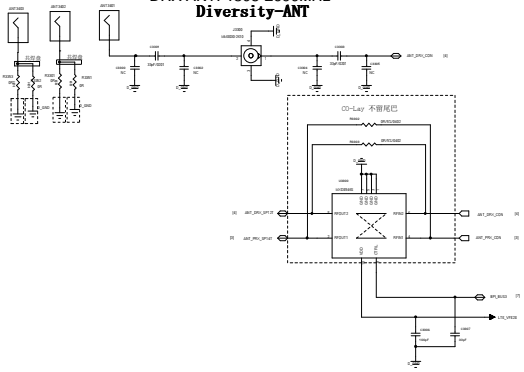

B12 TX
B8 TX
B28 TX
B25(2) TX
B1 TX
B3 TX
B66(4) TX
B5+20TX
B13 TX
3/4G_PAIN_LB
3/4G_PAIN_MB
3/4G_PAIN_HB
B34+39 TX
B41(38) TRX
B7 TX
B40 TRX
Power Net Connection
VBAT to TXM
From PMIC
PA_VCC1
PA_VCC2
Note:
Use 0603 for lower Capacitance drop
Note:
Reserve at least one tuning cap. For PMIC VPA total cap requirement,
the total cap at RF side should be in 6.2uF +7/-5%.
Note:
Please use the phase3 HBL PA to support B1/3 CA
B1 PA input need LPF for harmonic rejection
Phase3 LMB PA Pin20 is LB1
Reserved Shunt C for MIPI C-load Tuning
Control the Total Capacitance Range 1pF~3pF
LPF for more margin on Tx spur issue

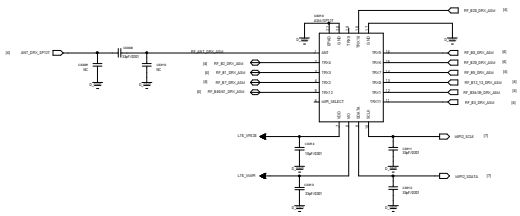

HMLB_Primary-ANT
Skyworks at Pin18
Qorvo & Murata at Pin17
sequence by alphabet
Reserved NC filter layout, in default 0 ohm is used
NC filter for Qorvo TDM SPN32B
RSH12= NC ohm
CSH10= 10 pF(This value should be optimized for both MIPI total C-Load and NC Filter Performance)
Reserved Shunt C for MIPI C-load Tuning
Control the Total Capacitance to 25pF+-3pF
2G_PAIN_HB
2G_PAIN_LB
High pass filter for GS Tx in GT Rx
band noise rejection
B1
B25(B2) PRX
B3
B66(B4) PRX
B26(B5/6/18/19) PRX
B8 PRX
B20 PRX
B28A+B PPX
B7 PRX
放一起
B13 PRX
B12(17) PRX
33_RF_MT6177M_RF_PRX
MTK Confidential

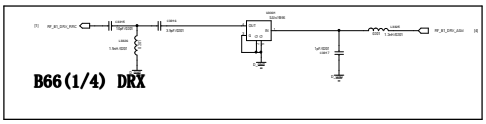
分集天线弹片

DRX ANT: 1805-2690MHz

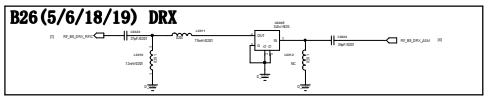
Diversity-ANT



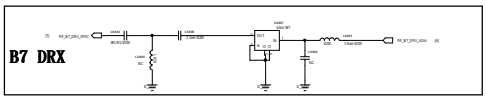




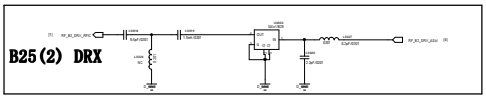
B66(1/4) DRX



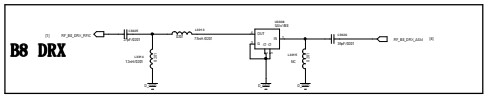
B26(5/6/18/19) DRX



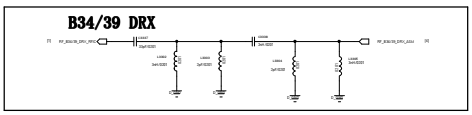
B7 DRX



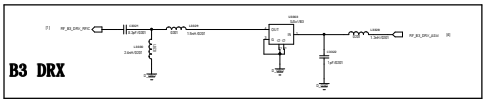
B25(2) DRX



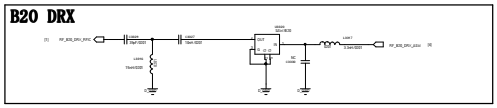
B8 DRX



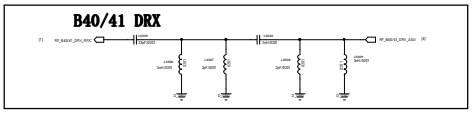
B34/39 DRX



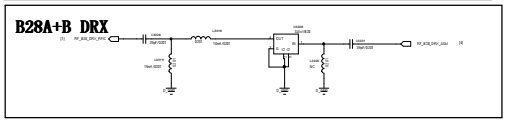
B3 DRX



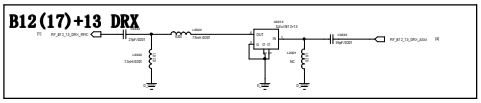
B20 DRX



B40/41 DRX

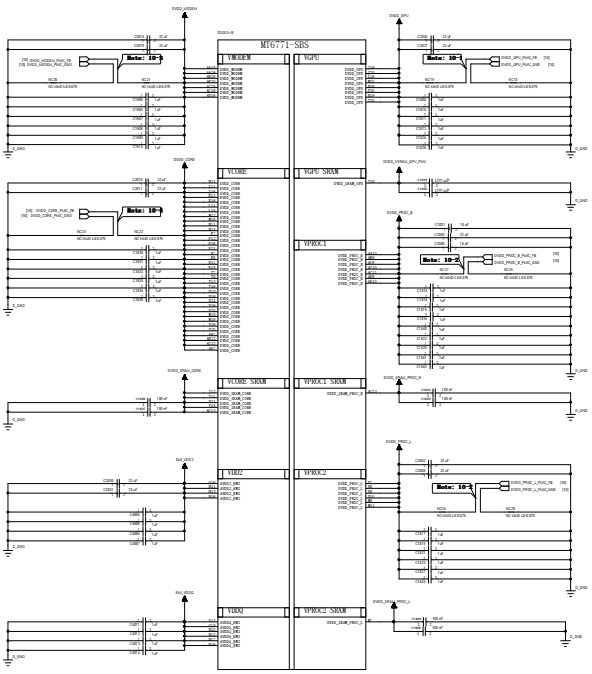


B28A+B DRX



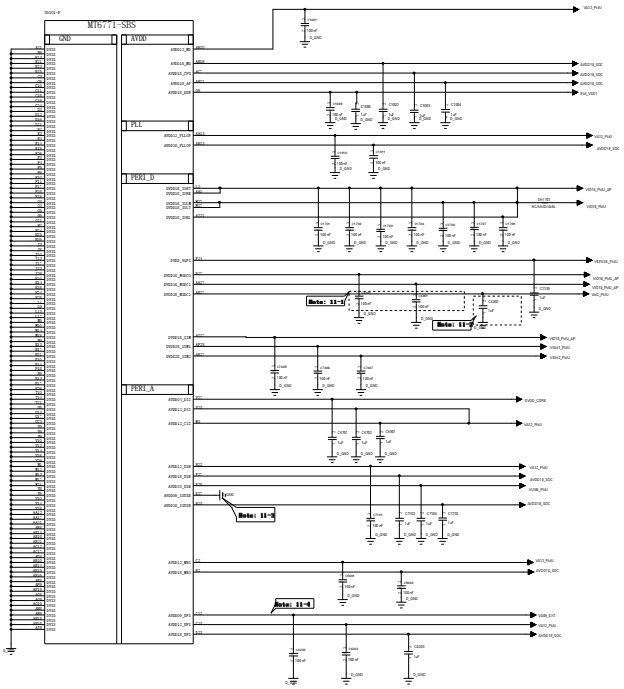
B12(17)+13 DRX

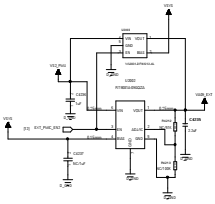
	34_RF_MT6177M_RF_DRX
	MTK Confidential



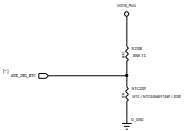
Schematic design notice of "10_BB_POWER_PDN" page.

Note 10-1:	Differential pair of DVDD_GPU remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)
Note 10-2:	Differential pair of DVDD_PROC remote sense must be close to BB's ball Remote sense trace with GND shielding to PMIC (Differential)
Note 10-3:	Differential pair of DVDD_MODEM remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)
Note 10-4:	Differential pair of DVDD_CORE remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)



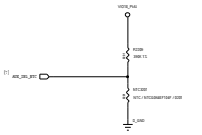


Schematic design notice of "11_HB_POWER_IO" page.
Note 11-1: C4101 closed DVDD18_MSDC0 150mil C4301 closed DVDD18_MSDC1 150mil
Note 11-2: C4302 closed DVDD28_MSDC1 150mil
Note 11-3: Connects "AVDD09_SSUSB" to GND when USB3.0 is not used.
Note 11-4: Connects "AVDD09_UFS" to GND when UFS is not used.



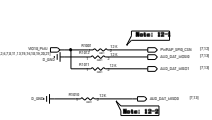
Thermistor to sense AP temperature

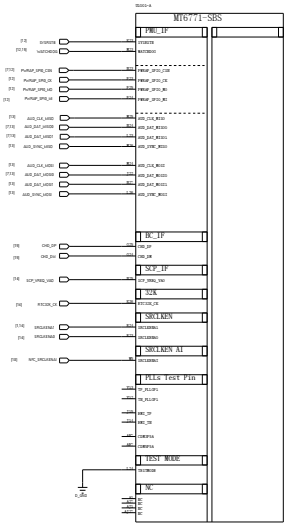
1. RTC3550must keep a distance about 4~5 cm away from AP and far from other heat sources 10 cm at least.
2. The distance is the shortest distance from package edge to edge.

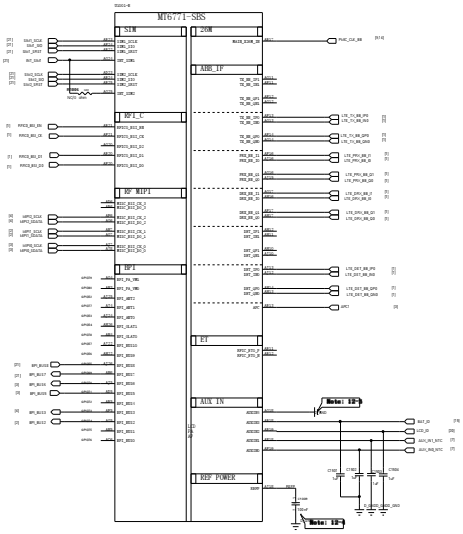


Thermistor to sense RF PA temperature

1. RTC3550 must close to LTE Band 7 PA or the hottest PA Class.
2. The distance is the shortest distance from package edge to edge.







Schematic design notice of "12_BB_1" page.

Note 12-1: "PWRAP_SPI0_CSN" and "AUD_DAT_MOSI0" are bootstrap pins to select which interface will be the JTAG pin out.

PWRAP_SPI0_CSN	AUD_DAT_MOSI0	AP_JTAG	IO_JTAG
HI	LO	N/A	N/A
HI	HI	SPI_CSB/SPI_CLK/ SPI_MO/SPI_MI/EINT8	N/A
LO	LO	SPI_CSB/SPI_CLK/ SPI_MO/SPI_MI/EINT8	DPI_11/DPI_HSYNC/DPI_VSYNC/DPI_DE/ DPI_CK/DPI_D8/DPI_D9
LO	HI	MSDC1_CLK/CMD/ DAT0/DAT1/DAT2	N/A

Note 12-2: "AUD_DAT_MISO0" is bootstrap pin to enable serial JTAG output over USB2.0 interface or not.
When "AUD_DAT_MISO0" is pulled to high in system start up and then USB2.0 interface will be switched into serial JTAG mode.

"AUD_DAT_MISO1" is bootstrap pin to select system booting up from eMMC or UFS device.

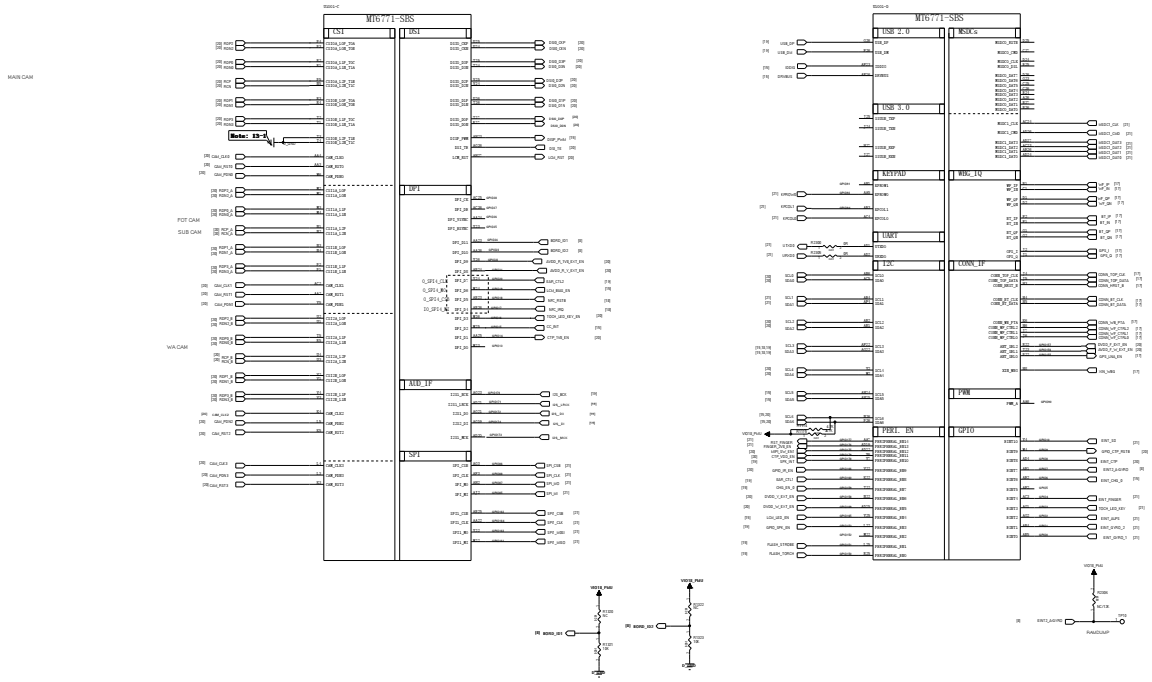
AUD_DAT_MISO1	Booting device
LO	eMMC
HI	UFS

Note 12-3: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

Note 12-4: The de-coupling cap. for REFP (AJ18 ball) have to be placed as close to BB as possible.

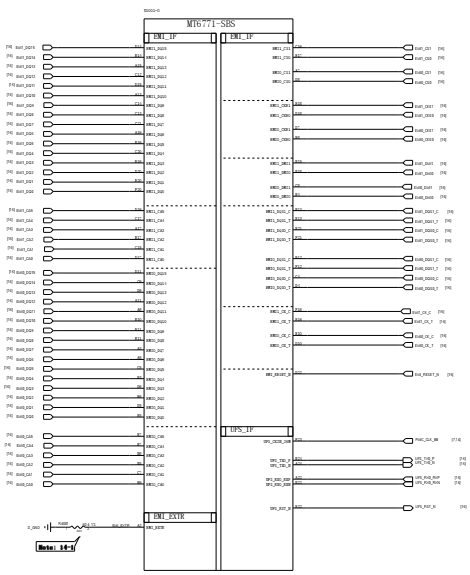
Note 12-5: AUD_SYNC_MISO and AUD_CLK_MISO are DDR type feature in bootstrap

AUD_SYNC_MISO	AUD_CLK_MISO	DDR
LO	LO	LPDDR4X
LO	HI	LPDDR4X(Ext x 2 EN)
HI	LO	LPDDR3
HI	HI	LPDDR4X(Ext x 1 EN)



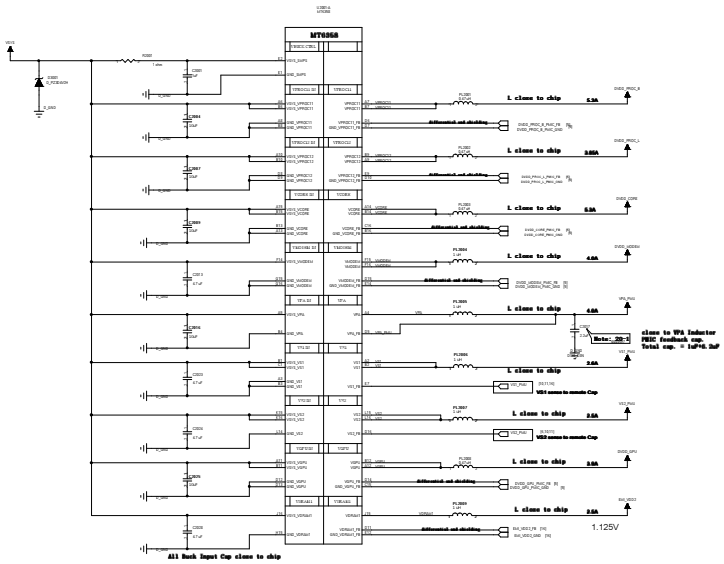
Note 13-1:

CSI ports which are no use could be connected to GND or set in NC.
For detail information, please refer to MT6771 Design Notice



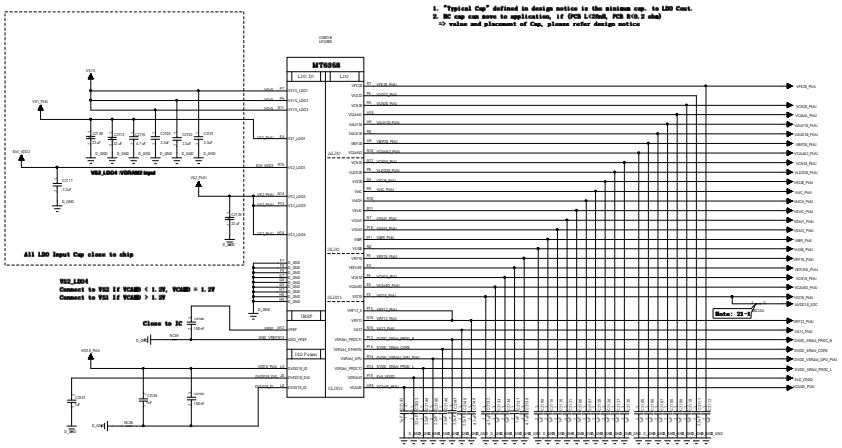
Schematic design notice of "14_BB_3" page.

Note 14-1: The resistor of EMI_EXTR for DRAM has to be placed near to BB as close as possible
R4001, please select 60.4 ohm 1% resistor



Schematic design notice of "20_POWER_MT6358-Buck" page.

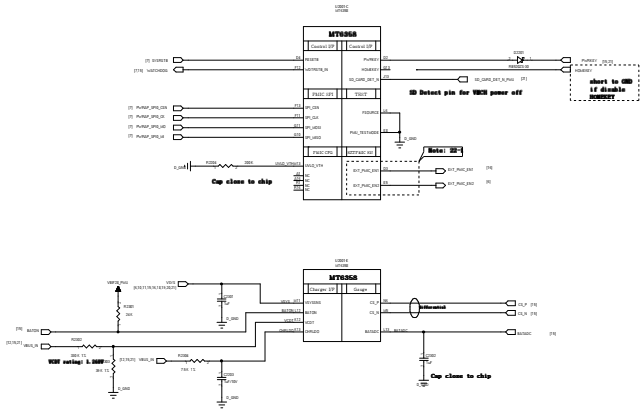
Note 20-1: Please select C2017 with 0402 size



Schematic design notice of "21_POWER_MT6358-LDO" page.

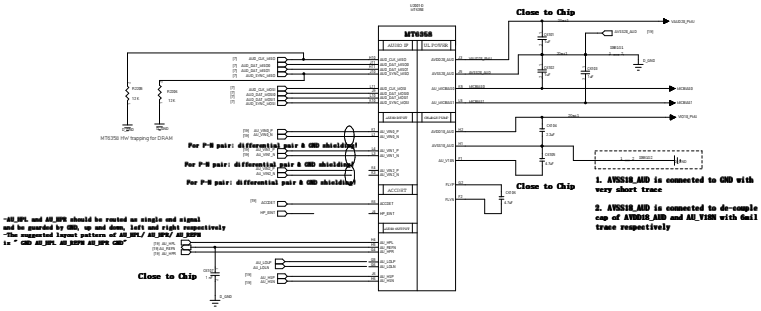
Note 21-1: Please set SH2101 close to C2132, making star connection between VIO18_PMU and AVDD18_SOC near to LDO cap. C2132

Please also refer to MT6358 design notice for further detail design information



Schematic design notice of "22_POWER_MT6358-General"

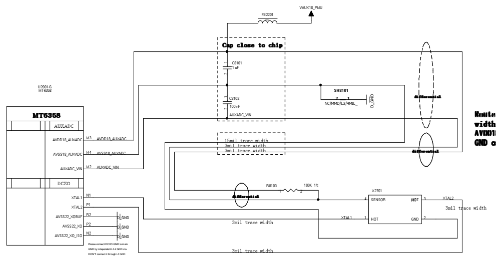
Note 22-1: EXT_PMIC_EN1 : For UFS_1V8, and keep floating if it is not used
EXT_PMIC_EN2 : For VA09 of SSUSB/UFS, and keep floating if it is not used



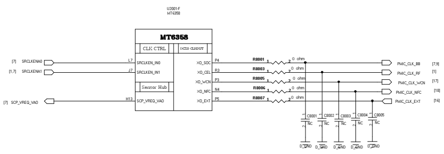
Schematic design notice of "23_POWER_MT6358-Audio"

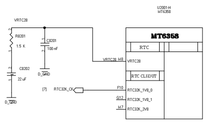
Note 23-1: VDRAM 2 / VDRAM1 output voltage vs. trap pin.

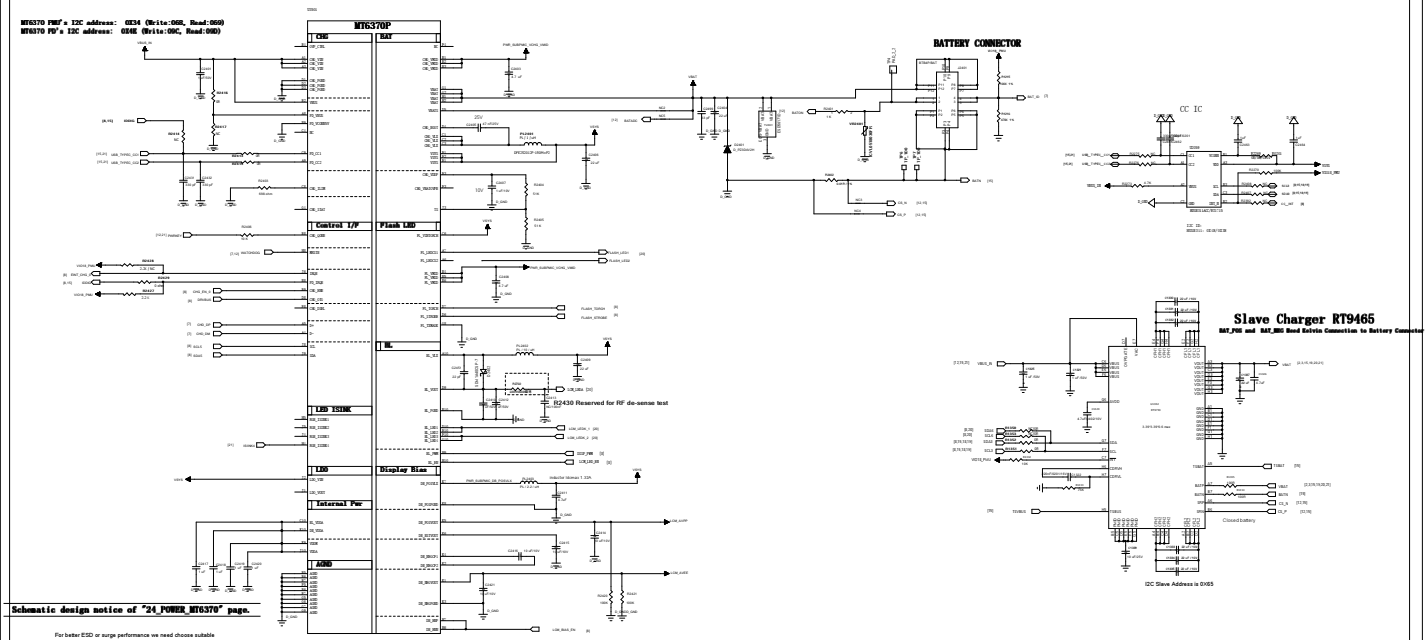
HW GPIO configuration		Trapping Option		DRAM type	VDRAM2 Power source (VS2_LDO1_ball)
AUD_SYNC_MISO	AUD_CLK_MISO	VDRAM1	VDRAM2		
0	0	1.125V	0.6V	LP4X	VDRAM1
0	1	OFF	1.8V	LP4X (Ext x 2 EN)	VS1
1	0	1.225V	OFF	LP3	VDRAM1
1	1	1.125V	1.8V	LP4X (Ext x 1 EN)	VS1



Route AVDD18_AUXADC/AUXADC_VIN with 3mil trace width and with well GND shielding.
AVDD18_AUXADC/AUXADC_VIN need to be shielded with GND or AVSS18_AUXADC.







Schematic design notice of "24_POWER_MT6370" page.

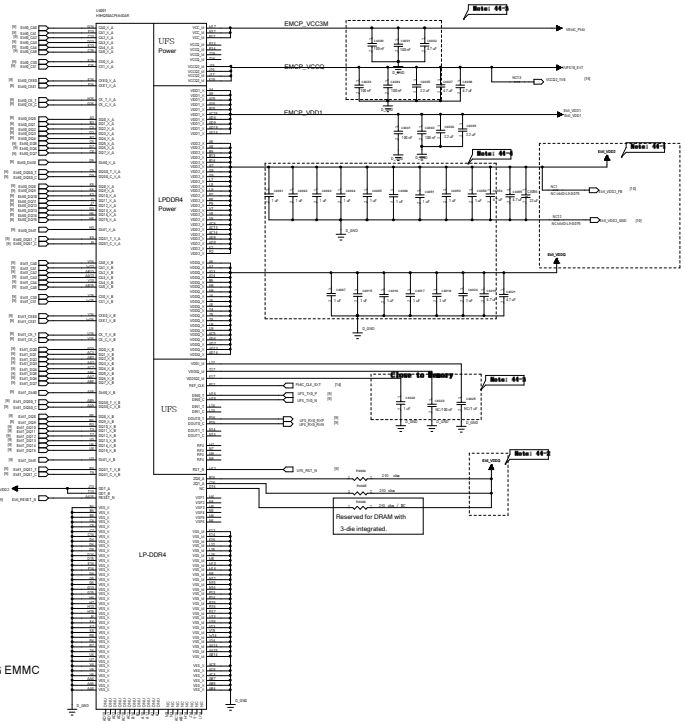
For better ESD or surge performance we need choose suitable device for system protection. Please refer to [Surge device selection

Note 24-1:

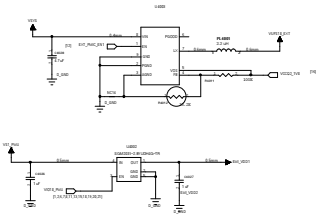
Schematic design notice of "27_POWER_SubPMIC-HV powers" page.

Note 27-1: It is recommended to reserve 0-ohm and cap. for BOM fine tune to minimize RF de-sense.

Note 27-2: It is recommended to reserve 0-ohm for BOM fine tune to minimize RF de-sense.

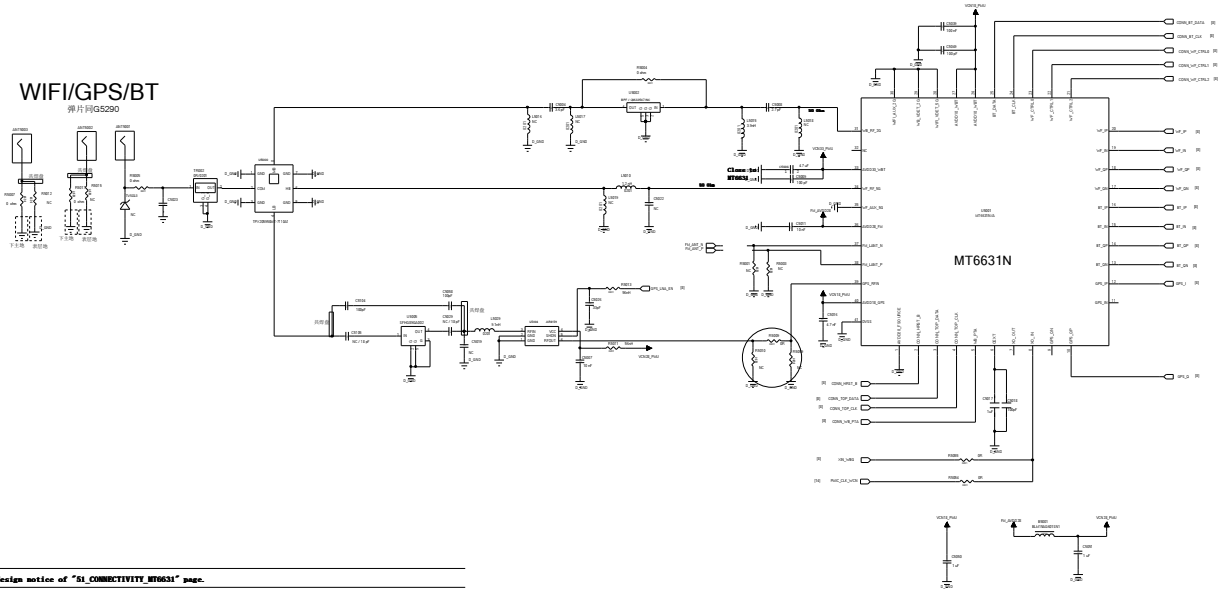


3G LPDDR4X+32G EMMC



Schematic design notice of "44_Memory_eMMC_LPDDR4X"

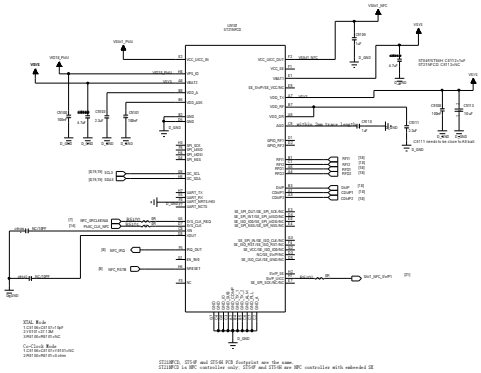
Note 44-1:	Please refer to power supply related page select VDRAM 2 / VDRAM1 output voltage properly for LPDDR4X
Note 44-2:	DRAM ZQx resistor = 240ohm (1%) that must be connected to VDDQ.
Note 44-3:	Please refer to eMCP vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDD1 power domains of eMMC.
Note 44-4:	VDD2 VDDQ decoupling cap: closed to DRAM ball. For other cap for PMIC (>10uF, at PMIC page): please also refer to MMD and layout guide for placement.



Schematic design notice of "51_CONNECTIVITY_MT6631" page.

Note 51-1:

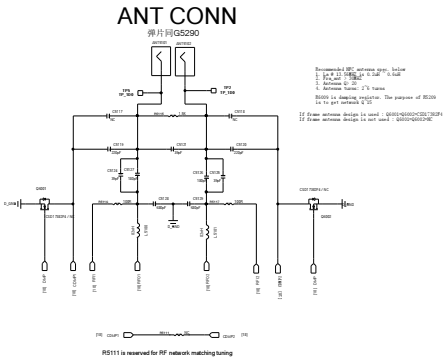
Note 51-1: Add 3dB resistor attenuator at external LNA output for more AGC saturation margin. Please let total RF loss < 6dB from external LNA output to GPS chip-input.



ST21NFCD, ST54F and ST54H PCB footprint are the same.
ST21NFCD is NFC controller only. ST54F and ST54H are NFC controller with embedded SE

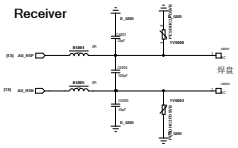
SE ball name definition for ST54F, ST54H, and ST21NFCD, respectively

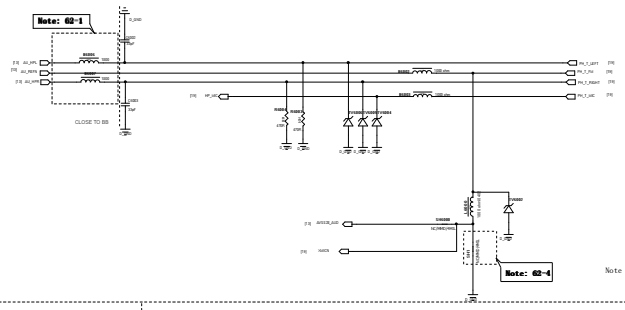
Ball	ST21NFCD	ST54F	ST54H
D5	NC	SE_SWP	NC
D4	NC	SE_SPI_MISO	SE_SPI_INT
D6	NC	SE_GND	SE_ISO_CLK
E3	NC	SE_SPI_SCK	SE_SPI_OUT(MISO)
E4	NC	SE_SPI_NSS	SE_SPI_NSS
E5	NC	SE_VCC	SE_SWP
E7	NC	NC	SE_SPI_SCK
E8	NC	SE_SPI_MOSI	SE_ISO_IO0
F4	NC	SE_ISO_RST	SE_ISO_RST
G2	NC	SE_ISO_IO0	SE_VCC
G3	NC	SE_ISO_CLK	SE_SPI_IN(MOSI)



RS111 is reserved for RF network matching tuning

Receiver

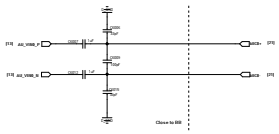




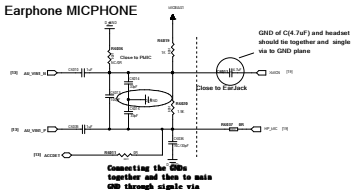
Note 62-4:

	Earphone Jack @ Main board	Earphone Jack @ Sub board
R6202	1 ohm	0.05ohm

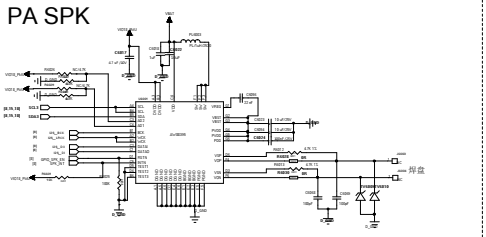
MAIN MIC



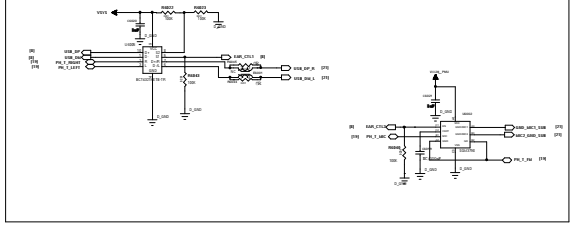
Earphone MICPHONE



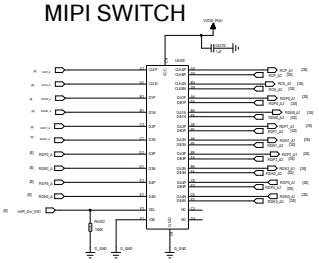
PA SPK



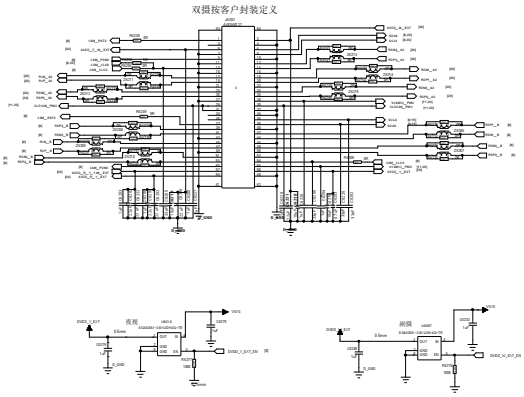
USB-DP/DM-AU-HPL/R-SWITCH-TYPE-C



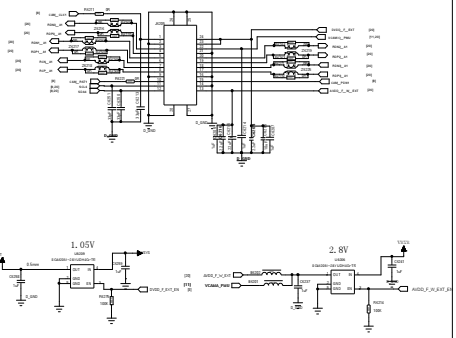
MIPI SWITCH



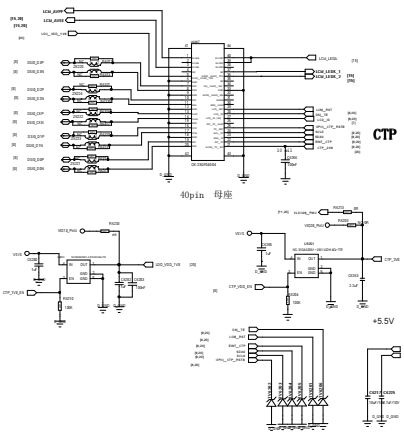
双摄按客户封装定义



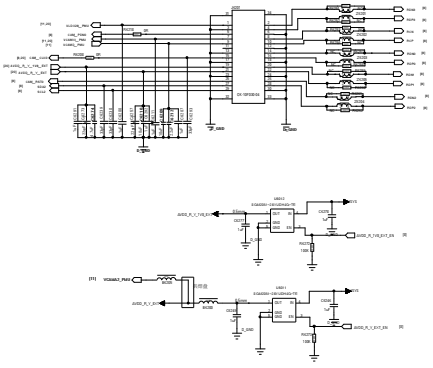
FOT CAM 前摄像头



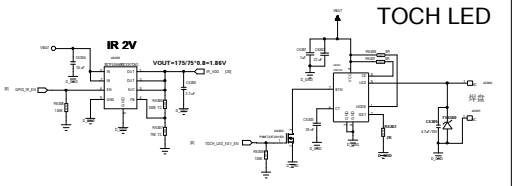
Main LCM



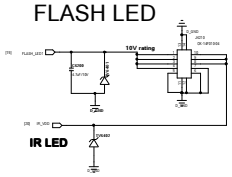
MAIN CAM



TOCH LED

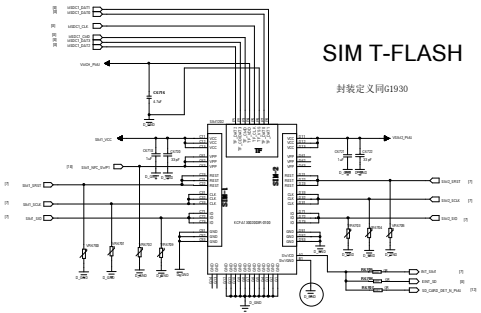


FLASH LED



SIM T-FLASH

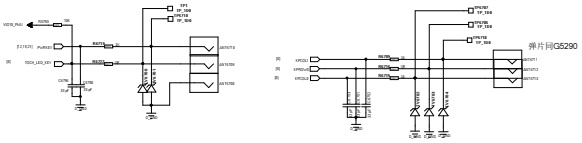
封装定义同G1930



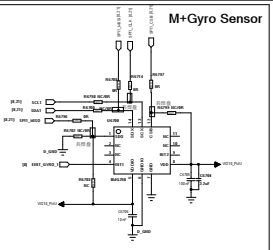
SIDE KEY

Volume Up ： KPROW0+KPCOL1

Volume Down： KPROW0 + KPCOL0

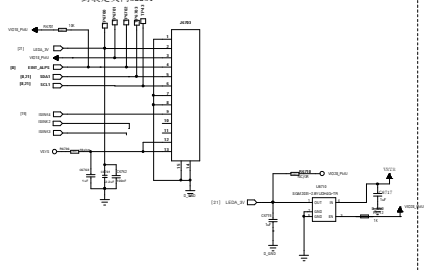


M+Gyro Sensor



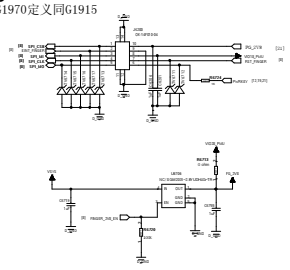
ALS & PS Sensor

封装定义同G2231

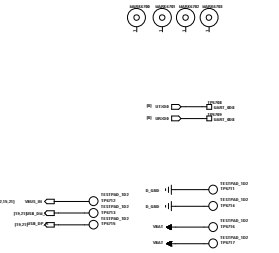


Finger Sensor

封装同G1970定义同G1915



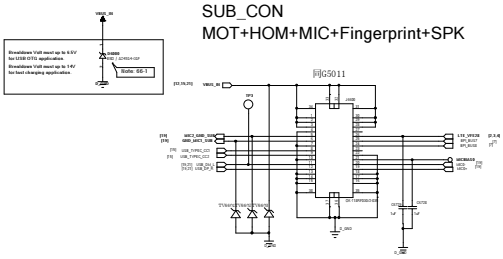
LOG



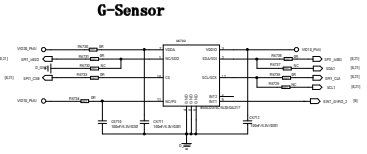
SUB_CON

MOT+HOM+MIC+Fingerprint+SPK

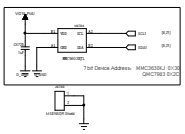
同G5011



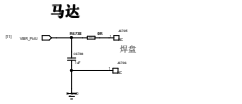
G-Sensor



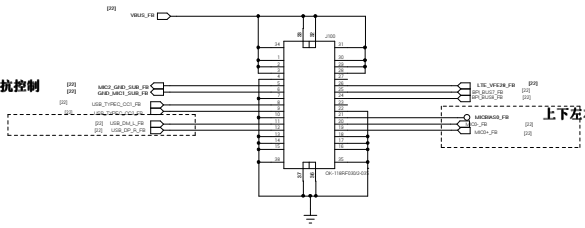
COMPASS



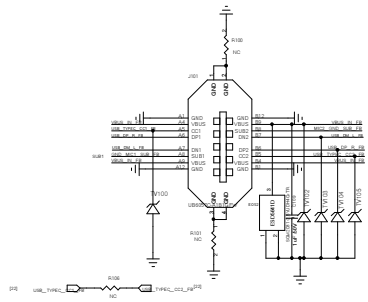
马达



这两根要做阻抗控制

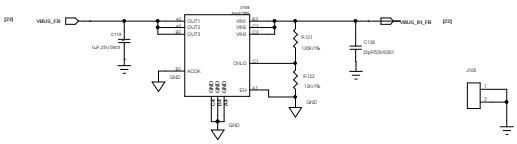


上下左右不包地，避开电源线

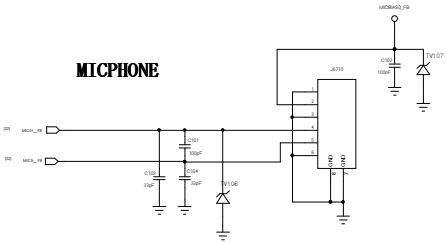


下主地　表层地

OVP



MICPHONE



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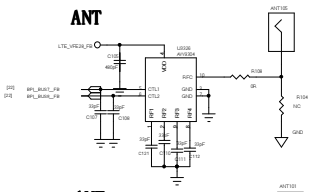

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