Wireless RS-485

Theory of Operation

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Ref 1: Wireless-485 Rev C Design Package

1 Introduction

This document attempts to capture the electrical operation of the Wireless-485 product at a high level.

2 Functionality: Cable Replacement

The Wireless-485 product acts as an RS-485 cable replacement. Its initial application is to replace the cable between an outdoor swimming pool controller and an indoor keypad for controlling pool and pool accessory functionality. But because of its transparent operating mode, it can be used in any application that can benefit from replacing an RS-485 cable connection with a wireless link.

A block diagram of the Wireless-485 design is included in Figure 1. This block diagram is appropriate for both sides of the link. The block diagram indicates the major ICs being used in the design as well as the oscillators being used. For generating RF frequencies, the CC430F5147 contains an internal VCO and PLL that phase locks the generated RF carrier to the 26MHz input reference frequency. This block diagram captures the Wireless-485 design as it is currently being built in production and does not include any population options that are not being utilized.

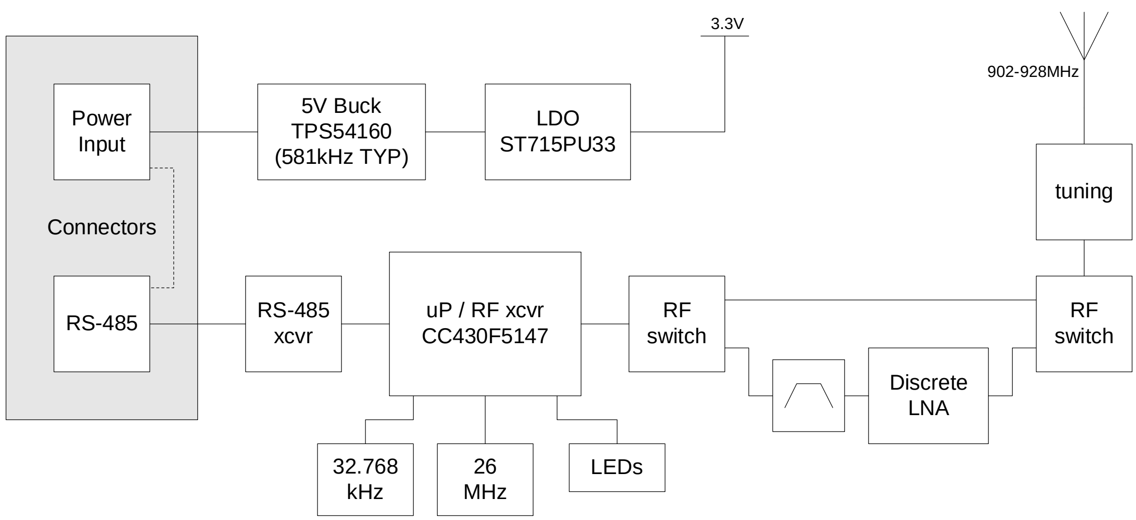

Figure 1 Electronics Block Diagram

The wireless link used for the cable replacement functions operates in the 902-928MHz ISM band. It employs frequency hopping to comply with FCC Part 15.247. Power output is less than 20mW, but excellent range is achieved with a very sensitive receiver with very narrow selectivity. Channel selectivity filters are set to a bandwidth of 105.6kHz, and additional bandpass filtering is employed to provide additional out-of-band rejection. Over the air data rate is 38kHz, and narrowband FM modulation is used.

In compliance with FCC Part 15.247, 50 hopping channels are utilized. Frequency allocation for each logical channel is shown in Table 1. Note that the system only uses even logical channel numbers in the range of 4 – 102 inclusive. Logical channel numbers are based on channel spacing of 249.939kHz, and the system's actual channel spacing is 499.878kHz. Physical channels start at 902.9962MHz and are evenly spaced at 499.878kHz up to the last physical frequency of 927.4902MHz.

Channel #	Frequency (MHz)	Channel #	Frequency (MHz)	Channel #	Frequency (MHz)	Channel #	Frequency (MHz)
4	902.9962	30	909.494614	54	915.49315	80	921.991564
6	903.496078	32	909.994492	56	915.993028	82	922.491442
8	903.995956	34	910.49437	58	916.492906	84	922.99132
10	904.495834	36	910.994248	60	916.992784	86	923.491198
12	904.995712	38	911.494126	62	917.492662	88	923.991076
14	905.49559	40	911.994004	64	917.99254	90	924.490954
16	905.995468	42	912.493882	66	918.492418	92	924.990832
18	906.495346	44	912.99376	68	918.992296	94	925.49071
20	906.995224	46	913.493638	70	919.492174	96	925.990588
22	907.495102	48	913.993516	72	919.992052	98	926.490466
24	907.99498	50	914.493394	74	920.49193	100	926.990344
26	908.494858	52	914.993272	76	920.991808	102	927.490222
28	908.994736			78	921.491686		

Table 1 Frequency Allocation Table

The system dwells at 400mS per channel, regardless of data that is transmitted over the wireless link. During periods of heavy transmission, data will be transmitted on a channel for 400mS until the next channel hop, ensuring equal distribution across channels. During light data transmission, the system will still hop at a 400mS interval, with background link packets as well as payload data packets being transmitted on the hop channel that is assigned at the time of packet transmission. This hop pattern is followed regardless of the presence of an interfering signal.

If there is not enough time to transmit an entire packet before it is time to hop to the next channel, transmission of the packet is held off until after the hop and the frequency has been changed and has settled to the new channel.

The hop sequence is pseudo-random and distributed across the full 50 channels. An example of this hop sequence, expressed in logical channel numbers, follows:

66, 20, 52, 94, 24, 80, 4, 58, 92, 36,
72, 16, 50, 98, 32, 74, 8, 60, 86, 42,
68, 22, 44, 100, 26, 76, 12, 54, 90, 38,
64, 18, 46, 102, 30, 78, 6, 62, 84, 40,
70, 14, 48, 96, 28, 82, 10, 56, 88, 34

Because of the frequency hopping scheme, the point to point wireless link employs a master (the outdoor transceiver in the initial application) and a slave (the indoor transceiver in the initial application). The master controls the hop sequence and link establishment. However, from the communications standpoint, both sides are equal peers, as there is not a concept of higher priority packets from one side or the other.

Once linked, any data packet that appears on the RS-485 interface on one side is transmitted wirelessly to the other side, and is subsequently output on the RS-485 interface. Because the system is half-duplex, collisions are possible. But unlike RS-485 collisions, the wireless collisions are not detectable; packets simply do not make it all the way across. The wireless link does not support acknowledgements or retries, so packet confirmation and retries should be employed at a higher level.

3 Establishing a Link

Because of the frequency hopping, units must be linked before data can be sent across. Linked simply refers to two units with matching linking identification numbers (LinkIDs) that are hopping synchronously and are ready to send data back and forth. To allow for coexistence without sharing data, each pair of units includes a LinkID with every packet sent.

When two units are first powered up and are not linked, the master (the outdoor transceiver) will begin following its normal pseudo-random hop sequence at the proper interval, listening for link request packets. The slave will search for the master by sending link request packets and listening for a response. While doing this, the slave hops through the hop frequencies at an accelerated rate, which allows its hop pattern to overlap with the master's after some amount of time. Once they have landed on the same channel, the slave will use responses from the master to adjust its internal DPLL to lock onto the timing of the master. Once the DPLL locks, the slave will complete the link request, and the two units are defined as being linked as they continue to hop through frequencies together.

As the slave determines it needs to, it will send additional packets and wait for a response from the master to help refine and maintain DPLL lock. If it ever determines that DPLL lock has been lost, it will again hop through the hop pattern at an accelerated rate and attempt to relink to the master.

While it is first trying to establish link, the slave will alternate transmitting packets at high and low power levels. When responses start coming in, the slave will track how many responses were received in response to both power levels being used. Once the DPLL is locked and the link is established, the slave sets its power level to the one that received the most responses. The slave then indicates the power level being used to the master, and the master adjusts its power level to match that of the slave.

Once the link is established, the slave is responsible for the transmit power level of both sides. Based on received signal strength (RSSI), the slave will determine the optimum power level, share this with the master, and the master will set its power level to match that of the slave.

4 Antennas

The Wireless-485 units employ internal PC trace antennas for the wireless link. These full-band antennas achieve good efficiencies without the use of exotic materials. The gain of the PCB antenna is approximately 1 dBi. No dynamic tuning of the antennas is needed.

There are only provisions for the on-board antenna; there is no connector and no routing path for any external antennas.

5 Architecture

The Wireless-485 product is centered on the CC430 processor / sub GHz transceiver. The processor in the CC430 maintains the wireless link with hopping and power control, monitors the RS-485 interface for packets to send, and manages all communications across the link and out the RS-485 interface. The design does not employ a power amplifier, but it does employ a discrete LNA with band filtering.

The RS-485 interface is through a transceiver IC. A power management section takes incoming voltage and converts to the on-board voltages needed for all subsystems to operate properly.