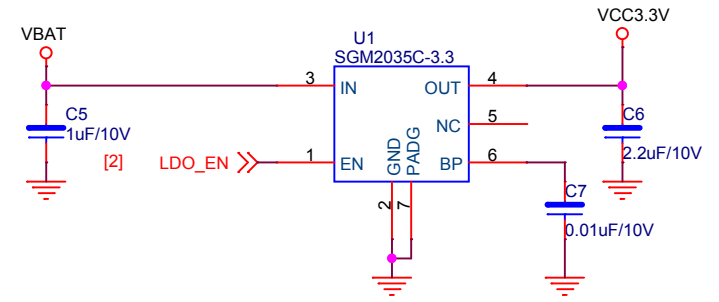
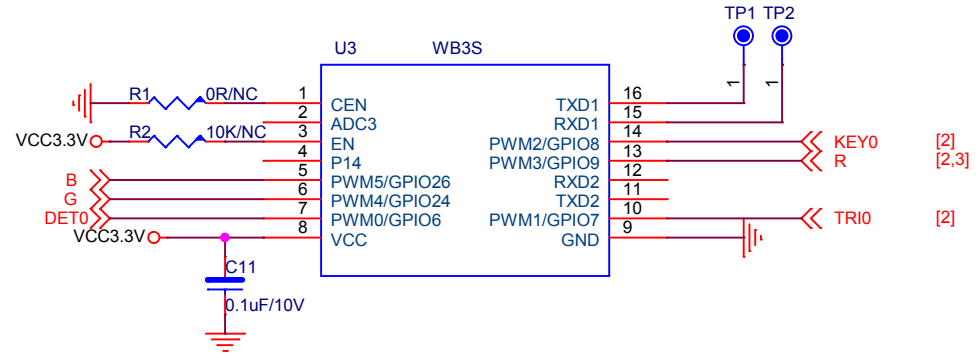
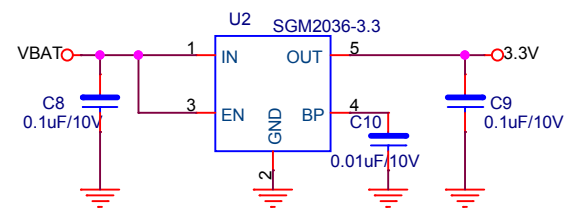


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[2,3]  
[2,3]



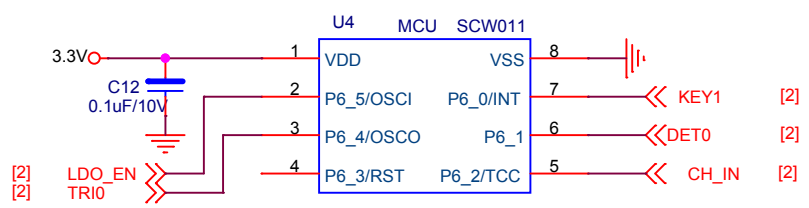
[2]



[2,3]  
[2,3]  
[2]

[2]  
[2,3]

[2]

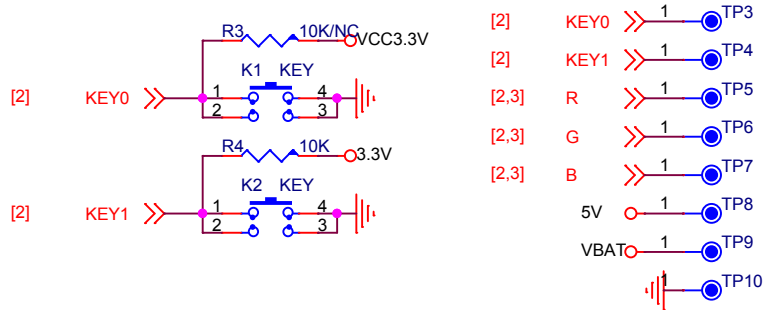


[2]  
[2]

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[2]

[2]

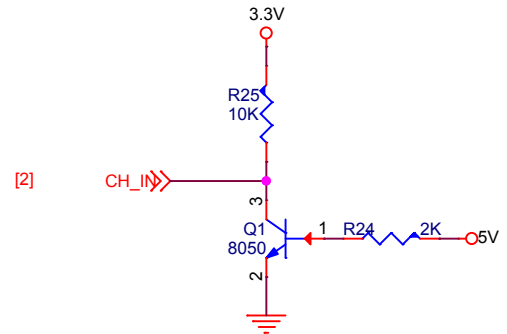
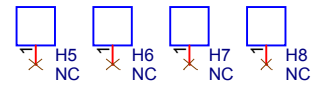
[2,3]

[2,3]

[2,3]

[2,3]

### TP & MARK



[2]

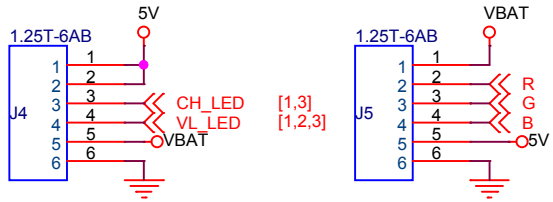
D

C

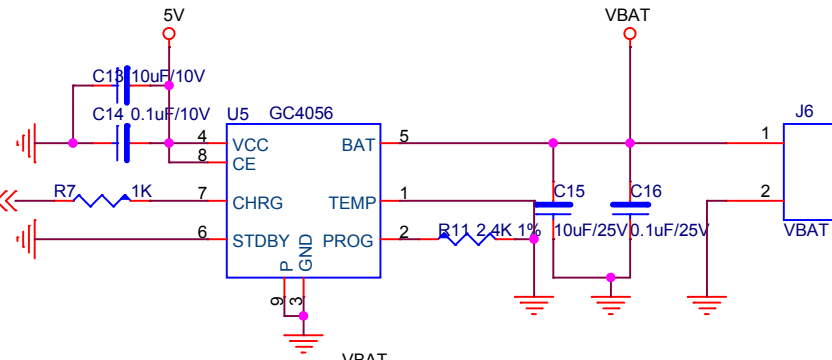
B

A

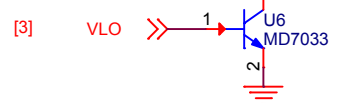
D



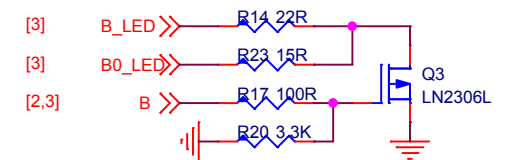
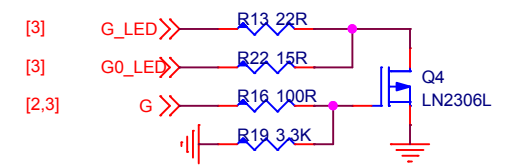
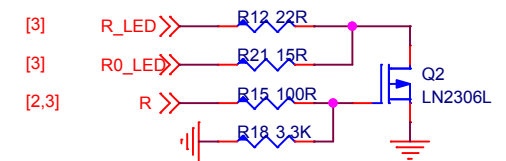
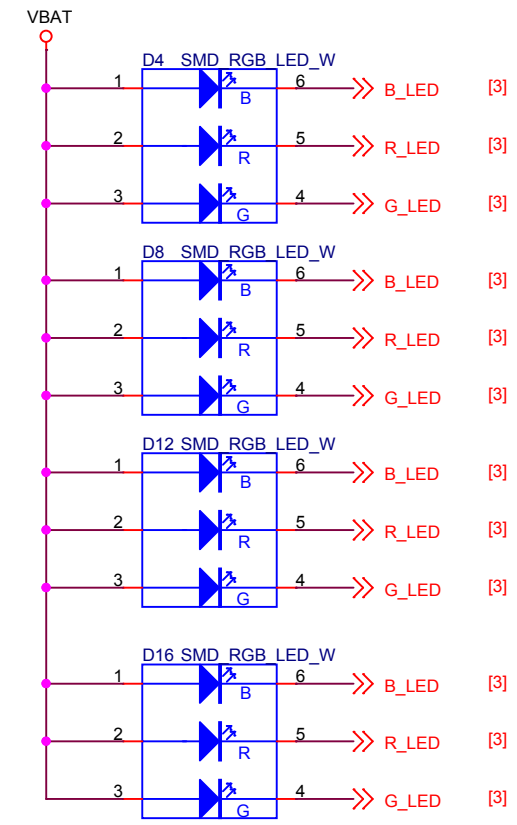
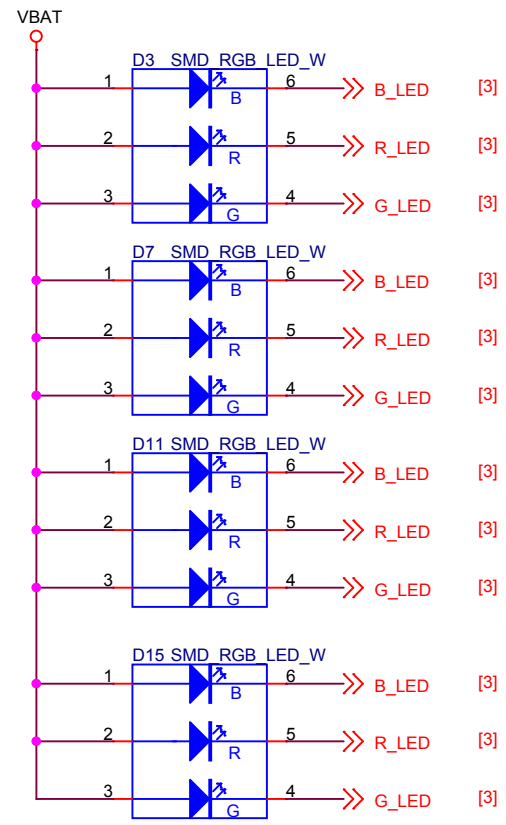
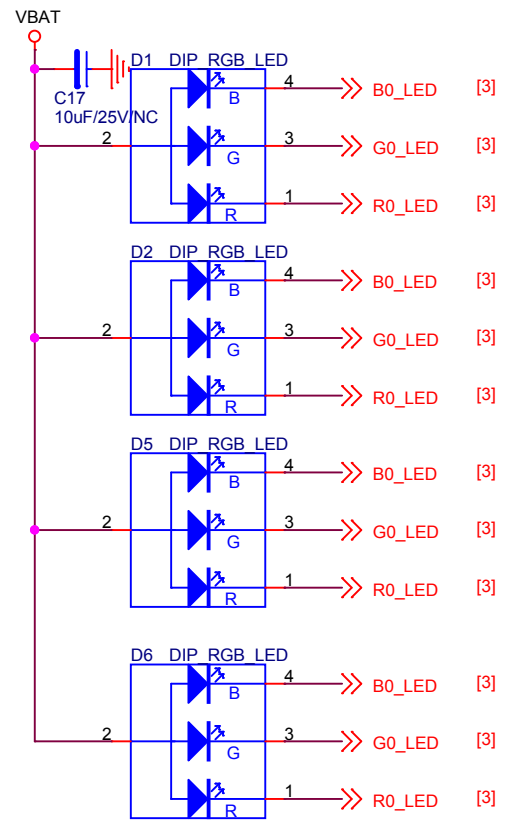
[2,3] CH\_LED  
[2,3] CH\_LED  
[2,3] CH\_LED



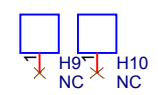
[3] VLO >> R5 1K << VL\_LED [1,2,3]  
[3] ADC0 >> R6 0R << VBAT << R9 NC << ADC0 [3]



C

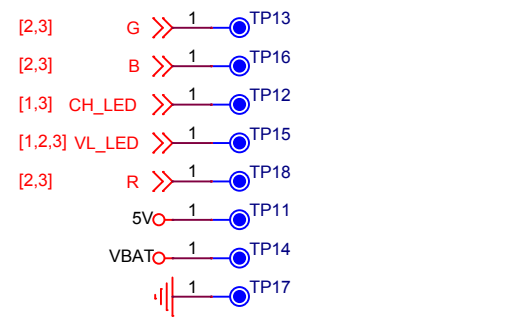
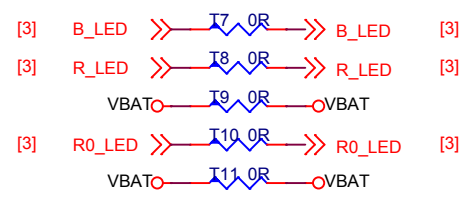
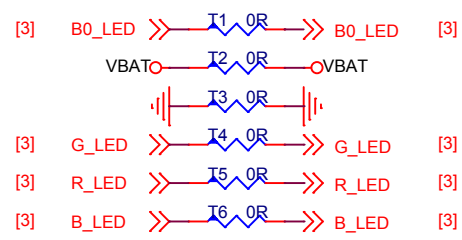


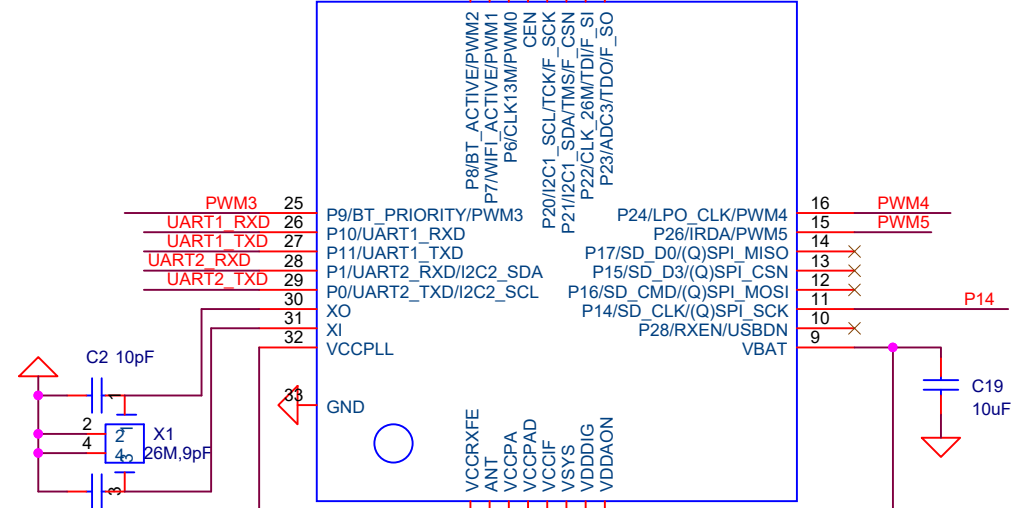
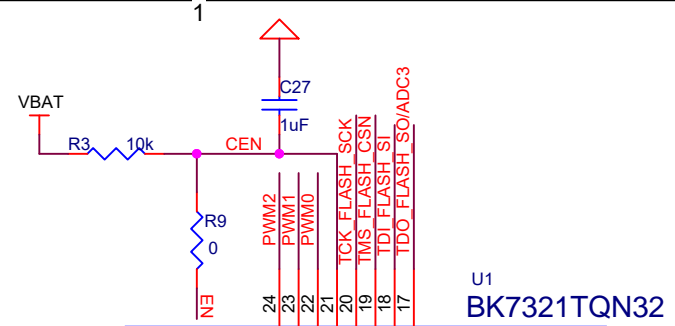
B



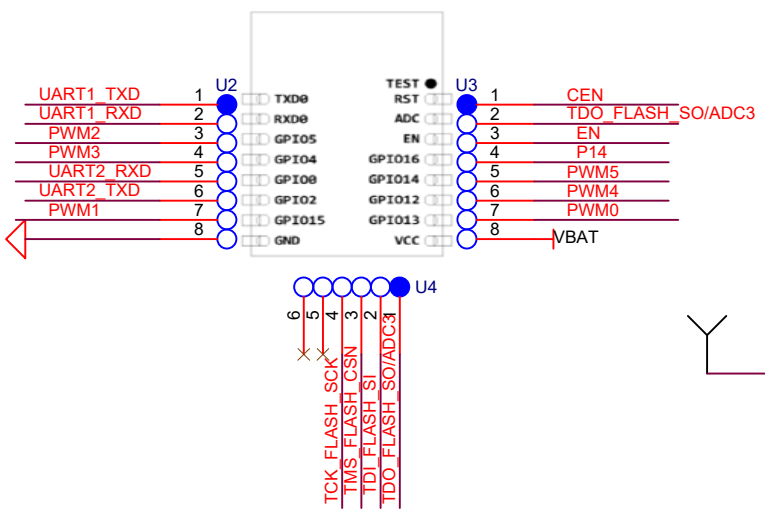
# TP & MARK

A

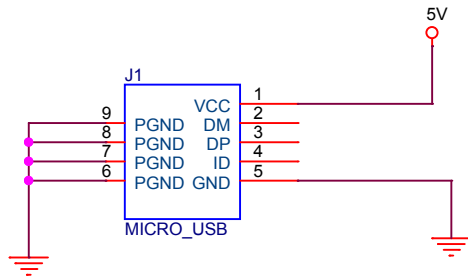




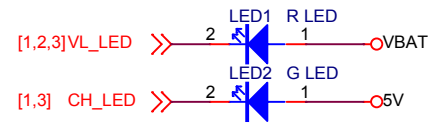
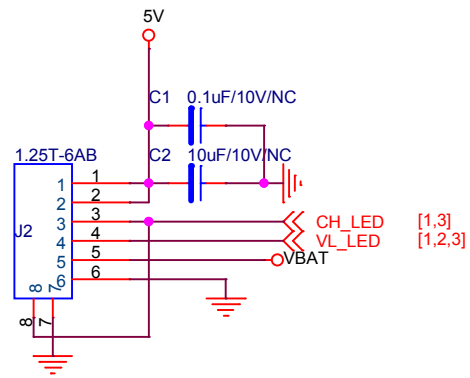
**BOTTOM VIEW**



D

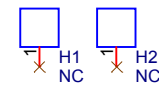


C



B

# TP & MARK



A