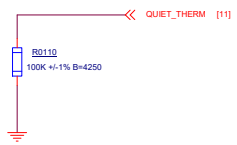
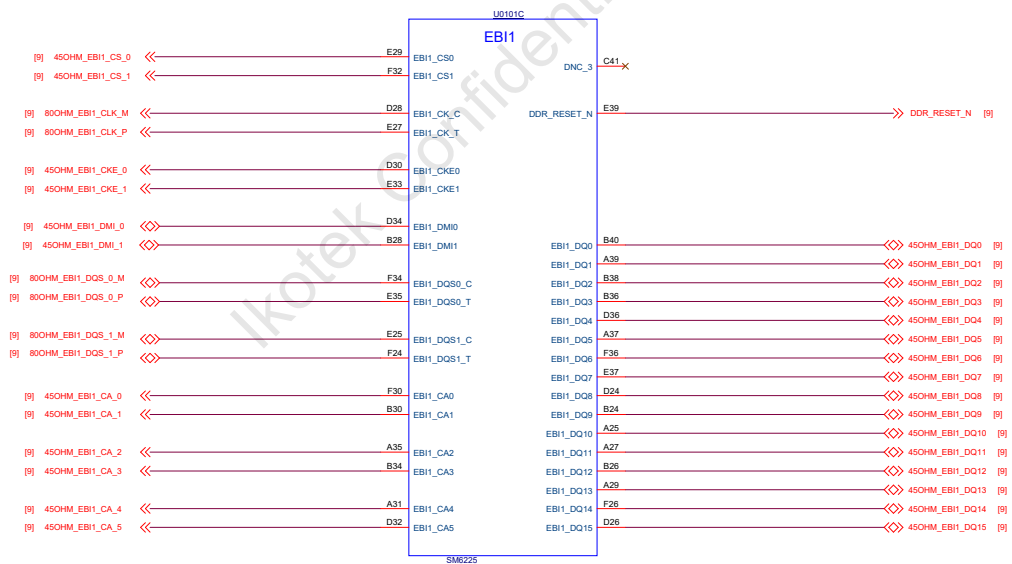
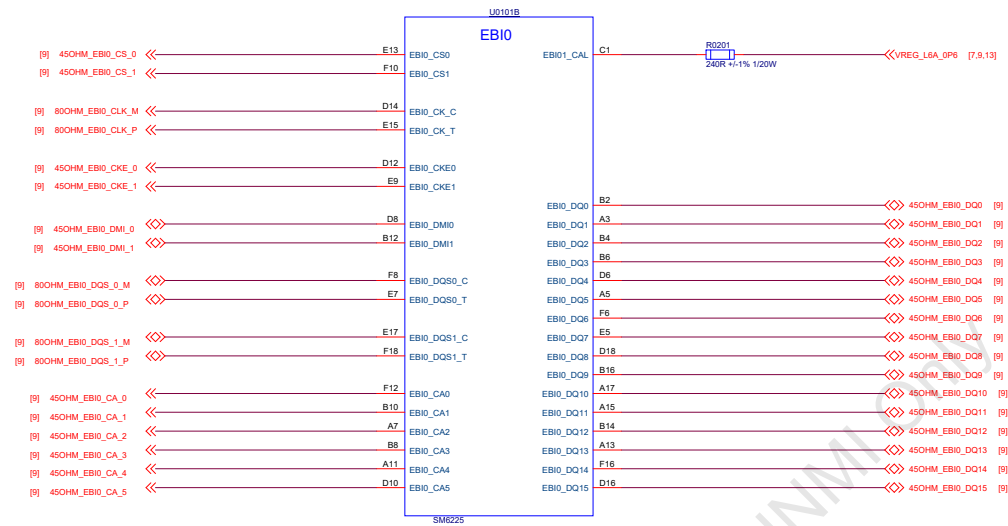


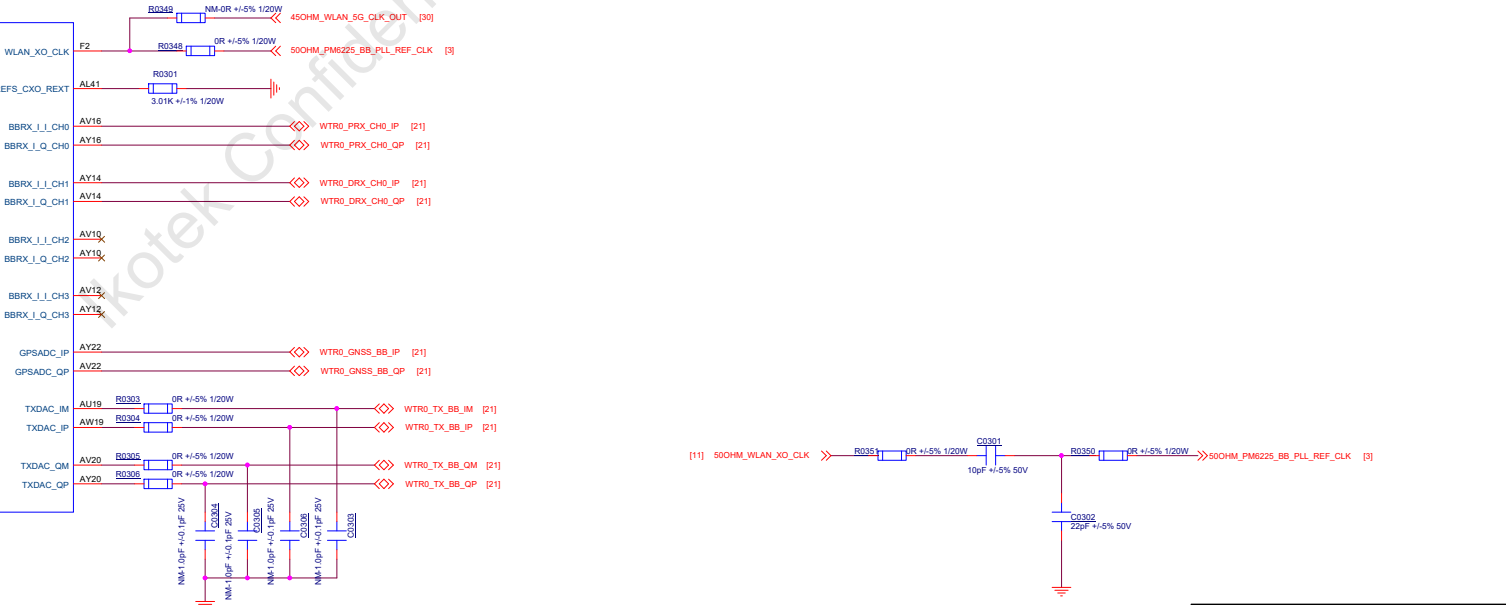
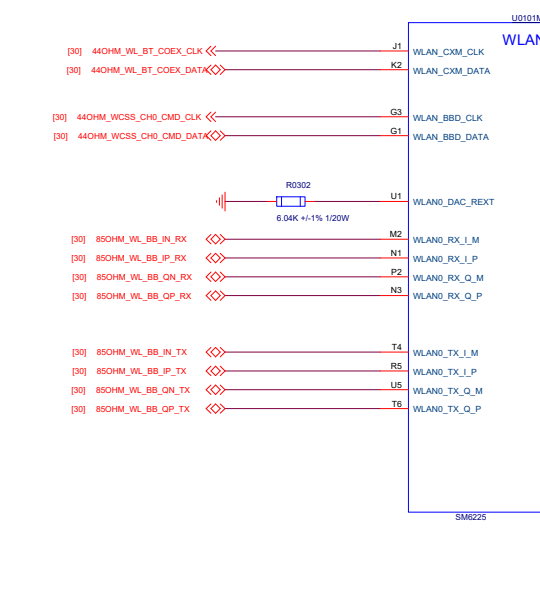
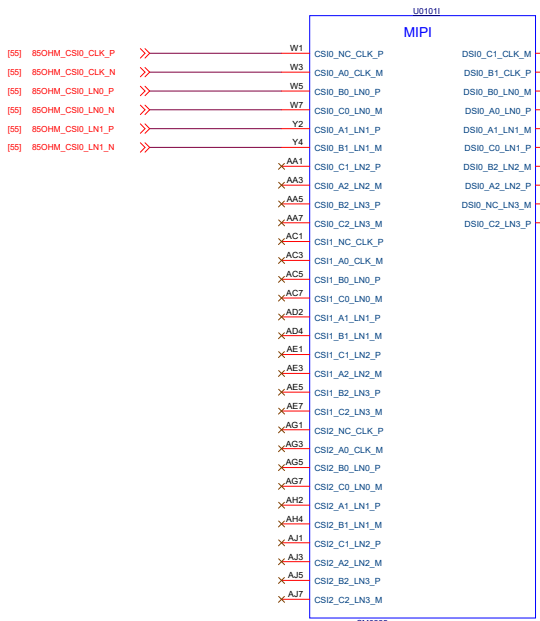
Place the resistors connected to the REXT pins near to SM and route away from noisy signals.

- 1) Place near the SM
- 2) Route the SPMI signals in Daisy Chain/Star routing from SM to the PMICS to avoid stubs.



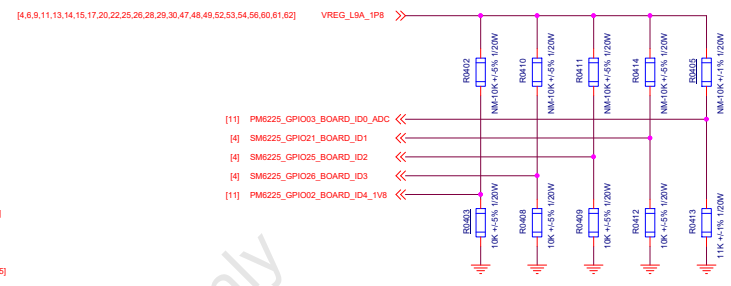
Organization			
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GPIO		GPIO	
[00] SM6225_GPIO0_CTS_MISO_1V8	AH36	GPIO_0	AT38
[00] SM6225_GPIO1_RTS_MOSI_1V8	AH38	GPIO_1	AU39
[00.61] SM6225_GPIO2_TX_CLK_1V8	AG39	GPIO_2	AU37
[00.61] SM6225_GPIO3_RX_CS0_1V8	AH40	GPIO_3	AT36
[14.15,20.50,52.54,59.60.61] SM6225_GPIO4_APPS_I2C_SDA_1V8	AM40	GPIO_4	AL33
[14.15,20.50,52.54,59.60.61] SM6225_GPIO5_APPS_I2C_SCL_1V8	AL39	GPIO_5	AL35
[20.56,59.61] SM6225_GPIO6_TP_UC_SDA_1V8	AM36	GPIO_6	AN35
[20.56,59.61] SM6225_GPIO7_TP_I2C_SCL_1V8	AM38	GPIO_7	BB40
[30] SM6225_GPIO8_WCN_UART_CTS	H4	GPIO_8	BC39
[30] SM6225_GPIO8_WCN_UART_RTS	H6	GPIO_9	BA39
[30] SM6225_GPIO10_WCN_UART_TXD	J7	GPIO_10	BA41
[30] SM6225_GPIO11_WCN_UART_RXD	J5	GPIO_11	AY40
[54.62] SM6225_GPIO12_DEBUG_UART_TX_1V8	AN39	GPIO_12	AY38
[54.62] SM6225_GPIO13_DEBUG_UART_RX_1V8	AN37	GPIO_13	AY36
[56] SM6225_GPIO14_FP_MISO_1V8	AJ41	GPIO_14	AW35
[56] SM6225_GPIO15_FP_MOSI_1V8	AK40	GPIO_15	AM34
[56] SM6225_GPIO16_FP_CLK_1V8	AK38	GPIO_16	AR41
[56] SM6225_GPIO17_FP_CSN_1V8	AJ39	GPIO_17	AH34
[60] SM6225_GPIO18_HALOW_INT_1V8	M6	GPIO_18	AH40
[61] SM6225_GPIO19_SE_INT_1V8	AW3	GPIO_19	AV38
[58] SM6225_GPIO20_CAM_MCLK0	L5	GPIO_20	AV36
[4] SM6225_GPIO21_BOARD_ID1	L7	GPIO_21	AJ37
[20.56] SM6225_GPIO22_CCI_I2C_SDA0	BB8	GPIO_22	D2
[20.56] SM6225_GPIO23_CCI_I2C_SCL0	BC7	GPIO_23	BC3
[59] SM6225_GPIO24_LCD_MIPI_ID1_V18	BA3	GPIO_24	AR39
[4] SM6225_GPIO25_BOARD_ID2	BA1	GPIO_25	E1
[4] SM6225_GPIO26_BOARD_ID3	AY2	GPIO_26	E3
[54] SM6225_GPIO27_RJ12_GPIO2_1V8	K4	GPIO_27	AU35
[52] SM6225_GPIO28_EDP_DET_V18	K6	GPIO_28	AW39
[15,20,48.61] SM6225_GPIO29_I2C_SDA_1V8	BC5	GPIO_29	AR35
[15,20,48.61] SM6225_GPIO30_I2C_SCL_1V8	BB8	GPIO_30	AP36
[01] SM6225_GPIO31_LCD_BL_EN_1V8	AV6	GPIO_31	AP40
[60] SM6225_GPIO32_BLSPE_GPIO2_1V8	AV4	GPIO_32	AP38
[61] SM6225_GPIO33_SE_ALARM_1V8	AV2	GPIO_33	BA31
[20] SM6225_GPIO34_SE_3V3_EN_1V8	AU7	GPIO_34	BC33
[52] SM6225_GPIO35_EDP_RESET_N	AW7	GPIO_35	AY39
[14] SM6225_GPIO36_AW9523B_INT_N	AW5	GPIO_36	BB30
[24] SM6225_GRPFC1_B23/25/39	AU5	GPIO_37	BA33
[24] SM6225_GRPFC1_B23/25/39	AU3	GPIO_38	BB32
[23] SM6225_GRPFC2_B12/13/14/17/71_TRX	AU1	GPIO_39	BB34
[23] SM6225_GRPFC3_B12/13/14/17/71_TRX	AT9	GPIO_40	BC35
[23] SM6225_GRPFC4_PRX_BB20/28	AR5	GPIO_41	BC31
[23] SM6225_GRPFC5_PRX_BB20/28	AT6	GPIO_42	BA29
[23] SM6225_GRPFC6_TRX_B12/13/14/17	AP2	GPIO_43	AY28
[23] SM6225_GRPFC7_TRX_BB20	BB2	GPIO_44	BA35
[24] SM6225_GRPFC8_PRX_B14/66	AY4	GPIO_45	BA37
[22] SM6225_GRPFC9_PRX_B30/38/40/41	BA7	GPIO_46	BB36
[28] SM6225_GRPFC10_DRX_B12/13/14/17/71	AT4	GPIO_47	BB38
[26] SM6225_GRPFC11_DRX_BB20/28	AN1	GPIO_48	BA25
[27] SM6225_GRPFC12_DRX_B30/38/40/41	AN3	GPIO_49	AY26
[27] SM6225_GRPFC13_DRX_B25/34/39	AN5	GPIO_50	AW25
[25] SM6225_GRPFC14_PDDET	AL5	GPIO_51	BB26
[22] SM6225_GRPFC15_TDD_PRX_LNA_EN	AL3	GPIO_52	BA27
[4,6,9,11,13,14,15,17,20,22,25,26,28,29,30,47,48,49,52,53,54,56,60,61,62] VREG_L8A_1P8	AT2	GPIO_53	BB28
[28,29] 500HM_RFFE2_DATA	AR3	GPIO_54	AW27
[28,29] 500HM_RFFE2_CLK	AR7	GPIO_55	AW29
[22,25,28] 500HM_RFFE3_DATA	AP6	GPIO_56	AY30
[22,25,28] 500HM_RFFE3_CLK	AN7	GPIO_57	AW31
[29] 500HM_RFFE4_DATA	AM4	GPIO_58	AV33
[29] 500HM_RFFE4_CLK	AM2	GPIO_59	AY33
[21] 500hm_RFFE5_DATA	AL7	GPIO_60	
[21] 500hm_RFFE5_CLK	AL7	GPIO_61	
[31] SM6225_EXT_GPS_LNA_EN0	AY6	GPIO_62	
[21] 500hm_GSM0_TX_PHASE_D	BA5	GPIO_63	
		GPIO_64	

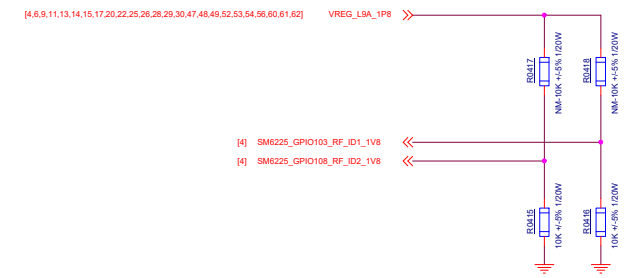
Board ID



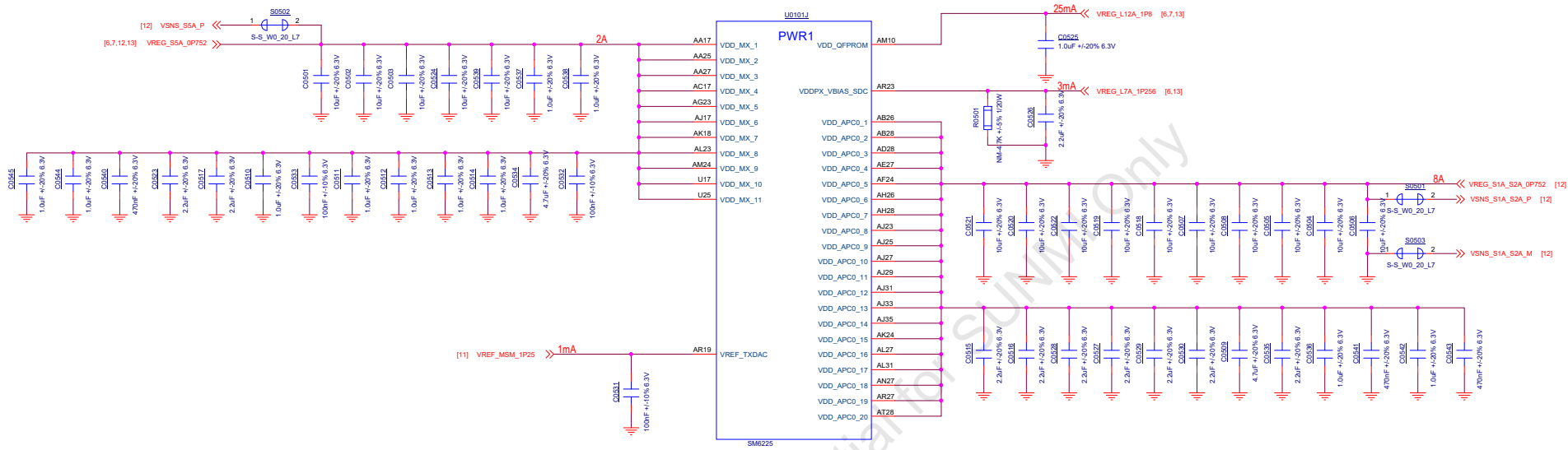
- [11] PM6225_GPIO03_BOARD_ID0_ADC
- [4] SM6225_GPIO21_BOARD_ID1
- [4] SM6225_GPIO25_BOARD_ID2
- [4] SM6225_GPIO26_BOARD_ID3
- [11] PM6225_GPIO02_BOARD_ID4_V18

GPIO	WDOG_DISABLE	BOOT_CONFIG[0]
GPIO_50	FAST_BOOT_SEL_0	BOOT_CONFIG[1]
GPIO_51	FAST_BOOT_SEL_1	BOOT_CONFIG[2]
GPIO_53	FAST_BOOT_SEL_2	BOOT_CONFIG[3]
GPIO_55	FAST_BOOT_SEL_3	BOOT_CONFIG[4]

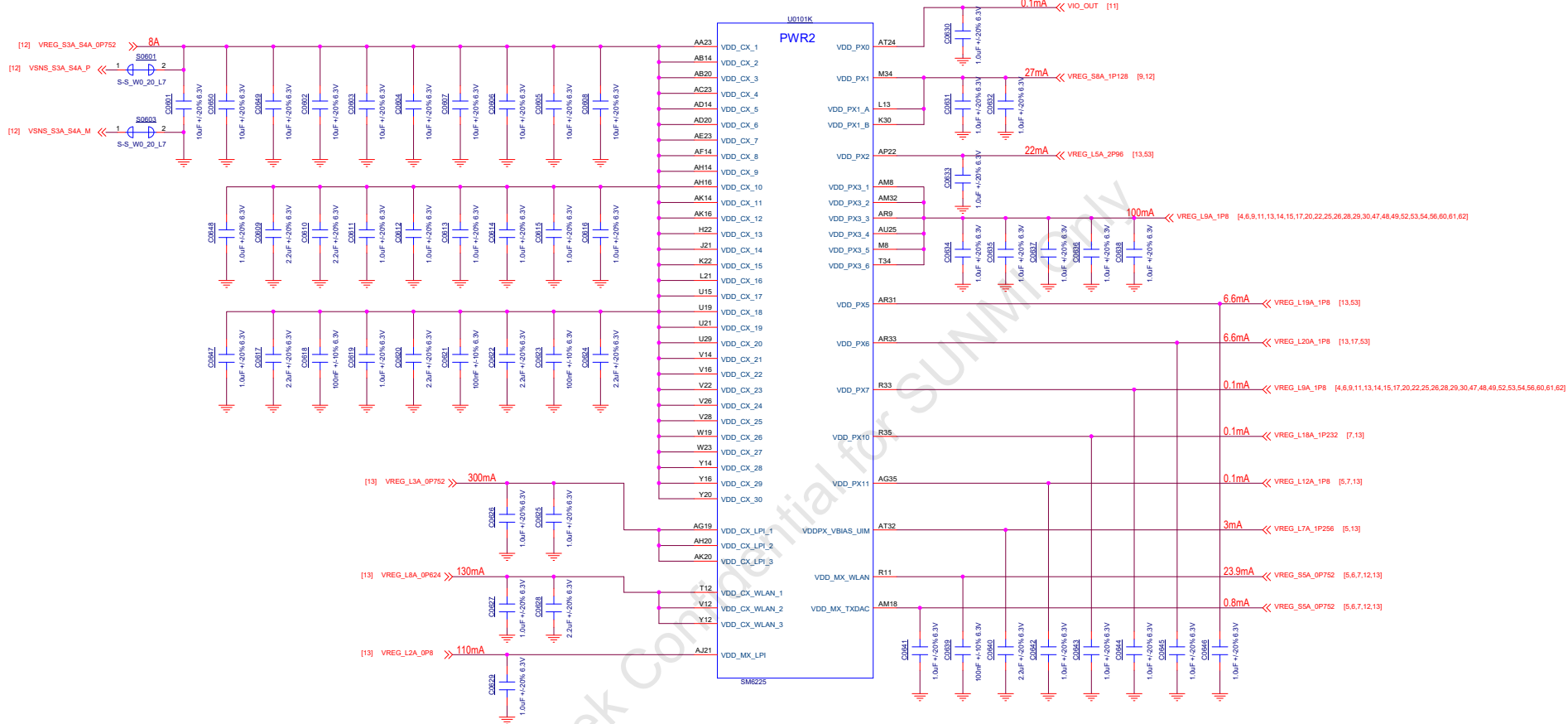
FAST_BOOT[3:0]	BOOT Sequence
0b0000	uBMC -> SD -> eBL (eBL path - USB only)
0b0001	SD -> uBMC -> eBL (eBL path - USB only)
0b0010	SD -> eBL (eBL path - USB only)
0b0011	USB -> eBL
0b0100	UFS -> SD -> eBL (eBL path - USB only)
0b0101	SD -> UFS -> eBL (eBL path - USB only)
0b0110	UFS -> eBL (eBL path - USB only)
0b0111	uBMC -> SD -> eBL (eBL path - USB only)
0b1000	uBMC -> eBL (eBL path - USB only)



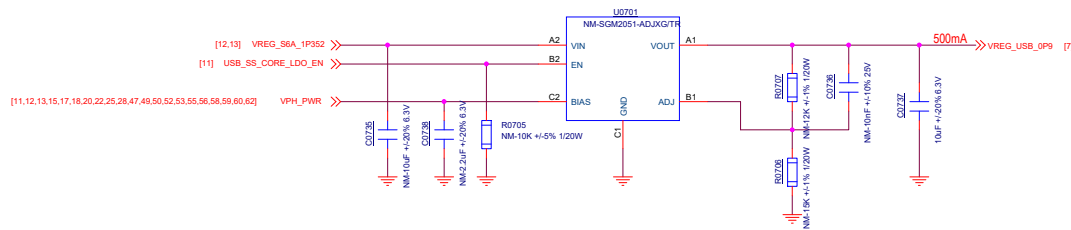
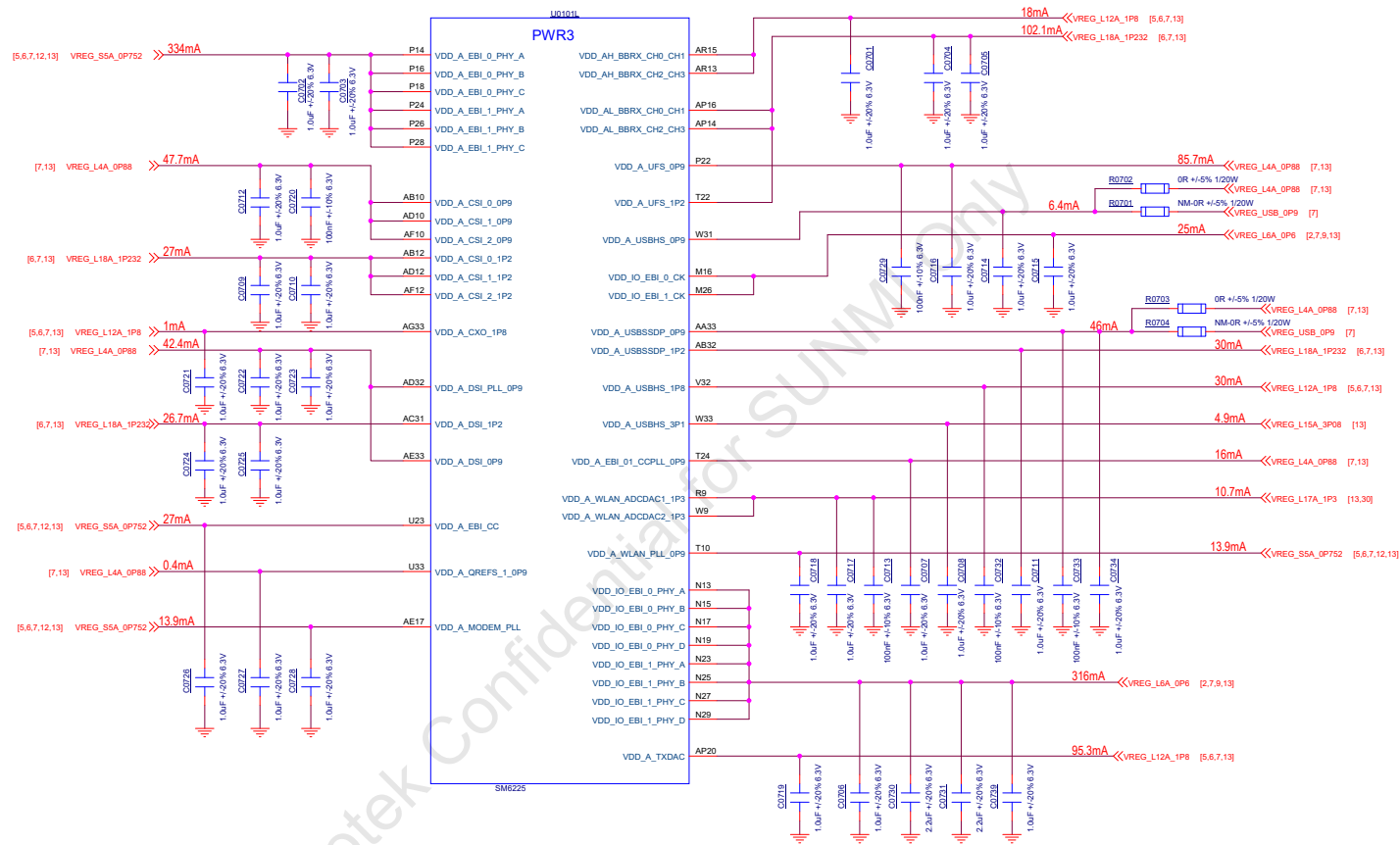
- [4] SM6225_GPIO103_RF_ID1_V18
- [4] SM6225_GPIO108_RF_ID2_V18



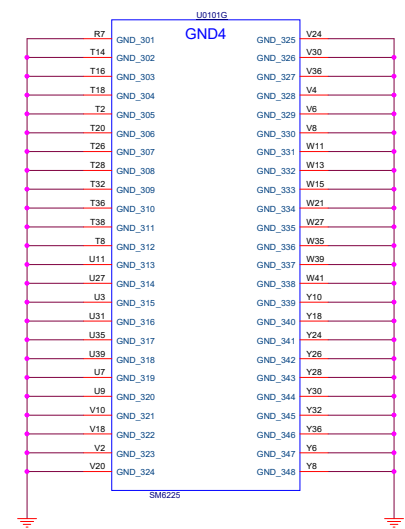
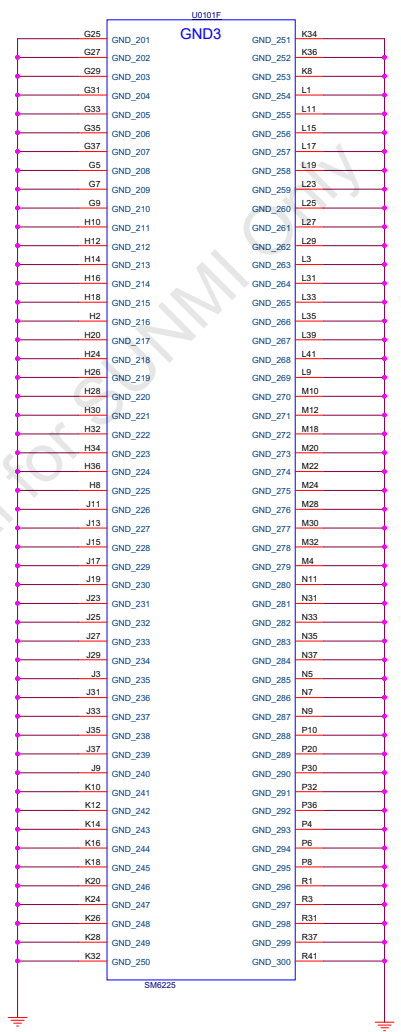
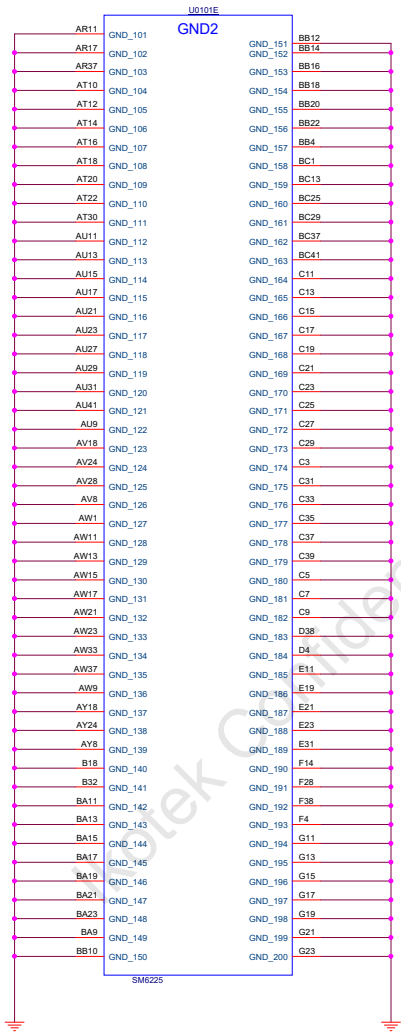
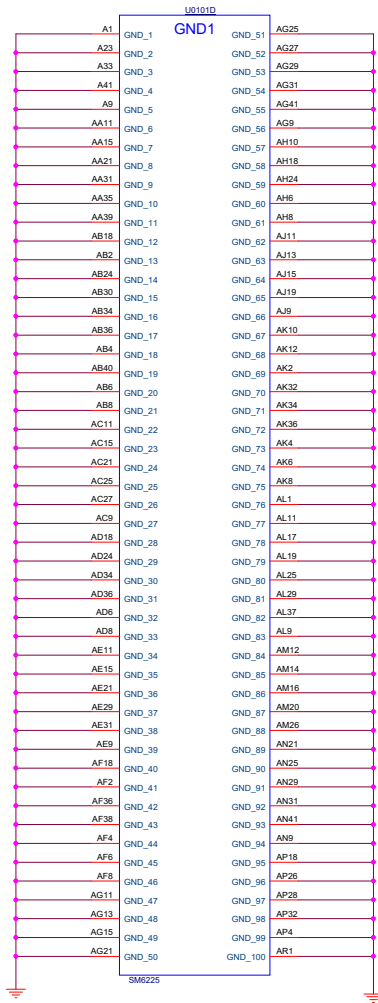
Organization	Quectel ODM Solutions		
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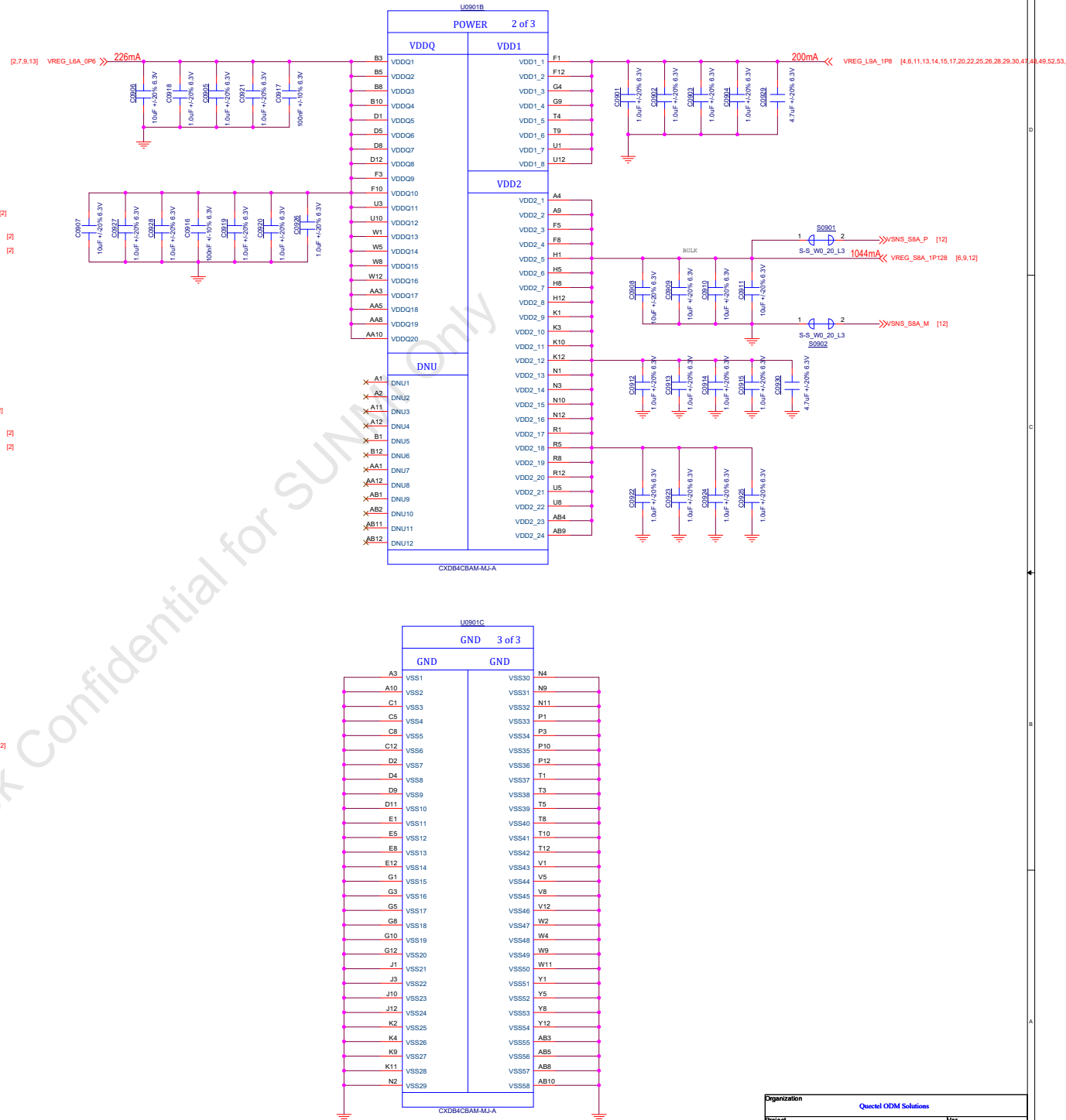
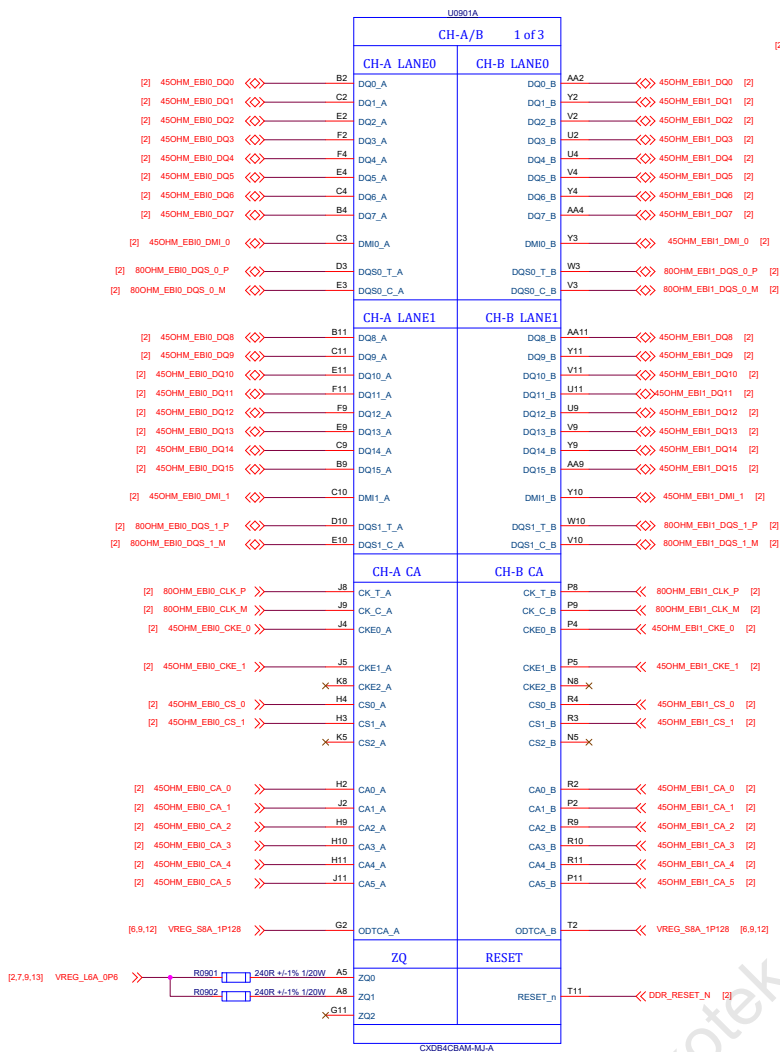


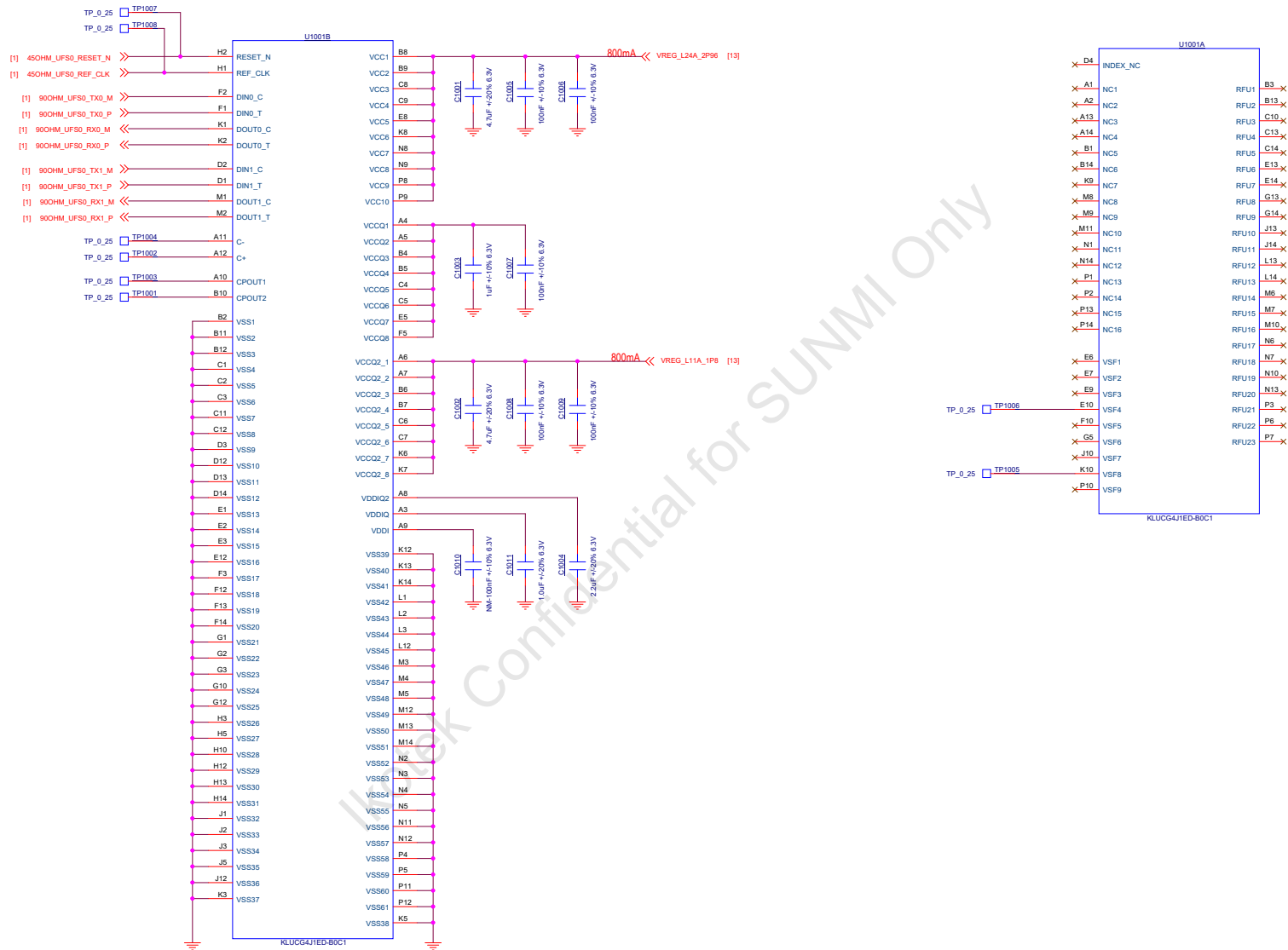
Organization	Quectel ODM Solutions		
Project	T3-EU	Ver	V1.1
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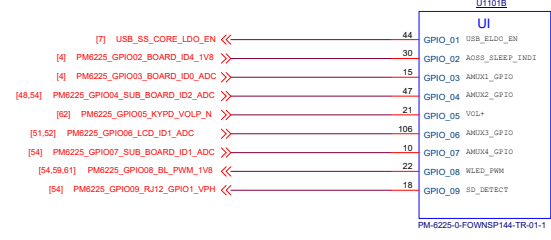
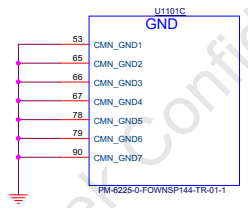
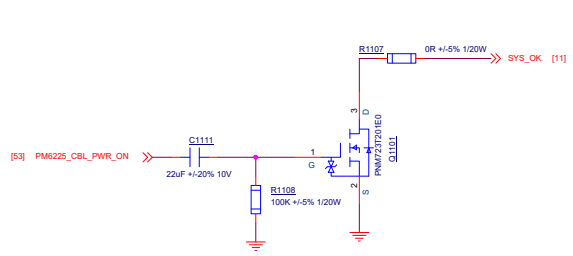
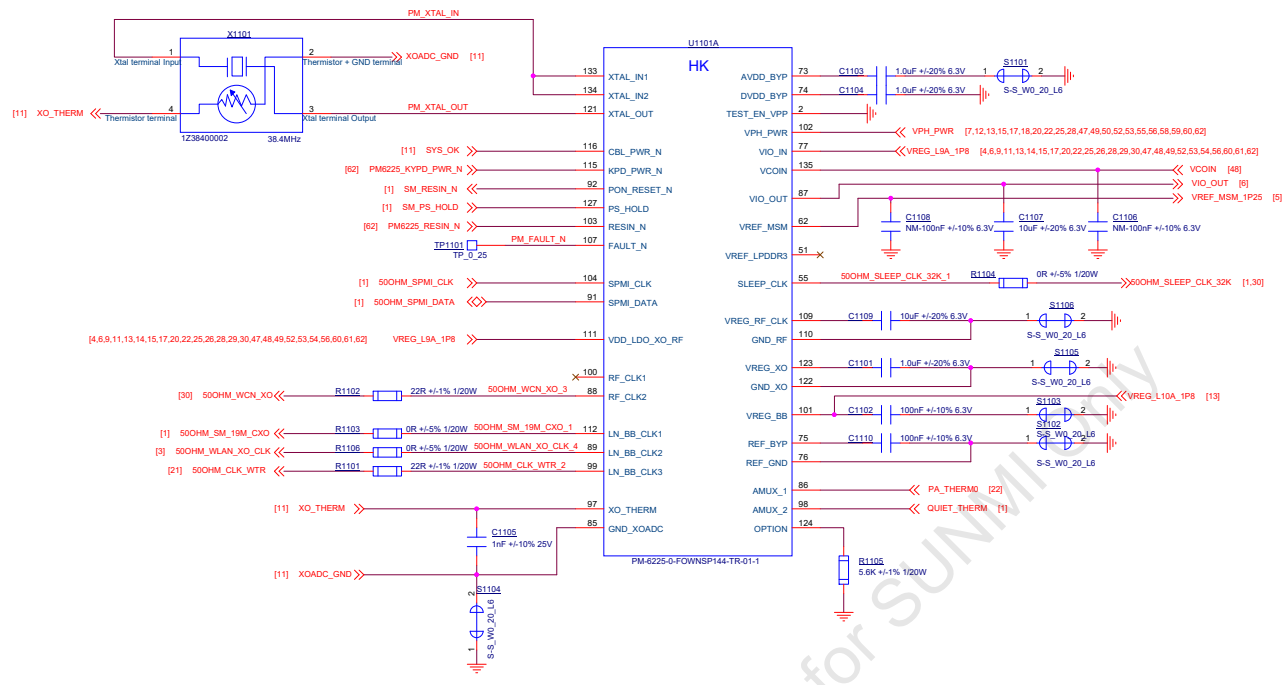
Organization	Quectel ODM Solutions		
Project	T3-EU	Ver	V1.1
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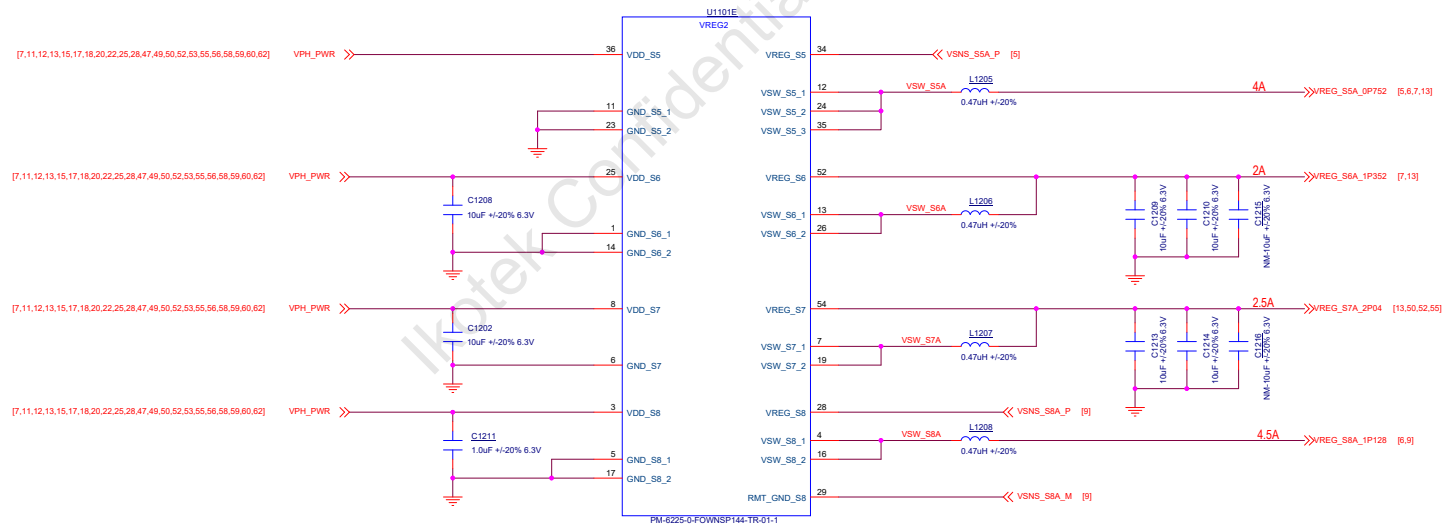
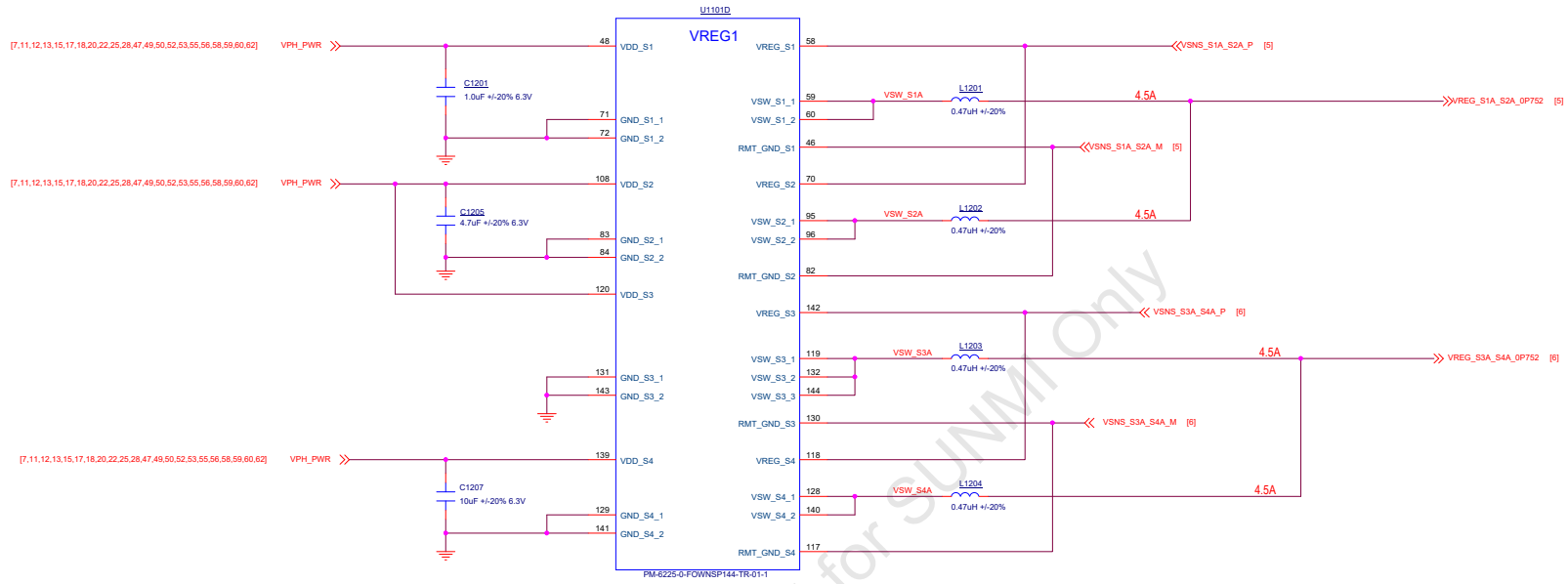




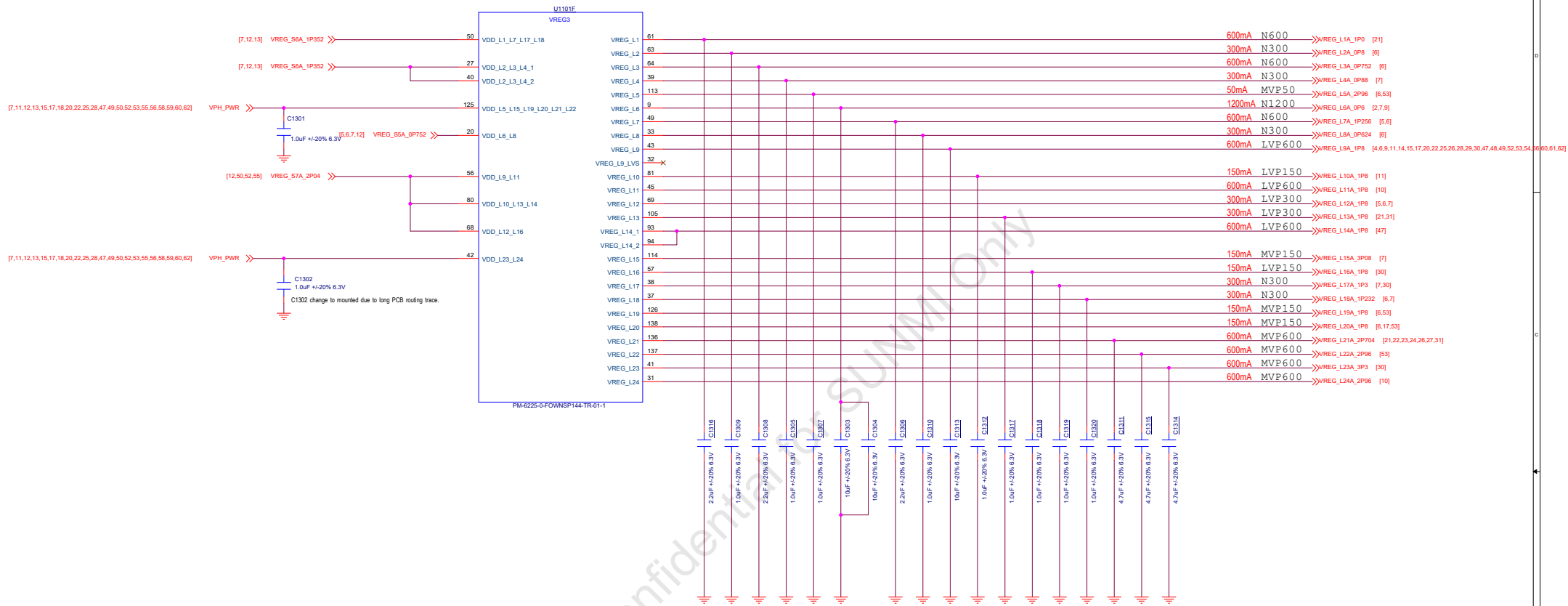


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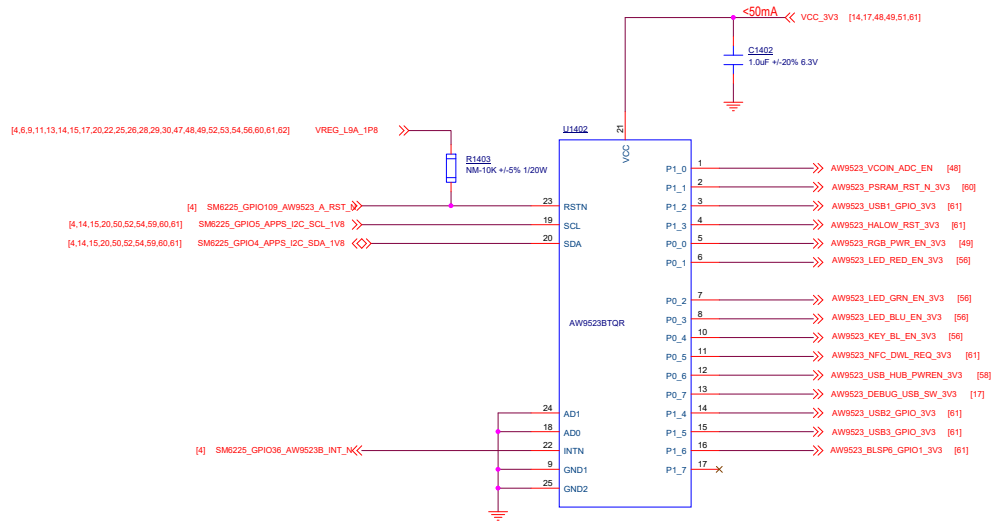
NOTE: Place these caps close to PMIC.
 Prioritize N1200s over N300s for placement.

N1200F(2 x 10uF)
 Min : 20uF , Max : 44uF
 N1200 (1x 4.7uF)
 Min : 4.7uF , Max : 22uF
 N600 (1x 2.2uF)
 N300 (1 X 1uF)
 Min : 1uF , Max : 10uF

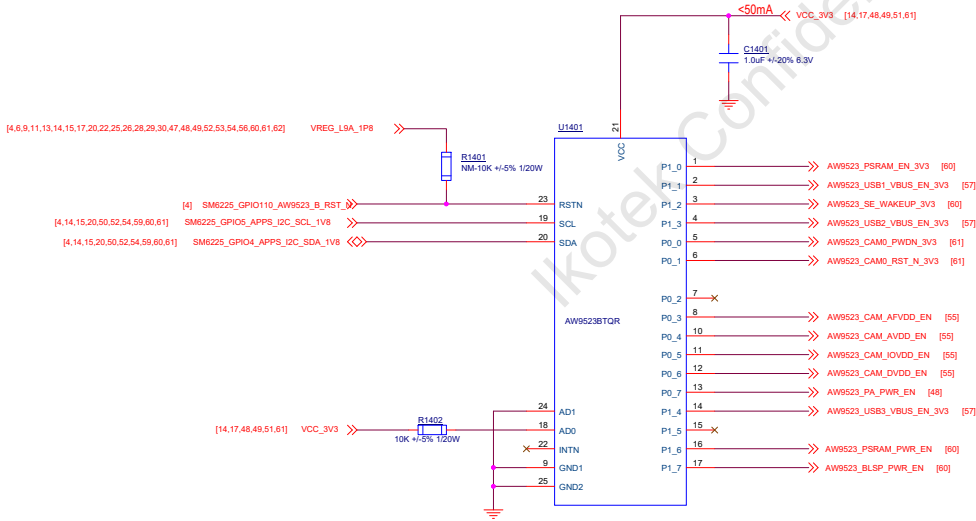
Doesn't have to be close to its pin

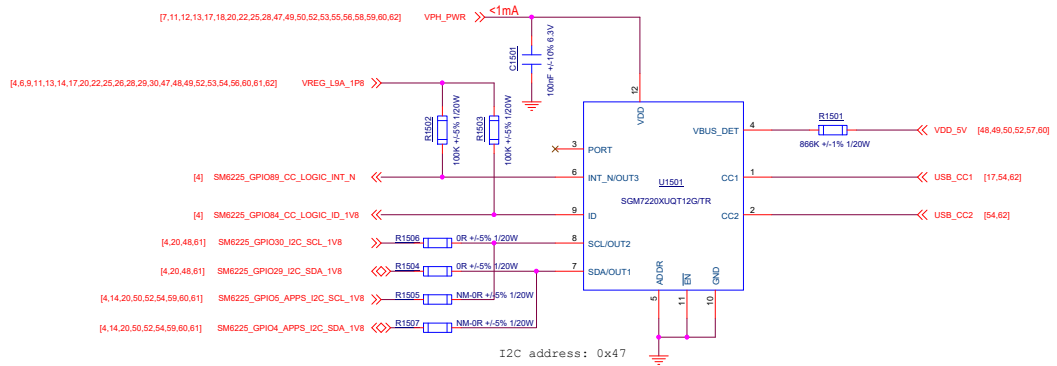
Pseudo-Capless
 MVP150 - Min : 0.47uF , Max : 5uF
 MVP600 - Min : 4.7uF , Max : 23.5uF
 LVP600 - Min : 4.7uF , Max :

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AD1	AD0	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0	P0_7	P0_6	P0_5	P0_4	P0_3	P0_2	P0_1	P0_0
GND	GND	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GND	VBAT	0	0	0	0	1	1	1	1	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
VBAT	GND	1	1	1	1	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	0	0	0	0
VBAT	VBAT	1	1	1	1	1	1	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

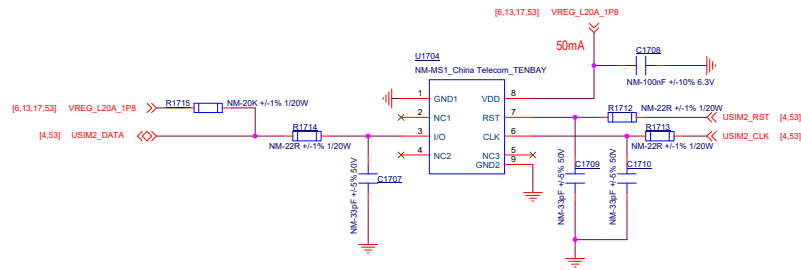




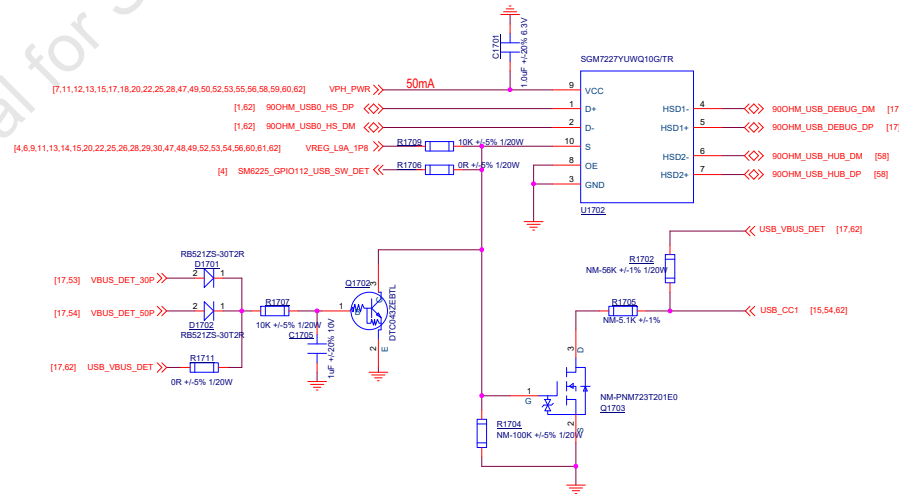
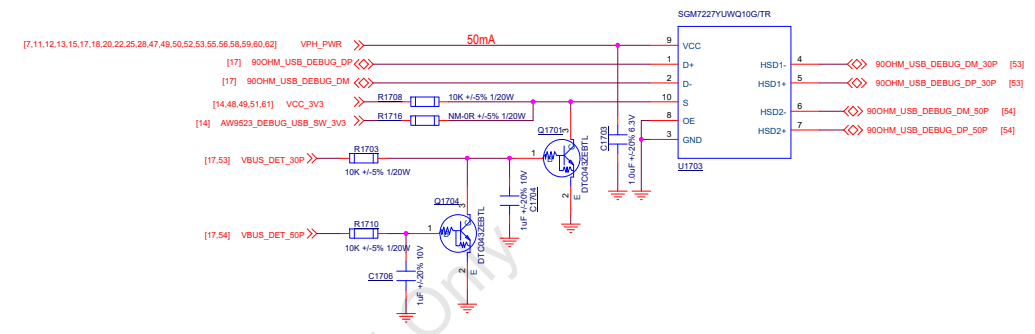
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eSIM



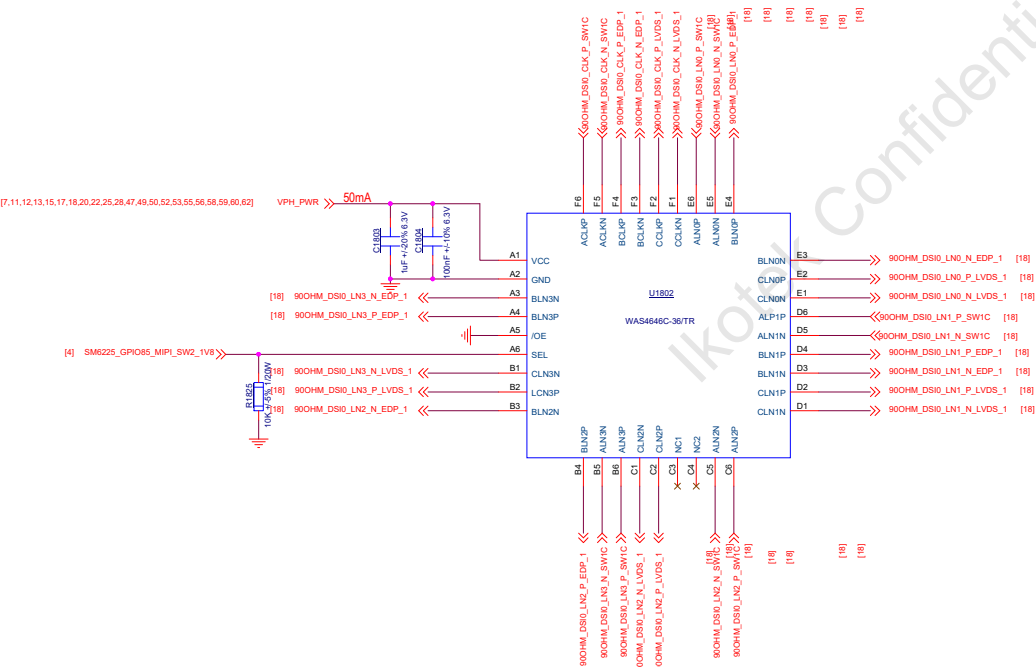
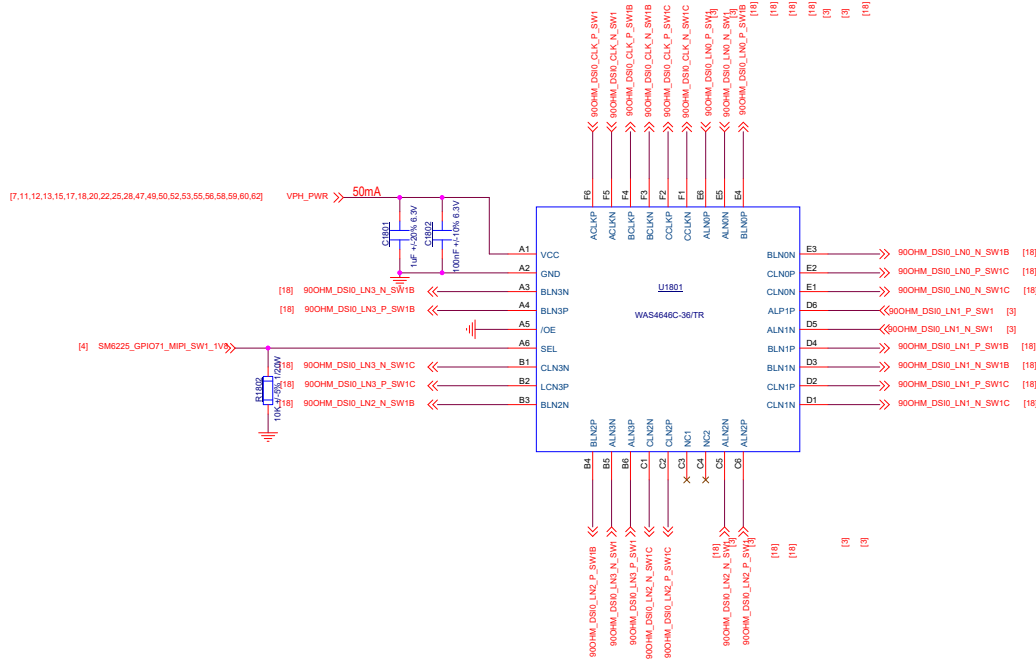
USB DEBUG SWITCH



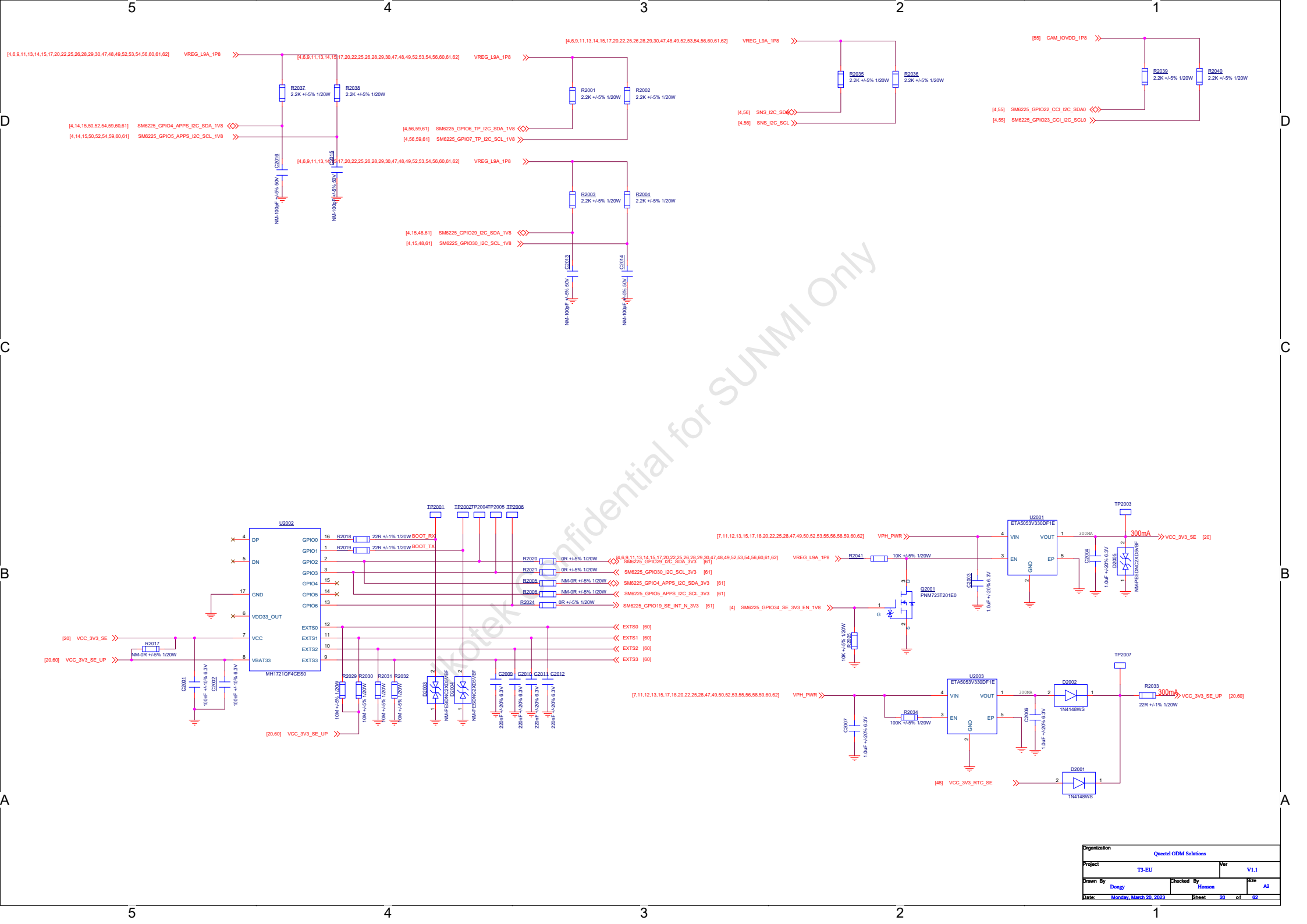
FUNCTION TABLE

OE	s	HSD1+, HSD1-	HSD2+, HSD2-
0	0	ON	OFF
0	1	OFF	ON
1	x	OFF	OFF

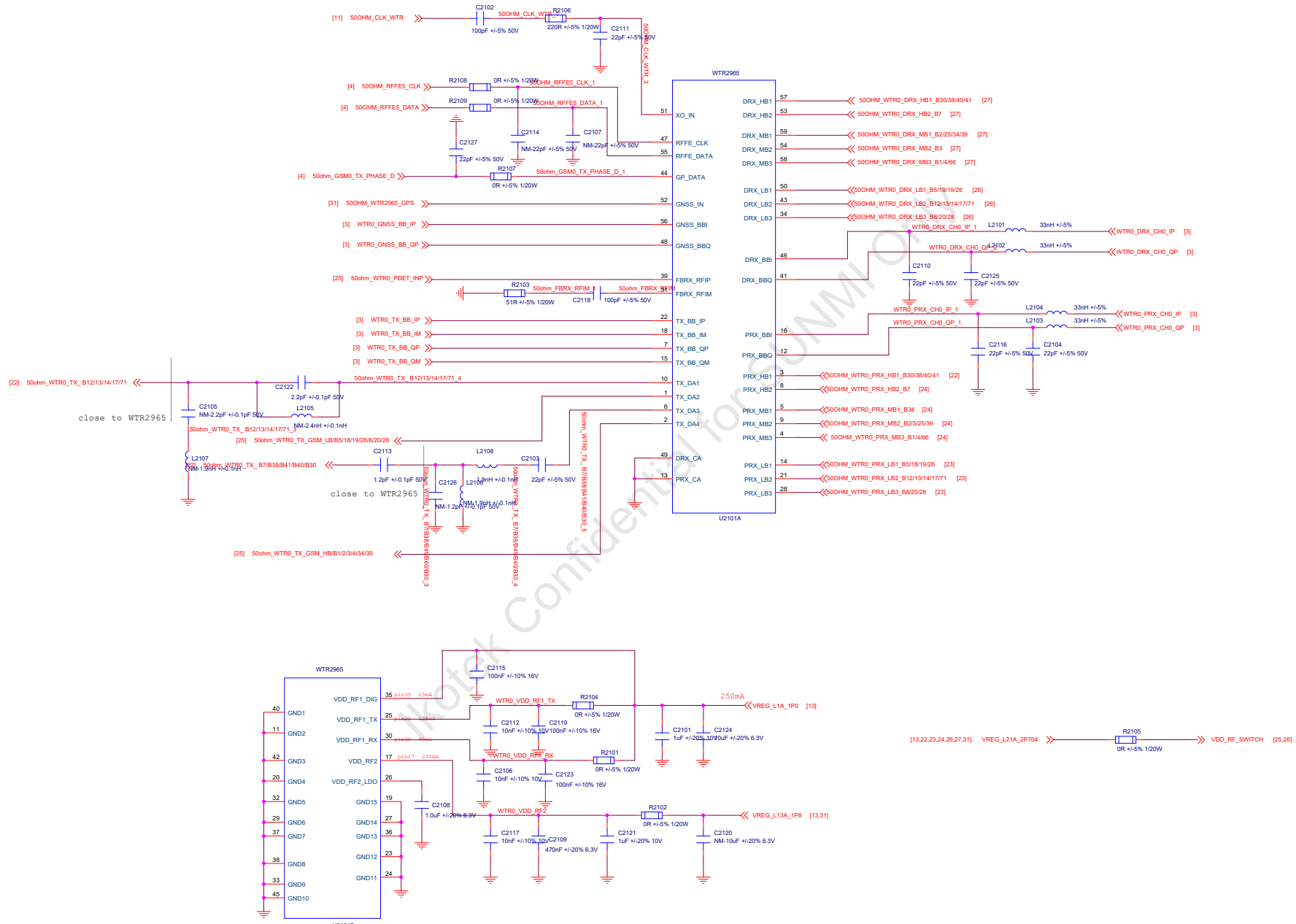
Switches Shown For Logic "0" Input



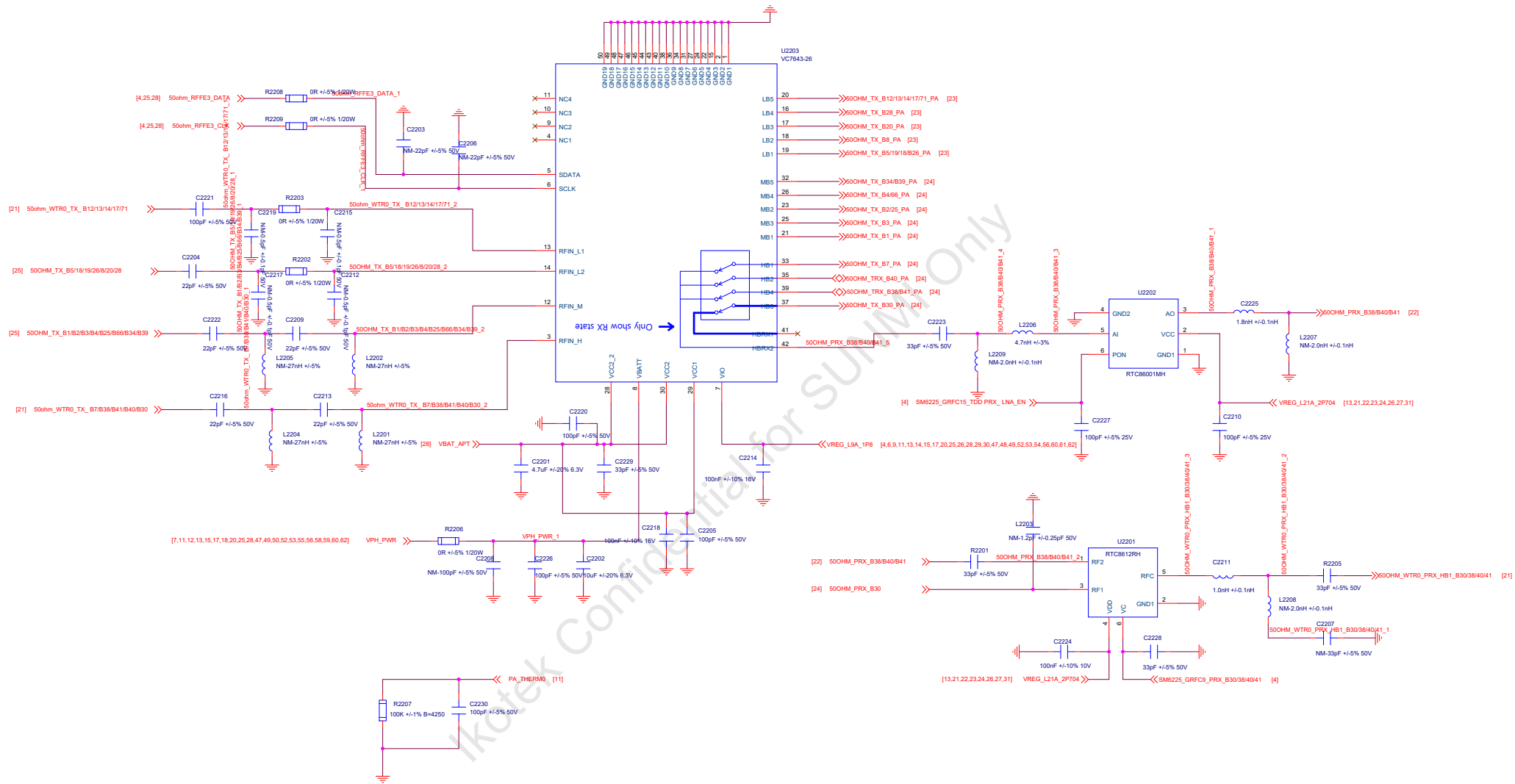
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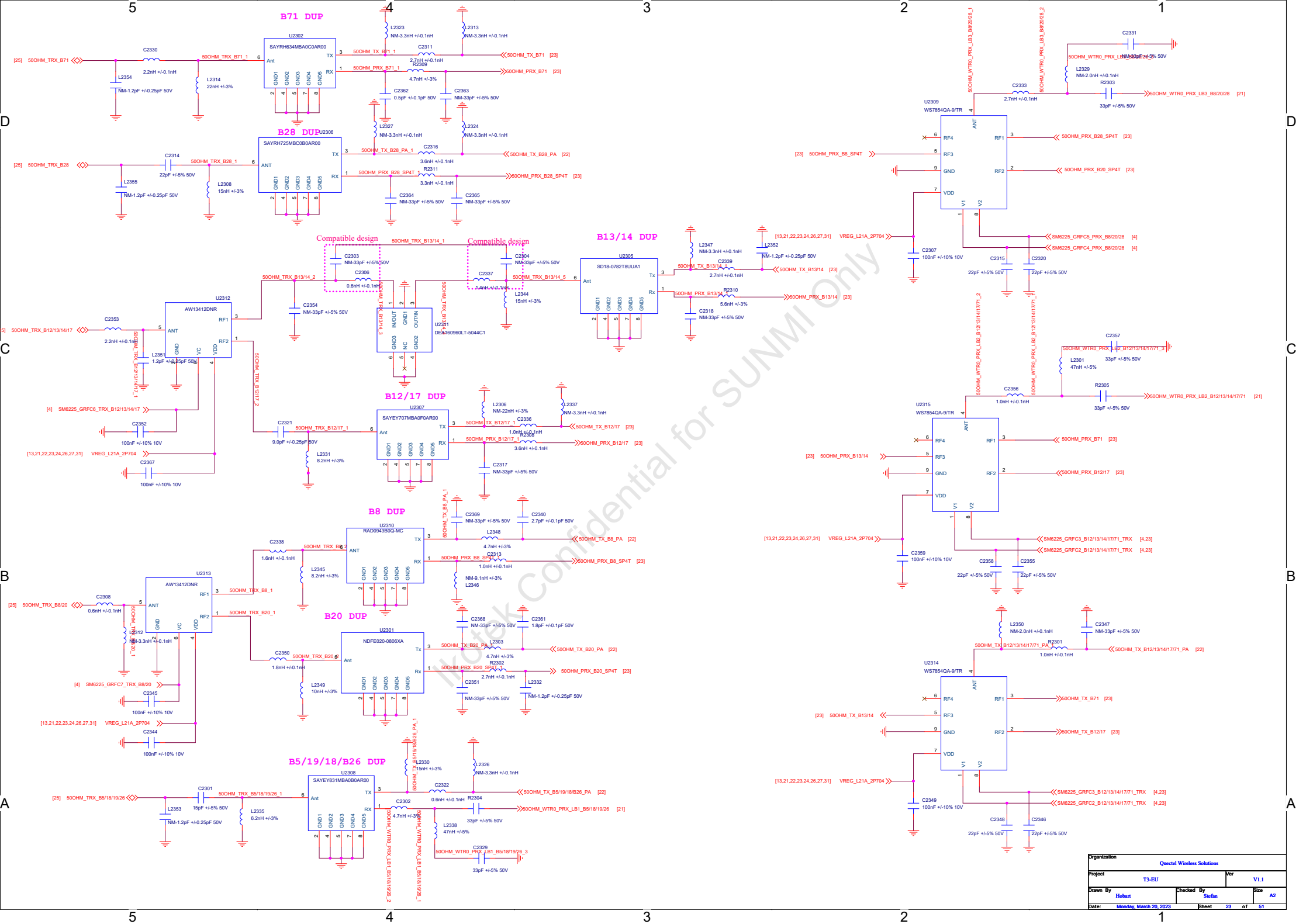
Organization			
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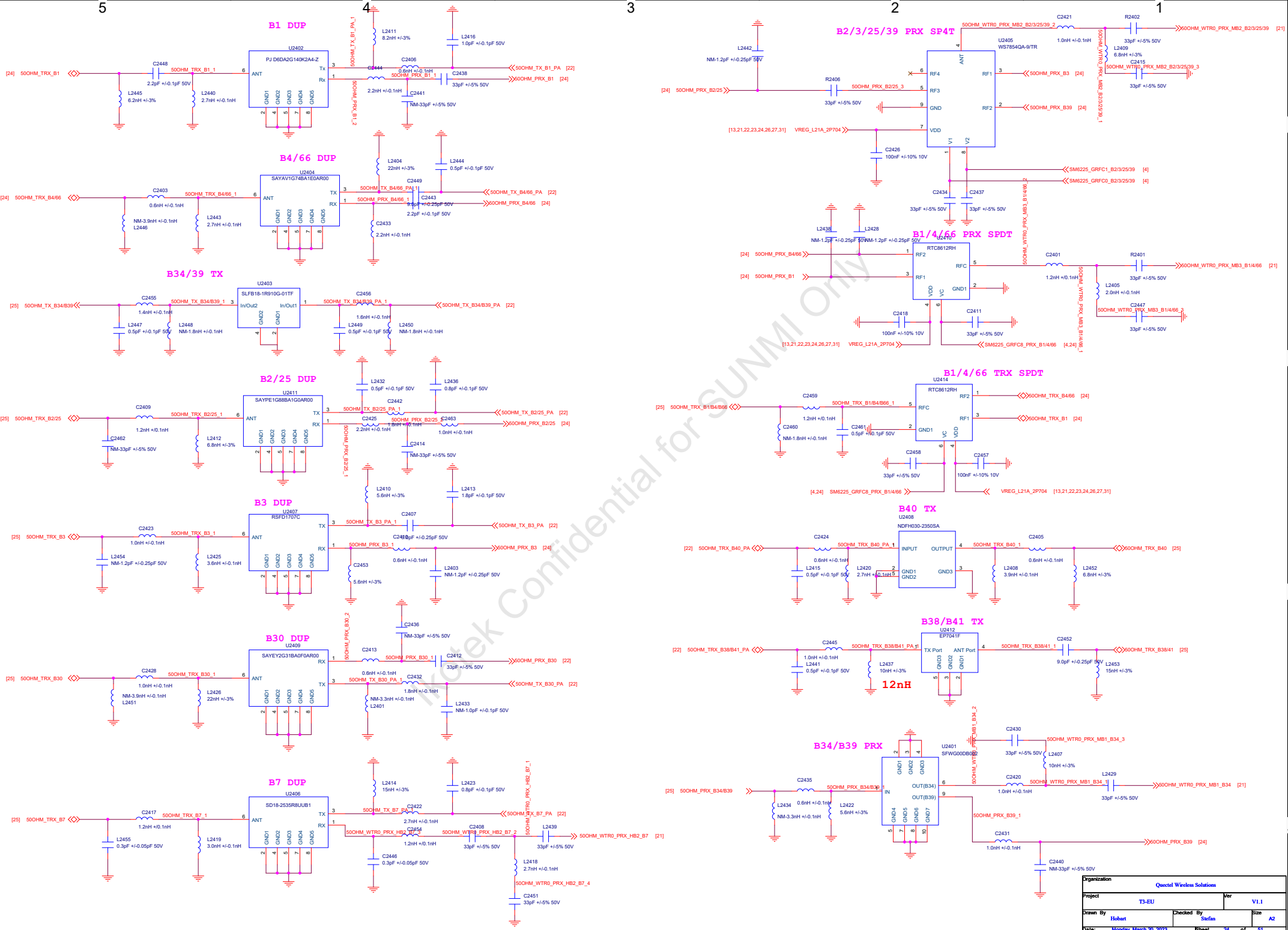
Organization			
Quectel Wireless Solutions			
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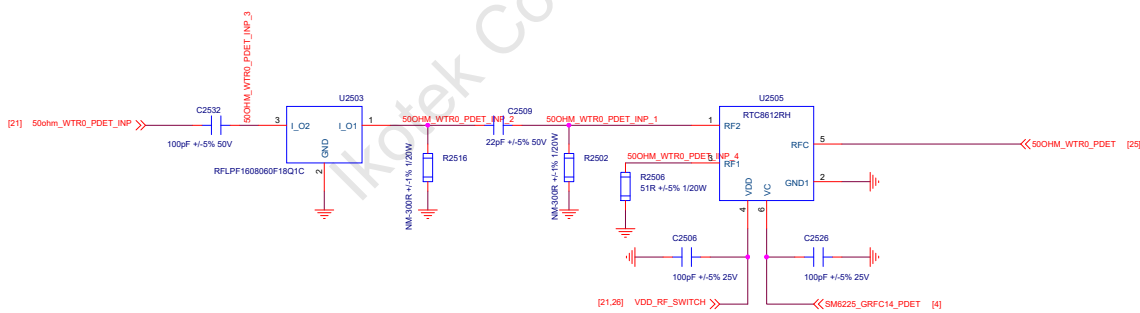
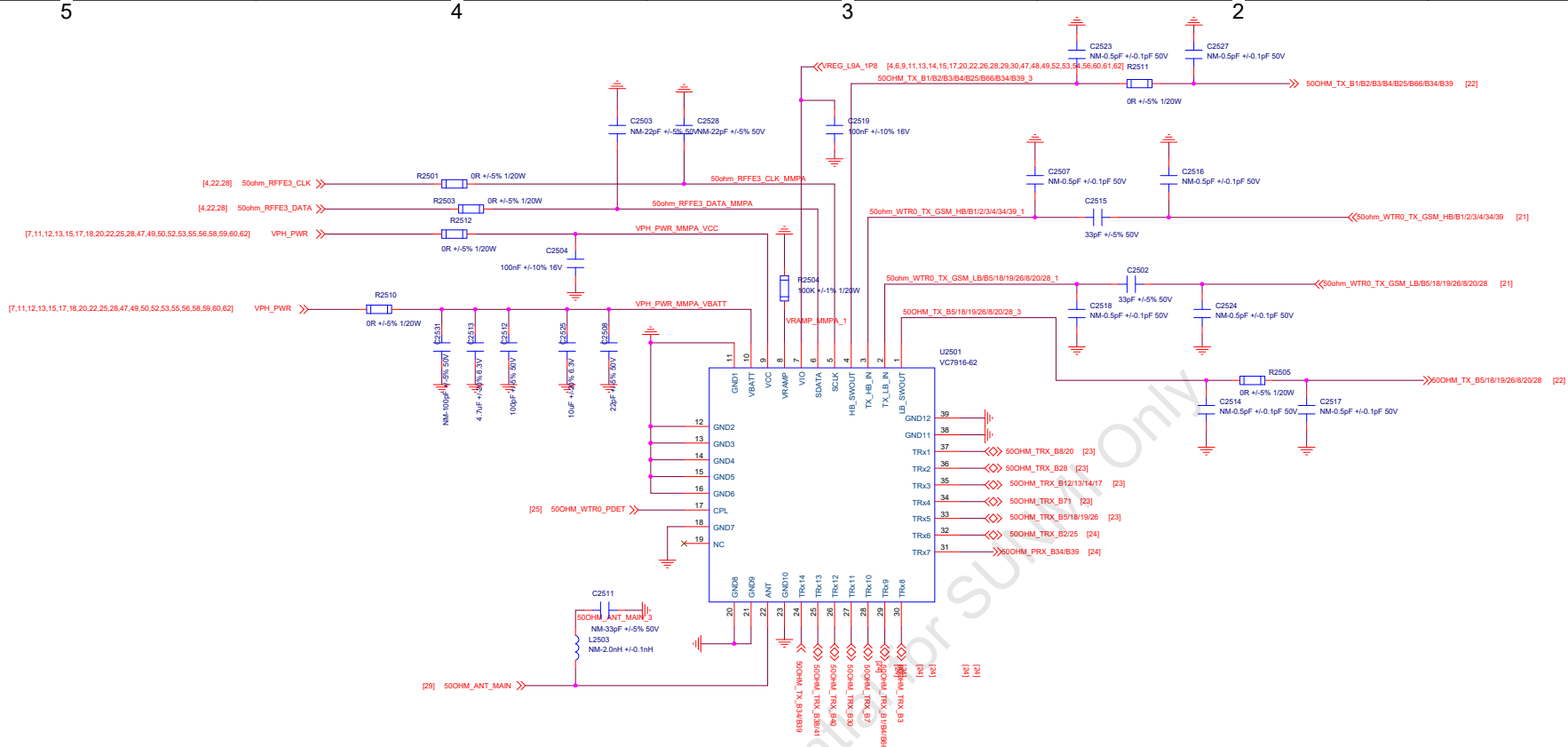
Organization		Quectel Wireless Solutions	
Project	T3-EU	Ver	V1.1
Drawn By	Hobart	Checked By	Stefan
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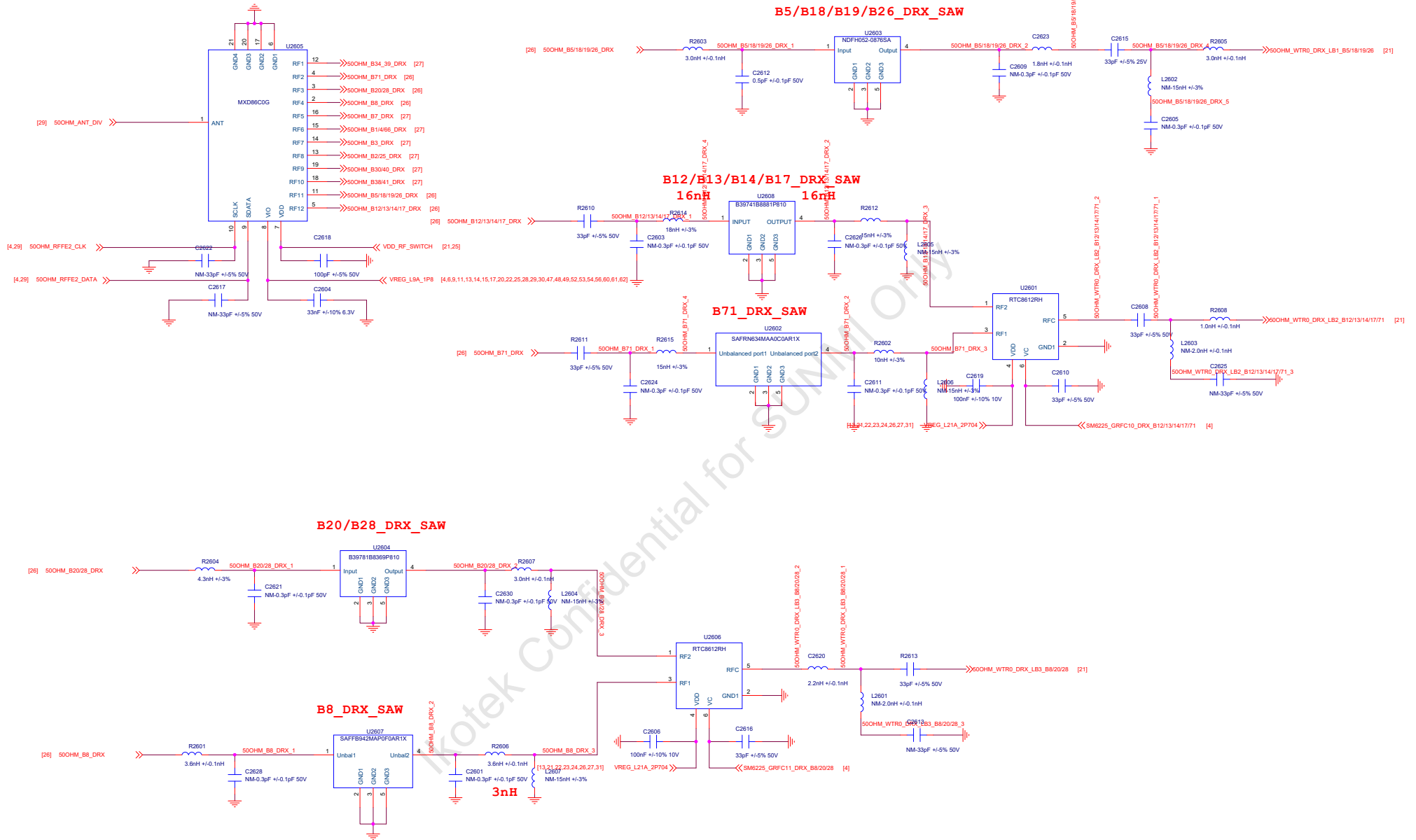
Organization		Quectel Wireless Solutions	
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Drawn By	Hobart	Checked By	S Stefan
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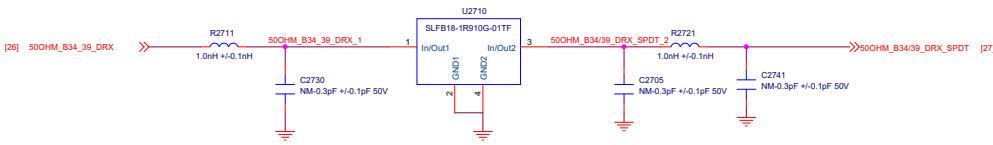


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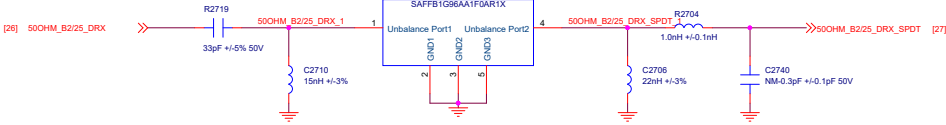


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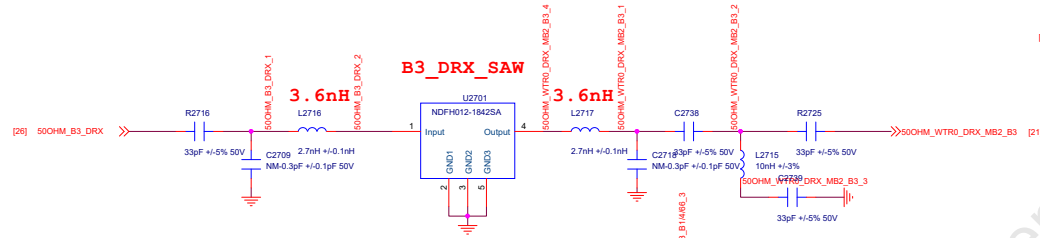
B34_B39_DRX_SAW



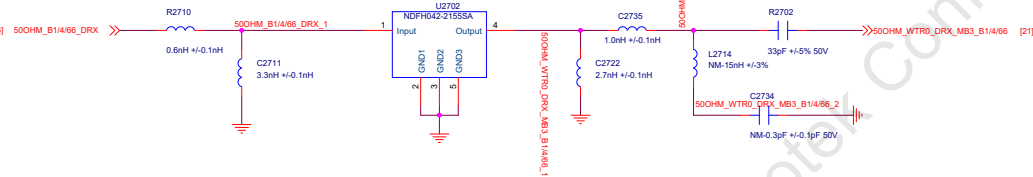
B2/B25_DRX_SAW



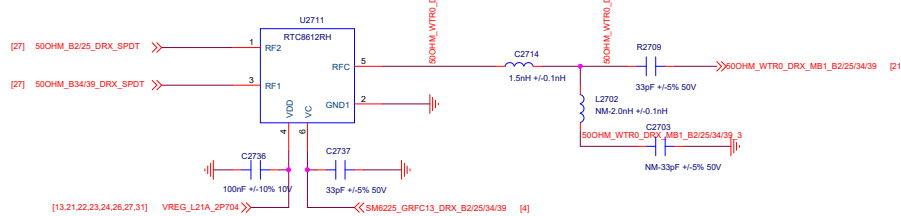
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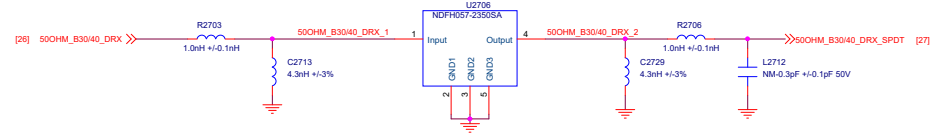
B1/B4/B66_DRX_SAW



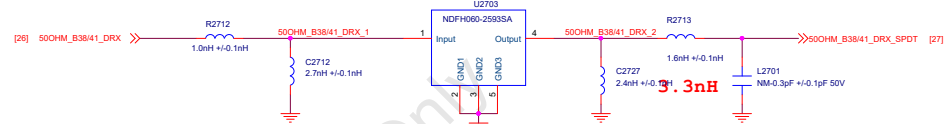
B2/25/34/39_DRX_SPDT



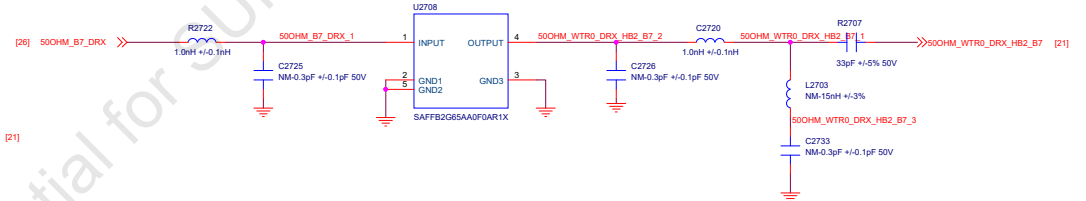
B30/B40_DRX_SAW



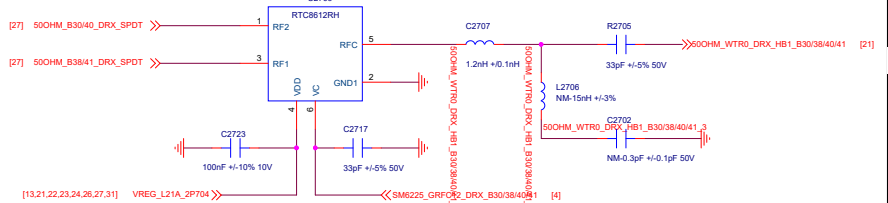
B38/B41_DRX_SAW



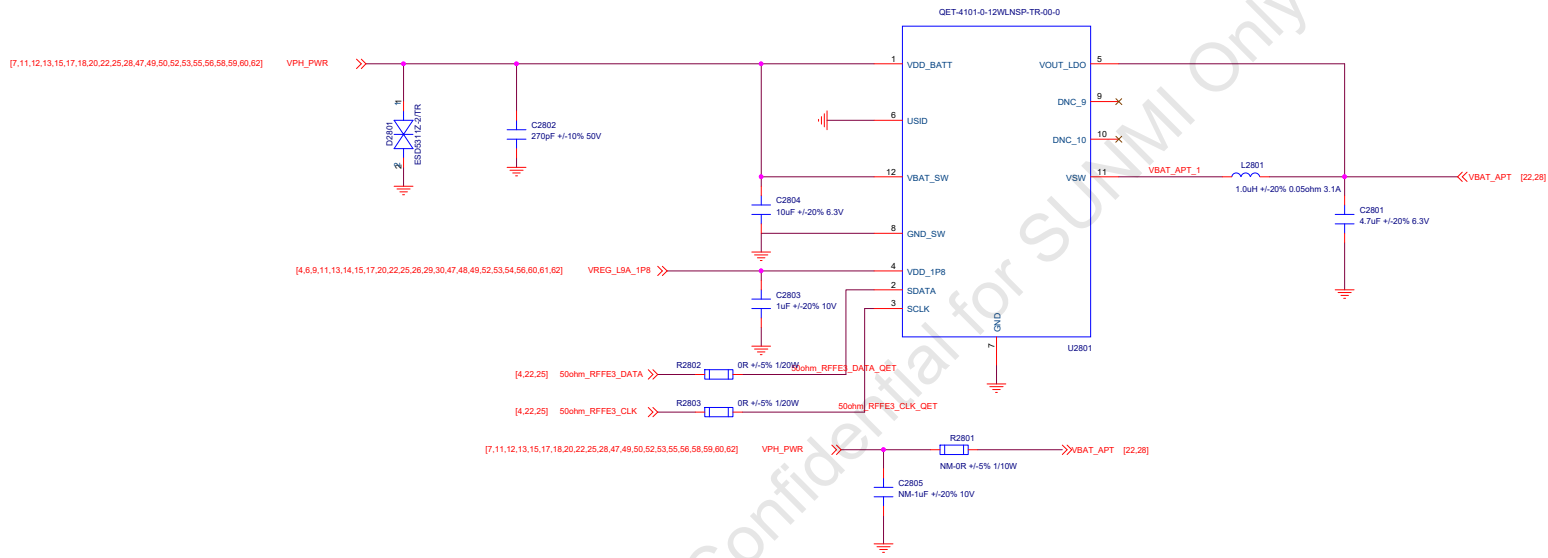
B7_DRX_SAW



B30/38/40/41_DRX_SPDT



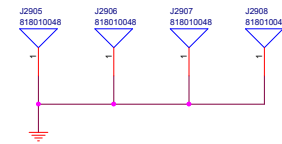
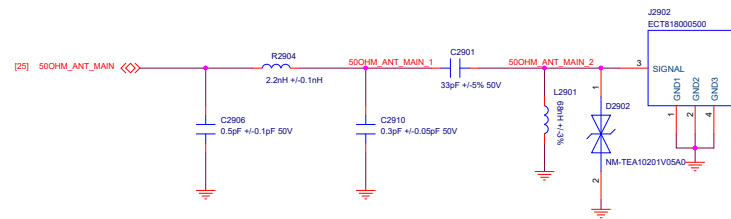
Organization			
Questel Wireless Solutions			
Project	T3-EU	Ver	V1.1
Drawn By	Hobart	Checked By	Stefan
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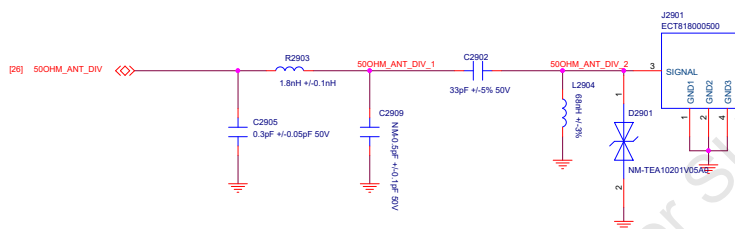
Ikotek Confidential for SUMMI Only

Organization			
Questel Wireless Solutions			
Project	T3-EU	Ver	V1.1
Drawn By	Hobart	Checked By	Stefan
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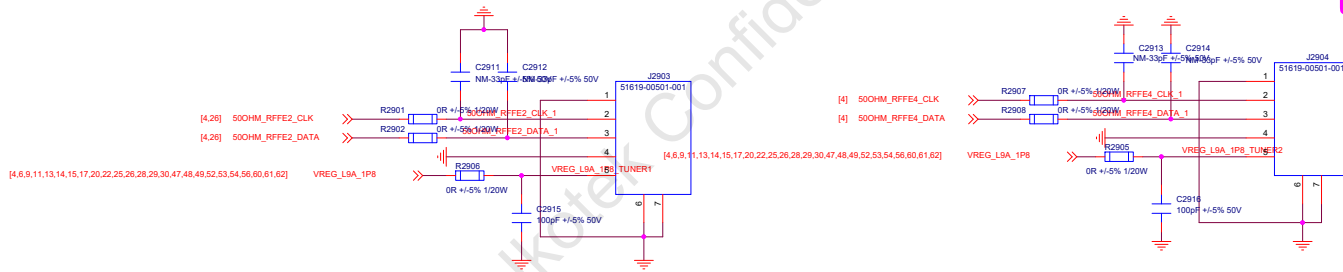
MAIN_ANT



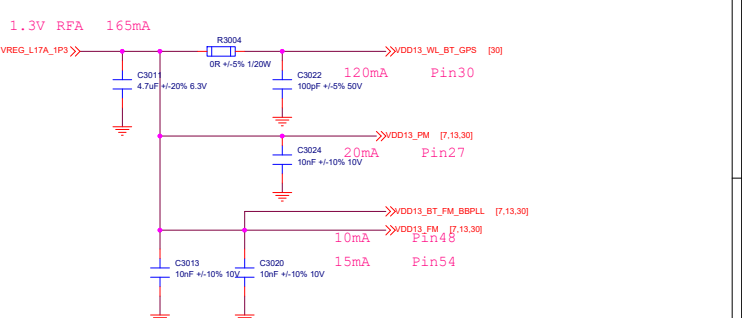
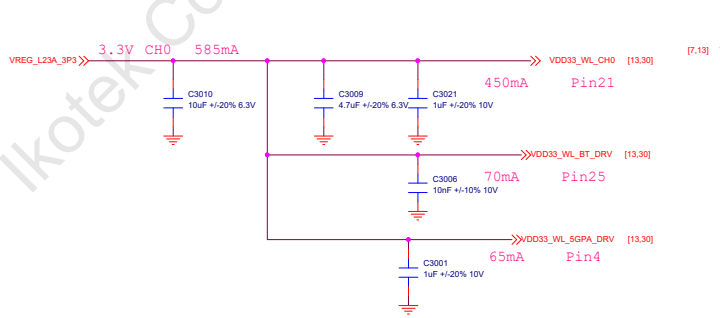
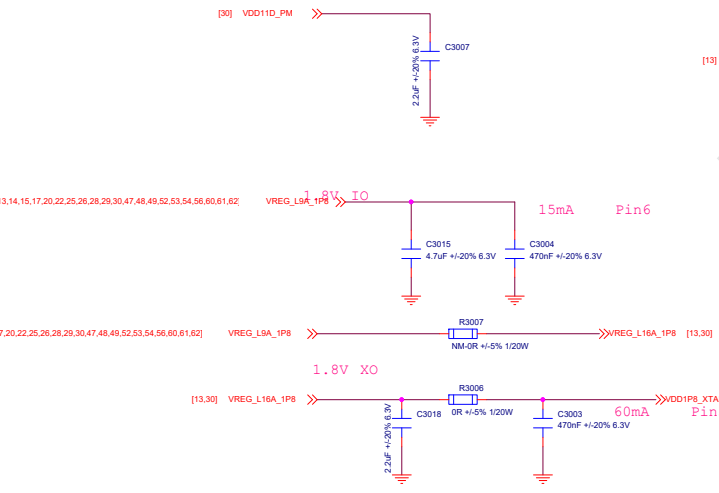
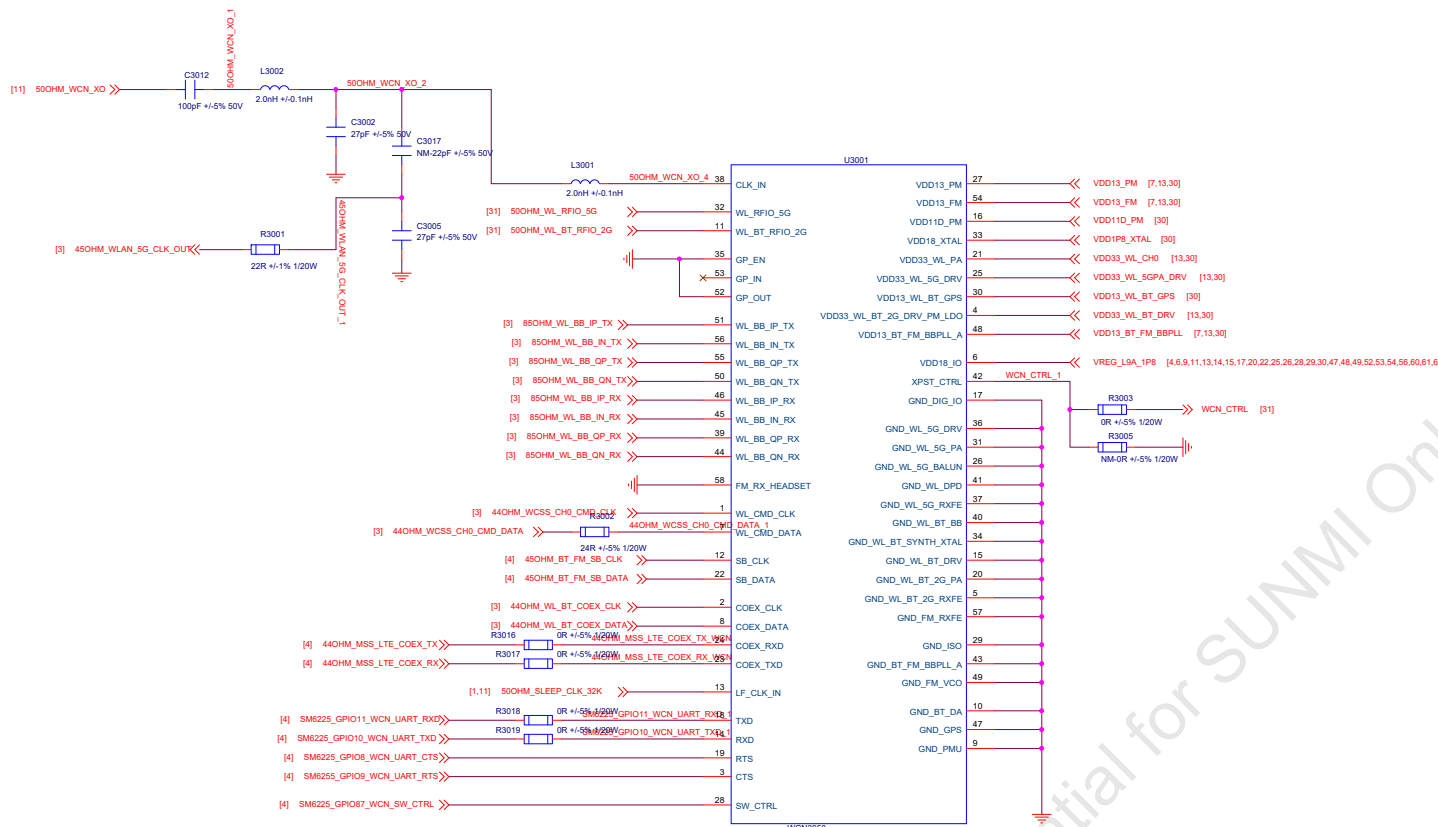
DIV_ANT



tuner



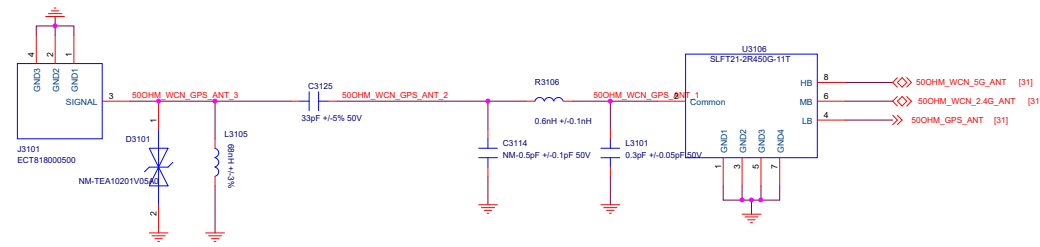
Organization			
Questel Wireless Solutions			
Project	T3-EU	Ver	V1.1
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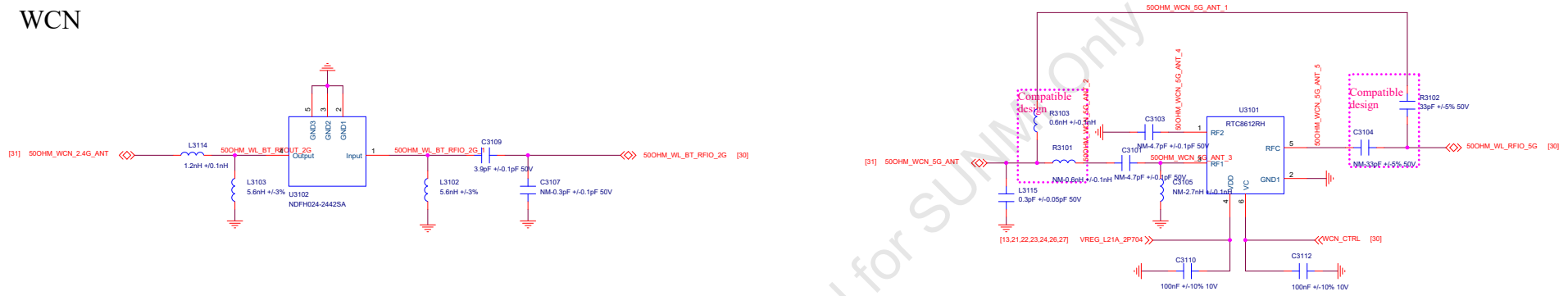
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Organization			
Quectel Wireless Solutions			
Project	T3-EU	Ver	V1.1
Drawn By	Hobart	Checked By	Stefan
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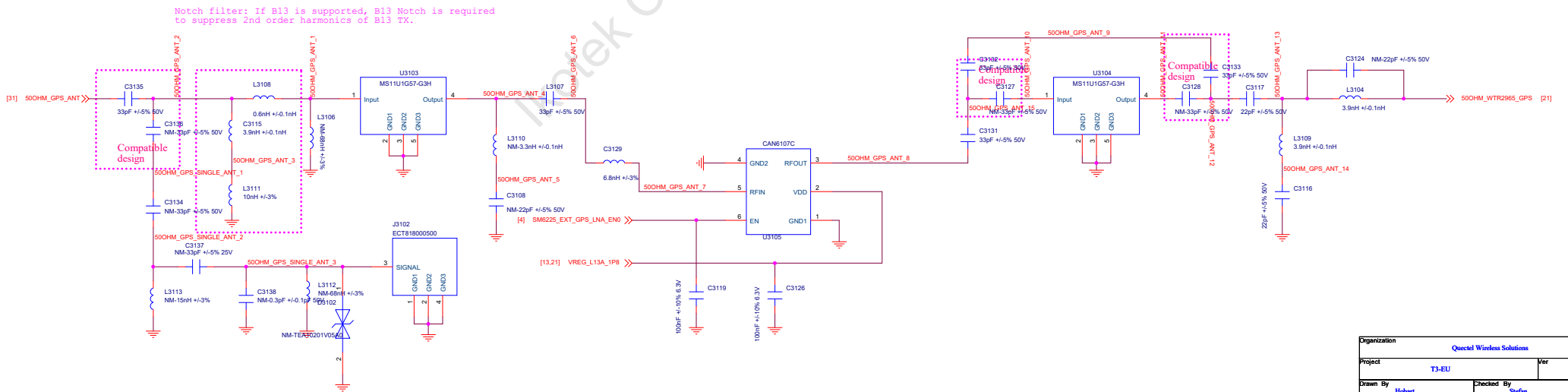
WIFI_BT_GPS_ANT



WCN

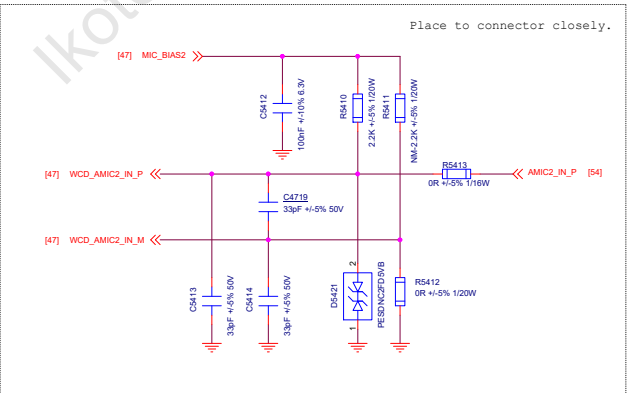
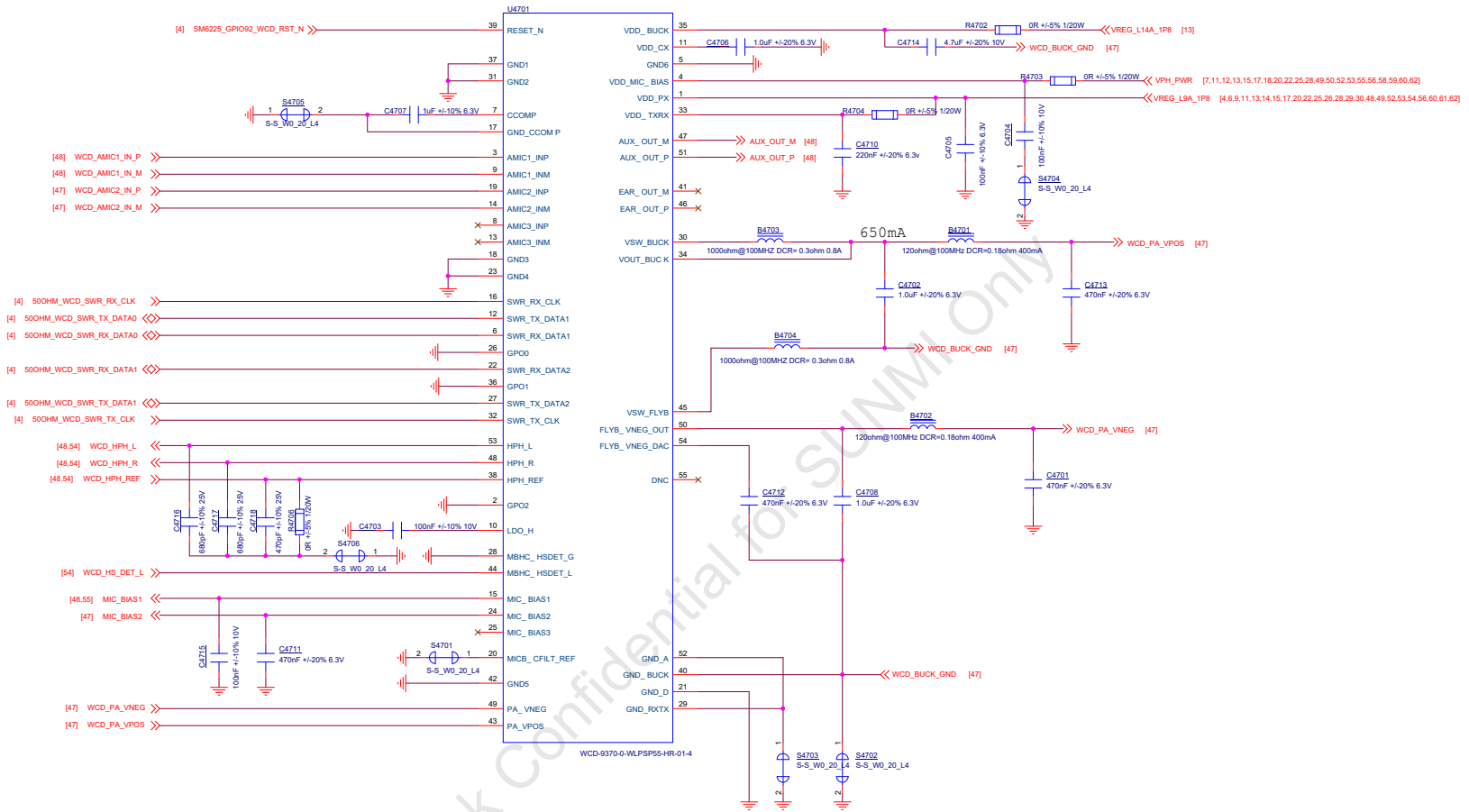


GPS



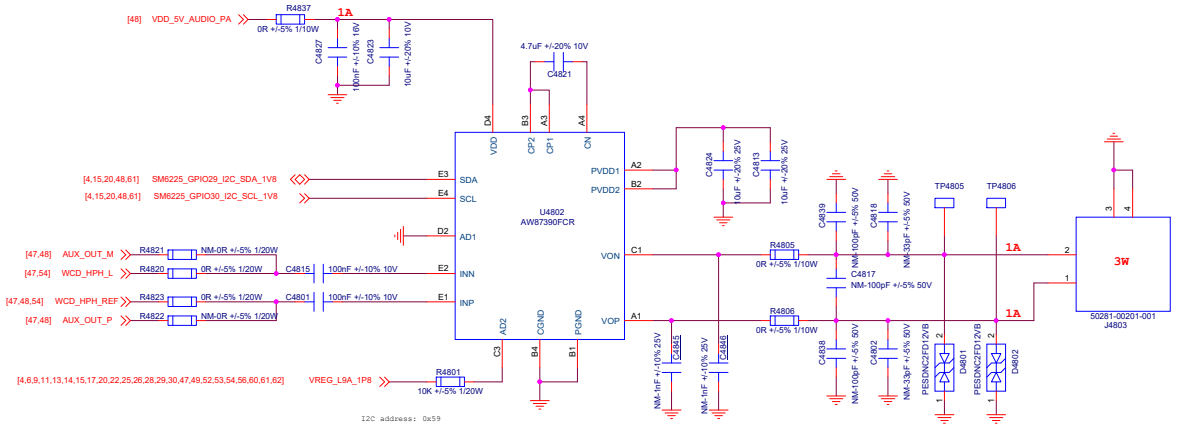
Organization	Quectel Wireless Solutions		
Project	T3-EU	Ver	V1.1
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CODEC

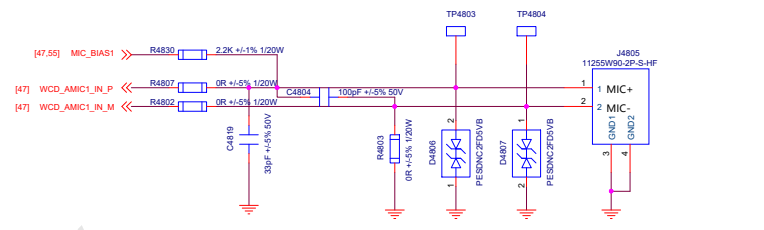


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Project	T3-EU	Ver	V1.1
Drawn By	Dongy	Checked By	Hosoon
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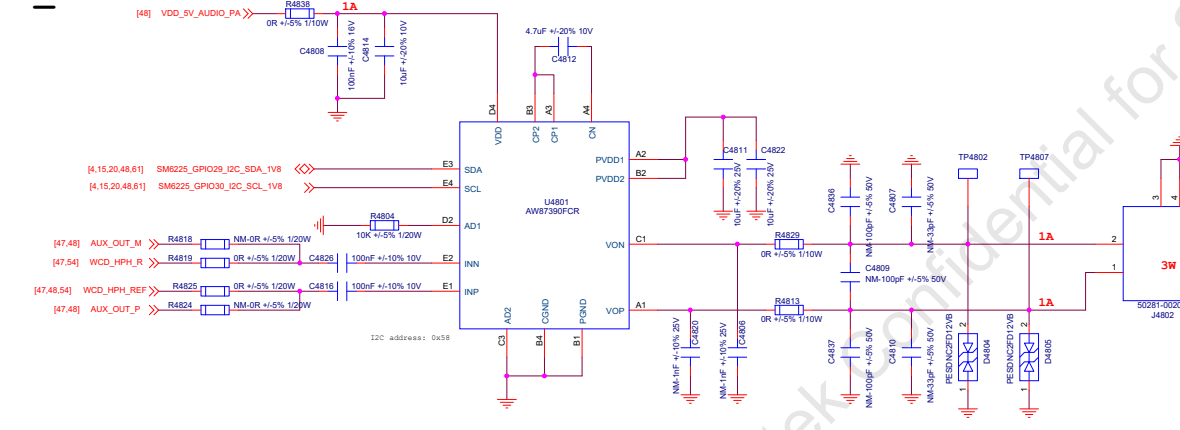
SPK_L



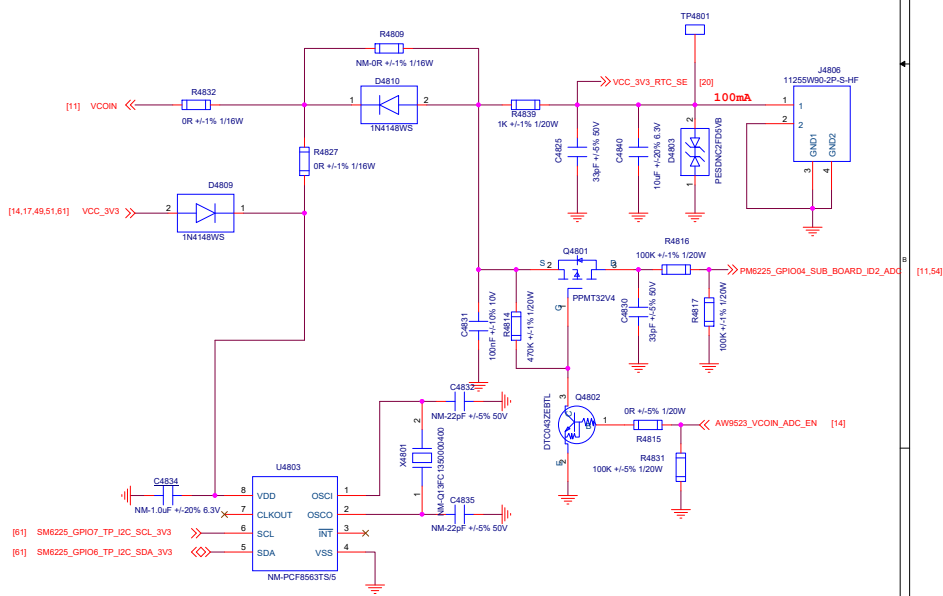
AMIC



SPK_R

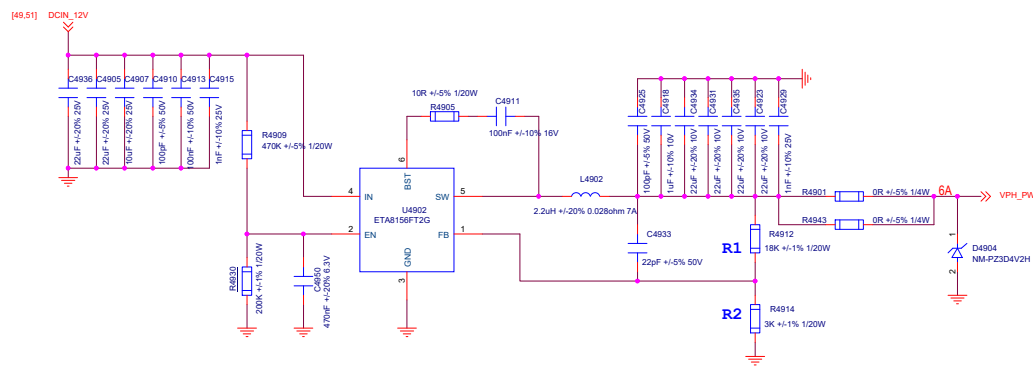


RTC



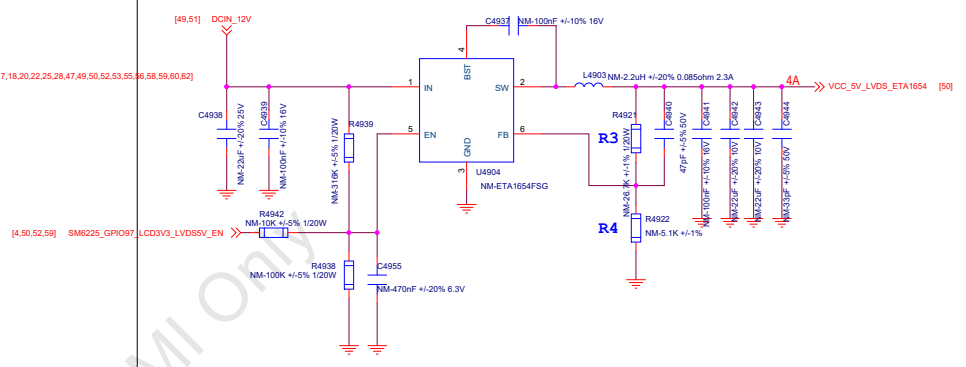
Organization	Quectel ODM Solutions		
Project	T3-EU	Ver	V1.1
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DC12V to 4V



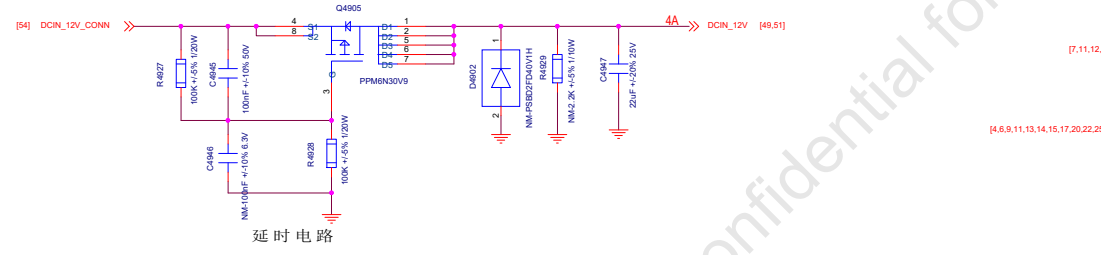
$V_{OUT} = 0.6 * (R1/R2 + 1) = 4.2V$
 ETA8156FT2G Resistors R2 has to between 1K to 24K

DC12V to 5V

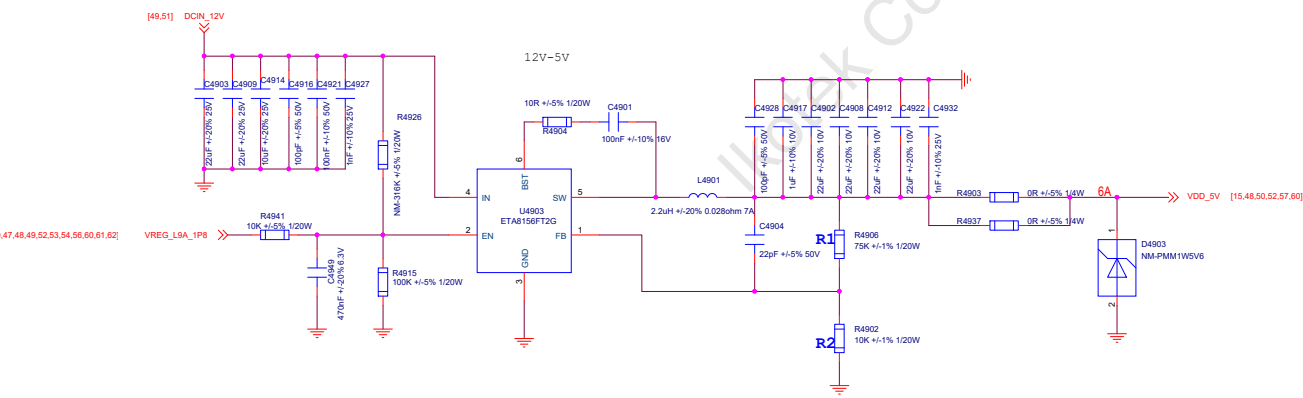


$V_{OUT} = 0.805 * (R3/R4 + 1) = 5.019V$

DC12V to 5V

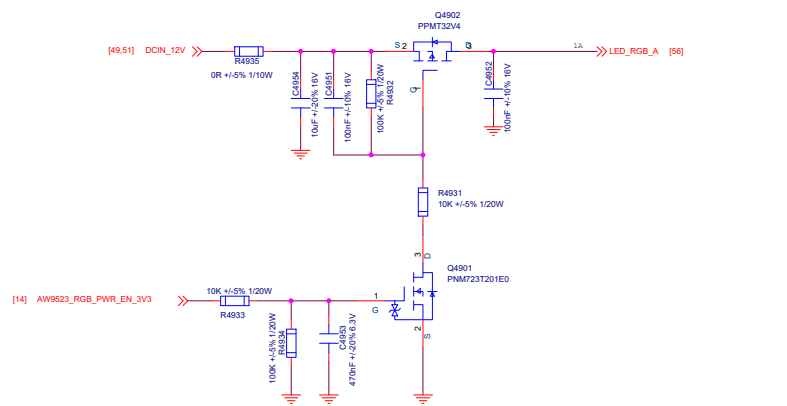
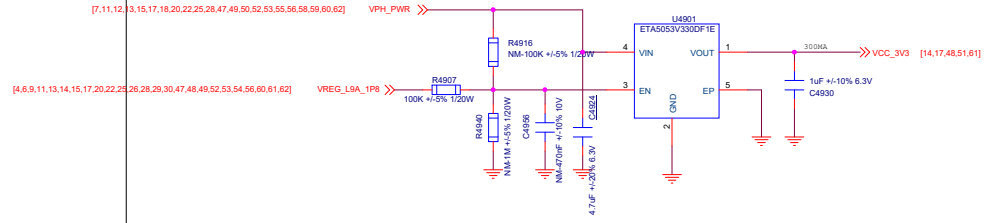


延时电路

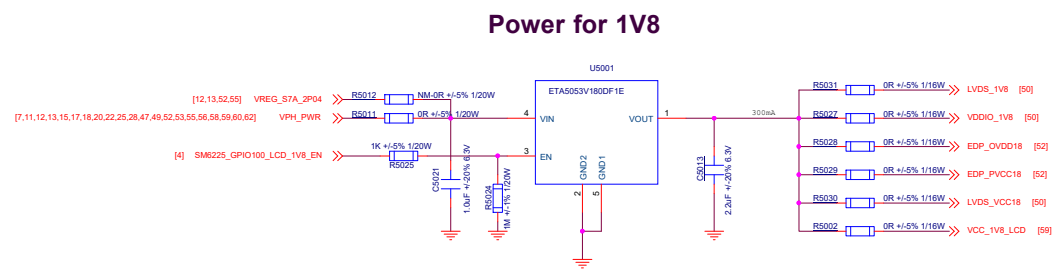
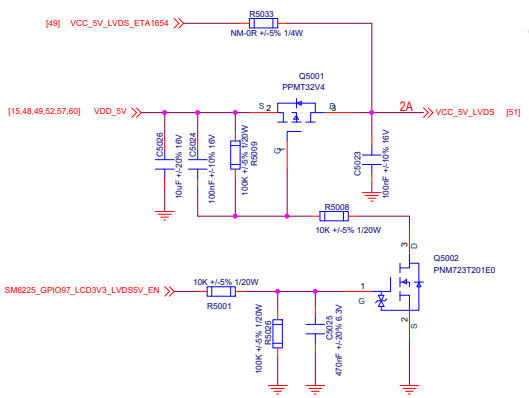
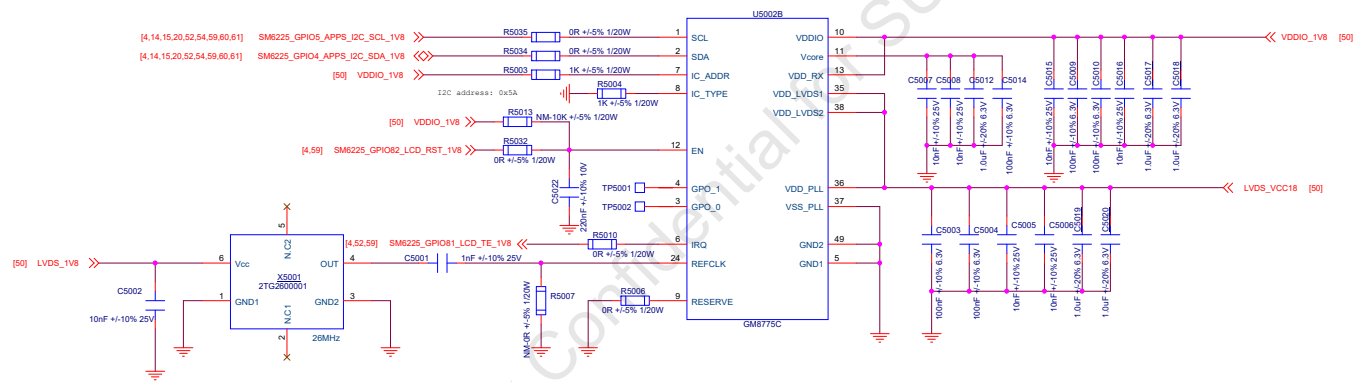


$V_{OUT} = 0.6 * (R1/R2 + 1) = 5.1V$
 ETA8156FT2G Resistors R2 has to between 1K to 24K

VCC_3V3



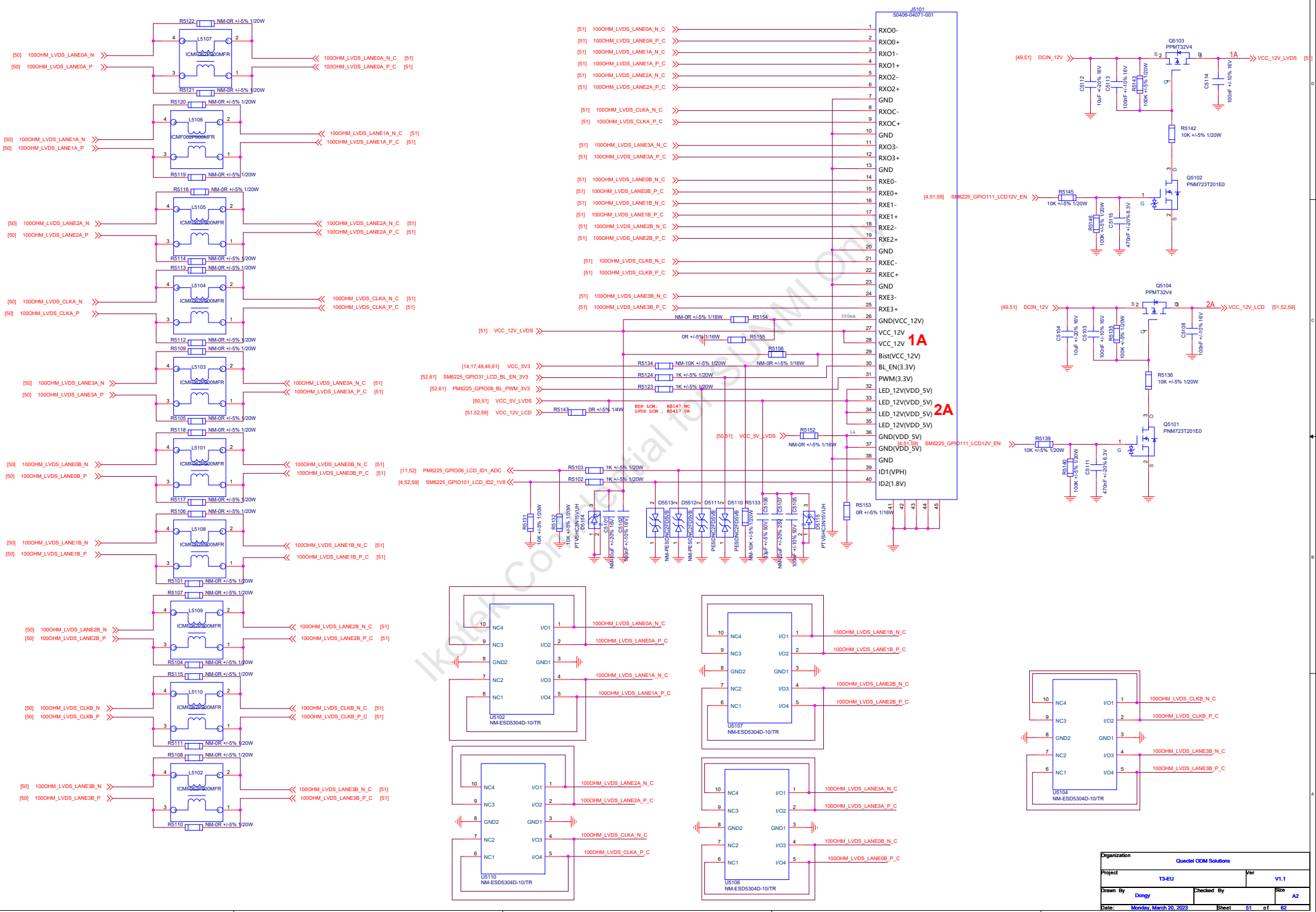
Organization		Quectel ODM Solutions	
Project	T3-EU	Ver	V1.1
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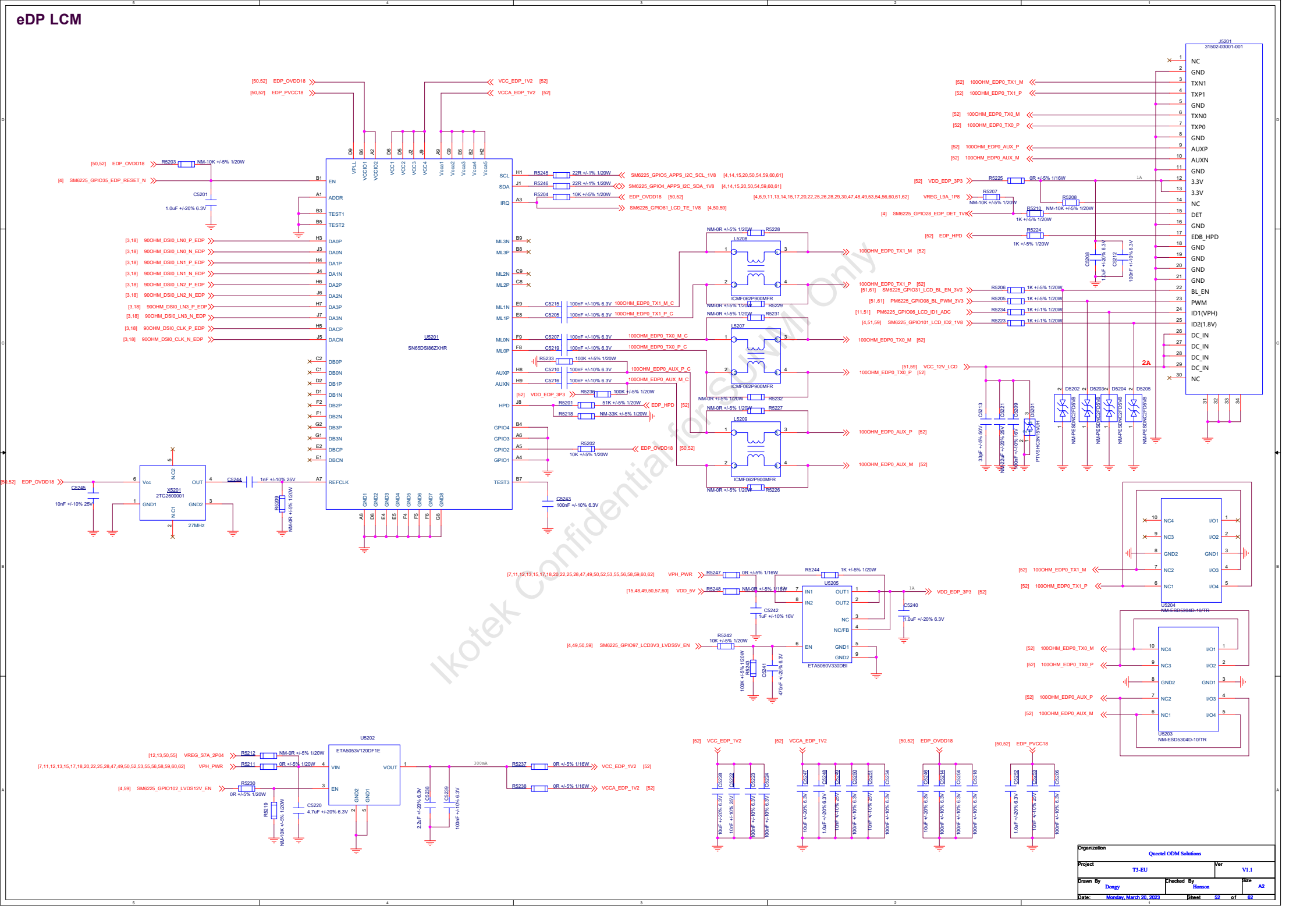
Power for 1V8

Organization	Quectel ODM Solutions		
Project	TS-EU	Ver	V1.1
Drawn By	Dongy	Checked By	Hoson
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LVDS_CONNECTOR

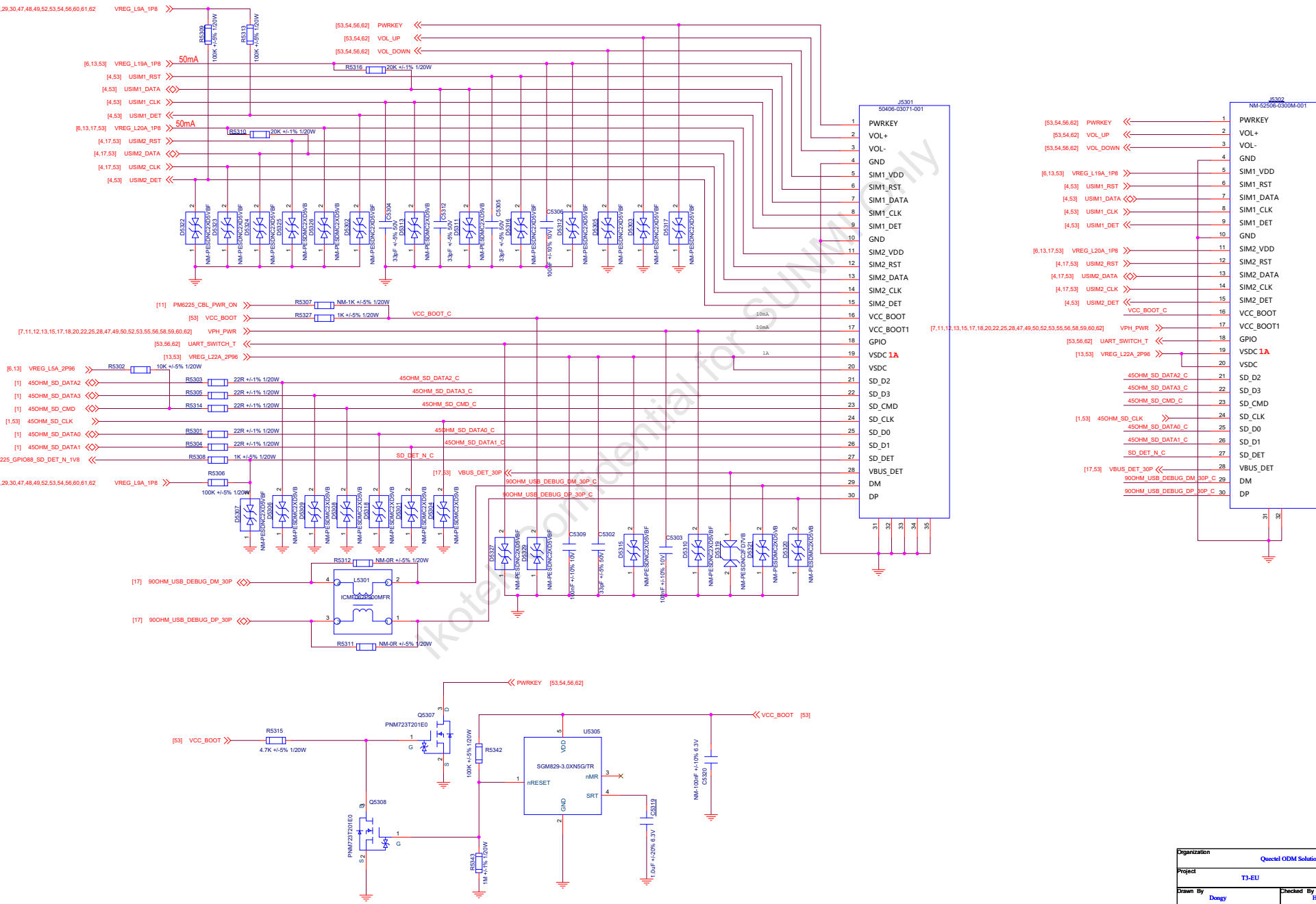


Organization			
Quectel ODM Solutions			
Project	TS-EU	Ver	V1.1
Drawn By	Dongy	Checked By	Size
			A2
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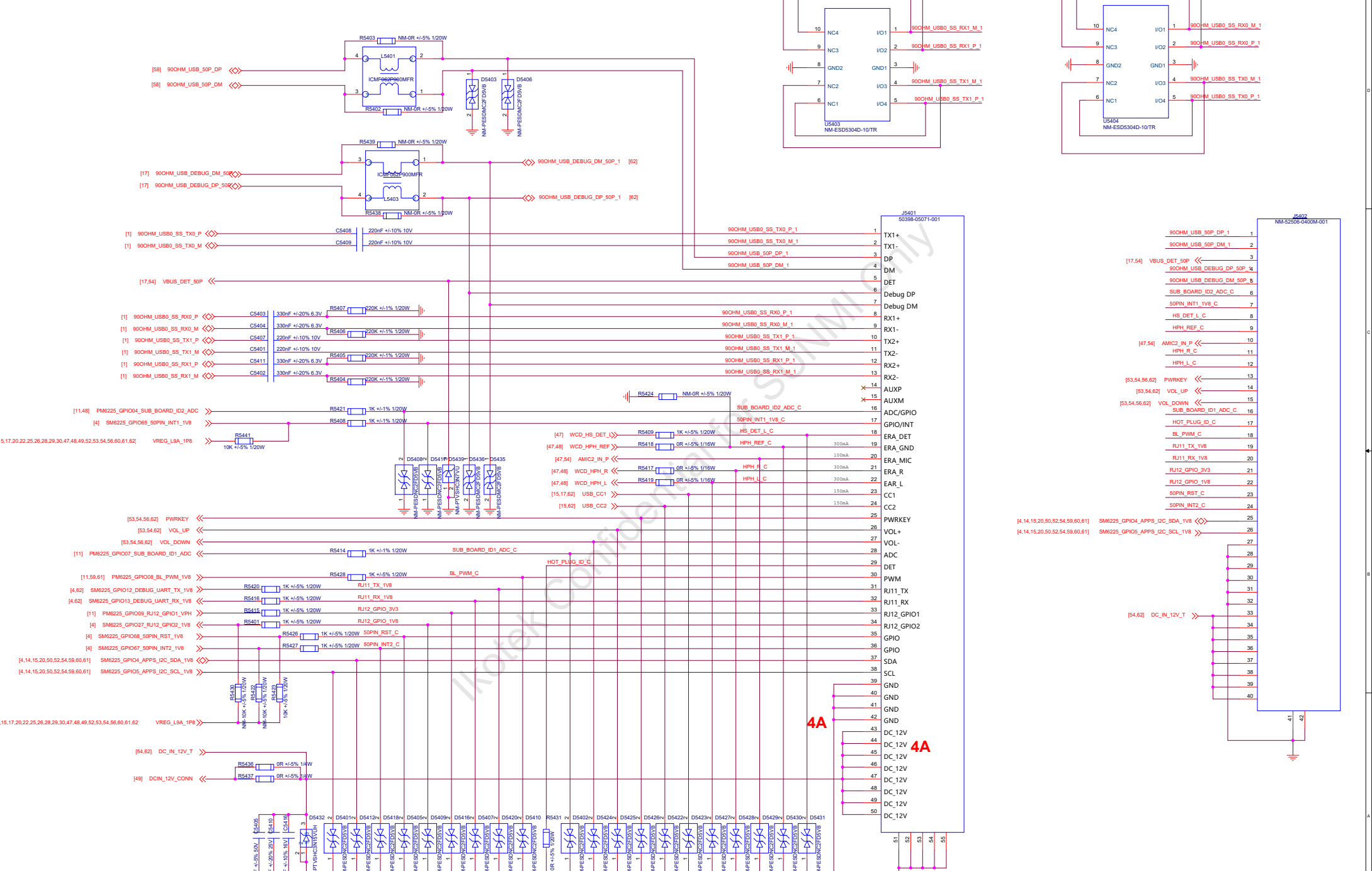
Organization	Quectel ODM Solutions		
Project	T3-EU	Ver	V1.1
Drawn By	Dongy	Checked By	Hosoon
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30P CONNECTOR



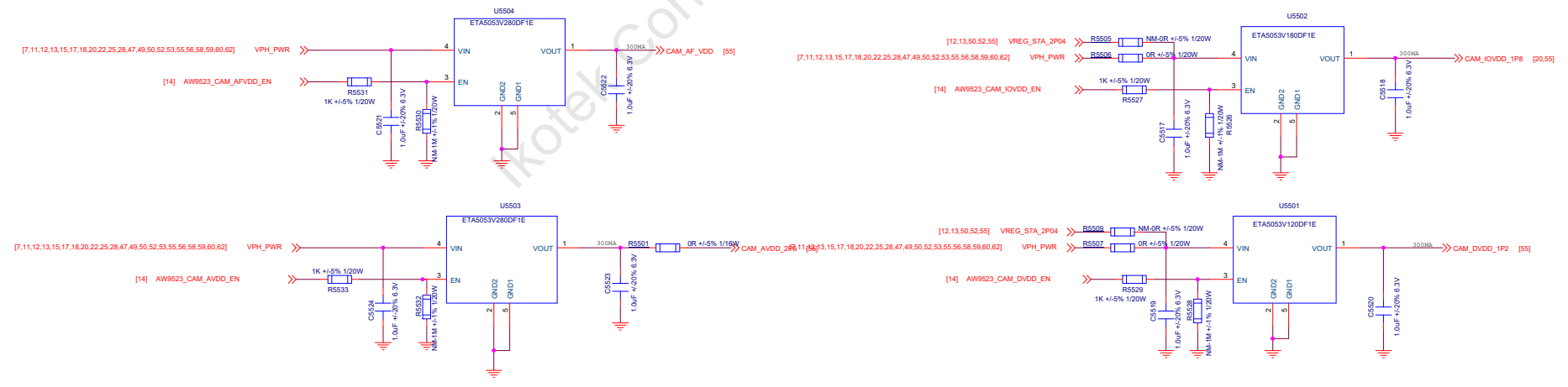
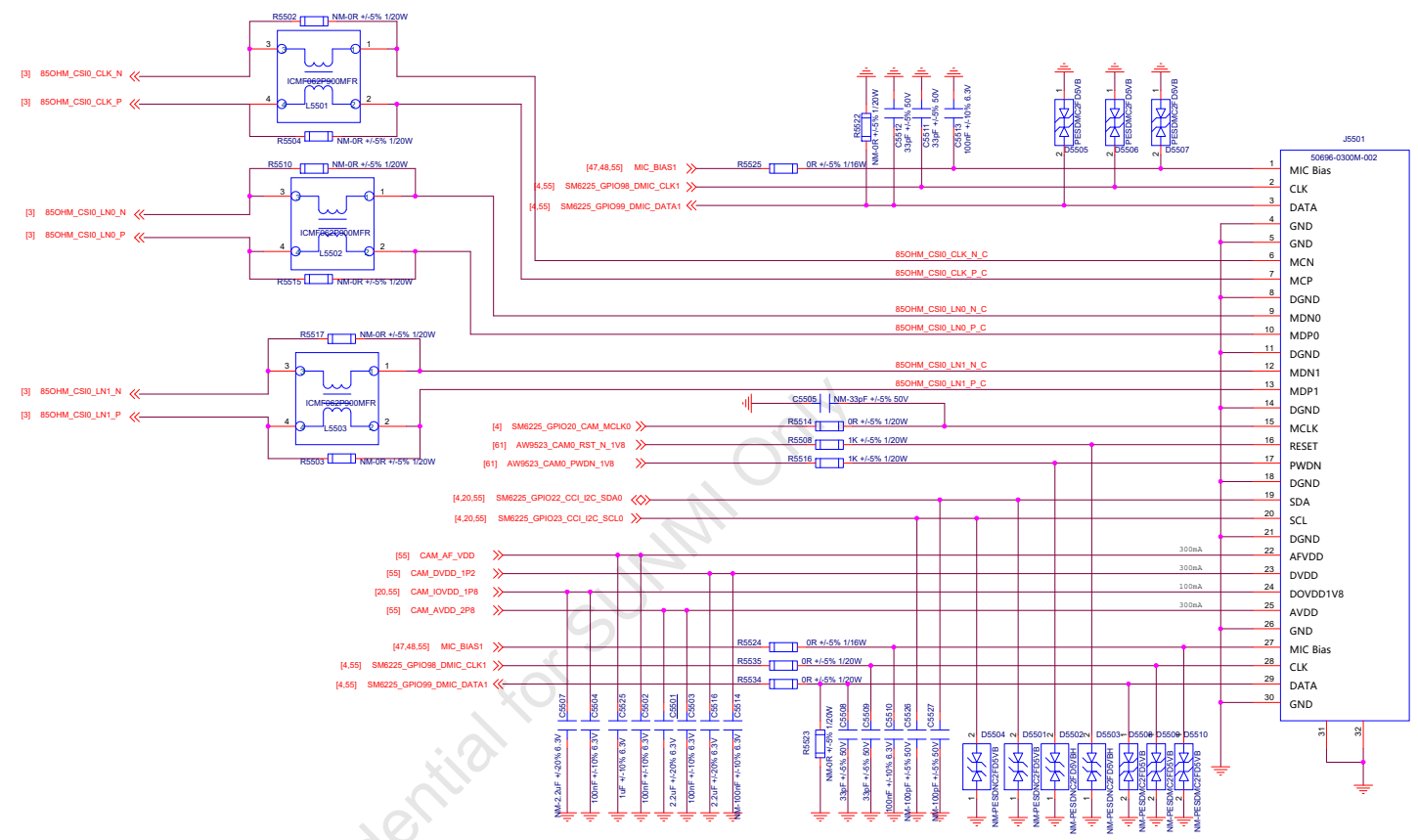
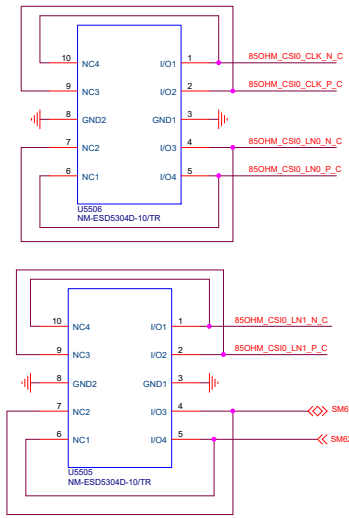
Organization	Quectel ODM Solutions		
Project	T3-EU	Ver	V1.1
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50P CONNECTOR



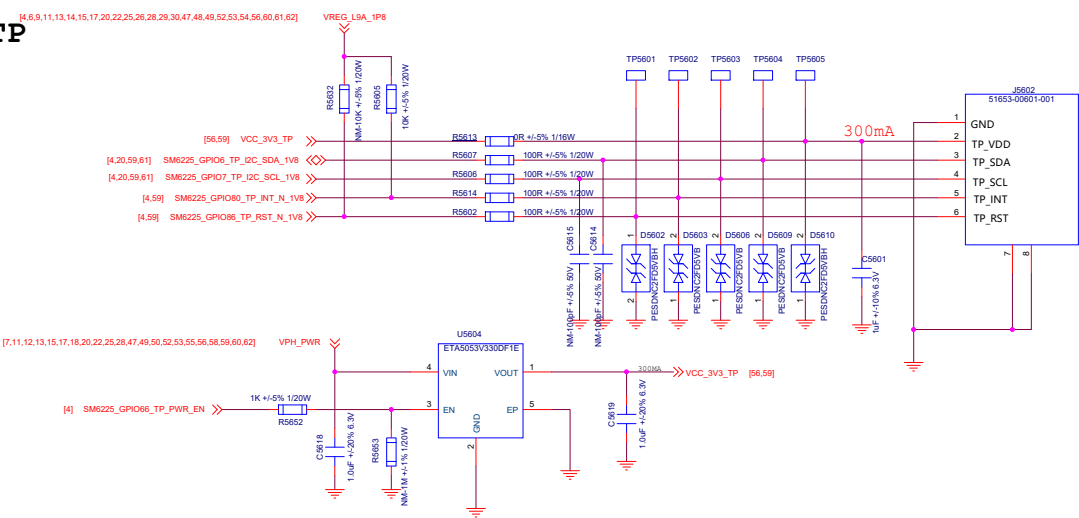
Organization			
Quectel ODM Solutions			
Project	T3-EU	Ver	V1.1
Drawn By	Dongy	Checked By	Hosoon
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MIPI CAMERA

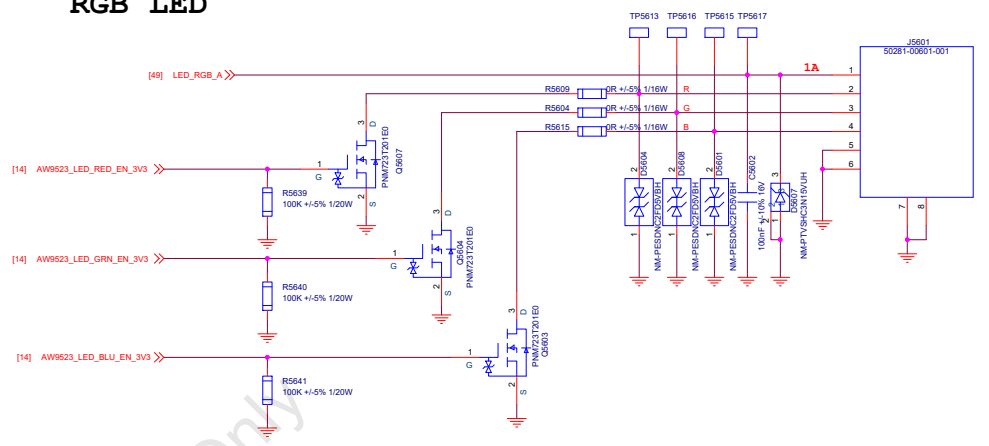


Organization	Quectel ODM Solutions		
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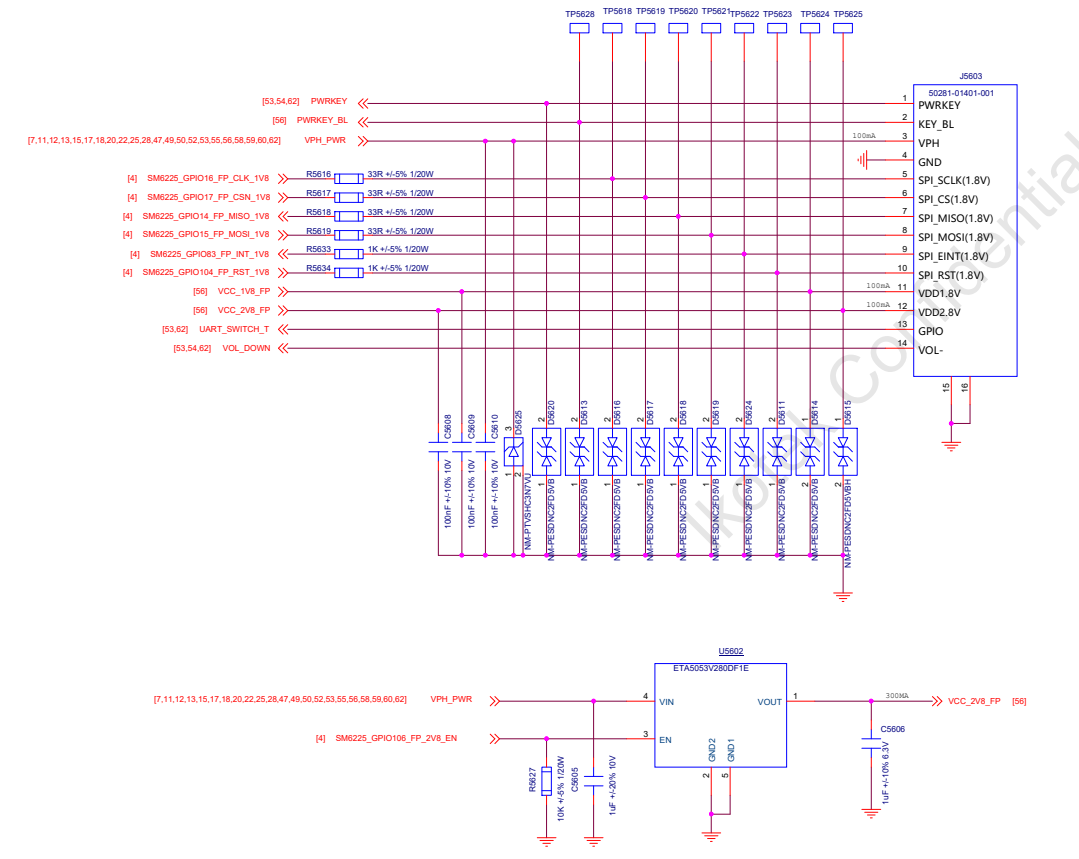
TP



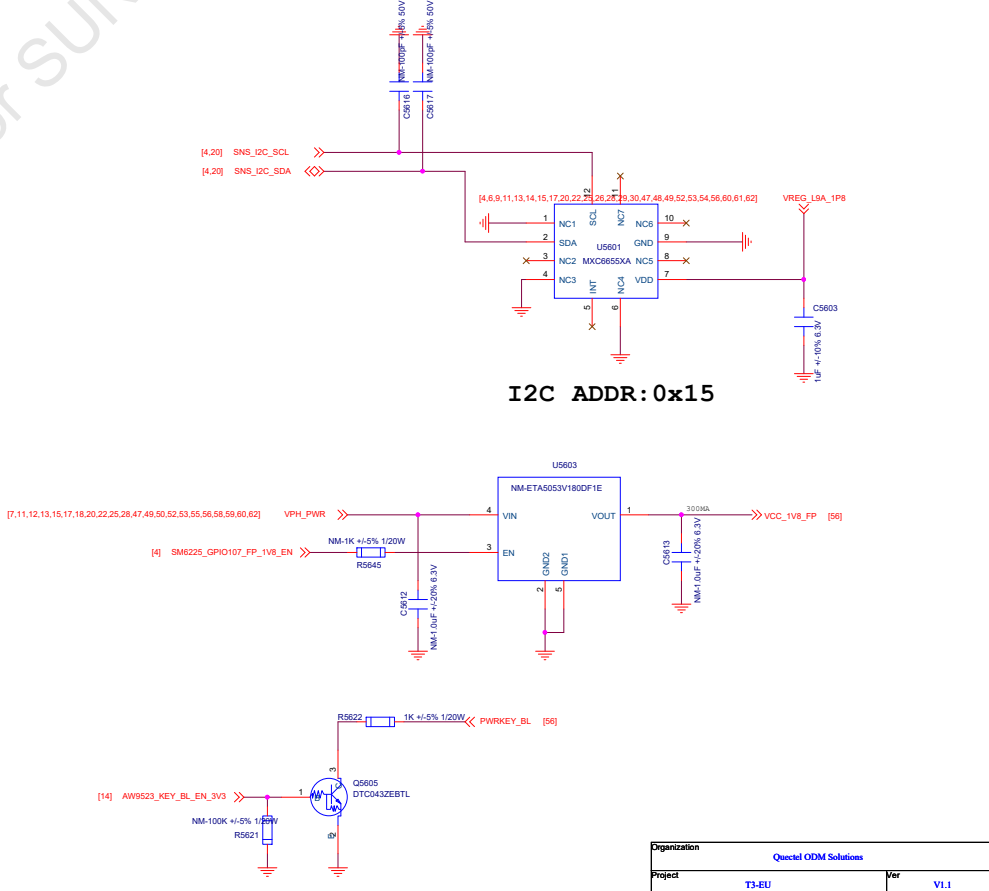
RGB LED



PWRKEY



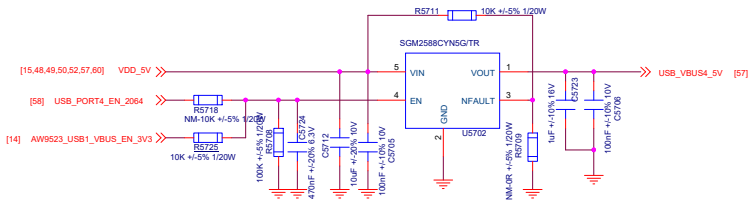
G-SENSOR



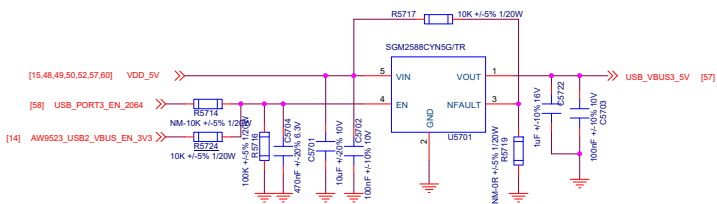
Organization	Quectel ODM Solutions		
Project	T3-EU	Ver	V1.1
Drawn By	Dengy	Checked By	Hosoon
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USB CON

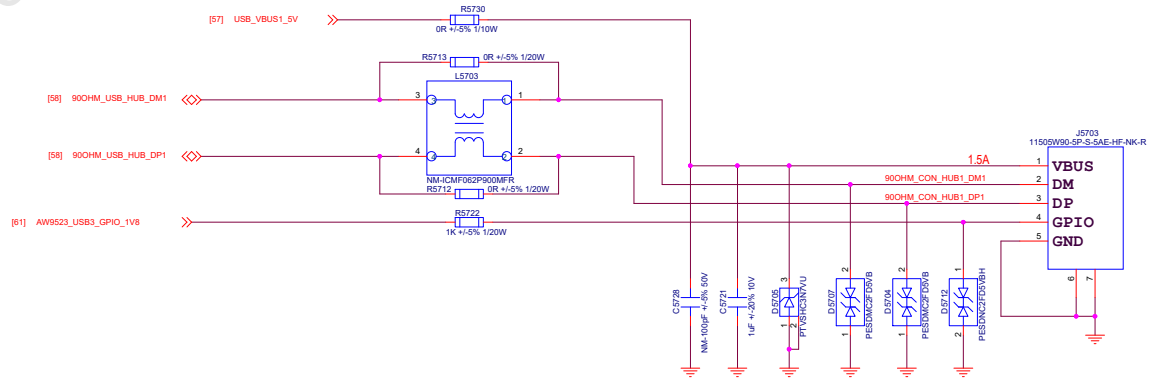
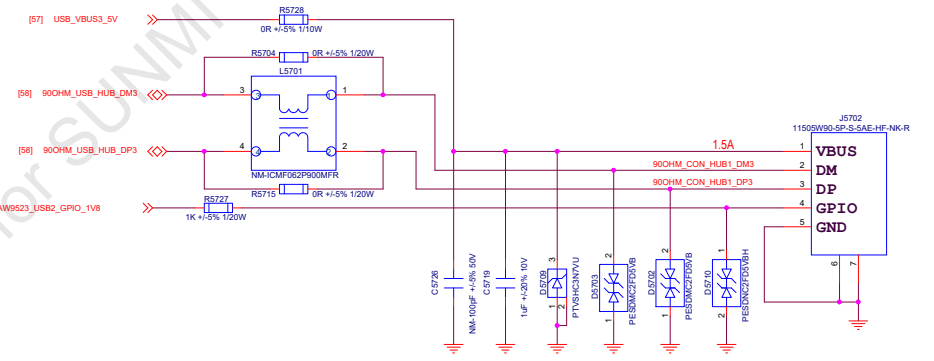
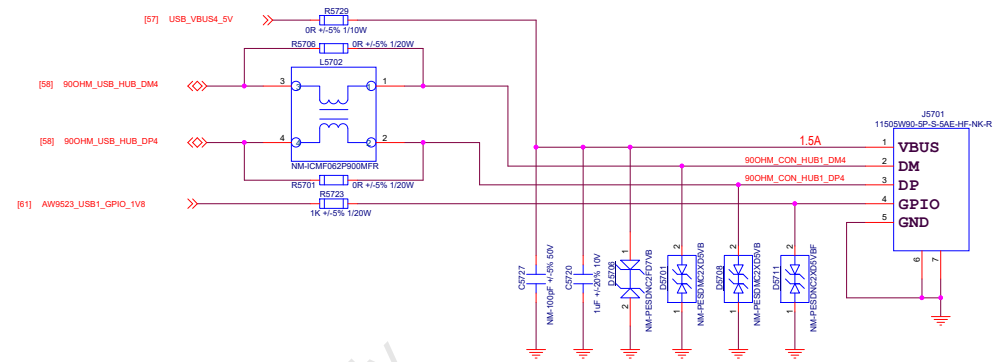
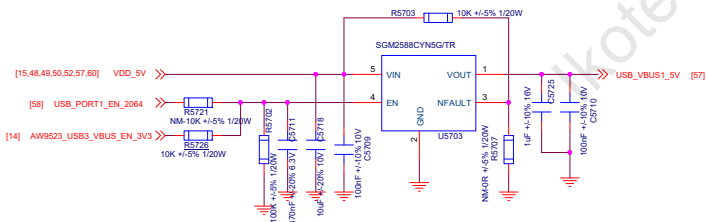
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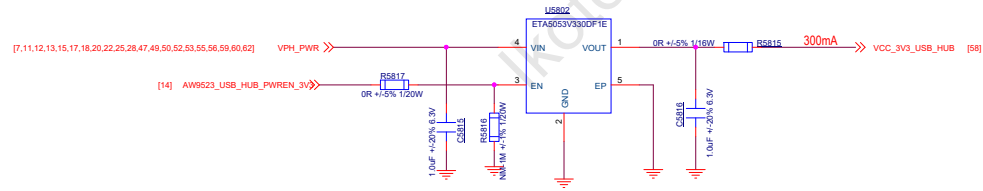
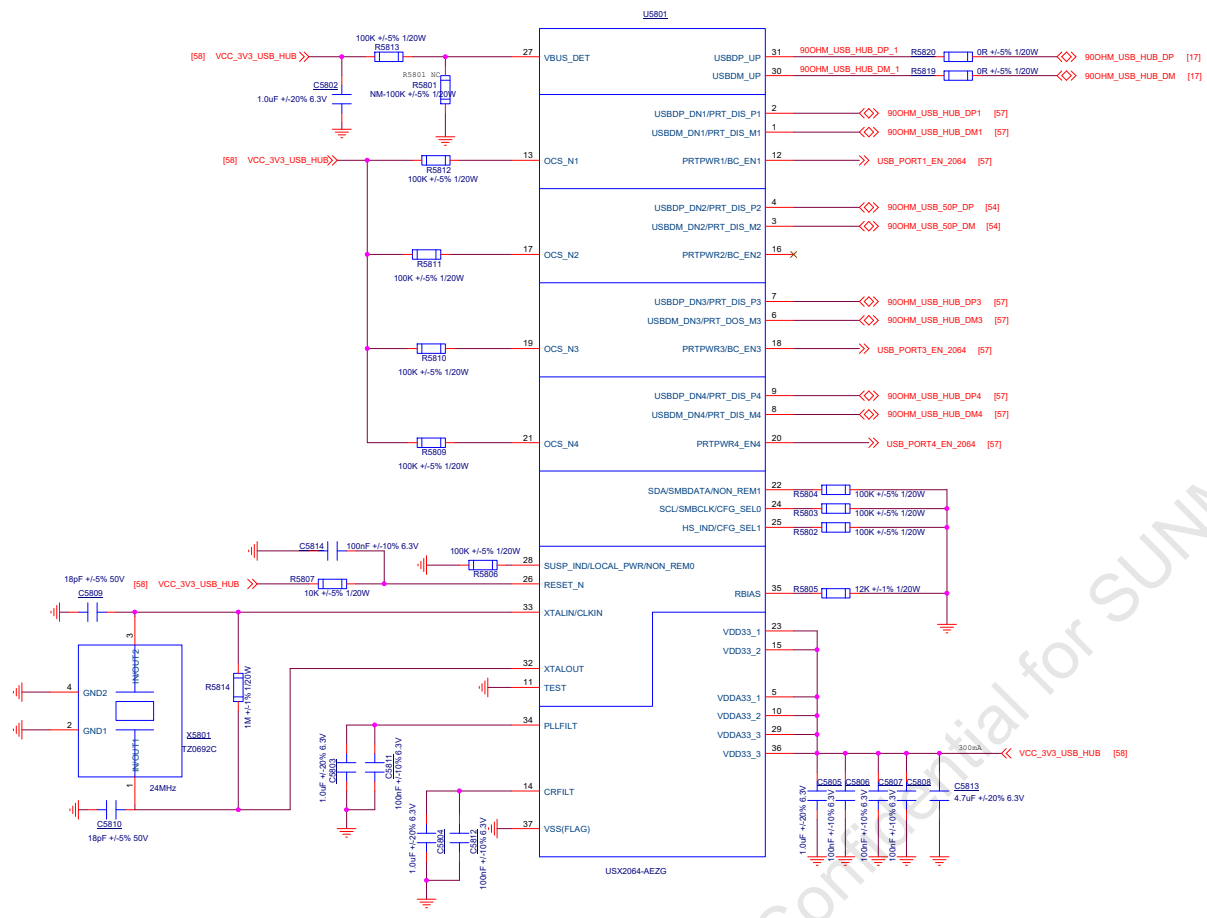
USB2_VBUS_OCP



USB3_VBUS_OCP

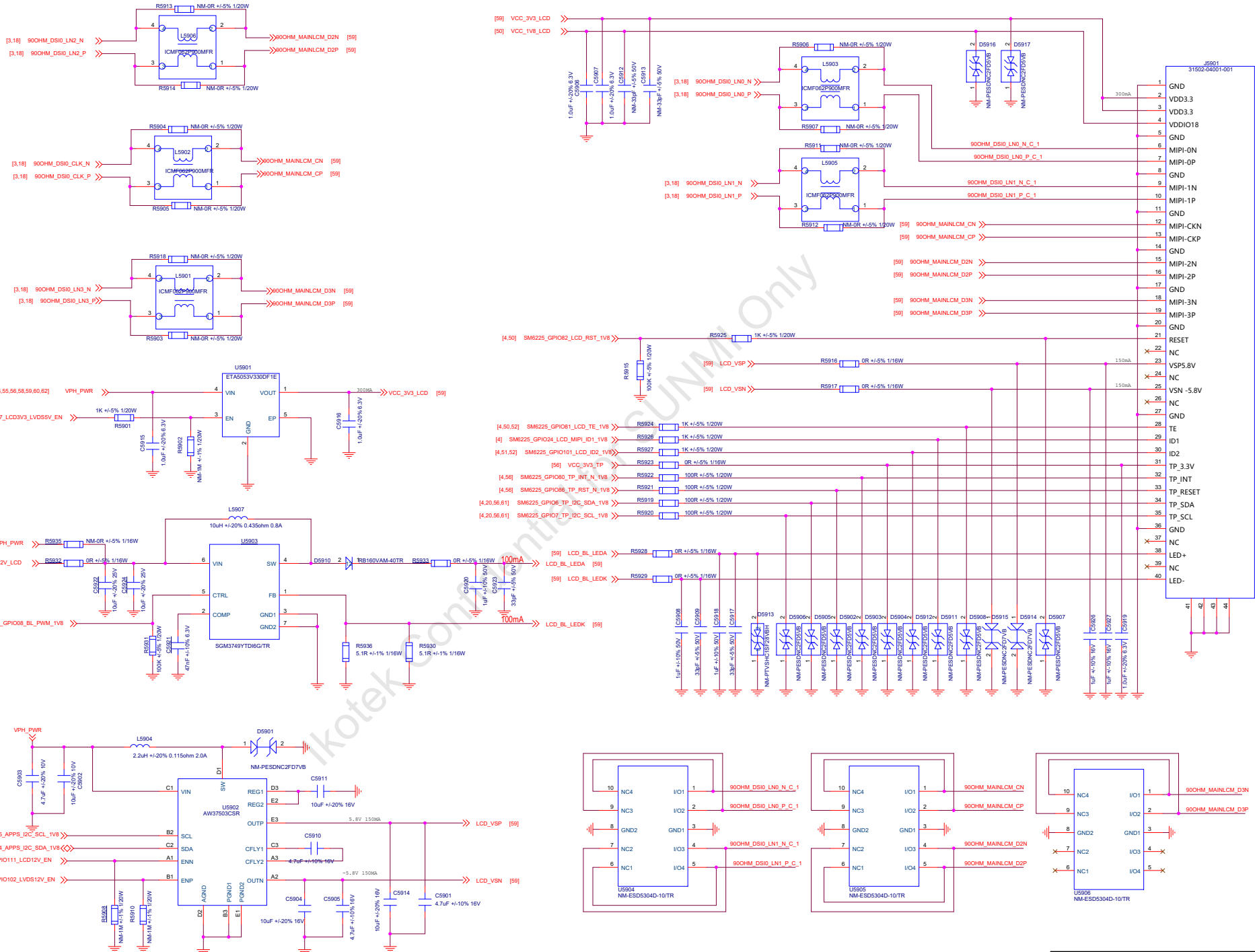


Organization	Quectel ODM Solutions		
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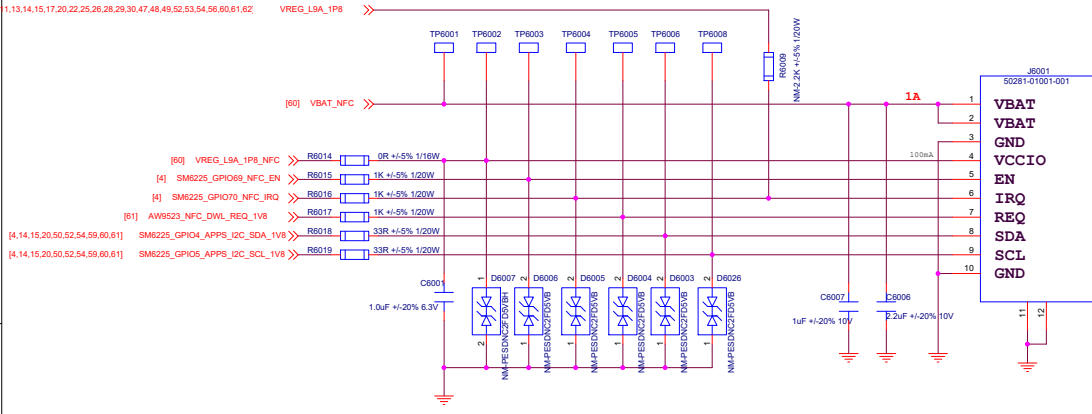
Organization	Quectel ODM Solutions		
Project	T3-EU	Ver	V1.1
Drawn By	Dongy	Checked By	Hosoon
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MIPI LCM

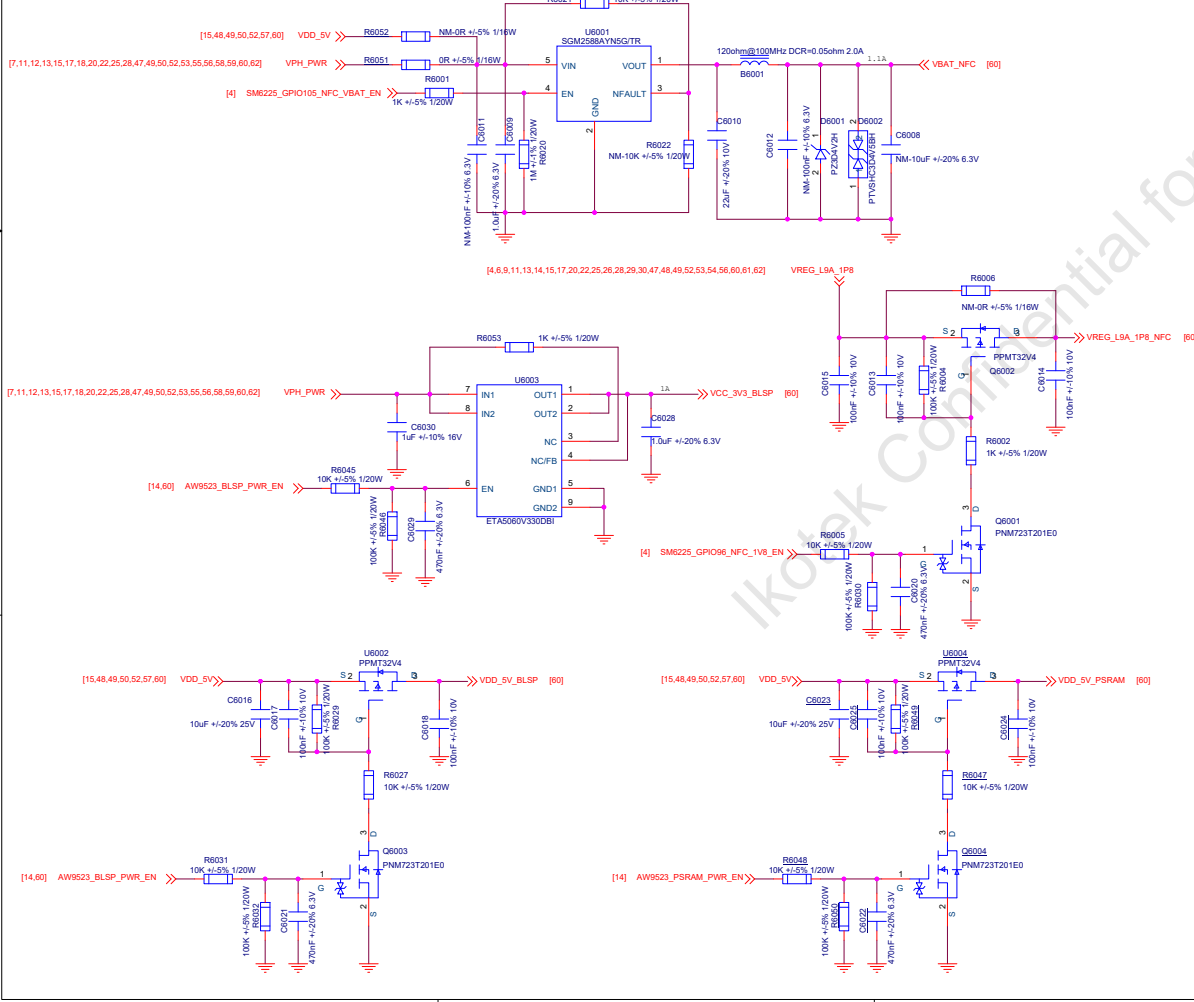


Organization			
Quectel ODM Solutions			
Project	T3-EU	Ver	V1.1
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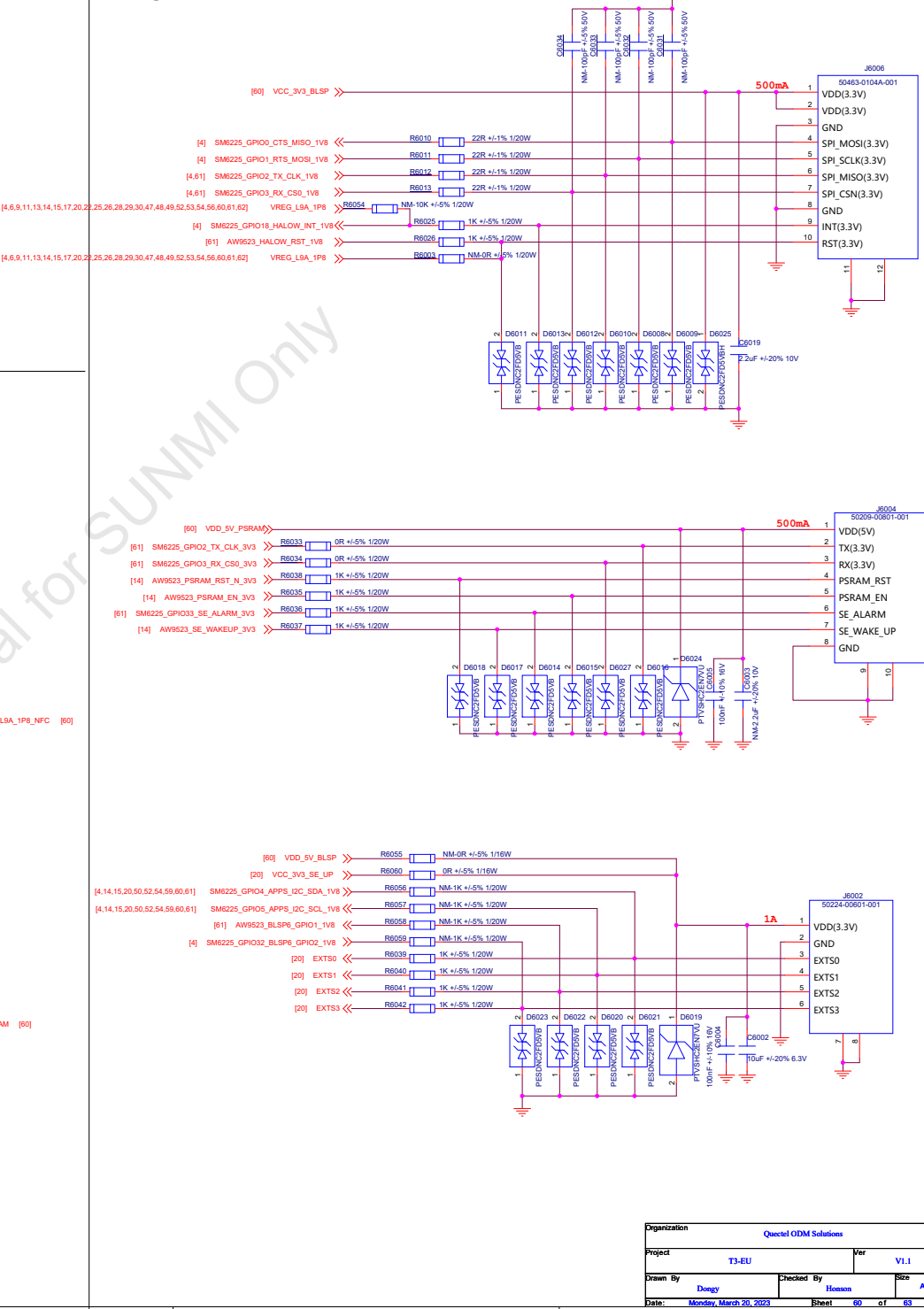
NFC



NFC POWER

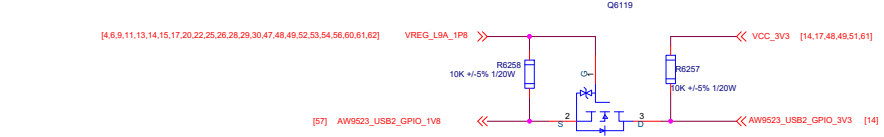
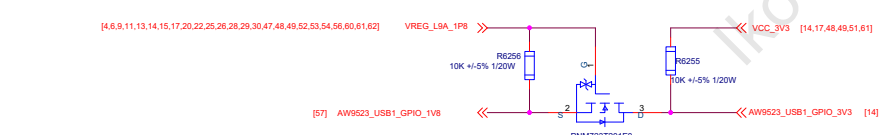
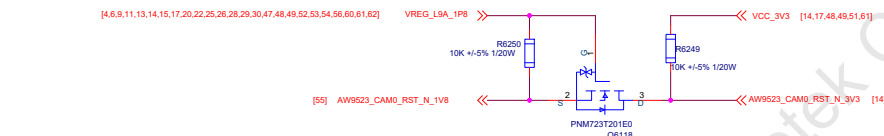
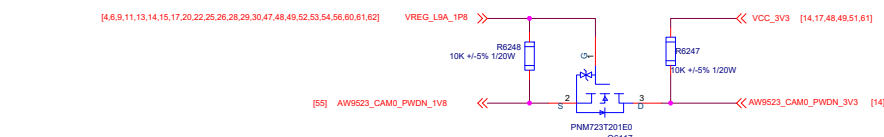
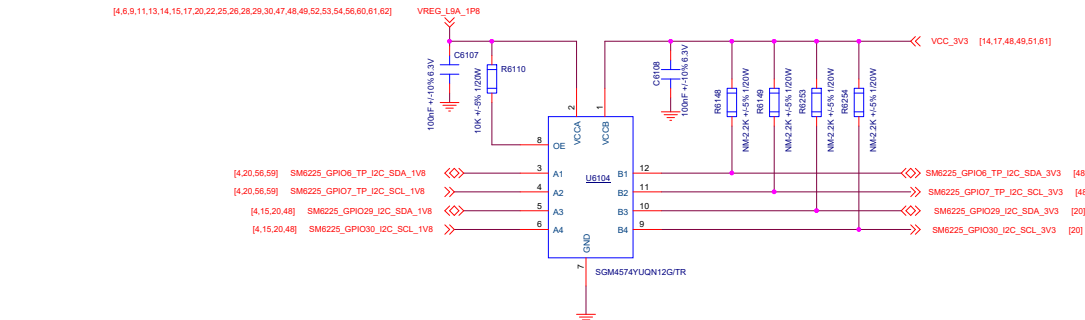
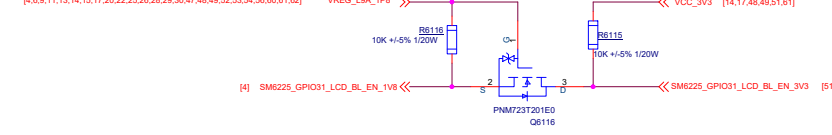
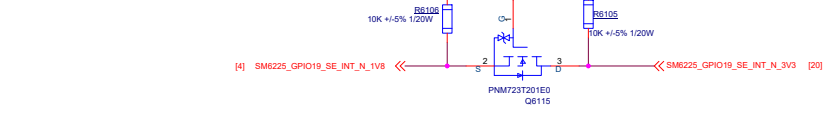
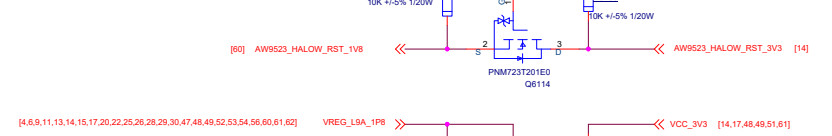
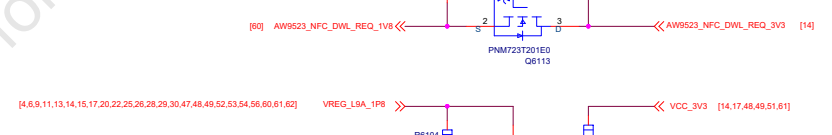
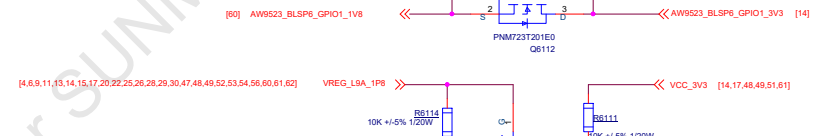
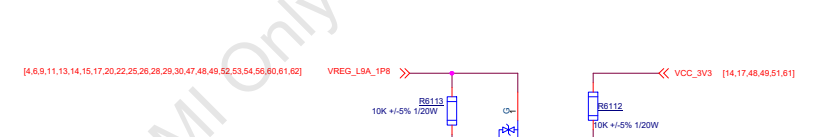
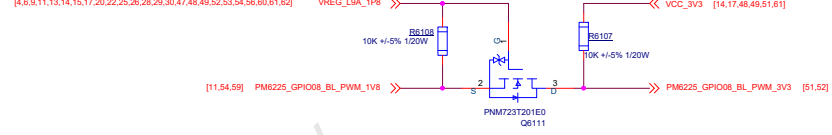
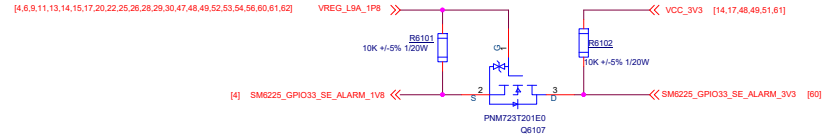
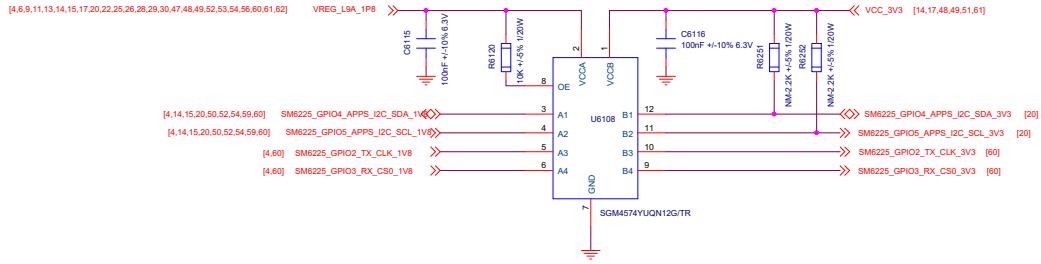


BLSP



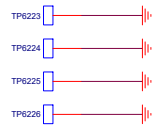
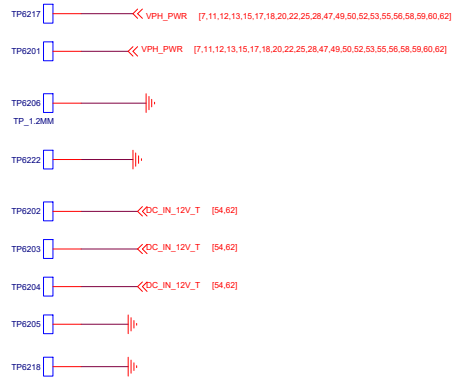
Organization				Quectel QDM Solutions
Project		T3-EU	Ver	V1.1
Drawn By	Dongy	Checked By	Hosam	Size
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QUP[0]

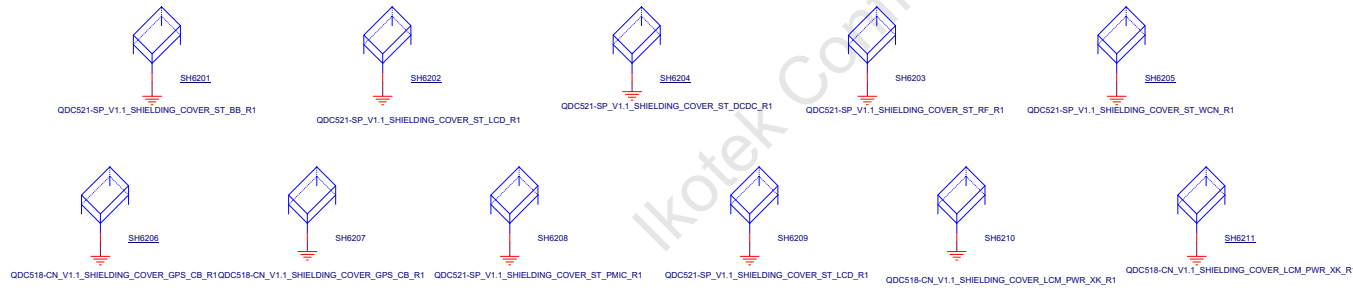


Organization	Quectel ODM Solutions		
Project	T3-EU	Ver	V1.1
Drawn By	Dongy	Checked By	Houwen
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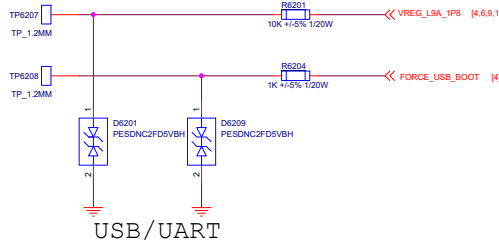
POWER



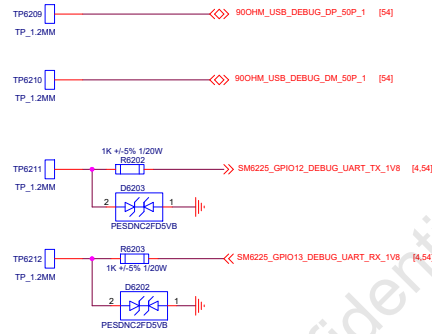
屏蔽罩



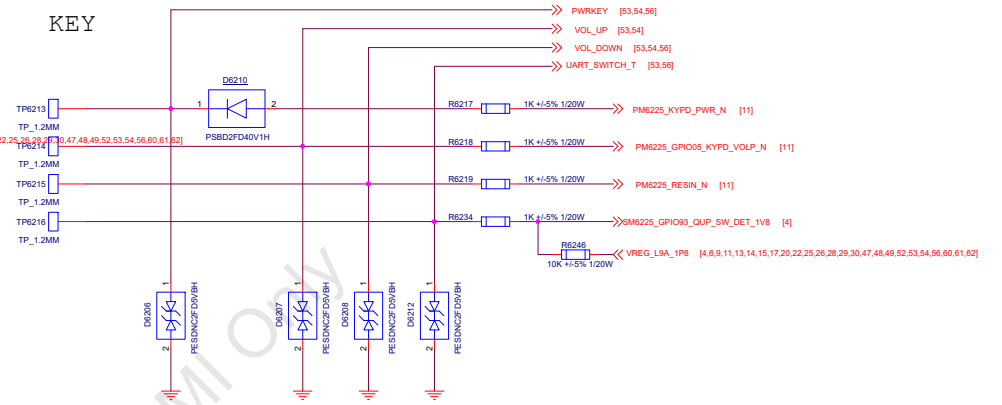
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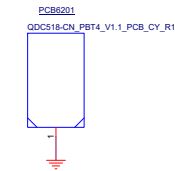
USB/UART



KEY



PCB

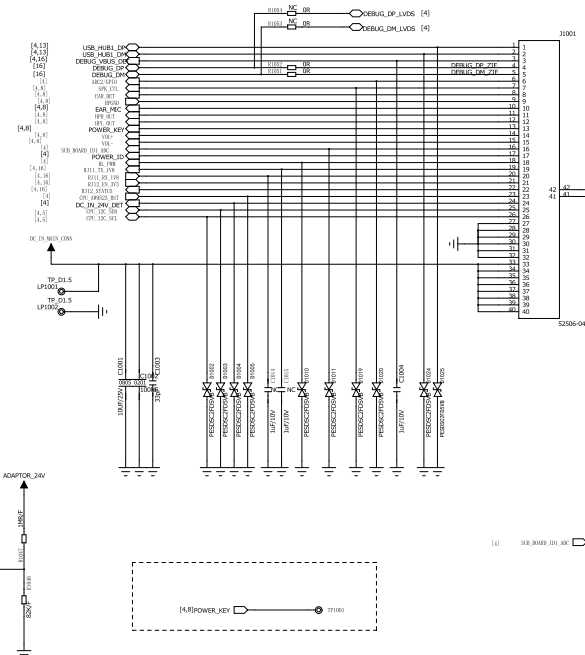
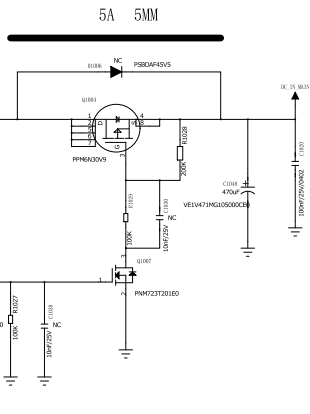
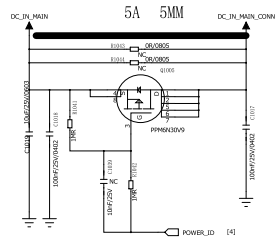
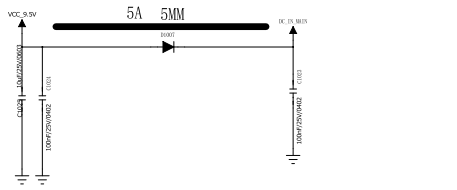


HOLE

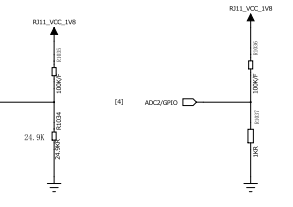
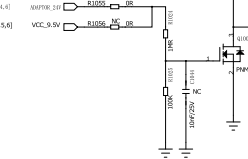
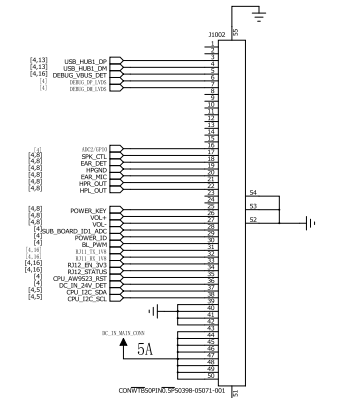


IO CONNECT

REVISION RECORD			
LTR	ECO NO.	APPROVED	DATE



Pin	Signal
1	USB_HUB1_DP
2	USB_HUB1_DM
3	DC_IN_MAIN_VCC
4	DC_IN_MAIN_GND
5	DC_IN_MAIN_DET
6	POWER_LED
7	VBAT
8	VBAT_GND
9	VBAT_DET
10	VBAT_DET_GND
11	VBAT_DET_VCC
12	VBAT_DET_GND
13	VBAT_DET_VCC
14	VBAT_DET_GND
15	VBAT_DET_VCC
16	VBAT_DET_GND
17	VBAT_DET_VCC
18	VBAT_DET_GND
19	VBAT_DET_VCC
20	VBAT_DET_GND
21	VBAT_DET_VCC
22	VBAT_DET_GND
23	VBAT_DET_VCC
24	VBAT_DET_GND
25	VBAT_DET_VCC
26	VBAT_DET_GND
27	VBAT_DET_VCC
28	VBAT_DET_GND
29	VBAT_DET_VCC
30	VBAT_DET_GND
31	VBAT_DET_VCC
32	VBAT_DET_GND
33	VBAT_DET_VCC
34	VBAT_DET_GND
35	VBAT_DET_VCC
36	VBAT_DET_GND
37	VBAT_DET_VCC
38	VBAT_DET_GND
39	VBAT_DET_VCC
40	VBAT_DET_GND
41	VBAT_DET_VCC
42	VBAT_DET_GND
43	VBAT_DET_VCC
44	VBAT_DET_GND
45	VBAT_DET_VCC
46	VBAT_DET_GND
47	VBAT_DET_VCC
48	VBAT_DET_GND
49	VBAT_DET_VCC
50	VBAT_DET_GND
51	VBAT_DET_VCC
52	VBAT_DET_GND
53	VBAT_DET_VCC
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55	VBAT_DET_VCC
56	VBAT_DET_GND
57	VBAT_DET_VCC
58	VBAT_DET_GND
59	VBAT_DET_VCC
60	VBAT_DET_GND
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63	VBAT_DET_VCC
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77	VBAT_DET_VCC
78	VBAT_DET_GND
79	VBAT_DET_VCC
80	VBAT_DET_GND
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83	VBAT_DET_VCC
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86	VBAT_DET_GND
87	VBAT_DET_VCC
88	VBAT_DET_GND
89	VBAT_DET_VCC
90	VBAT_DET_GND
91	VBAT_DET_VCC
92	VBAT_DET_GND
93	VBAT_DET_VCC
94	VBAT_DET_GND
95	VBAT_DET_VCC
96	VBAT_DET_GND
97	VBAT_DET_VCC
98	VBAT_DET_GND
99	VBAT_DET_VCC
100	VBAT_DET_GND



D

C

B

A

D

C

B

A

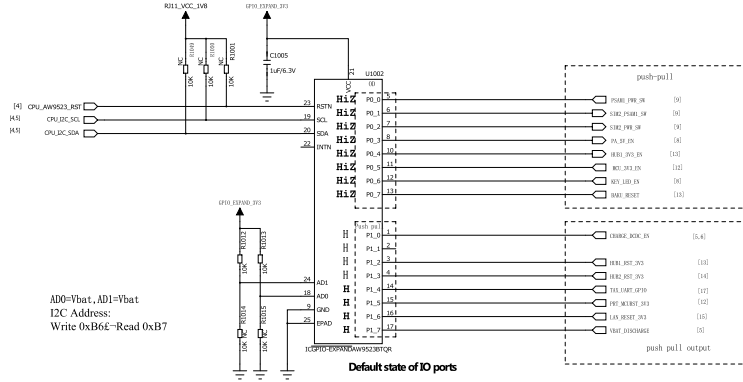
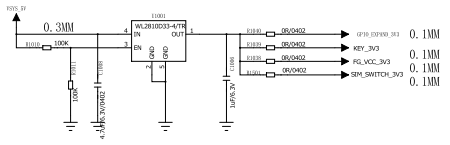


Table 1. Default state of IO ports, AD1/AD0 and P0_x/P1_x

ADD	ADD	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0	P0_6	P0_5	P0_4	P0_3	P0_2	P0_1	P0_0
GND	GND	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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AWINIC 上海艾为电子技术有限公司 AW9523B datasheet May 2016 V1.1.1

ADD	VBAT	GND	0	0	0	0	1	1	1	1	0	0	0	0	HZ	HZ	HZ
VBAT	GND	1	1	1	1	1	0	0	0	0	HZ	HZ	HZ	HZ	0	0	0
VBAT	VBAT	1	1	1	1	1	1	1	1	1	HZ	HZ	HZ	HZ	HZ	HZ	HZ

AD0=Vbat, AD1=Vbat
I2C Address:
Write 0xB6-Read 0xB7

Default state of IO ports

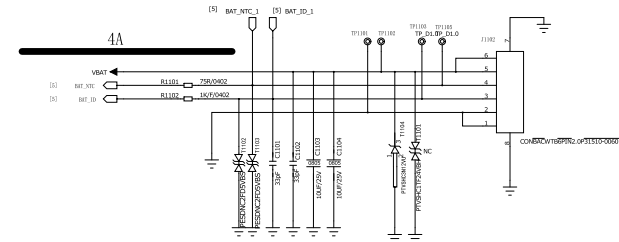
1	0	1	1	0	AD1	AD0	R/W
---	---	---	---	---	-----	-----	-----

AD1/AD0 value match with AW9523B pin AD1/AD0 respectively

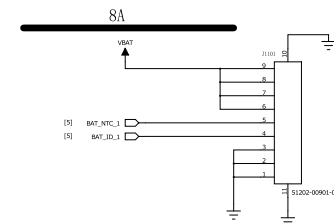
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CHECKED: <Checked By>		DATED: <Checked Date>		TITLE: Luxembourg	
QUALITY CONTROL: <QC By>		DATED: <QC Date>		CODE: <Code>	SIZE: A01. BLOCK DIAGRAM
RELEASED: <Released By>		DATED: <Release Date>		SCALE: <Scale>	DRAWING NO: 12.0.C
				SHEET: 4P 18	

REVISION RECORD		
LTR	ECO NO:	APPROVED: DATE:

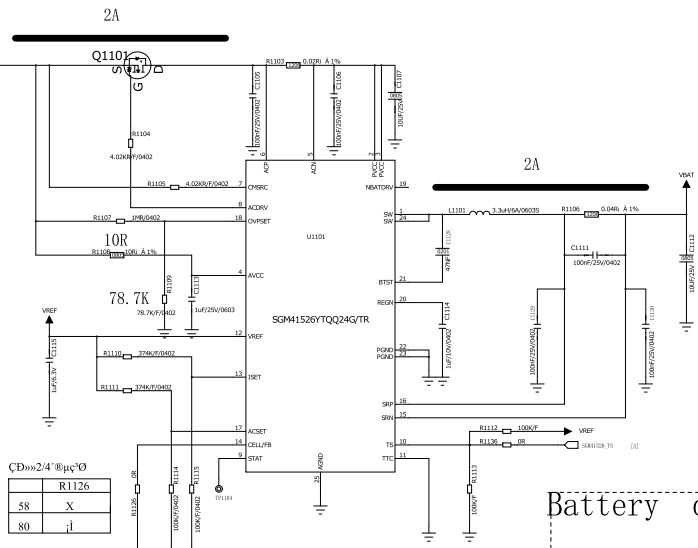
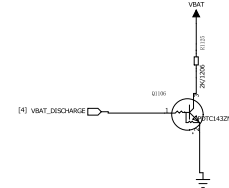
58 Battery CON



80 Battery CON



Battery discharge

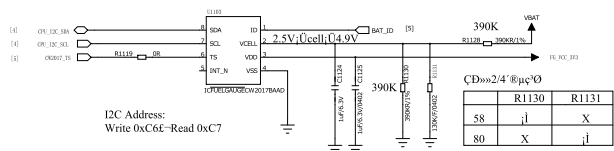


CD»»2'4'@µs'0

CELL Pin Voltage	Charge Voltage Regulation
Floating	8.8V (2 Cells)
VREF	12.8V (3 Cells)
AGND	16.8V (4 Cells)

58	80
X	i
i	X

Fuel Gauge



I2C Address:
Write 0xC6E-Read 0xC7

CD»»2'4'@µs'0

58	80
i	X
X	i

Logic Level (SEL pin, Pin 6)	Function
L	B0 connected to A
H	B1 connected to A

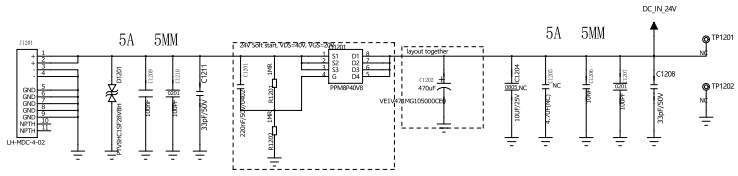
COMPANY: Sunmi

TITLE: Luxembourg

DRAWN: ZMQ	DATED: 23.02.27	CODE:	SIZE:	DRAWING NO:	REV:
CHECKED: <Checked By>	DATED: <Checked Date>	<Code>	A01.BLOCK DIAGRAM	2.0.C	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	<Scale>			
RELEASED: <Released By>	DATED: <Release Date>				

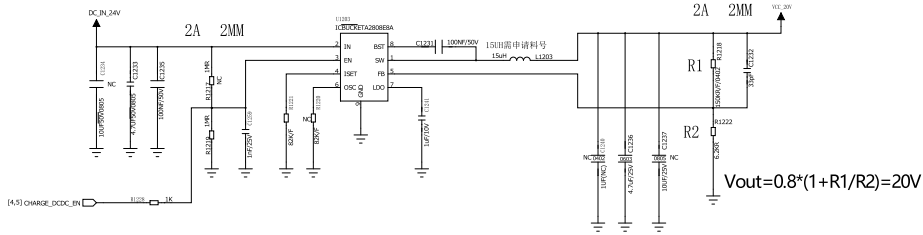
SHEET: 5P 18

24V DCIN

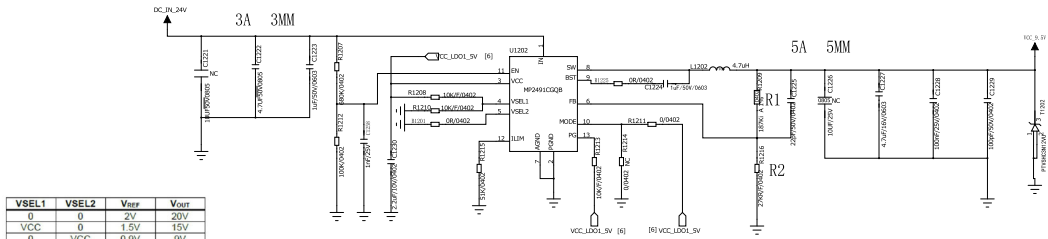


Reference FTP: DC-IN_STD_SCH_V1.1_20221209

DCDC 24V-20V 3A



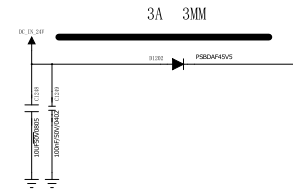
DCDC 24V-9.5V 6A



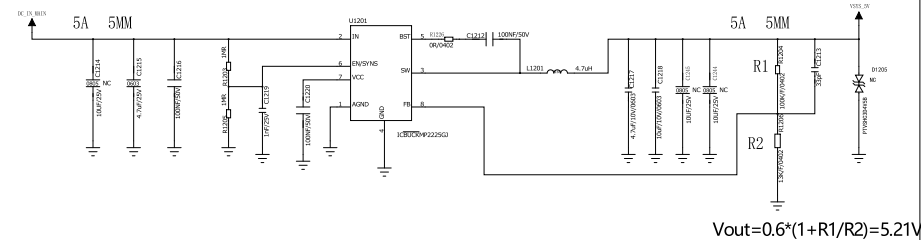
VSEL1	VSEL2	Vref	Vout
0	0	2V	20V
VCC	0	1.5V	15V
0	VCC	0.9V	9V
1/2*VCC	0	1.2V	12V
VCC	VCC	0.5V	5V

Reference FTP: Manila_MB_SCH_V1.0.A_20220826-1536

REVISION RECORD			
LTR	ECD NO.	APPROVED:	DATE

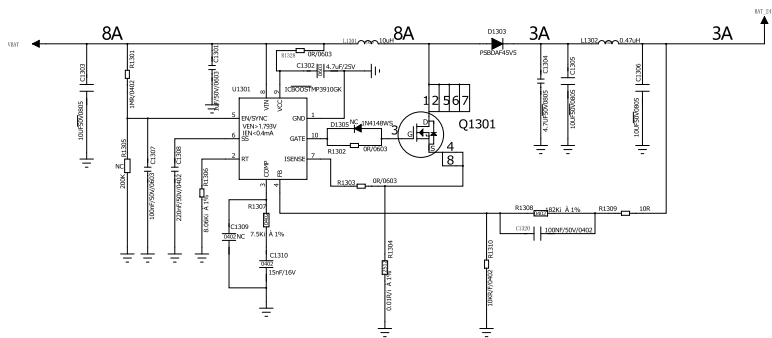


DCDC VBAT/9.5V - 5V 5A



COMPANY:		Sunmi			
TITLE:		Luxembourg			
DRAWN:	ZMQ	DATED:	23.02.27	CODE:	
CHECKED:	<Checked By>	DATED:	<Checked Date>	SIZE:	
QUALITY CONTROL:	<QC By>	DATED:	<QC Date>	DRAWING NO.:	A01.BLOCK DIAGRAM 2.0.C
RELEASED:	<Released By>	DATED:	<Release Date>	SCALE:	
				SHEET:	6P 18

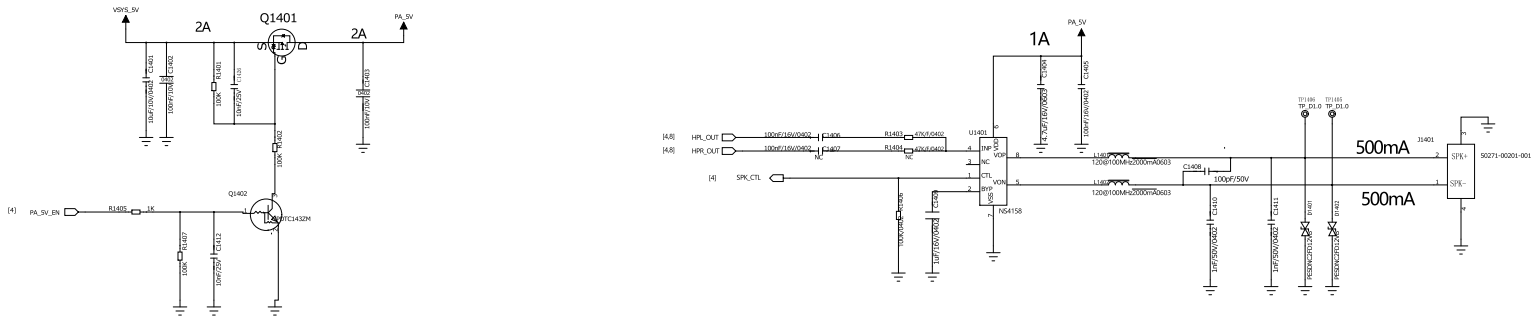
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LTR	ECD NO.	APPROVED	DATE



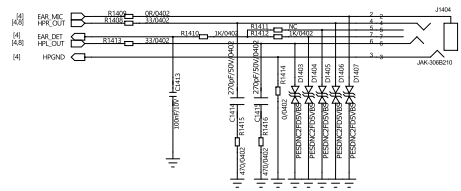
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TITLE:		Luxembourg			
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CHECKED:	<Checked By>	DATE:	<Checked Date>	SIZE:	
QUALITY CONTROL:	<QC By>	DATE:	<QC Date>	DRAWING NO.:	A01.BLOCK DIAGRAM 2.0.C
RELEASED:	<Released By>	DATE:	<Release Date>	SCALE:	
					SHEET: 7 of 18

REVISION RECORD			
LTR	ECC NO.	APPROVED	DATE

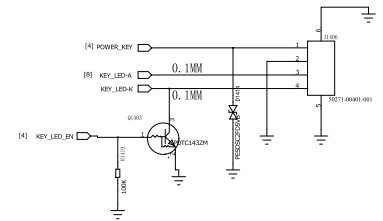
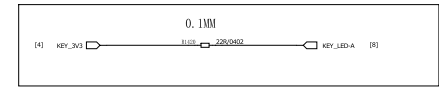
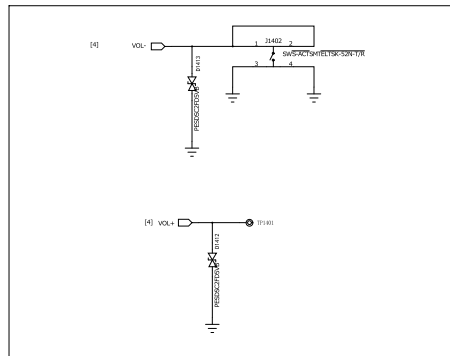
Audio PA



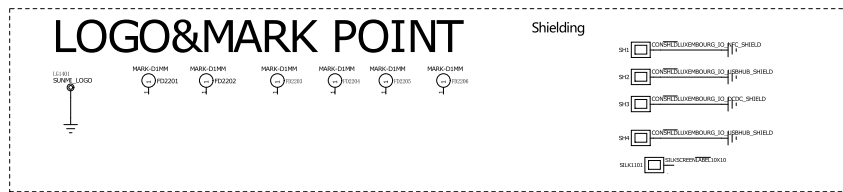
Audio JACK



KEY



LOGO&MARK POINT

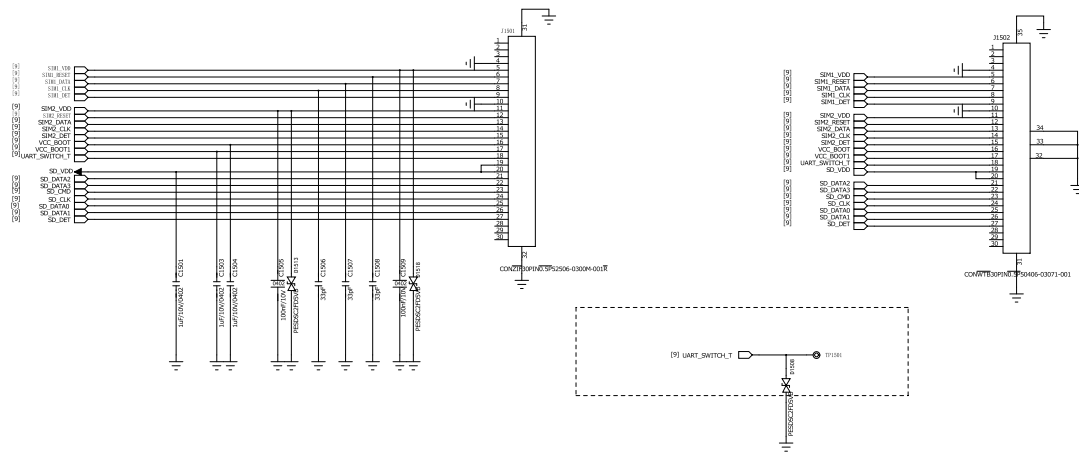


COMPANY: Sunmi			
TITLE: Luxembourg			
DRAWN: ZMQ	DATE: 23.02.27	CODE: <Code>	SIZE: A01. BLOCK DIAGRAM 2.0.C
CHECKED: <Checked By>	DATE: <Checked Date>	QUALITY CONTROL: <QC By>	DATE: <QC Date>
RELEASED: <Released By>	DATE: <Release Date>	SCALE: <Scale>	SHEET: 8P 18

ZIF

LVDS

REVISION RECORD			
LTR	ECD NO.	APPROVED	DATE



序号	定义	电压
1	POWERKEY	1.8V
2	VOL+	1.8V
3	VOL-	1.8V
4	GNID	1.8V
5	SIM1_VDD	1.8V
6	SIM1_RESET	1.8V
7	SIM1_DATA	1.8V
8	SIM1_CLK	1.8V
9	SIM1_DET	1.8V
10	GNID	1.8V
11	SIM2_VDD	1.8V
12	SIM2_RESET	1.8V
13	SIM2_DATA	1.8V
14	SIM2_CLK	1.8V
15	SIM2_DET	1.8V
16	VCC_BOOT	1.8V
17	VCC_BOOT	1.8V
18	GPIO——OUP——Switch	1.8V
19	SDCARD_VDD	1.8V
20	SDCARD_VDD	1.8V
21	SDCARD_DS	1.8V
22	SDCARD_DS	1.8V
23	SDCARD_CMD	1.8V
24	SDCARD_CLK	1.8V
25	SDCARD_DS	1.8V
26	SDCARD_DS	1.8V
27	SDCARD_DET	1.8V
28	DEBUG_VBUS1	1.8V
29	USB_DEBUG_D-	1.8V
30	USB_DEBUG_D+	1.8V

开机键 and 音量-键连FASTBOOT

主板预留开机电路，
通过通用IO兼容CBL开机电路方式

主板上点 硬件电路的焊点 (核心板上设计POWER
+ 音量键 VBAT
基于CPU的GPIO和UART的切换, 主板预留测试

16 37pin 连接在一起, 则可以通
过主机电路实现自动开机

返回

30PIN定义: LVDS连接

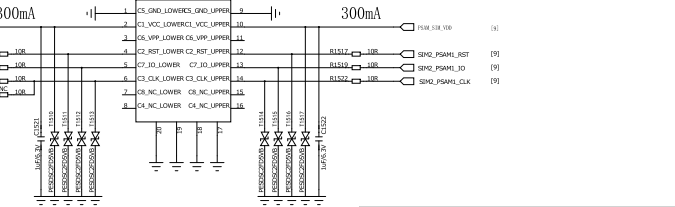
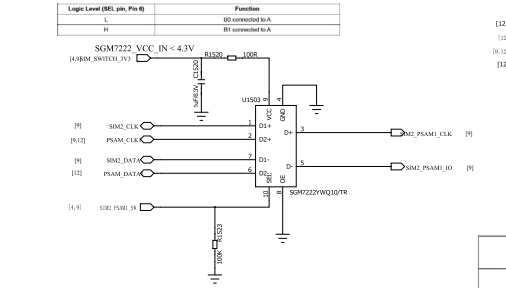
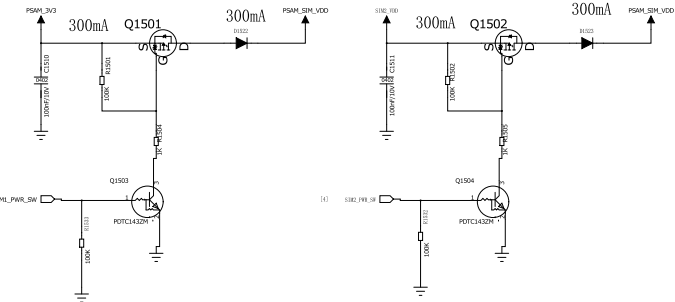
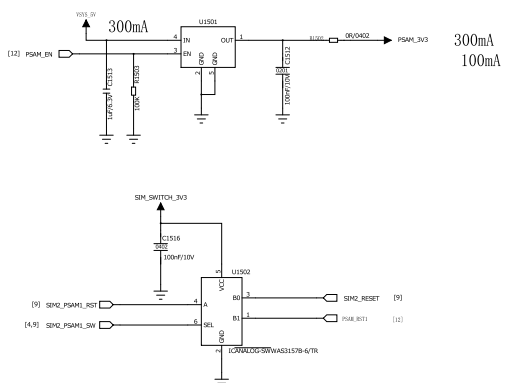
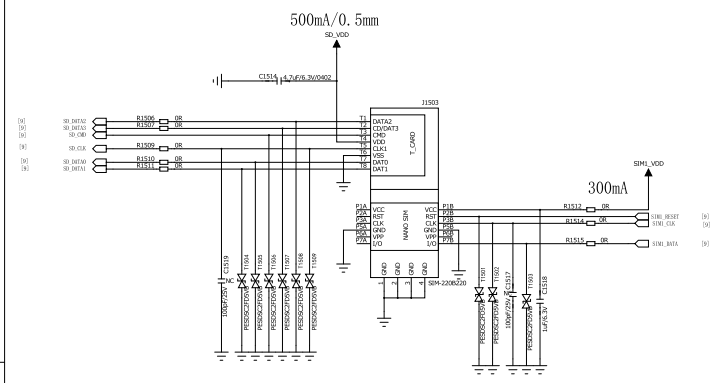
30PIN定义: ZIF连接

连接型号: S-50398-050

连接型号: 52506-0300M-001

T+SIM1

SIM2/PSAM1+PSAM2



OE	s	HSD1+ HSD1-	HSD2+ HSD2-
0	0	ON	OFF
0	1	OFF	ON
1	x	OFF	OFF

COMPANY: Sunmi

TITLE: Luxembourg

DRAWN: ZMQ DATED: 23.02.27

CHECKED: <Checked By> DATED: <Checked Date>

QUALITY CONTROL: <QC By> DATED: <QC Date>

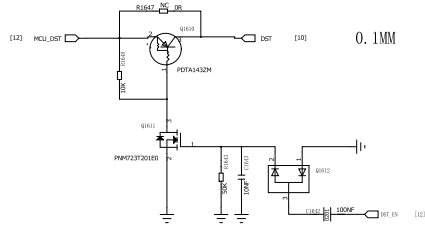
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CODE: <Code> SIZE: A01.BLOCK DIAGRAM 2.0.C

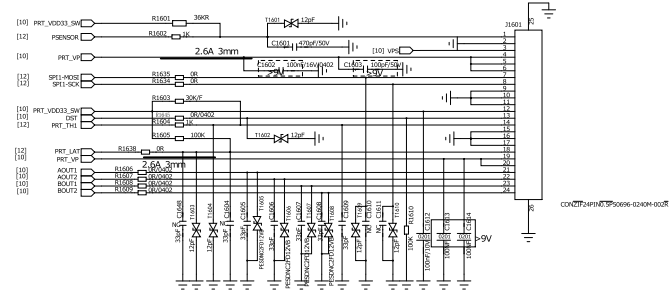
DRAWING NO. REV: 18

REVISION RECORD			
LTR	ECD NO.	APPROVED	DATE

D

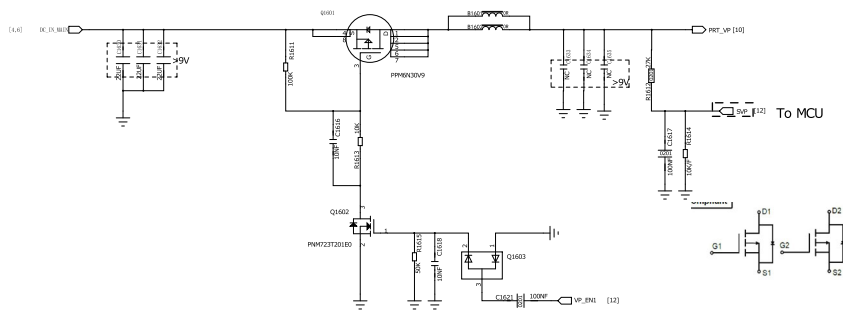


Printer connect

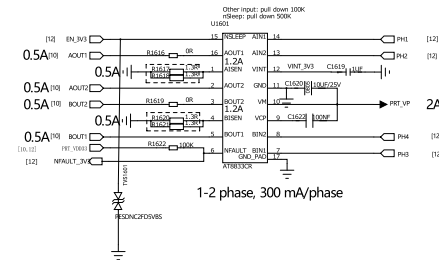


Printer Power

4A 4MM

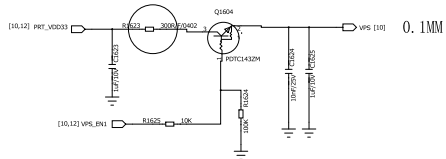


Printer MOTO Driver



Power for Sensor

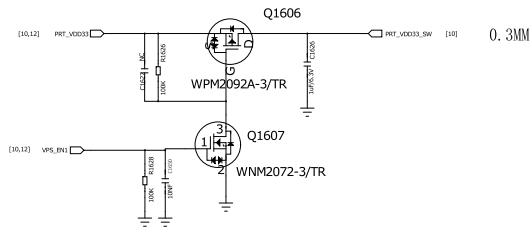
0.1MM



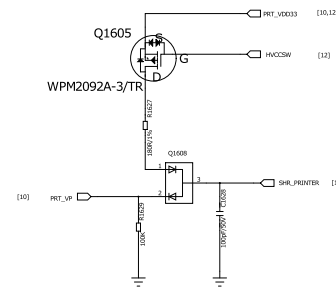
B

Printer VDD Supply Switch

0.3MM



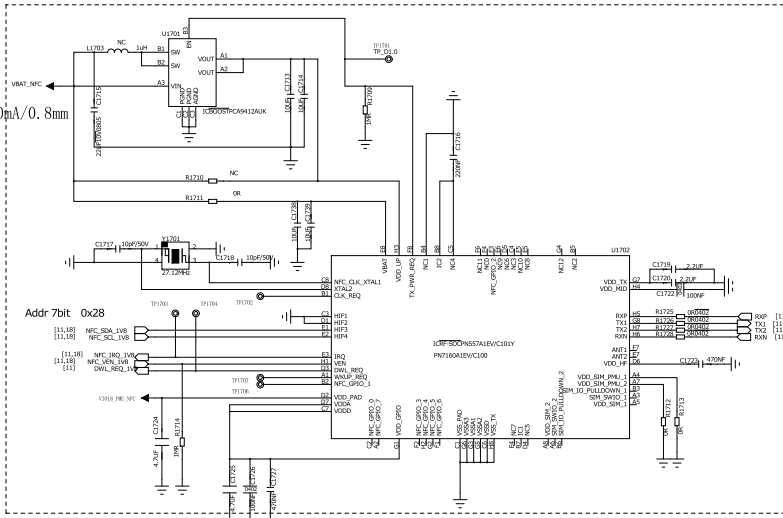
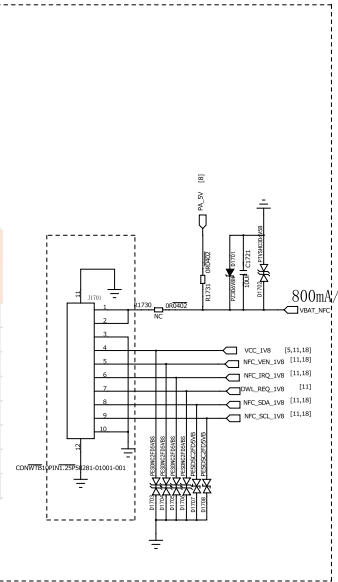
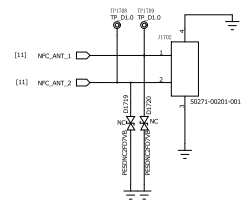
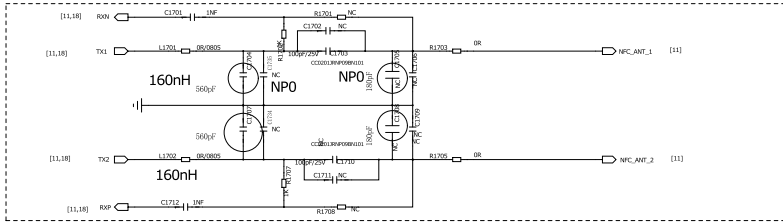
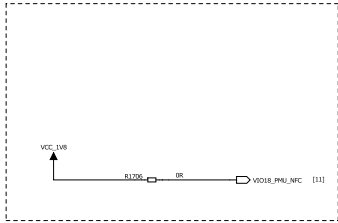
Printer Heating Dot Check



A

COMPANY: Sunmi				
TITLE: Luxembourg				
DRAWN: ZMQ	DATED: 23.02.27	CODE:	SIZE:	DRAWING NO:
CHECKED: <Checked By>	DATED: <Checked Date>	<Code>	A01. BLOCK DIAGRAM	REV: 2.0
QUALITY CONTROL: <QC By>	DATED: <QC Date>	<Scale>	SHEET: 10 18	
RELEASED: <Released By>	DATED: <Release Date>			

REVISION RECORD			
LTR	ECD NO.	APPROVED:	DATE



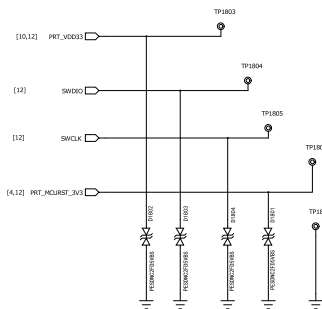
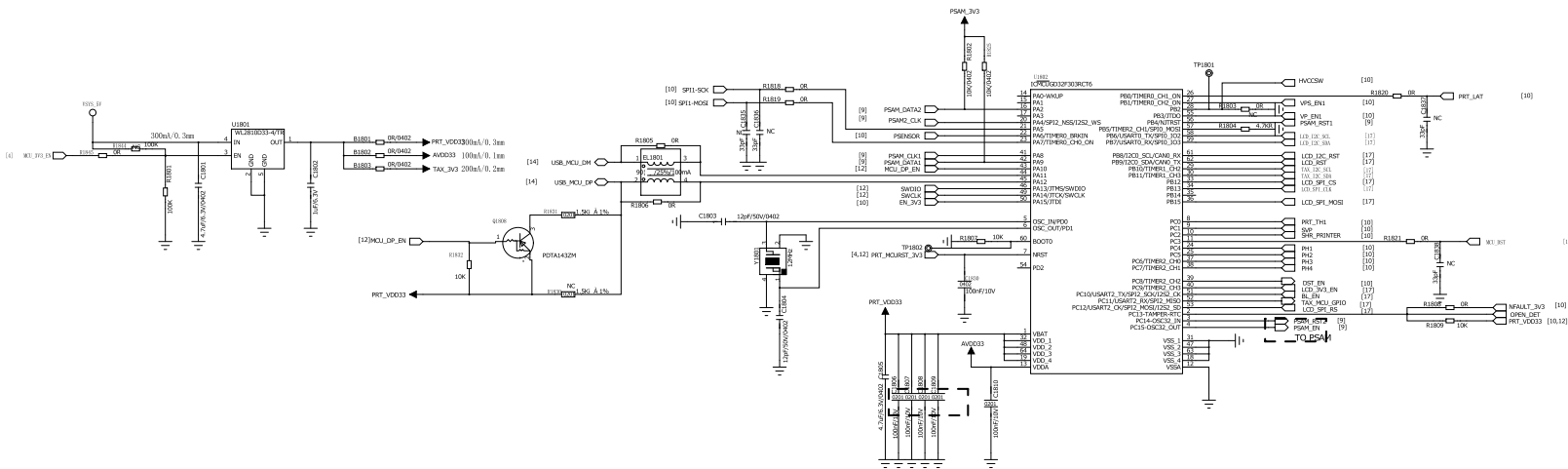
HIF2	HIF1	IIC_WRITE	IIC_READ
0	0	0x50	0x51
0	1	0x52	0x53
1	0	0x54	0x55
1	1	0x56	0x57

序号	定义	
1	VBAT(3.6V-4.2V)	开关、延时电路, 1A
2	VBAT(3.6V-4.2V)	开关、延时电路, 1A
3	GND	
4	1.8V_VCCIO	1.8V
5	NFC_EN	1.8V
6	NFC_IRQ	1.8V
7	DWL_REQ	1.8V
8	IIC_SDA	1.8V
9	IIC_SCL	1.8V
10	GND	

COMPANY: Sunmi			
TITLE: Luxembourg			
DRAWN: ZMQ	DATE: 23.02.27		
CHECKED: <Checked By>	DATE: <Checked Date>	CODE: <Code>	SIZE: A01. BLOCK DIAGRAM 2.0.C
QUALITY CONTROL: <QC By>	DATE: <QC Date>		
RELEASED: <Released By>	DATE: <Release Date>	SCALE: <Scale>	SHEET: 18 / 18

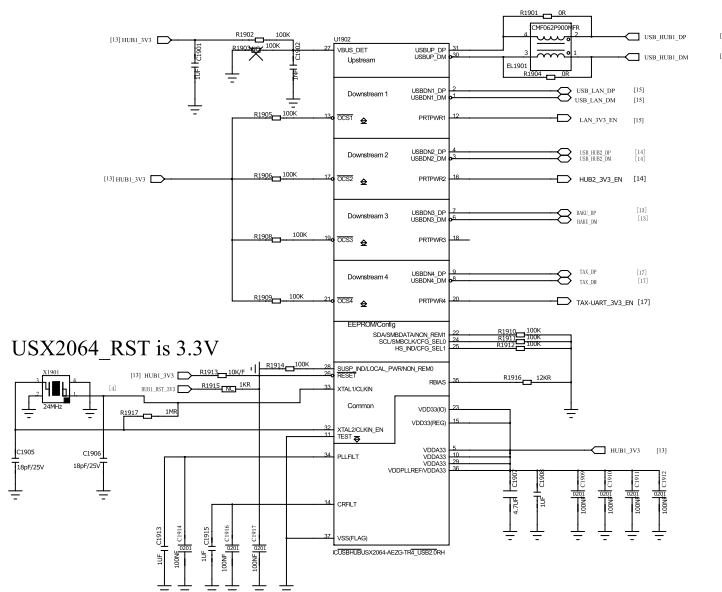
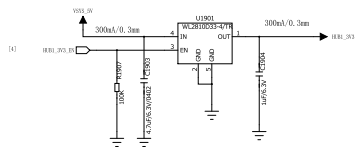
POWER

REVISION RECORD			
LTR	ECO NO.	APPROVED	DATE



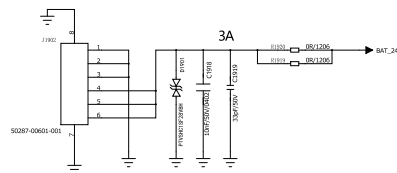
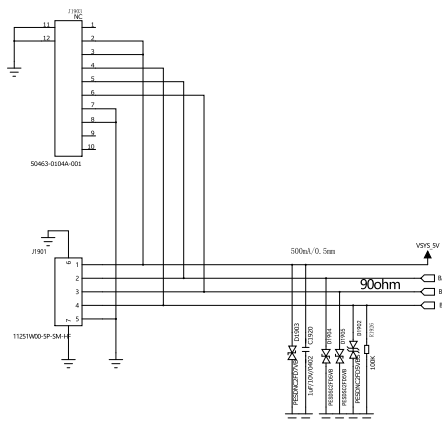
COMPANY: Sunmi			
TITLE: Luxembourg			
DRAWN: ZMQ	DATE: 23.02.27	CODE: <Code>	SIZE: A01. BLOCK DIAGRAM
CHECKED: <Checked By>	DATE: <Checked Date>	SCALE: <Scale>	DRAWING NO: 02.0.C
QUALITY CONTROL: <QC By>	DATE: <QC Date>		
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REVISION RECORD			
LTR	ECO NO.	APPROVED	DATE



USX2064_RST is 3.3V

BAKU connect

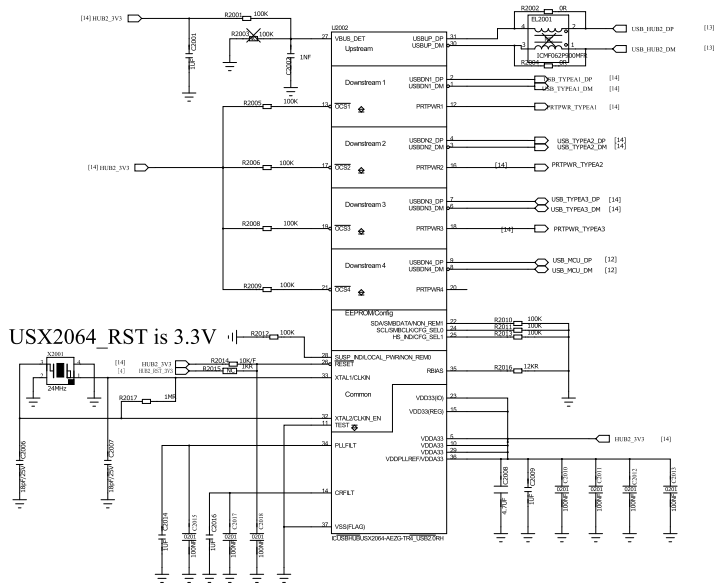
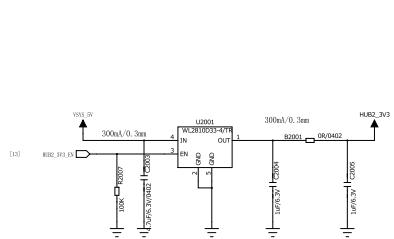


COMPANY:		Sunmi	
TITLE:		Luxembourg	
DRAWN:	ZMQ	DATE:	23.02.27
CHECKED:	<Checked By>	DATE:	<Checked Date>
QUALITY CONTROL:	<QC By>	DATE:	<QC Date>
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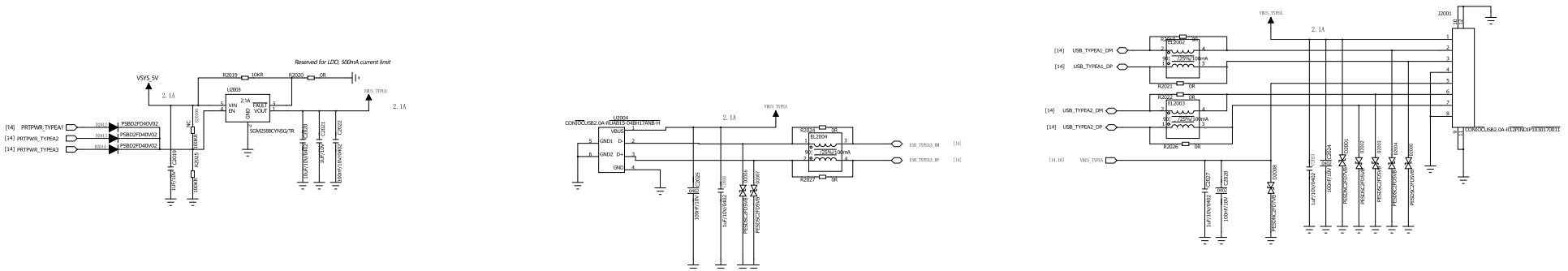
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REVISION RECORD		
LTR	ECC NO.	DATE



USX2064_RST is 3.3V

Double-deck TYPE-A

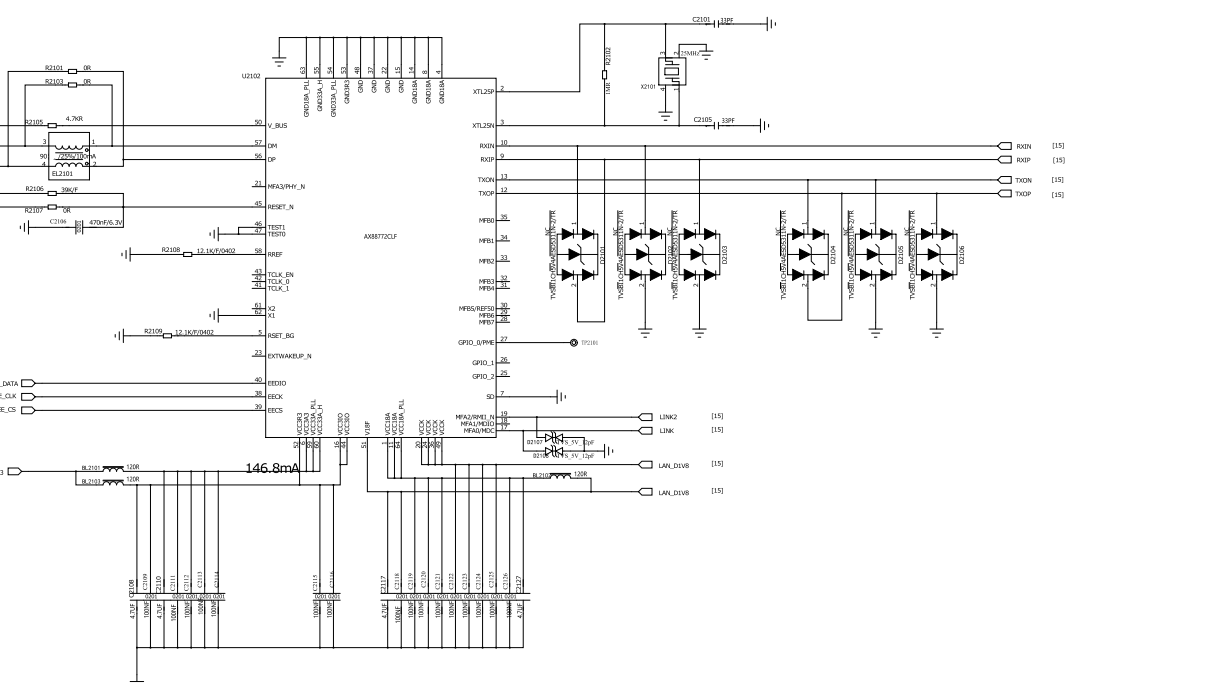
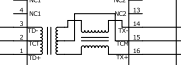
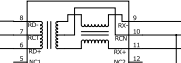
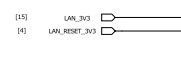
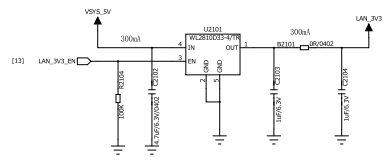


Reference FTP:USB2.0 interface and MOS switch circuit_V1.1
 Reference FTP:100M LAN_LAN9513_V1.1
 Reserve a GPIO to control reset signal
 Add Common-mode TVS

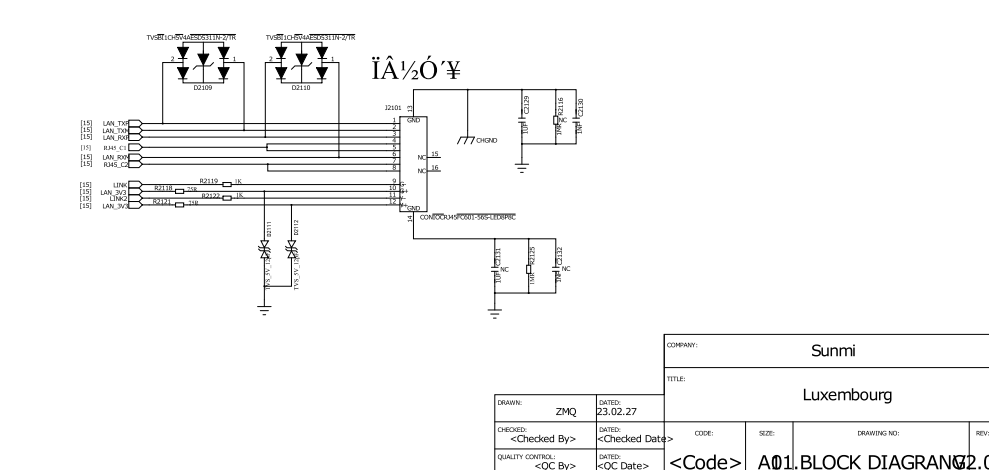
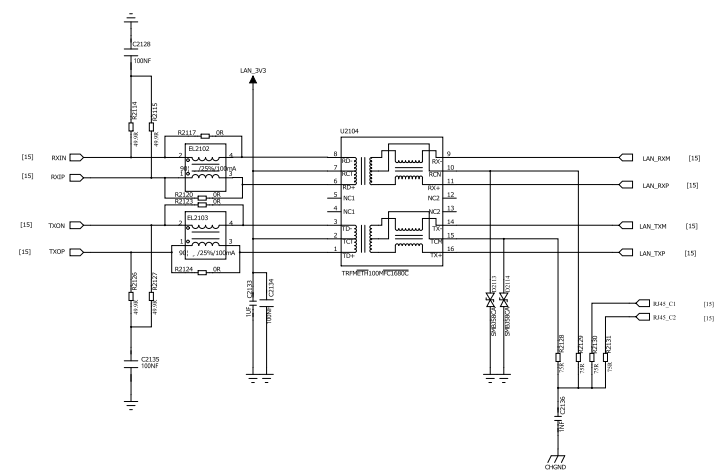
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CHECKED: <Checked By>		DATED: <Checked Date>		TITLE: Luxembourg	
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RELEASED: <Released By>		DATED: <Release Date>		SCALE: <Scale>	
SHEET: 14				18	

USB-LAN

REVISION RECORD			
LTR	ECO NO.	APPROVED	DATE



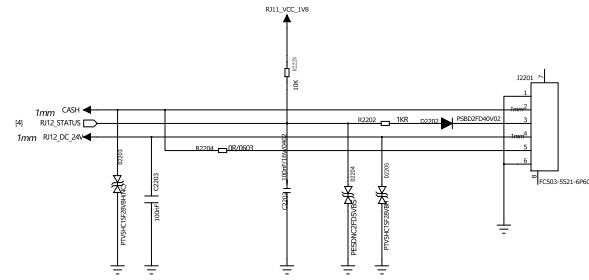
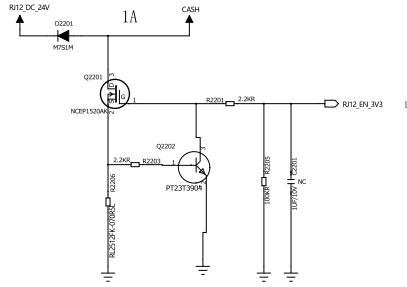
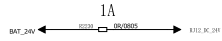
RJ45



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RELEASED: <Released By>		DATE: <Release Date>	
SCALE: <Scale>		SHEET: 15 / 18	

COMPANY: Sunmi
 TITLE: Luxembourg
 A01.BLOCK DIAGRAM 2.0.C

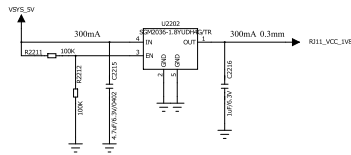
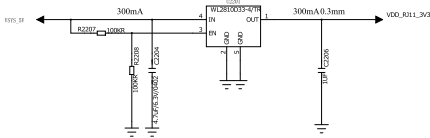
RJ12



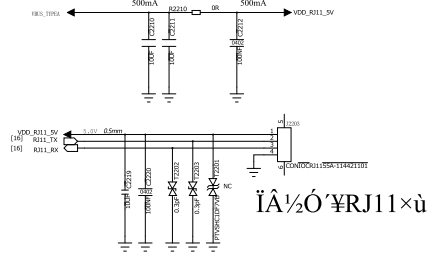
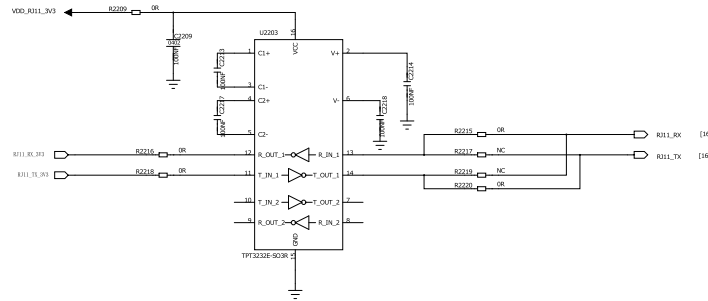
REVISION RECORD			
LTR	ECO NO.	APPROVED:	DATE

Reference FTP:RJ12_STD_SCH_V1.0_20211231

RS232

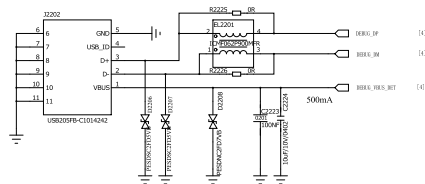


RJ11



TP_RJ11-UART_AudioJACK

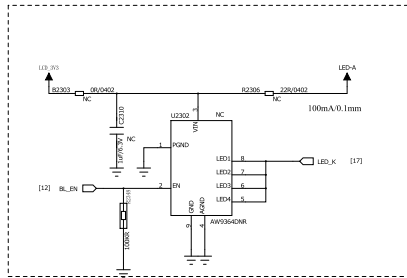
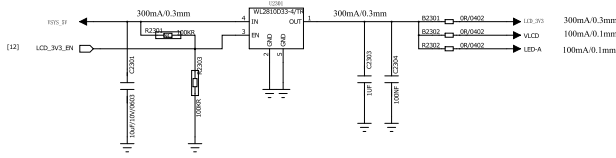
MicroUSB for Debug



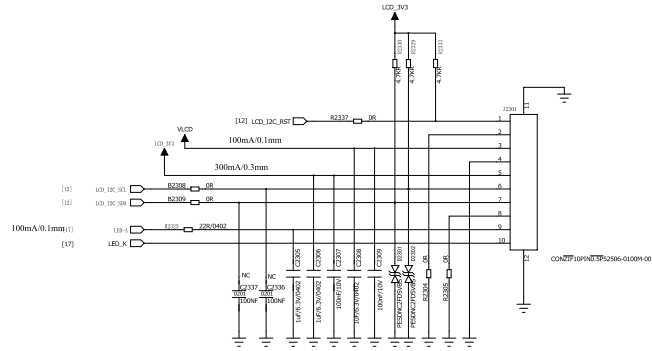
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CHECKED: <Checked By>		DATED: <Checked Date>		TITLE: Luxembourg	
QUALITY CONTROL: <QC By>		DATED: <QC Date>		DRAWING NO: A01.BLOCK DIAGRAM 2.0.C	
RELEASED: <Released By>		DATED: <Release Date>		SCALE: <Scale>	
SHEET: 16				18	

REVISION RECORD			
LTR	ECD NO.	APPROVED:	DATE:

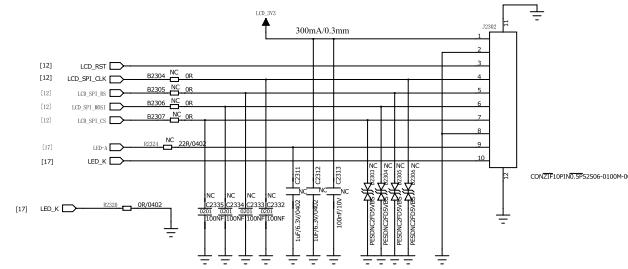
SUB LCD



LCD-I2C

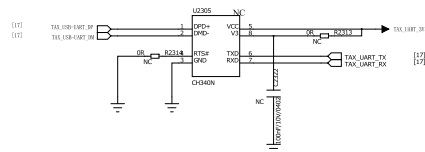
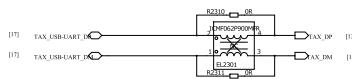
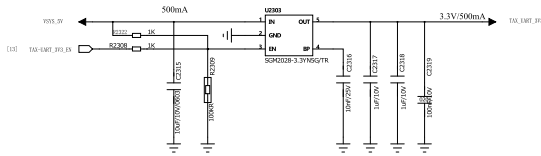


LCD-SPI

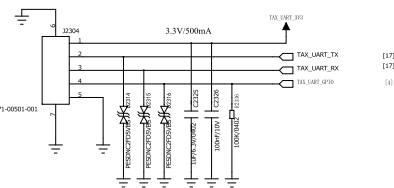
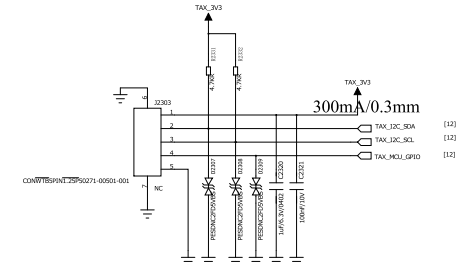


TAX-UART

NC

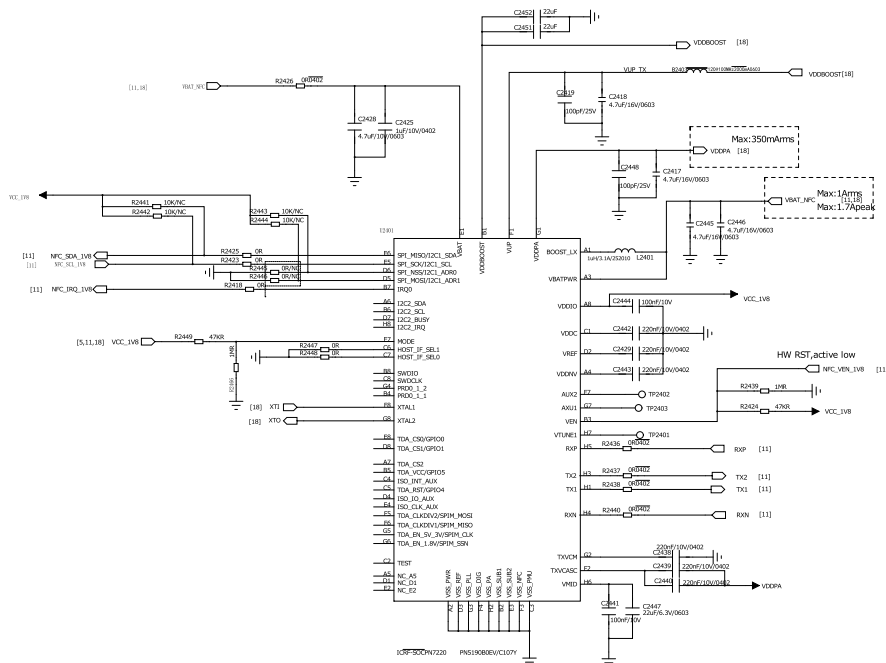


TAX-I2C/UART



COMPANY:		Sunmi			
TITLE:		Luxembourg			
DRAWN:	ZMQ	DATED:	23.02.27	CODE:	
CHECKED:	<Checked By>	DATED:	<Checked Date>	SIZE:	
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RELEASED:	<Released By>	DATED:	<Release Date>	SCALE:	
SHEET: 17					18

REVISION RECORD			
LTR	ECO NO.	APPROVED	DATE



DRAWN: ZMQ		DATED: 23.02.27		COMPANY: Sunmi			
CHECKED: <Checked By>				TITLE: Luxembourg			
QUALITY CONTROL: <QC By>				CODE:	SIZE:	DRAWING NO:	REV:
RELEASED: <Release By>				A01.BLOCK DIAGRAM 2.0.C			
DATE: <Checked Date>				SCALE: <Scale>			
DATE: <QC Date>				SHEET 18 / 18			
DATE: <Release Date>							