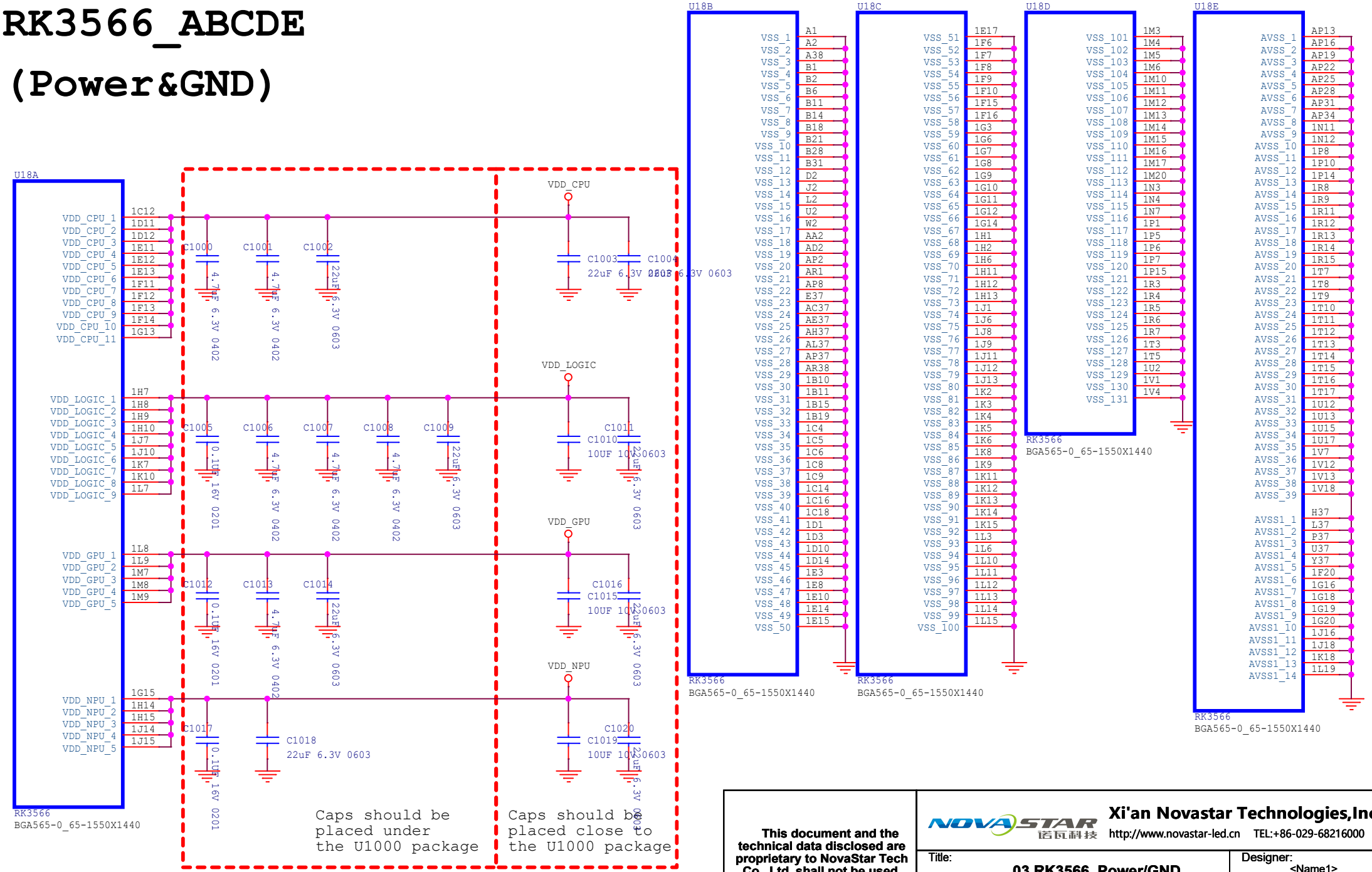
RK3566_ABCDE

(Power&GND)



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Title: 03.RK3566_Power/GND

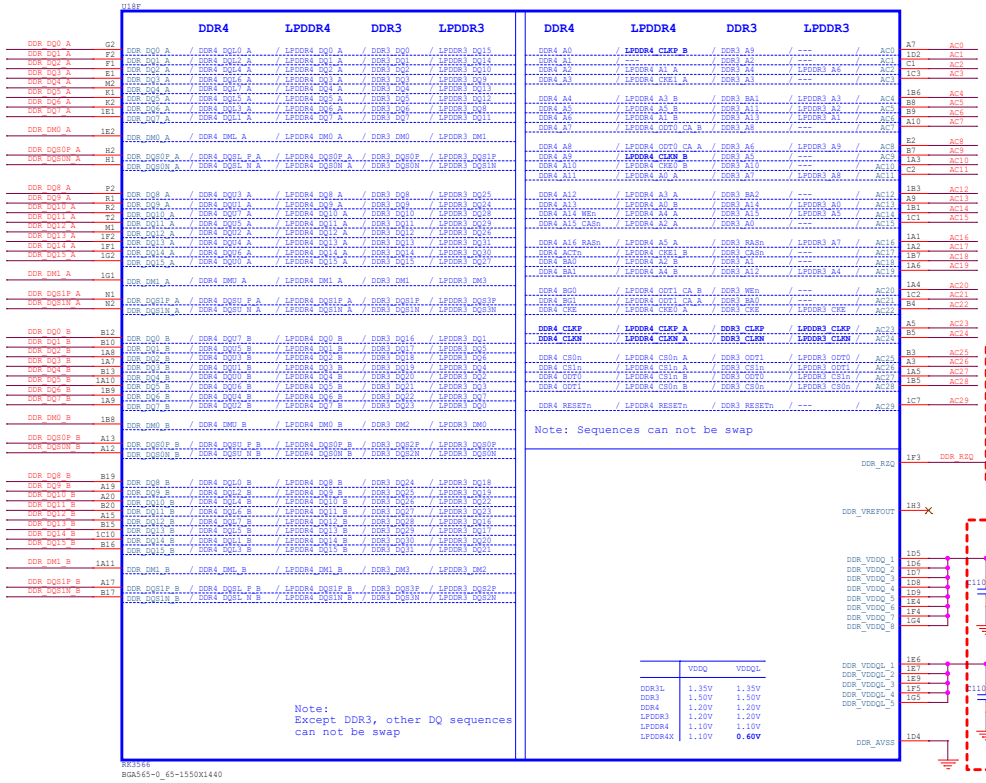
Designer: <Name1>

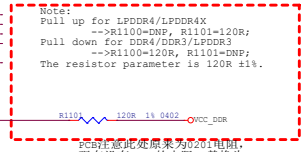
Board Name: <Doc2>

Date: Wednesday, February 03, 2021

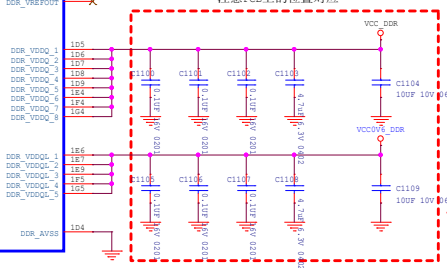
Sheet: 4 of 59

RK3566_F(DDR PHY)





PCB注意此处原来为0201电阻，
现在没有0201的电阻，替换为0402，
注意PCB上的位置对应

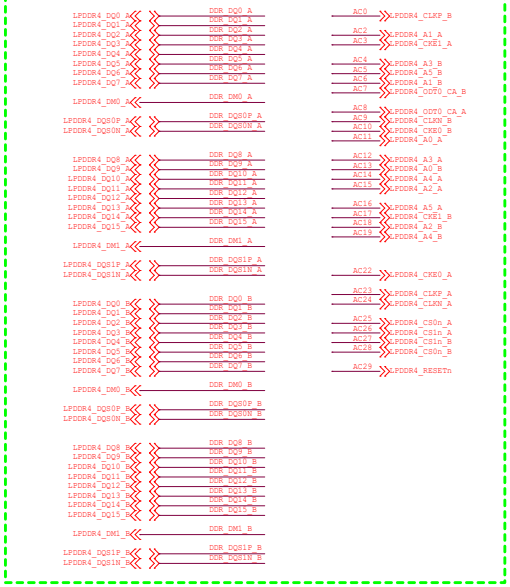


Caps should be placed under
the U1000 package

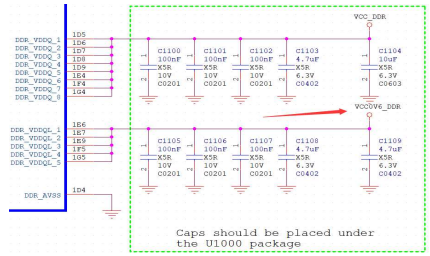
Attention!

For LPDDR4X DDR_VDDQL = 0.6V,
refer to the connection example
For LPDDR3 ultra low power mode,
DDR_VDDQ&DDR_VDDQL connect to VCC_DDRC

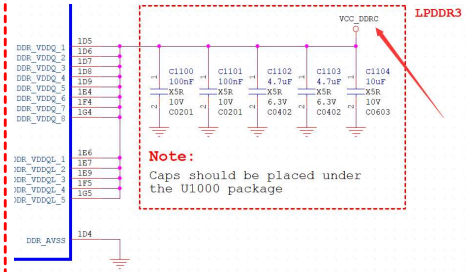
Default: DQ&CA Connection for LPDDR4/LPDDR4X



Note:
LPDDR4x mode:
Pin 1E6,1E7,1E9,1F5,1G5 connected to VCC0V6_DDR power supply
For example



Note:
LPDDR3 ultra low power mode:



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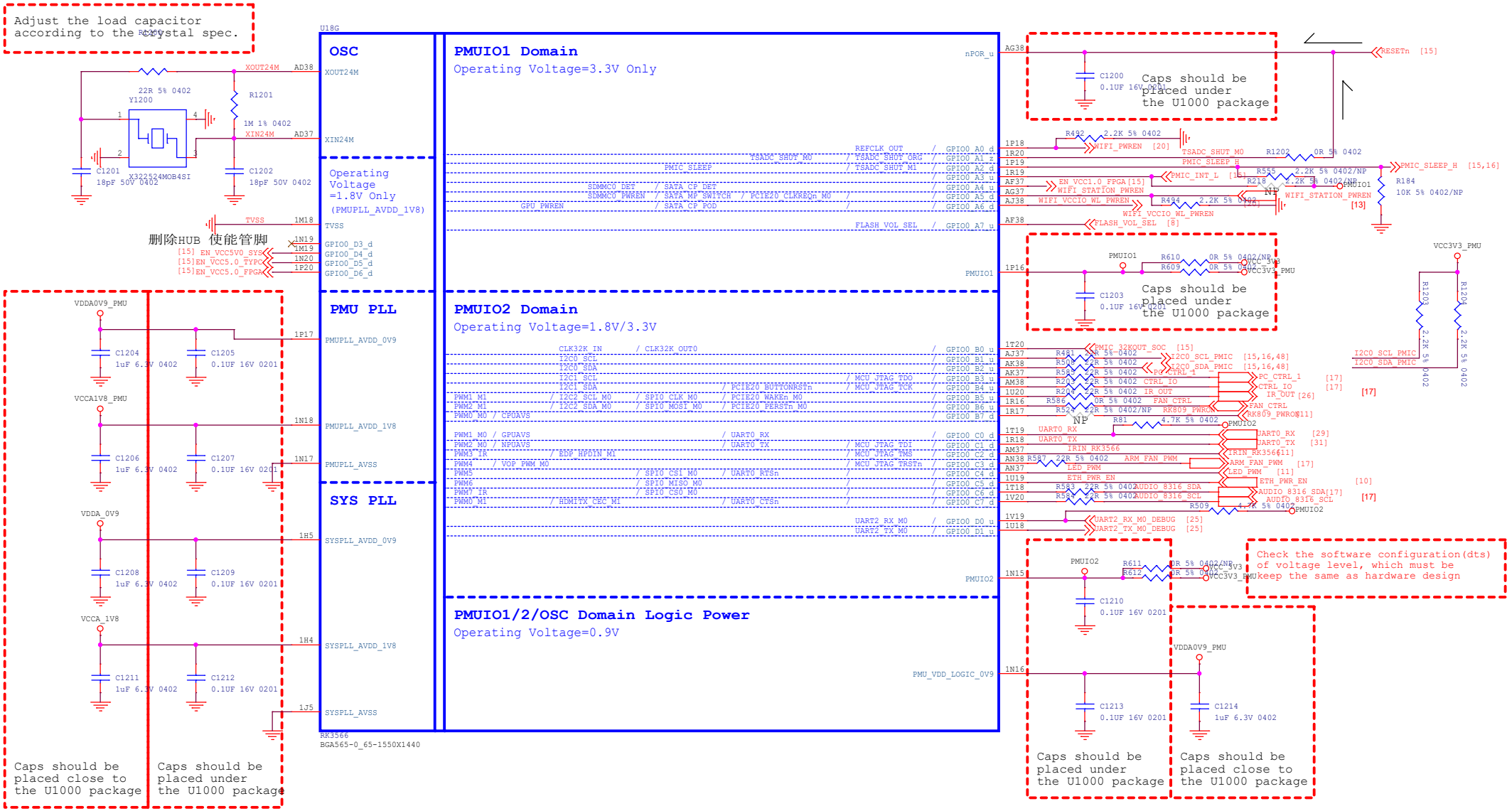
Title: 04.RK3566_DDR_PHY	Designer: <Name1>
Board Name: <Doc2>	
Date: Wednesday, February 03, 2021	Sheet: 5 of 59

RK3566_G(OSC/PLL/PMUIO1/2)



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Title: 05.RK3566_OSC/PLL/PMUIO	Designer: <Name1>
Board Name: <Doc2>	
Date: Wednesday, February 03, 2021	Sheet: 6 of 59

RK3566_I(VCCIO2 Domain)

U18I

VCCIO2 Domain

Operating Voltage=1.8V/3.3V

EMMC_D0	/ FLASH_D0	/ GPIO1_B4_u	A32	eMMC_D0/FLASH_D0 [19]
EMMC_D1	/ FLASH_D1	/ GPIO1_B5_u	B27	eMMC_D1/FLASH_D1 [19]
EMMC_D2	/ FLASH_D2	/ GPIO1_B6_u	B32	eMMC_D2/FLASH_D2 [19]
EMMC_D3	/ FLASH_D3	/ GPIO1_B7_u	B29	eMMC_D3/FLASH_D3 [19]
EMMC_D4	/ FLASH_D4	/ GPIO1_C0_u	B33	eMMC_D4/FLASH_D4 [19]
EMMC_D5	/ FLASH_D5	/ GPIO1_C1_u	A30	eMMC_D5/FLASH_D5 [19]
EMMC_D6	/ FLASH_D6	/ GPIO1_C2_u	B30	eMMC_D6/FLASH_D6 [19]
EMMC_D7	/ FLASH_D7	/ GPIO1_C3_u	A33	eMMC_D7/FLASH_D7 [19]
EMMC_CMD	/ FLASH_WRn	/ GPIO1_C4_u	A27	eMMC_CMD/FLASH_WRn [19]
EMMC_CLKOUT	/ FLASH_DQS	/ GPIO1_C5_d	A29	R1300 22R 5% 0402 eMMC_CLKOUT/FLASH_DQS [19]
EMMC_DATA_STROBE	/ FSPI_CS1n / FLASH_CLE	/ GPIO1_C6_d	1A16	eMMC_DATA_STROBE/FLASH_CLE [19]
EMMC_RSTn	/ FSPI_D2 / FLASH_WPn	/ GPIO1_C7_d	1B16	R469 22R 5% 0402/NP eMMC_RSTn/FSPI_D2/FLASH_WPn [19]
	FSPI_CLK / FLASH_ALE	/ GPIO1_D0_d	1A15	
	FSPI_D0 / FLASH_RDY	/ GPIO1_D1_u	1A17	
	FSPI_D1 / FLASH_RDn	/ GPIO1_D2_u	1A18	
	FSPI_CS0n / FLASH_CS0n	/ GPIO1_D3_u	1B17	
	FSPI_D3 / FLASH_CS1n	/ GPIO1_D4_u	1C15	

Default is determined by Pin
FLASH_VOL_SEL/GPIO0_A7_u:
L:VCCIO2 must supply 3.3V
H:VCCIO2 must supply 1.8V

VCCIO2 — 1C13

RK3566
BGA565-0_65-1550X1440

VCC_3V3 — R366 0R 5% 0402/NP — VCCIO_FLASH
VCC_1V8 — R367 0R 5% 0402 — VCCIO_FLASH

VCCIO_FLASH — C1300 0.1UF 16V 0201 — 1C13

Caps should be placed under the U1000 package

eMMC_D0/FLASH_D0 — eMMC_D0_1 — GND11 — eMMC_D0 — GND1

这两个测试点靠近EMMC放置

1. eMMC or Nand Flash:
   Short 'eMMC_D0/FLASH_D0' and GND to enter Maskrom Mode.

2. SPI Flash:
   Short 'FSPI_CLK/FLASH_ALE' and GND to enter Maskrom Mode.

Be sure to reserve the testpoints for firmware burning or update.

FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

RK3566_J(VCCIO3 Domain)

U18J

VCCIO3 Domain

Operating Voltage=1.8V/3.3V

PWM8_M1	/ SDMMC0_D0 / UART2_TX_M1 / UART6_TX_M1	/ GPIO1_D5_u	1E20	R363 22R 5% 0402 UART3_TX FPGA_RX_ARM_TX
PWM9_M1	/ SDMMC0_D1 / UART2_RX_M1 / UART6_RX_M1	/ GPIO1_D6_u	1F19	R365 22R 5% 0402 UART3_RX FPGA_TX_ARM_RX
SDMMC0_D2	/ ARM_JTAG_TCK/ UART5_CTSn_M0	/ GPIO1_D7_u	1D20	STB_GPIO3 STB_GPIO3 [17]
SDMMC0_D3	/ ARM_JTAG_TMS/ UART5_RTSn_M0	/ GPIO2_A0_u	1F18	ARM_FAN_SPEED ARM_FAN_SPEED [17]
PWM10_M1 / SDMMC0_CMD	/ UART5_RX_M0	/ GPIO2_A1_u	1E19	R440 0R 5% 0402 UART5_RX UART5_RX [26]
SDMMC0_CLK	/ TEST_CLKOUT / UART5_TX_M0	/ GPIO2_A2_d	G38	R439 0R 5% 0402 UART5_TX UART5_TX [26]

VCCIO3 — 1F17

RK3566
BGA565-0_65-1550X1440

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

FPGA-ARM UART

FPGA_RX_ARM_TX — FPGA_RX_ARM_TX [7,10]
FPGA_TX_ARM_RX — FPGA_TX_ARM_RX [7,10]

VCC_3V3 — C1301 0.1UF 16V 0201 — VCCIO3

Caps should be placed under the U1000 package

PMUIO1

FLASH_VOL_SEL [7] — R182 — Option1
Option2
10K 5% 0402

FLASH_VOL_SEL — VCC_3V3

UART5_RX R438 4.7K 5% 0402 — VCC_3V3

R183 — Option3
10K 5% 0402/NP

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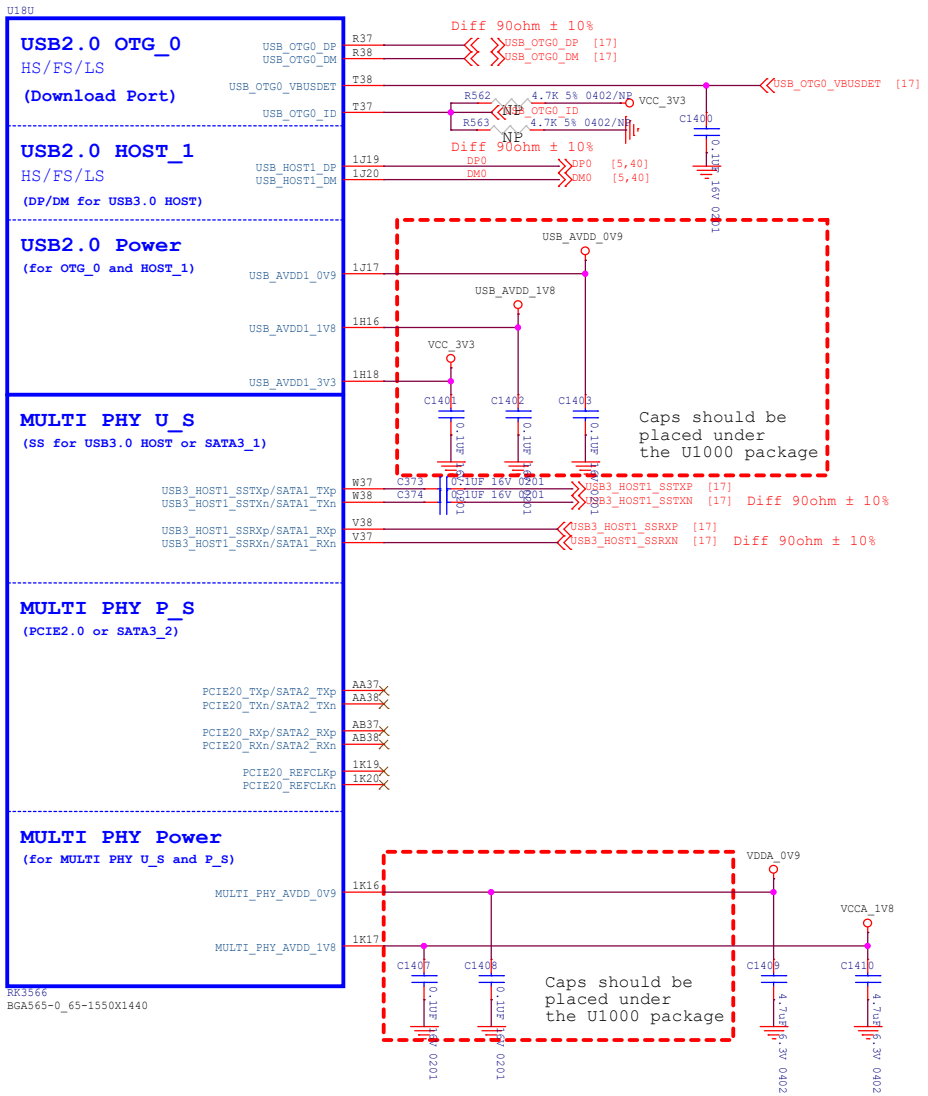
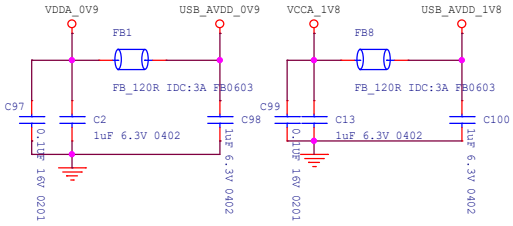
Title:	06.RK3566_EMMC	Designer:	<Name1>
Board Name:	<Doc2>		
Date:	Wednesday, February 03, 2021	Sheet:	7 of 59

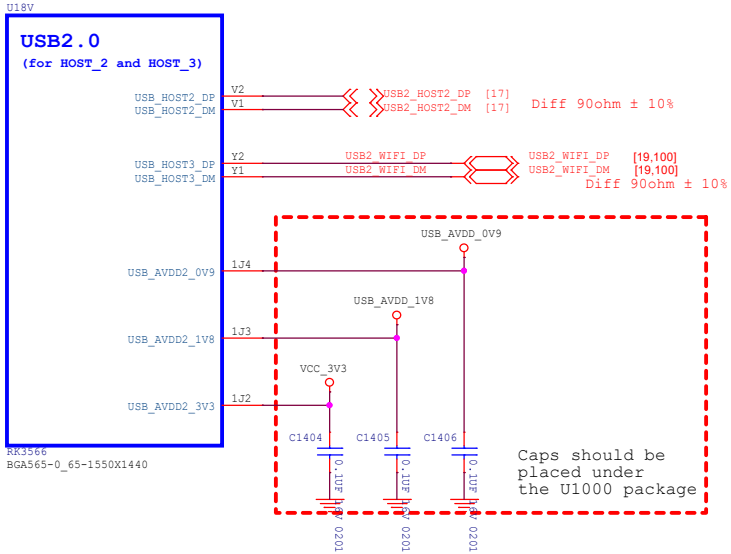
RK3566_U(USB3.0/PCIe2.0x1/SATA)



Power for USB



RK3566_V(USB2.0 HOST)



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Title: 07.RK3566_USB	Designer: <Name1>
Board Name: <Doc2>	
Date: Wednesday, February 03, 2021	Sheet: 8 of 59

RK3566_K(VCCIO4 Domain)

U18K

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

UART6_RX_M0		SDMMC1_D0	GPIO2_A3_u
UART6_TX_M0		SDMMC1_D1	GPIO2_A4_u
UART7_RX_M0		SDMMC1_D2	GPIO2_A5_u
UART7_TX_M0		SDMMC1_D3	GPIO2_A6_u
UART9_RX_M0		SDMMC1_CMD	GPIO2_A7_u
UART9_TX_M0		SDMMC1_CLK	GPIO2_B0_d
UART8_RTSn_M0	I2C4_SDA_M1	SDMMC1_PWREN	GPIO2_B1_d
UART8_CTSn_M0	I2C4_SCL_M1	SDMMC1_DET	GPIO2_B2_u
		UART1_RX_M0	GPIO2_B3_u
		UART1_TX_M0	GPIO2_B4_u
SPI1_CLK_M0		UART1_RTSn_M0	GPIO2_B5_u
SPI1_MISO_M0		UART1_CTSn_M0	GPIO2_B6_u
UART6_RTSn_M0	SPI1_MOSI_M0	I2S2_SCLK_RX_M0	GPIO2_B7_d
UART6_CTSn_M0	SPI1_CSO_M0	I2S2_LRCK_RX_M0	GPIO2_C0_d
UART7_RTSn_M0	SPI2_CLK_M0 / ETH0_REFCLKO_25M	I2S2_MCLK_M0	GPIO2_C1_d
UART7_CTSn_M0	SPI2_MISO_M0	I2S2_SCLK_TX_M0	GPIO2_C2_d
UART9_RTSn_M0	SPI2_MOSI_M0	I2S2_LRCK_TX_M0	GPIO2_C3_d
UART9_CTSn_M0	SPI2_CSO_M0	I2S2_SDO_M0	GPIO2_C4_d
UART8_TX_M0	SPI2_CS1_M0	I2S2_SDI_M0	GPIO2_C5_d
UART8_RX_M0	SPI1_CS1_M0 / CLK32K_OUT1		GPIO2_C6_d

RK3566
BGA565-0_65-1550X1440

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

GSV1011_INT_1 — R622 2K 1% 0402 — GSV1011_INT
LT9211_MCU_INT_1 — R623 2.4K 1% 0402 — R629 2K 1% 0402 — R630 2.4K 1% 0402 — LT9211_MCU_INT

ARM_LED1 — R496 100R 5% 0402 — D7 LED Yellow&Green 0603 — VCCIO_WL

HDMI_A_PWR_DET — HDMI_A_PWR_DET [7]
HDMI_B_PWR_DET — HDMI_B_PWR_DET [7]

1C19 SDMMC1_D0 [20]
1E18 SDMMC1_D1 [20]
1D18 SDMMC1_D2 [20]
1A20 SDMMC1_D3 [20]
B35 SDMMC1_CMD [20]
B37 R1501 22R 5% 0402 SDMMC1_CLK [20]
A35 UART8_RTSn_M0 [20]
B34 UART8_CTSn_M0 [20] C2204 2.2PF 50V 0402/NP
1C20 HOST_WAKE_BT_H [20]
F38 WIFI_REG_ON_H [20]
F37 BT_REG_ON_H [20]
G37 HDMI_A_PWR_DET
D38 R626 0R 5% 0402 WIFI_WAKE_HOST_H [20]
A37 R616 0R 5% 0402 BT_WAKE_HOST_H [20]
B36 HDMI_B_PWR_DET
C37 ARM_LED1 R495 4.7K 5% 0402 VCCIO_WL
1D19 LT9211_MCU_INT_1
1B20 GSV1011_INT_1
D37 UART8_TX_M0 [20] VCCIO_WL R331 4.7K 5% 0402
B38 UART8_RX_M0 [20]

1E16 VCCIO4 — VCCIO_WL — C1505 0.1UF 16V 0201

Caps should be placed under the U1000 package

WIFI使用SDIO3.0,
BANK电压使用1.8V

RK3566_O(SARADC/OTP)

U18O

SARADC
Recovery/

SARADC_VIN0	1D17	SARADC_VIN0 — SARADC_VIN0_KEY/RECOVERY [26]
SARADC_VIN1	1C17	SARADC_VIN1_HW_ID
SARADC_VIN2	1B18	LS_ADC0 — LS_ADC0 [11]
SARADC_VIN3	1A19	SARADC_VIN3
SARADC_AVDD_1V8	1D16	

OTP

OTP_VCC18	1D15	

RK3566
BGA565-0_65-1550X1440

VCCA_1V8 — C1504 0.1UF 16V 0201

Caps should be placed under the U1000 package

VCCA_1V8 — R1500 10K 5% 0402

Note:
The Pull Up resistor Must be mounted/STUFF

C1500 1nF 50V 0402 — C1501 1nF 50V 0402 — C1503 1nF 50V 0402/NP

Caps should be placed close to the U1000 package

SARADC_VIN3 — SARADC_VIN3 [6,10]

SARADC_VIN1_HW_ID	Rup	Rdown	ADC	
Version_1	10K	DNP	1023	1.8V
Version_2	20K	100K	852	1.5V
Version_3	18K	36K	681	1.2V
Version_4	51K	51K	512	0.9V
Version_5	36K	18K	340	0.6V
Version_6	100K	20K	170	0.3V
Version_7	DNP	10K	0	0V

Hardware board ID

VCCA_1V8 — R1502 20K 1% 0402 — SARADC_VIN1_HW_ID — R1503 100K 1% 0402

RK3566_N(VCCIO7 Domain)

U18N

VCCIO7 Domain

Operating Voltage=1.8V/3.3V

PWM14_M1	SPI3_CLK_M1	I2S3_MCLK_M1	GPIO4_C2_d
PWM15_IR_M1	SPI3_MOSI_M1	I2S3_SCLK_M1	GPIO4_C3_d
EDP_HPDIN_M0	SATA2_ACT_LED / SPDIF_TX_M2	I2S3_LRCK_M1	GPIO4_C4_d
PWM12_M1	SPI3_MISO_M1 / SATA1_ACT_LED / UART9_TX_M1	I2S3_SDO_M1	GPIO4_C5_d
PWM13_M1	SPI3_CSO_M1 / SATA0_ACT_LED / UART9_RX_M1	I2S3_SDI_M1	GPIO4_C6_d
HDMITX_SCL	I2C5_SCL_M1		GPIO4_C7_u
HDMITX_SDA	I2C5_SDA_M1		GPIO4_D0_u
HDMITX_CEC_M0	SPI3_CS1_M1		GPIO4_D1_u

RK3566
BGA565-0_65-1550X1440

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

VCC_3V3 — R7 2.2K 5% 0402

1U7 RTC337_INTn — RTC337_INTn [26]
AP12 R468 22R 5% 0402 ARMTOTPYEC_IN1 — R470 2.2K 1% 0402 — VCC_3V3
1V6 R452 22R 5% 0402 ARMTOTPYEC_IO1 — R453 2.2K 1% 0402 — VCC_3V3
1U6 R530 22R 5% 0402
1T6 R531 22R 5% 0402 UART9_TX_M1 [20] UART9_RX_M1 [20]
R529 4.7K 5% 0402 — VCC_3V3

AR12 R205 22R 5% 0402 ARM_R_HDMI_TX_SCL — R293 2.2K 1% 0402 — VCC_3V3
AP11 R206 22R 5% 0402 ARM_R_HDMI_TX_SDA — R294 2.2K 1% 0402 — VCC_3V3
1V5 ARM_CEC — ARM_CEC [7]

1N8 VCCIO7 — VCC_3V3 — C1506 0.1UF 16V 0201

Caps should be placed under the U1000 package

ARM IO

ARMTOTPYEC_IO1 — ARMTOTPYEC_IO1 [6,10]
ARMTOTPYEC_IO2 — ARMTOTPYEC_IO2 [6,10]

VCC_3V3

5V — R371 2.2K 5% 0402/NP — R372 2.2K 5% 0402/NP

ARM_HDMI_TX_SCL — Q8 SI2302A-TP — ARM_R_HDMI_TX_SCL
ARM_HDMI_TX_SDA — Q10 SI2302A-TP — ARM_R_HDMI_TX_SDA

C32 10pF 50V 0402/NP — C33 10pF 50V 0402/NP — GND

ARM_HDMI_TX_SCL — ARM_HDMI_TX_SCL [30]
ARM_HDMI_TX_SDA — ARM_HDMI_TX_SDA [30]

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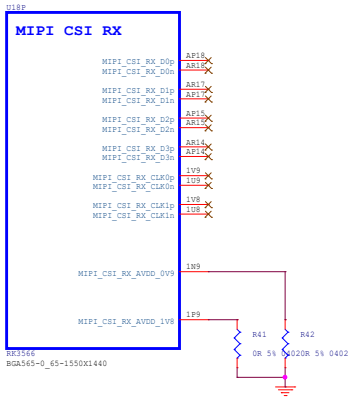
Title: 08.RK3566_SARADC/GPIO
Designer: <Name1>
Board Name: <Doc2>
Date: Wednesday, February 03, 2021
Sheet: 9 of 59

RK3566_P(MIPI_CSI_RX)



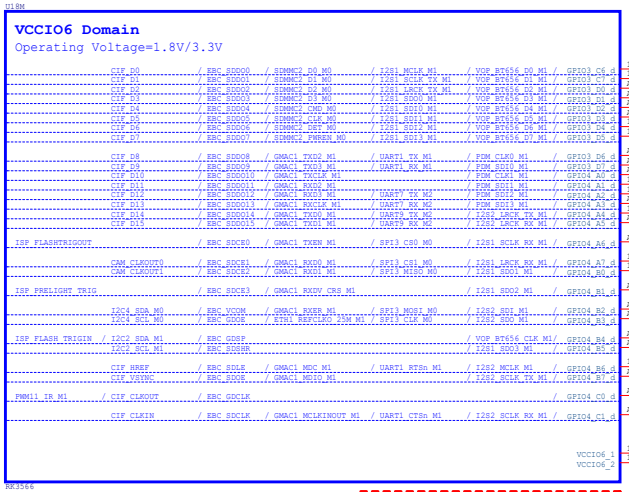
Usage of MIPI CSI Dx&CLKs		
Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

Usage of CIF Interface				
Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

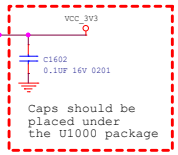
Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

BT1120 16bit Mode:
Default: D0-D7 <--> Y0-Y7 , D8-D15 <--> C0-C7
Swap ON: D0-D7 <--> C0-C7 , D8-D15 <--> Y0-Y7

RK3566_M(VCCIO6 Domain)



Check the software configuration(dts) of voltage level, which must be keep the same as hardware design



删除原ARMTOTPYEC_IO3,4信号

删除原type-c DET1信号

USB3.0使能修改为USB2.0 HOST的使能

GSV1011 IIC CBB内部有上拉

删除原type-c DET2信号

FPGA-ARM CIF

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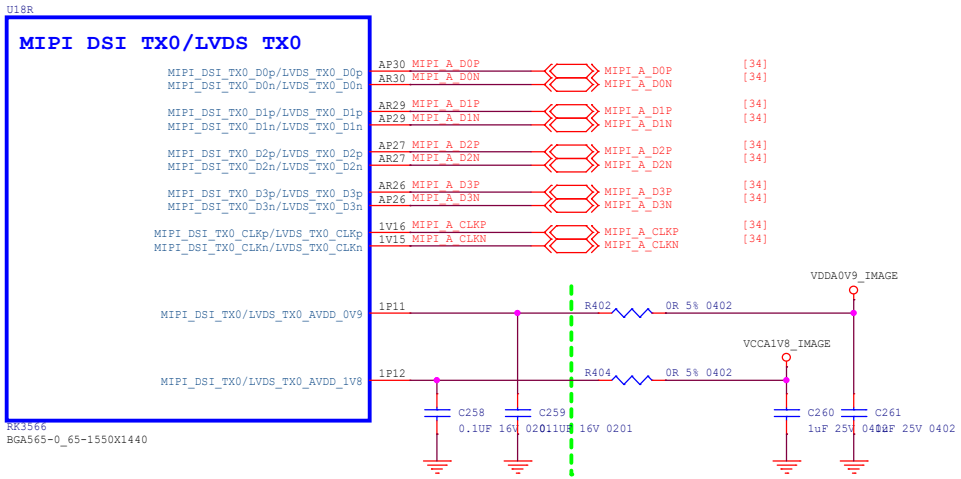
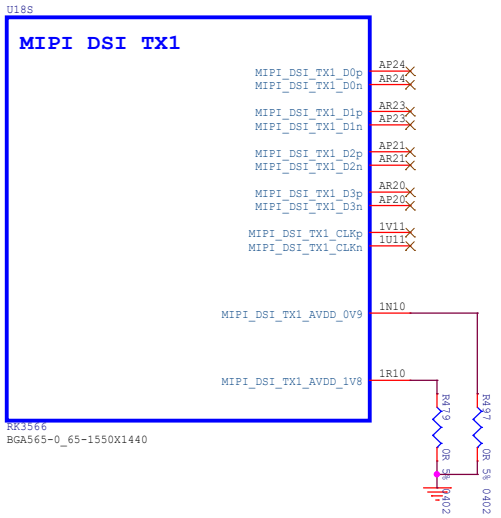
Title: 09.RK3566_VCCIO6 Domain	Designer: <Name1>
Board Name: <Doc2>	
Date: Wednesday, February 03, 2021	Sheet: 10 of 59

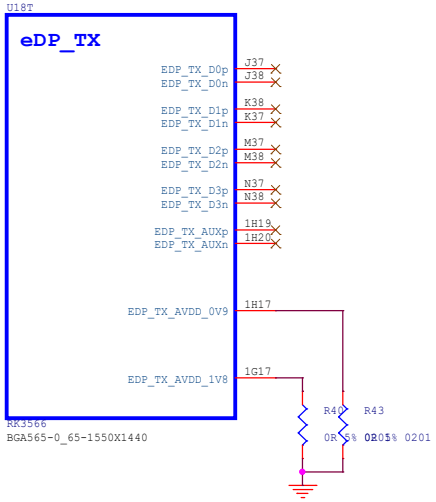
RK3566_R(MIPI_DSI_TX0/LVDS_TX0)



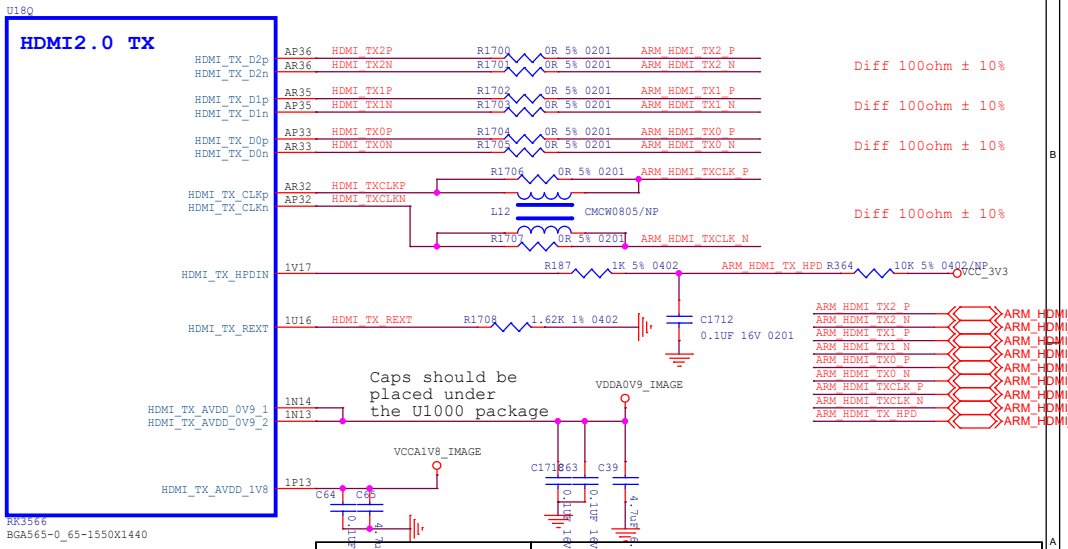
RK3566_S(MIPI_DSI_TX1)



RK3566_T(eDP TX)



RK3566_Q(HDMI2.0 TX)



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Title:	10.RK3566_VO_HDMI2.0_MIPI-DSI	Designer:	<Name1>
Board Name:	<Doc2>		
Date:	Wednesday, February 03, 2021	Sheet:	11 of 59

RK3566_L(VCCIO5 Domain)

U18L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

	VOP_BT1120_D0	/ SPI1_CS0_M1		/ SDMMC2_D0_M1	/ GPIO3_A1_d
	VOP_BT1120_D1		/ GMAC1_TXD2_M0 / I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
	VOP_BT1120_D2		/ GMAC1_TXD3_M0 / I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
	VOP_BT1120_D3		/ GMAC1_RXD2_M0 / I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
	VOP_BT1120_D4		/ GMAC1_RXD3_M0 / I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
	VOP_BT1120_CLK		/ GMAC1_TXCLK_M0 / I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
	VOP_BT1120_D5		/ GMAC1_RXCLK_M0	/ SDMMC2_DET_M1	/ GPIO3_A7_d
	VOP_BT1120_D6		/ ETH1_REFCLKO_25M_M0	/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
PWM8_M0	/ VOP_BT1120_D7		/ GMAC1_RXD0_M0 / UART4_RX_M1		/ GPIO3_B1_d
PWM9_M0	/ VOP_BT1120_D8		/ GMAC1_RXD1_M0 / UART4_TX_M1		/ GPIO3_B2_d
	VOP_BT1120_D9	/ I2C5_SCL_M0	/ GMAC1_RXDV_CRS_M0	/ PDM_SDI0_M2	/ GPIO3_B3_d
	VOP_BT1120_D10	/ I2C5_SDA_M0	/ GMAC1_RXER_M0	/ PDM_SDI1_M2	/ GPIO3_B4_d
PWM10_M0	/ VOP_BT1120_D11	/ I2C3_SCL_M1	/ GMAC1_TXD0_M0		/ GPIO3_B5_d
PWM11_IR_M0	/ VOP_BT1120_D12	/ I2C3_SDA_M1	/ GMAC1_TXD1_M0		/ GPIO3_B6_d
PWM12_M0			/ GMAC1_TXEN_M0 / UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
PWM13_M0			/ GMAC1_MCLKINOUT_M0 / UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
	VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
	VOP_BT1120_D14	/ SPI1_MISO_M1	/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
	VOP_BT1120_D15	/ SPI1_CLK_M1	/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0		/ VOP_PWM_M1	/ GMAC1_MDC_M0 / UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0		/ SPDIF_TX_M1	/ GMAC1_MDIO_M0 / UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

VCCIO5_1
VCCIO5_2

RK3566
BGA565-0_65-1550X1440

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

ARM_MAC_REF_CLK — ARM_MAC_REF_CLK [10]

GMAC_RXC — GMAC_RXC [10]
GMAC_RXCTL — GMAC_RXCTL [10]
GMAC_RXD0 — GMAC_RXD0 [10]
GMAC_RXD1 — GMAC_RXD1 [10]
GMAC_RXD2 — GMAC_RXD2 [10]
GMAC_RXD3 — GMAC_RXD3 [10]

GMAC_TXC — GMAC_TXC [10]
GMAC_TXCTL — GMAC_TXCTL [10]
GMAC_TXD0 — GMAC_TXD0 [10]
GMAC_TXD1 — GMAC_TXD1 [10]
GMAC_TXD2 — GMAC_TXD2 [10]
GMAC_TXD3 — GMAC_TXD3 [10]

1U5 R305 0R 5% 0402 ARM_SPI_CS_CFG
AR10 R1801 0R 5% 0402 GMAC_TXD2
AP10 R1801 0R 5% 0402 GMAC_TXD3
AR9 GMAC_RXD2
AP9 GMAC_RXD3
1U4 R1802 0R 5% 0402 GMAC_TXC
1V3 GMAC_RXC
C31 2.2PF 50V 0402/NP
AR7 R332 0R 5% 0402 FPGA_DONE_ARM
AP7 GMAC_RXD0
AR6 GMAC_RXD1
AP6 GMAC_RXCTL
1U3 MCU_BOOT MCU_BOOT [2]
1T4 R1804 0R 5% 0402 GMAC_TXD0
1V2 R1805 0R 5% 0402 GMAC_TXD1
AP5 R1806 0R 5% 0402 GMAC_TXCTL
AR4 ARM_MAC_REF_CLK
AP4 R436 22R 5% 0402 ARM_SPI_MOSI_CFG
AP3 MCU_RST MCU_RST [2]
AR2 R437 22R 5% 0402 ARM_SPI_CLK_CFG
1P3 OPS_ON OPS_ON [11]
1P4 OPS_CON OPS_CON [11]

VCCIO5
1N5
1N6
R333 0R 5% 0402 VCC_3V3
C1800 0.1uF 16V 0402

Caps should be placed under the U1000 package

ARM_SPI_CS_CFG — ARM_SPI_CS_C
ARM_SPI_CLK_CFG — ARM_SPI_CLK_
ARM_SPI_MOSI_CFG — ARM_SPI_MOSI
FPGA_DONE_ARM — FPGA_DONE_A

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Title: 11.RK3566_VO_GEPHY
Designer: <Name1>
Board Name: <Doc2>
Date: Wednesday, February 03, 2021

RK3566_H(VCCIO1 Domain)

U18H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

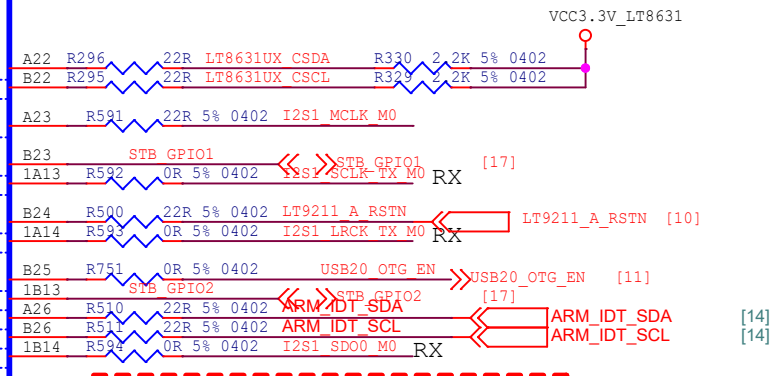
	/ I2C3_SDA_M0	/ UART3_RX_M0	/ AUDIOPWM_LOUT_p	/ GPIO1_A0_u
	/ I2C3_SCL_M0	/ UART3_TX_M0	/ AUDIOPWM_LOUT_n	/ GPIO1_A1_u
SCR_CLK	/ I2S1_MCLK_M0	/ UART3_RTSn_M0		/ GPIO1_A2_d
SCR_IO	/ I2S1_SCLK_TX_M0	/ UART3_CTSn_M0		/ GPIO1_A3_d
	I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0 / SPDIF_TX_M0	/ GPIO1_A4_d
SCR_RST	/ I2S1_LRCK_TX_M0	/ UART4_RTSn_M0		/ GPIO1_A5_d
	I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0 / AUDIOPWM_ROUT_p	/ GPIO1_A6_d
SCR_DET	/ I2S1_SDO0_M0	/ UART4_CTSn_M0	/ AUDIOPWM_ROUT_n	/ GPIO1_A7_d
	I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0 / PCIE20_CLKREQn_M2	/ GPIO1_B0_d
	I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0 / PCIE20_WAKEn_M2	/ GPIO1_B1_d
	I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0 / PCIE20_PERSTn_M2	/ GPIO1_B2_d
		I2S1_SDI0_M0	/ PDM_SDI0_M0	/ GPIO1_B3_d

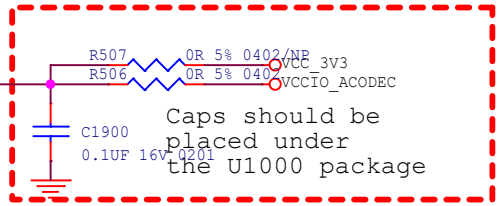
VCCIO1

RK3566
BGA565-0_65-1550X1440

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

LT8631UX_CSCL
LT8631UX_CSDA





VCCIO_ACODEC = 3.3V as default

FPGA-ARM INT

FPGA-ARM GPIOs

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Title: 12.RK3566_Audio_Interface

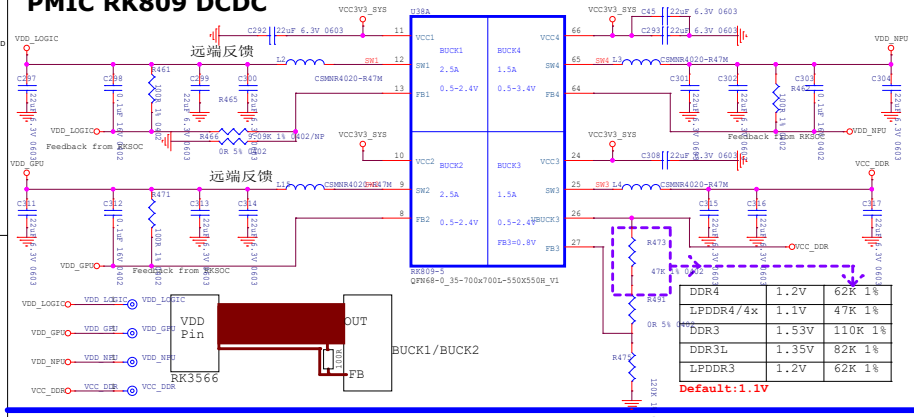
Designer: <Name1>

Board Name: <Doc2>

Date: Wednesday, February 03, 2021

Sheet: 13 of 59

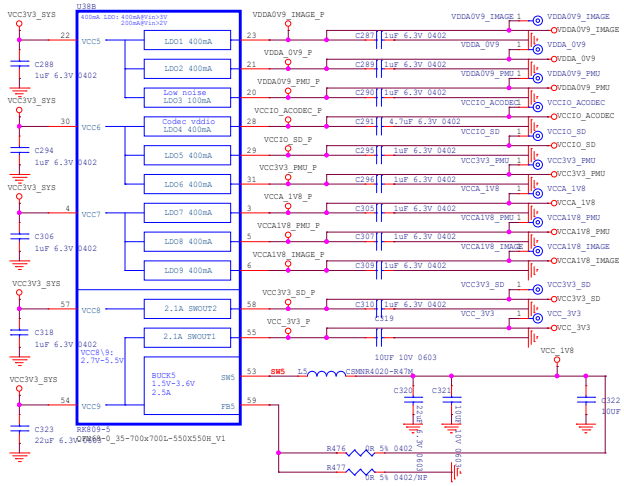
PMIC RK809 DCDC



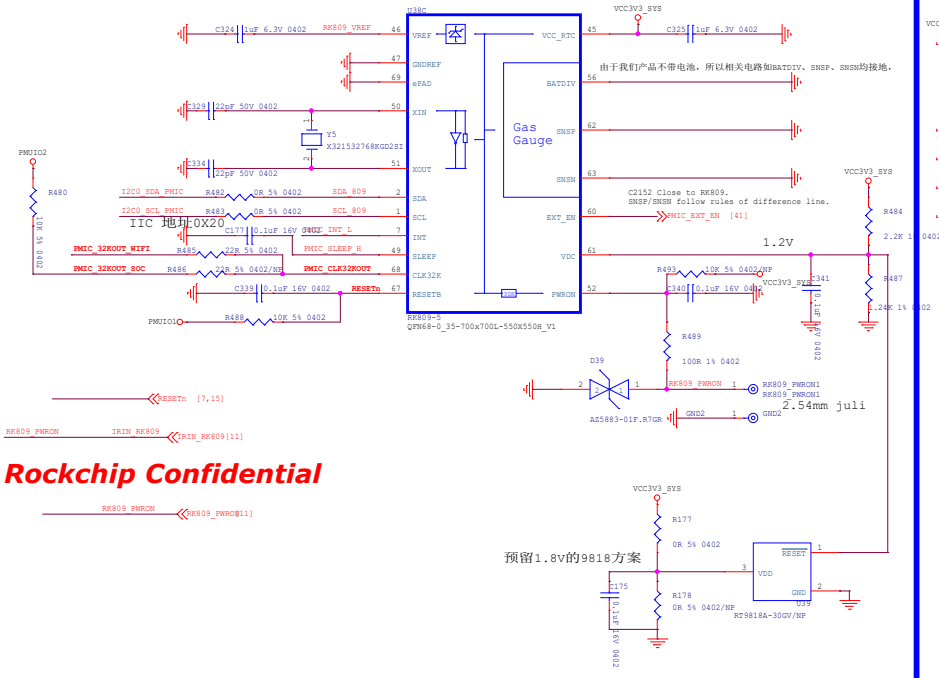
DDR4	1.2V	62K 1%
LPDDR4/4x	1.1V	47K 1%
DDR3	1.53V	110K 1%
DDL3L	1.35V	82K 1%
LPDDR3	1.2V	62K 1%

Default:1.1V

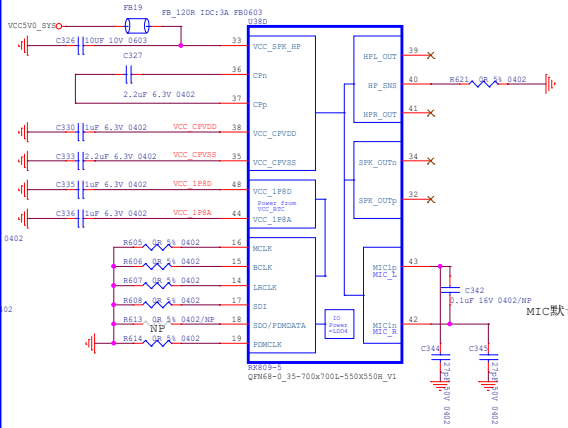
PMIC RK809 LDO



PMIC RK809 Managerment



PMIC RK809 CODEC



Rockchip Confidential

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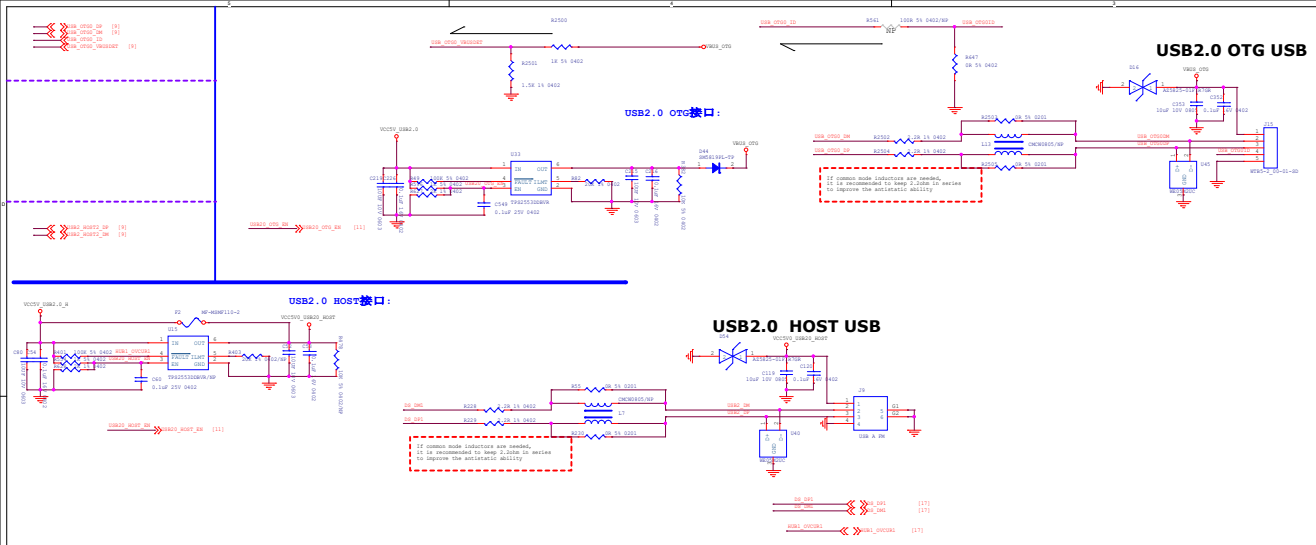
Title:	13.Power_PMIC_RK809
Designer:	<Name1>
Board Name:	<Doc2>
Date:	Sunday, May 09, 2021
Sheet:	14 of 59



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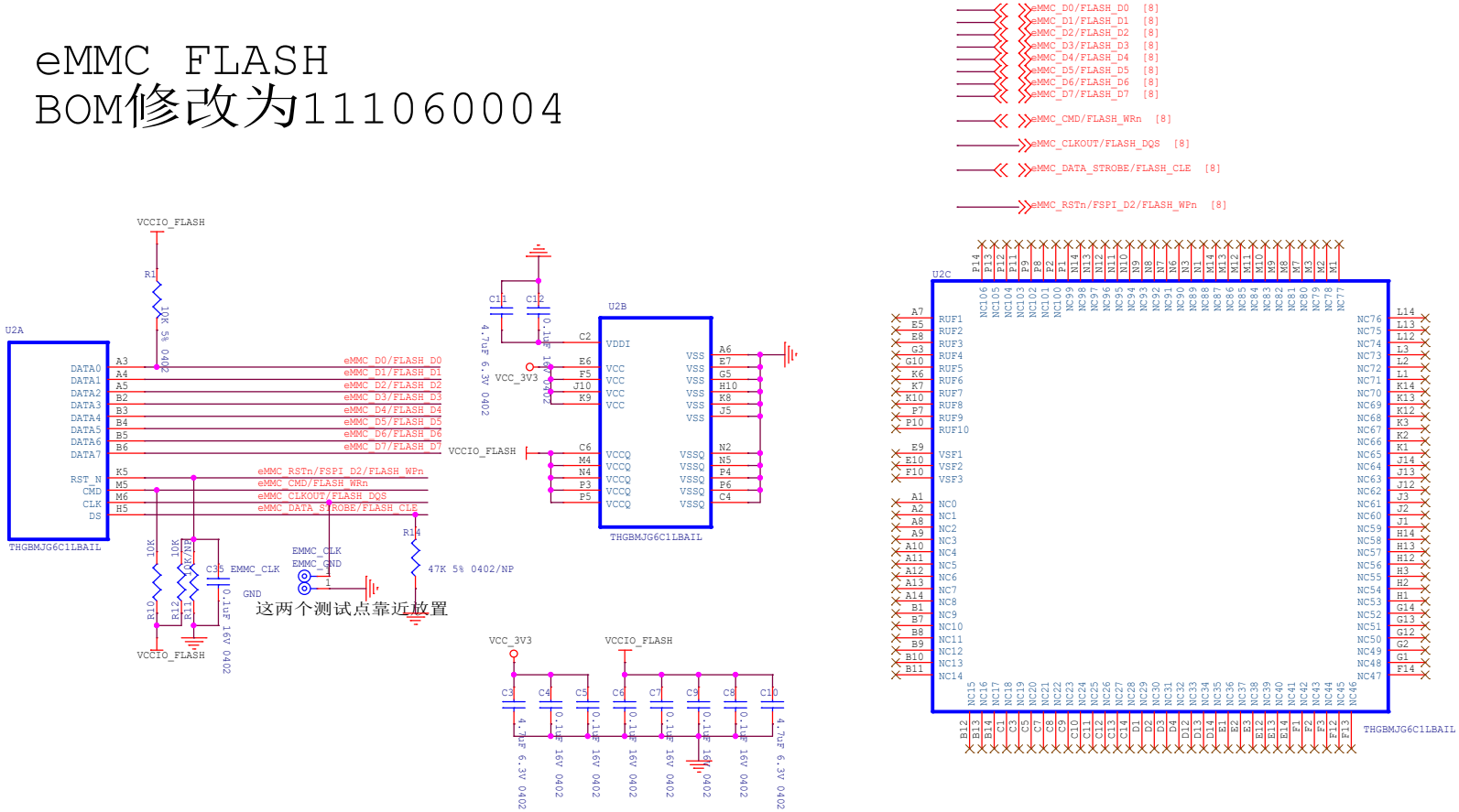
Title:	14.USB2/USB3_Port
Designer:	<Name1>
Board Name:	<Doc2>
Date:	Wednesday, February 03, 2021
Sheet	15 of 59

eMMC FLASH
BOM修改为111060004



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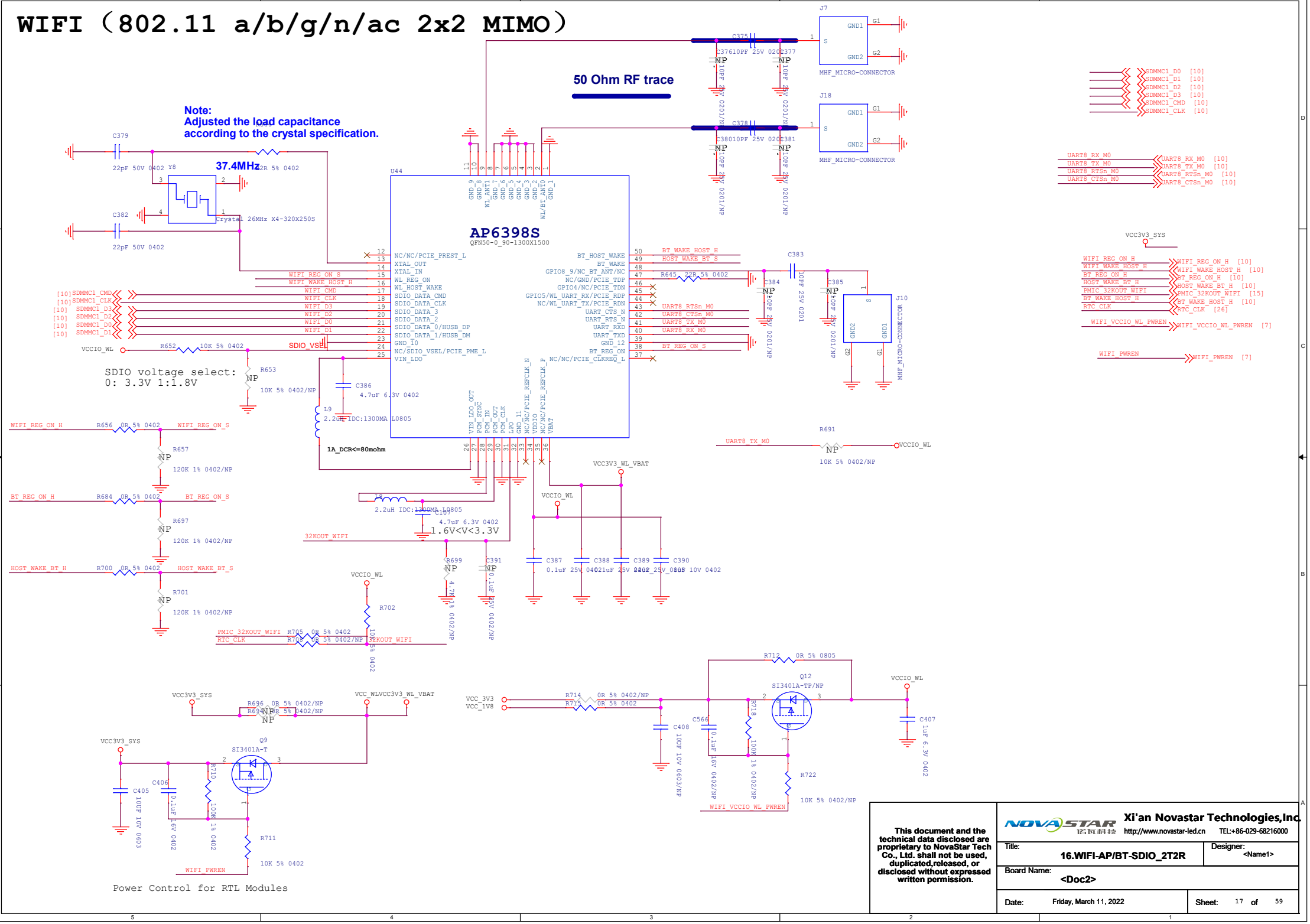
Title: 15.Flash-eMMC_Flash	Designer: <Name1>
Board Name: <Doc2>	
Date: Wednesday, February 03, 2021	Sheet: 16 of 59

WIFI（802.11 a/b/g/n/ac 2x2 MIMO）



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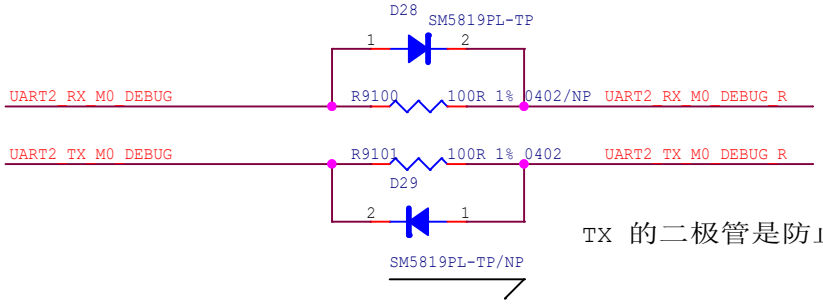
Title: 16.WIFI-AP/BT-SDIO_2T2R	Designer: <Name1>
Board Name: <Doc2>	
Date: Friday, March 11, 2022	Sheet: 17 of 59

UART2_RX_M0_DEBUG [7]

UART2_TX_M0_DEBUG [7]

Debug UART2



TX 的二极管是防止后端漏电

UART

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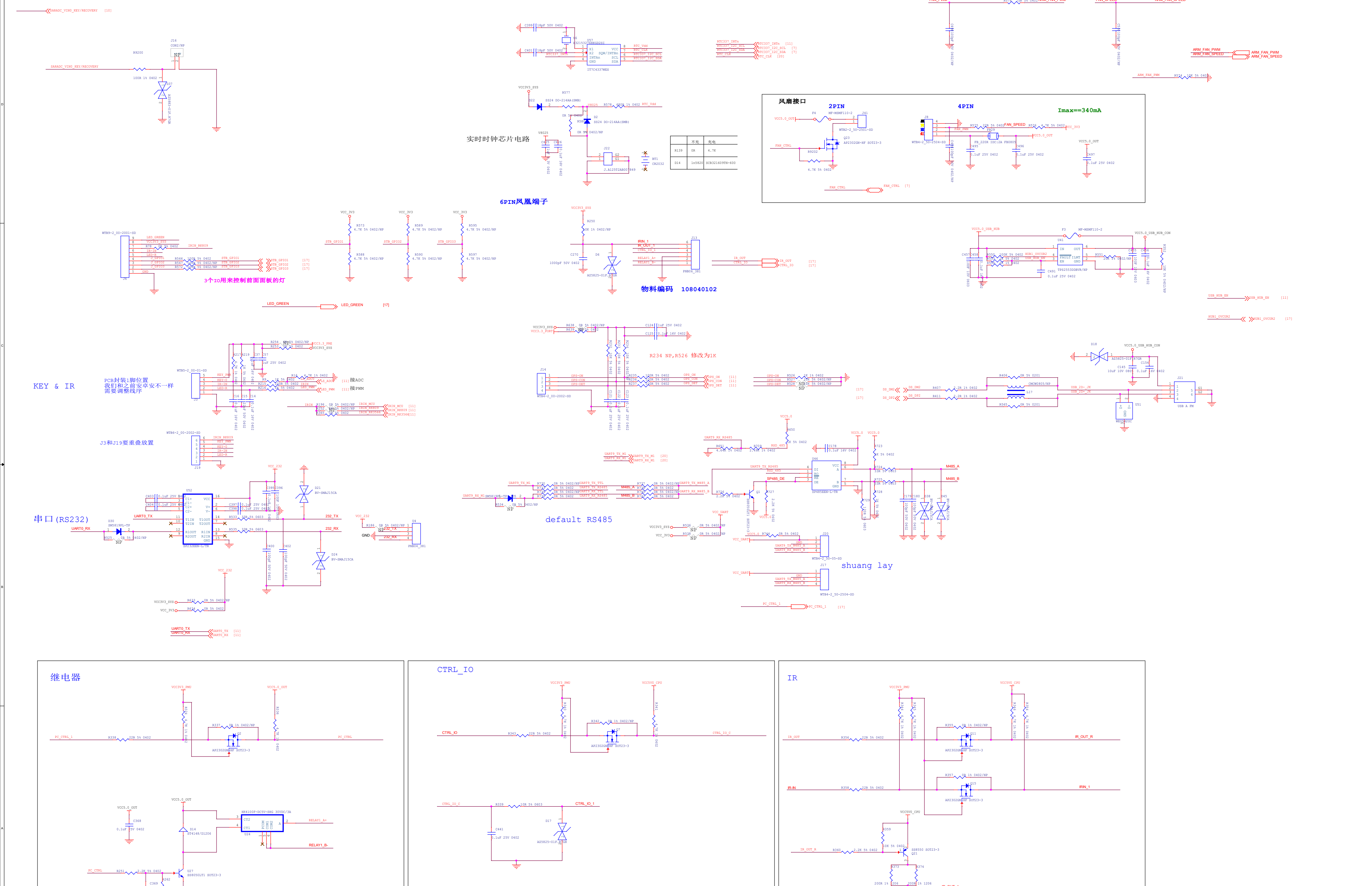
Title: 17.Debug_UART	Designer: <Name1>
Board Name: <Doc2>	
Date: Wednesday, February 03, 2021	Sheet: 18 of 59

ADC KEY



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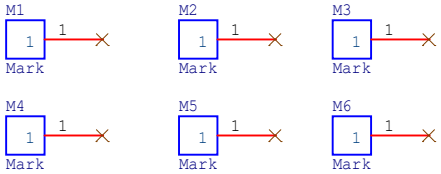
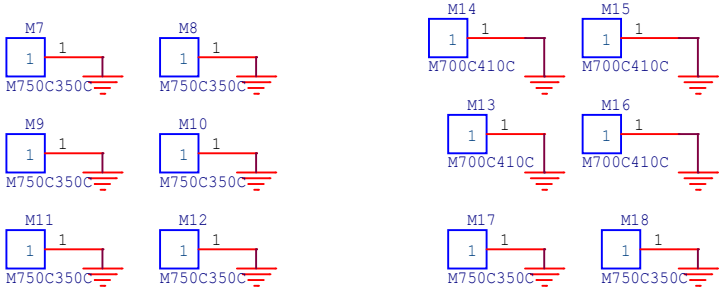
Title:	18.KEY/OTHER	Designer:	<Name1>
Board Name:	<Doc2>		
Date:	Wednesday, February 03, 2021	Sheet:	19 of 59

Page of Accessories

PCB Mark Point



Mechanical Hole



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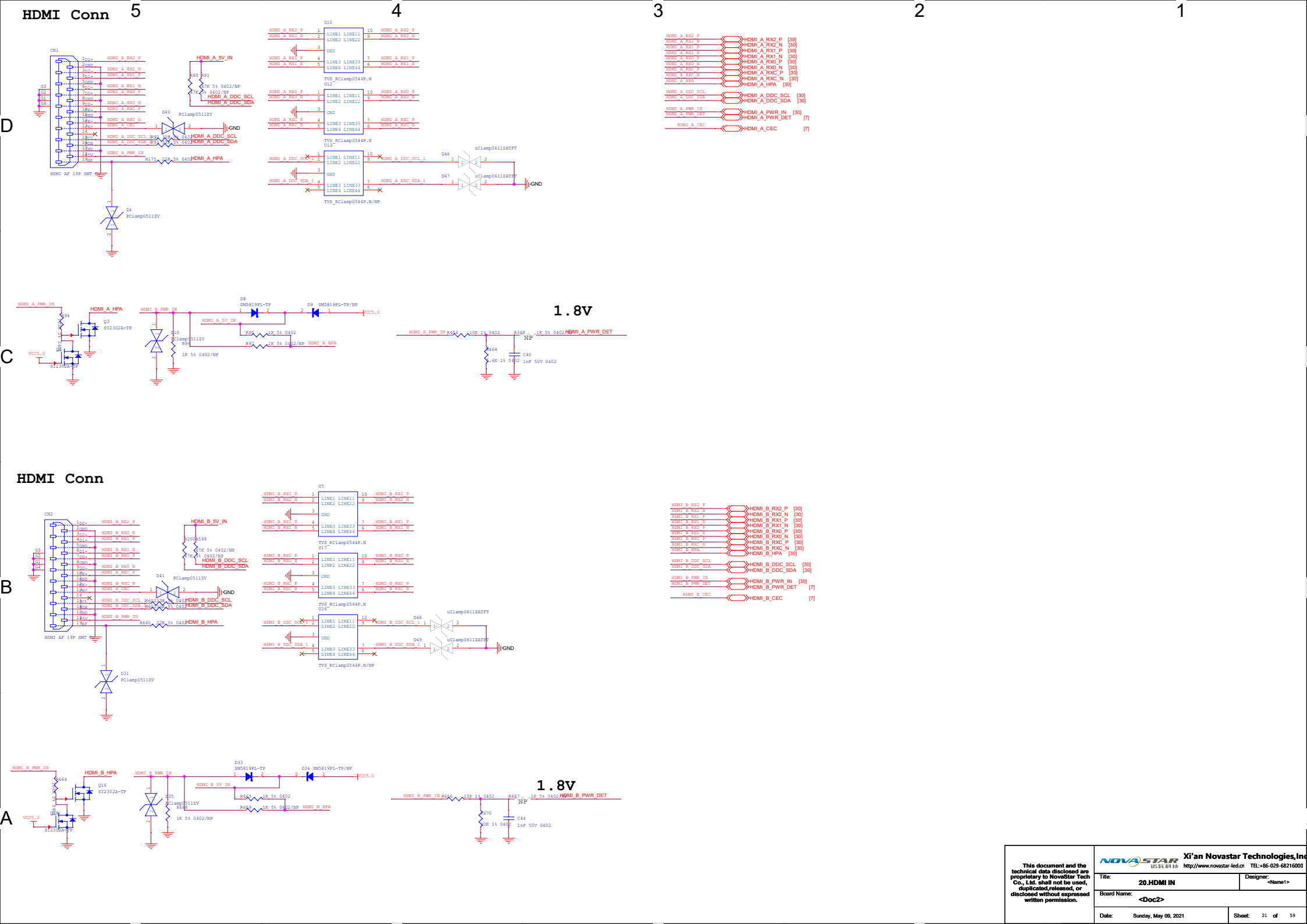
Title: 19.Mark/Hole

Designer: <Name1>

Board Name: <Doc2>

Date: Wednesday, February 03, 2021

Sheet: 20 of 59


HDMI Conn
5
4
3
2
1
D
C
B
A
HDMI_A_5V_IN
HDMI_A_DDC_SCL
HDMI_A_DDC_SDA
HDMI_A_HPA
HDMI_A_PWR_IN
HDMI_A_PWR_DET
HDMI_A_CEC
1.8V
HDMI Conn
HDMI_B_5V_IN
HDMI_B_DDC_SCL
HDMI_B_DDC_SDA
HDMI_B_HPA
HDMI_B_PWR_IN
HDMI_B_PWR_DET
HDMI_B_CEC
1.8V
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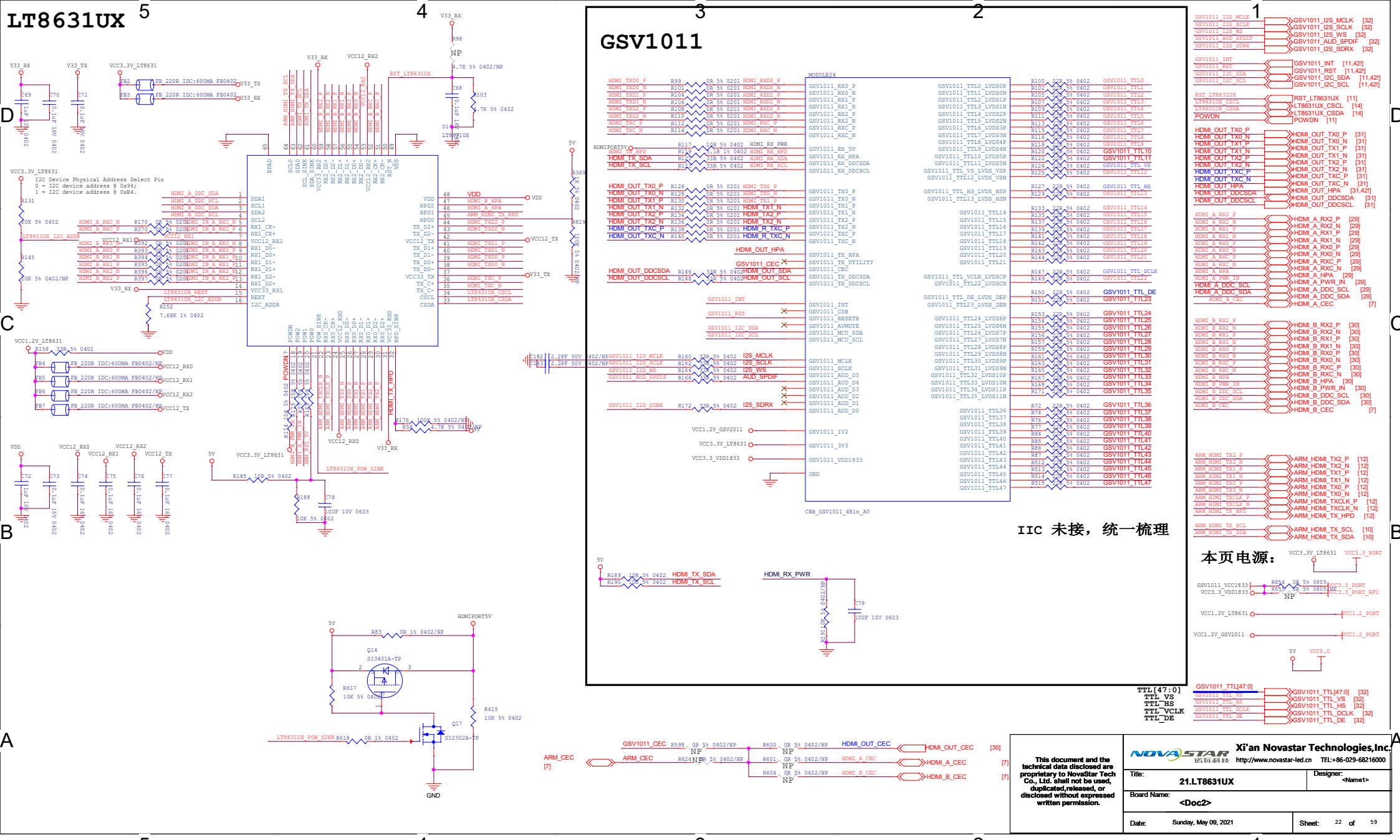
Title: 20.HDMI IN
Designer: <Name1>
Board Name: <Doc2>
Date: Sunday, May 09, 2021
Sheet: 21 of 59


LT8631UX
GSV1011
IIC 未接，统一梳理
本页电源：
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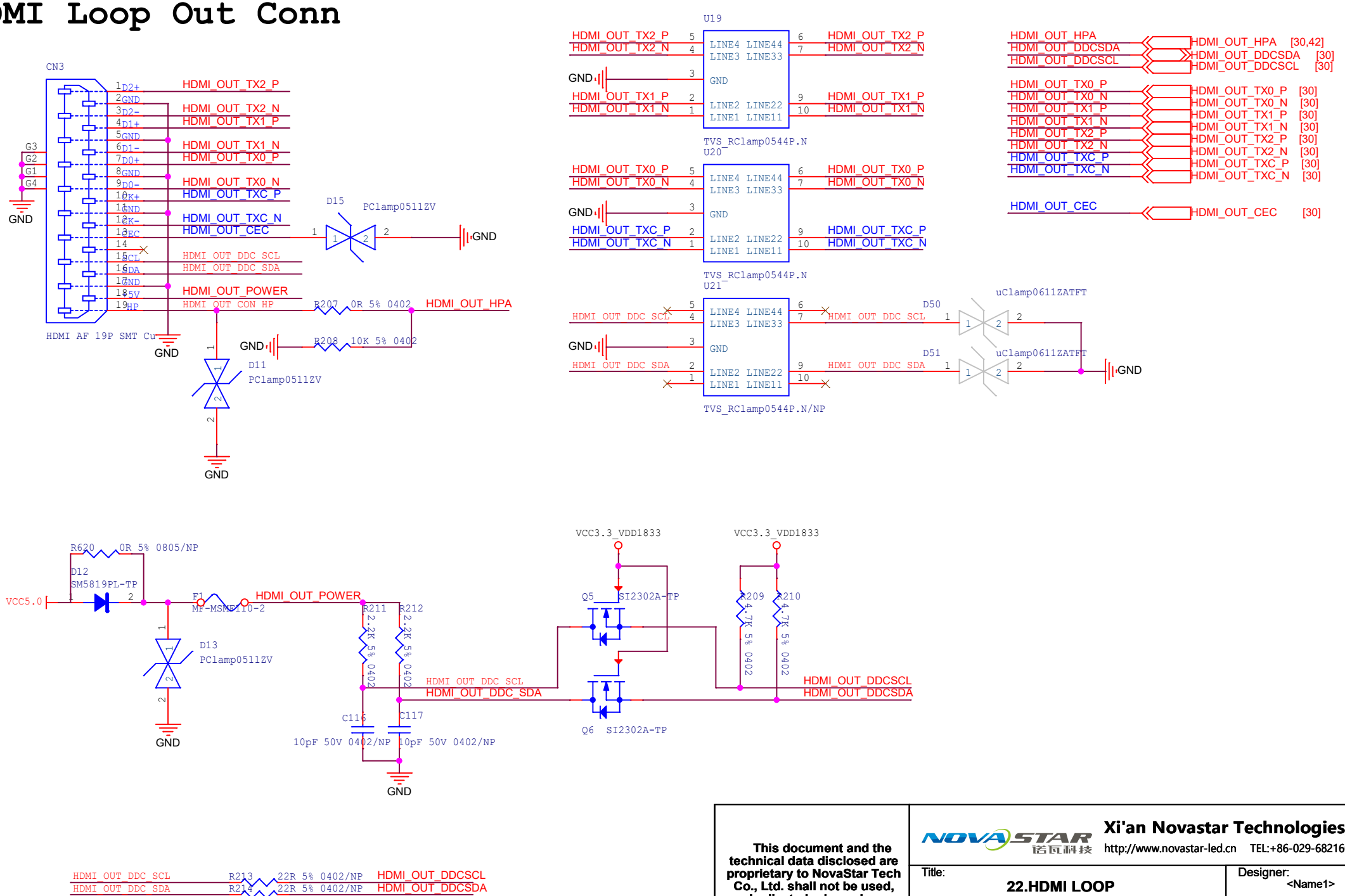
Title: 21.LT8631UX
Designer: <Name1>
Board Name: <Doc2>
Date: Sunday, May 09, 2021
Sheet: 22 of 59

HDMI Loop Out Conn



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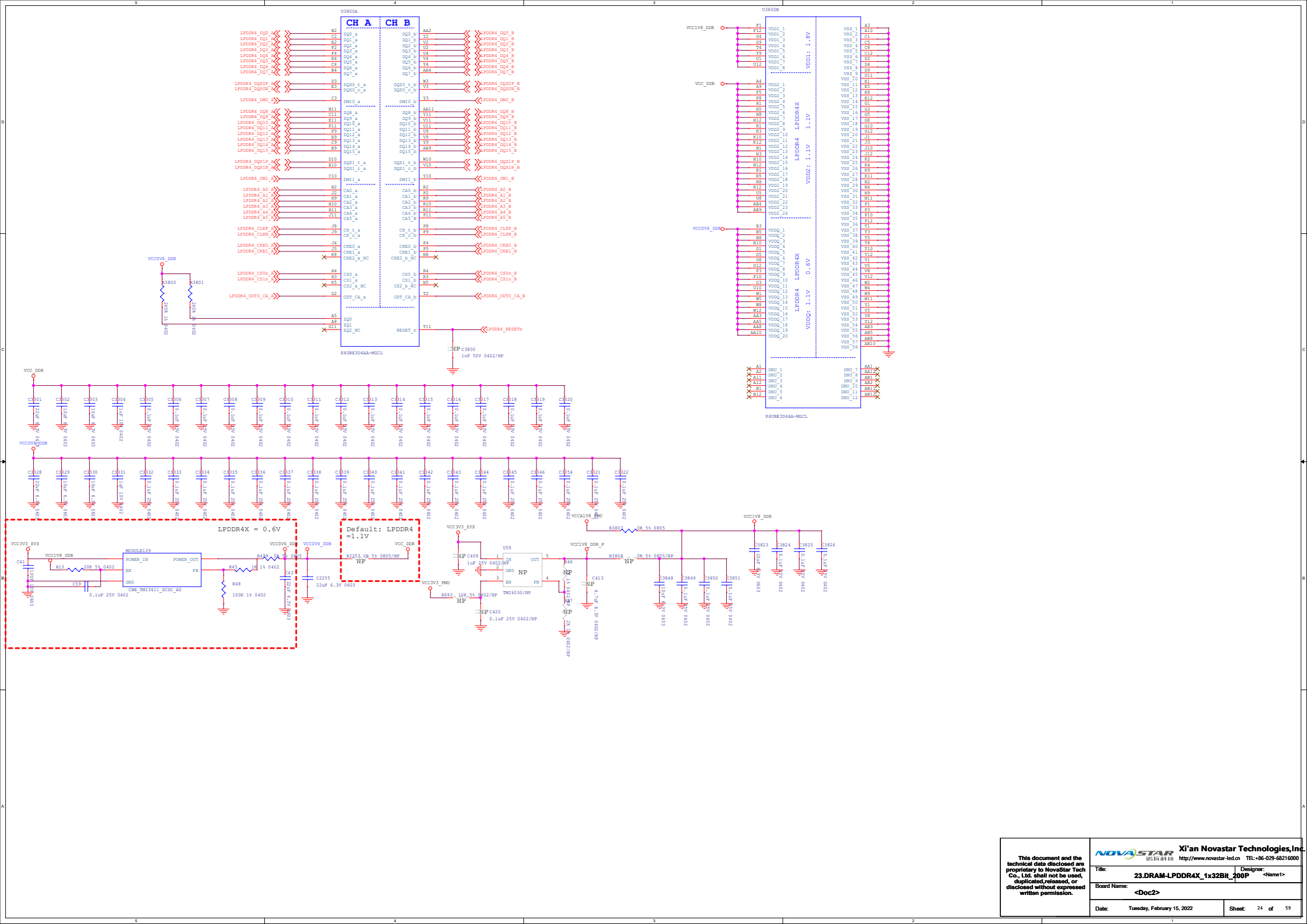
Title: 22.HDMI LOOP	Designer: <Name1>
Board Name: <Doc2>	
Date: Sunday, May 09, 2021	Sheet: 23 of 59



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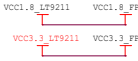
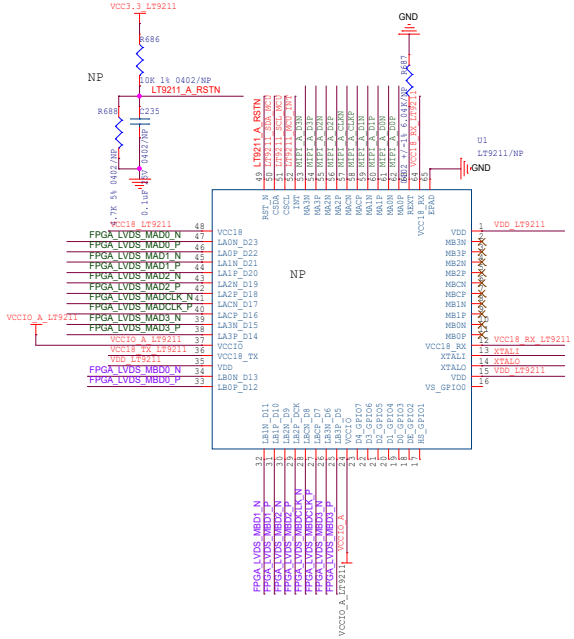
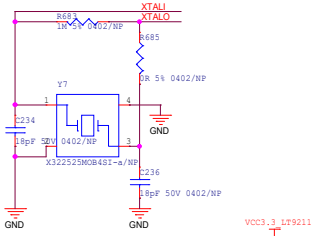
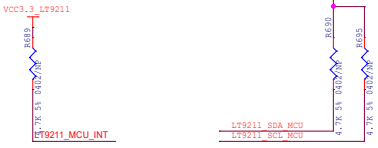
Title:	23.DRAM-LPDDR4X_1x32Bit_200P
Designer:	<Name1>
Board Name:	<Doc2>
Date:	Tuesday, February 15, 2022
Sheet:	24 of 59

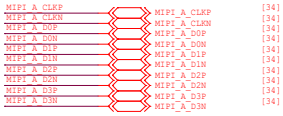
使用的电源

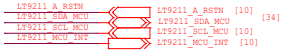


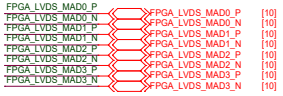


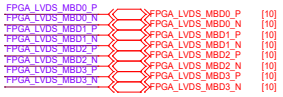


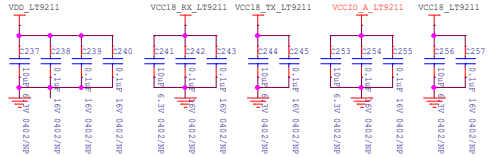


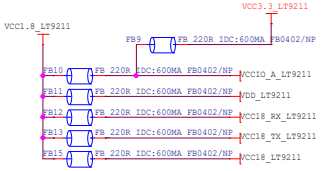












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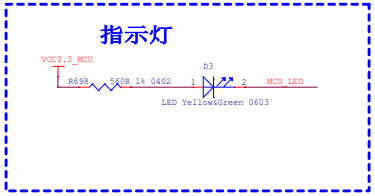
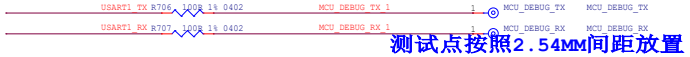
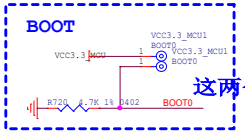
Title: 24.LVDS_MIPI_LT9211	Designer: <Name1>
Board Name: <Doc2>	
Date: Tuesday, February 15, 2022	Sheet: 25 of 59

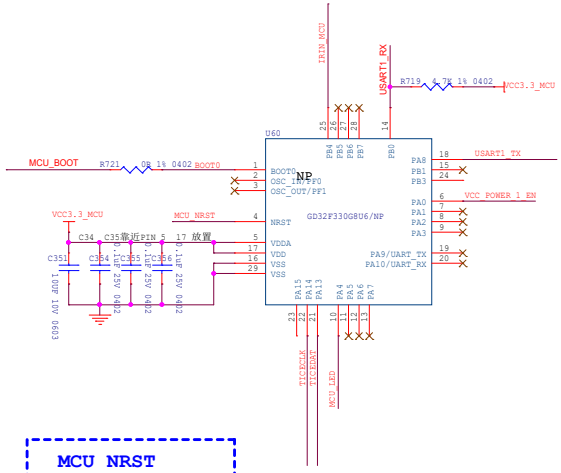


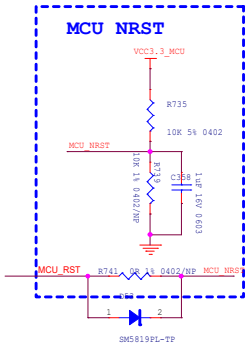


测试点按照2.54mm间距放置



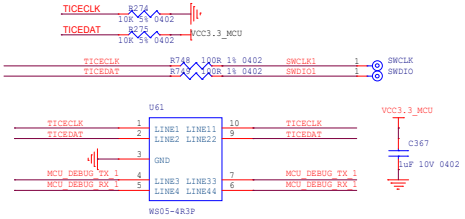
这两个测试点按照2.54mm间距放置

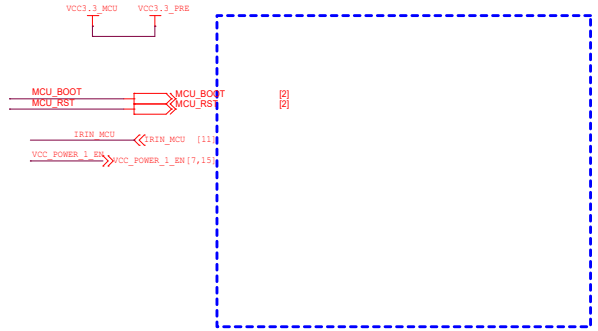




SWD

信号上标注丝印





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Title: 25.MCU_GDF330	Designer: <Name1>
Board Name: <Doc2>	
Date: Tuesday, February 15, 2022	Sheet: 26 of 59

Power In

5A max for each MOS

兼容设计

BOM中使用108010024

5.0V

Vout==0.8*（1+R1/R2）

Imax==5A

3.3V

3.3V/5V
default 5V

5.0V

输出3.3V

输出3.3V

VDD_CPU_EXT

内部芯片修改为113020022

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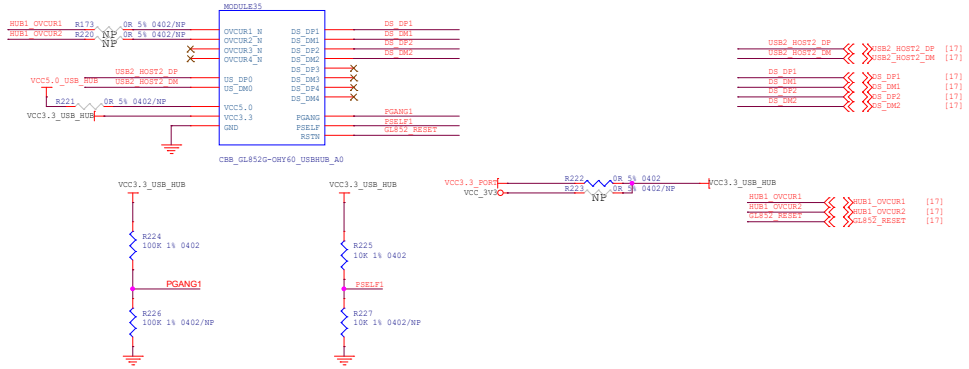
Title:	26.POWER
Designer:	<Name1>
Board Name:	<Doc2>
Date:	Wednesday, February 16, 2022
Sheet:	27 of 59



Xi'an Novastar Technologies,Inc.
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Title: 27.USB_HUB

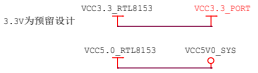
Designer: <Name1>

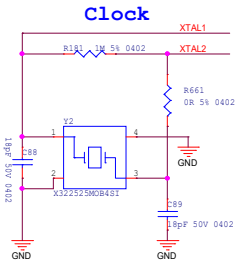
Board Name: <Doc2>

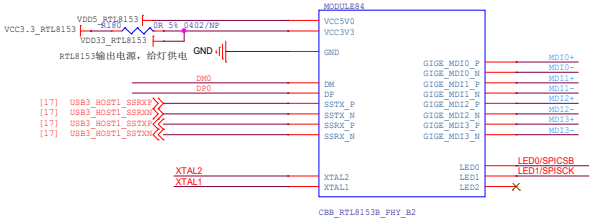
Date: Wednesday, August 17, 2022

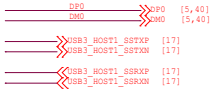
Sheet: 28 of 59

USB TO ETH

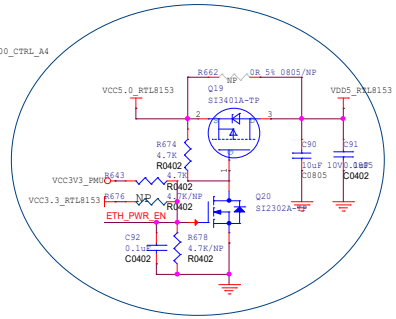


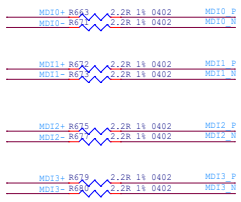


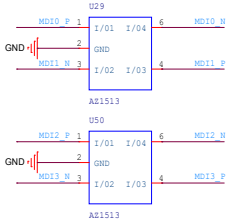


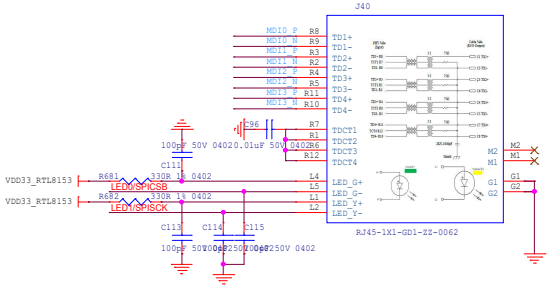


增加RTL8153电源控制,ARM控制,cankao VPR1000_CTRL_A4









LED灯默认不亮，默认管脚的默认状态为低

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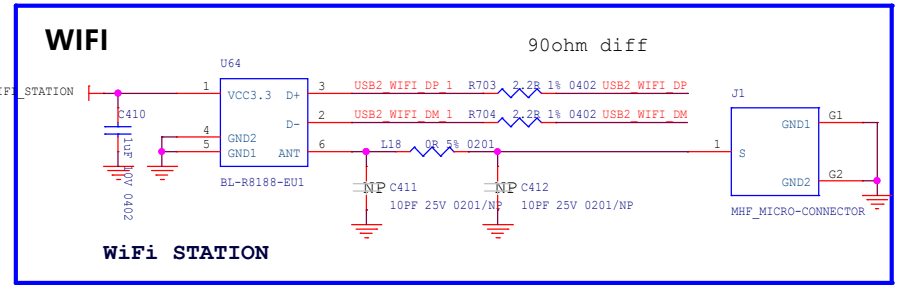
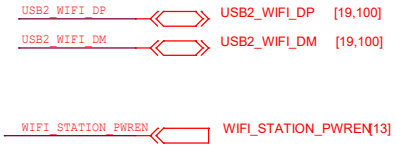
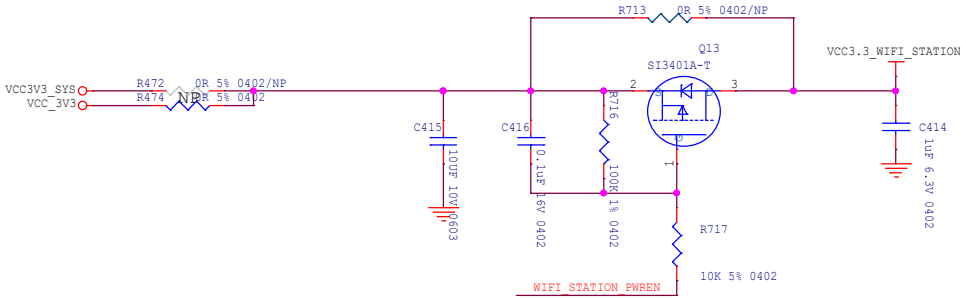
Title: 28.USB_ETH_RTL8153		Designer: <Name1>
Board Name: <Doc2>		
Date: Tuesday, February 15, 2022	Sheet: 29 of 59	





NP



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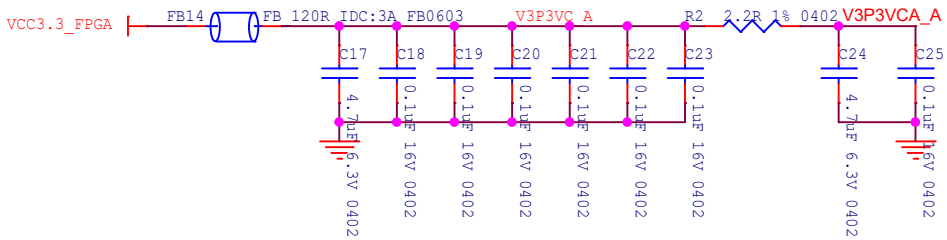
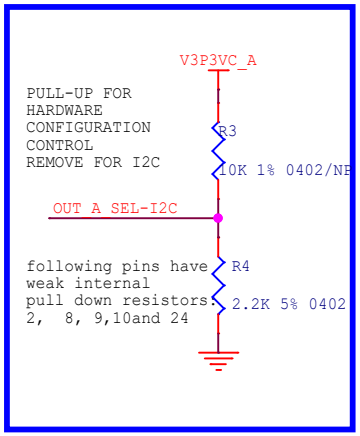
Title:	29.WIFI-STATION-USB_1T1R	Designer: <Name1>
Board Name:	<Doc2>	
Date:	Wednesday, February 16, 2022	Sheet: 30 of 59

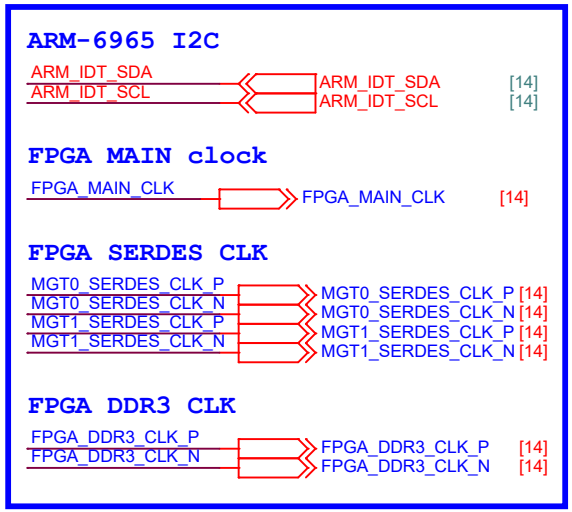
Clock

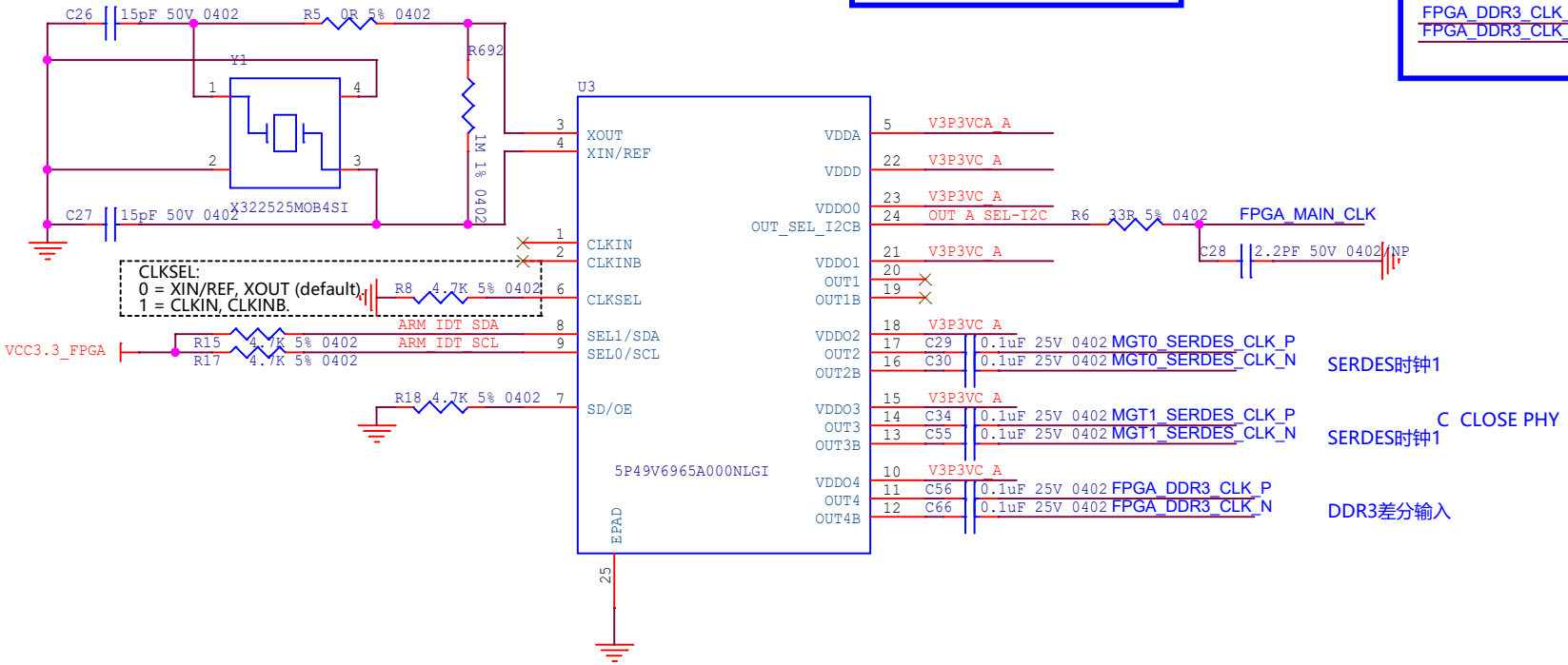
If a weak pull-down (10k?) is placed on OUT0_SEL_I2CB or it is left floating, pins 8 and 9 will act as the SDA and SCL pins of an I2C interface.

FPGA_CLK所需电源：VCC3.3_FPGA









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Title:	30.FPGA-CLK		
Size: A4	Project: S50C_E0	Document Number: <Doc2>	Rev: <Rev>
Designer: WX	CHKD: <Name2>	SUPV: <Name3>	
Date: Friday, August 26, 2022	Sheet: 31 of 59		

FPGA_IO所需电源：VCC1.8_FPGA、VCC3.3_FPGA、VCC2.5_FPGA、GSV1011_VCC1833

CFG MODE	M[2:0]
Master serial	000
Master SPI	001
Slave Serial	111

JTAG_FPGA

FPGA_CFG

FPGA LED

FPGA-ARM RGMII

Close to FPGA

FPGA-ARM DVP

该部分电阻靠近FPGA放置

FPGA-ARM RGMII

FPGA-ARM UART

FPGA MAIN clock

AUDIO IN&OUT*1

6.5G LOS信号

TTL OUT

FPGA-ARM CIF

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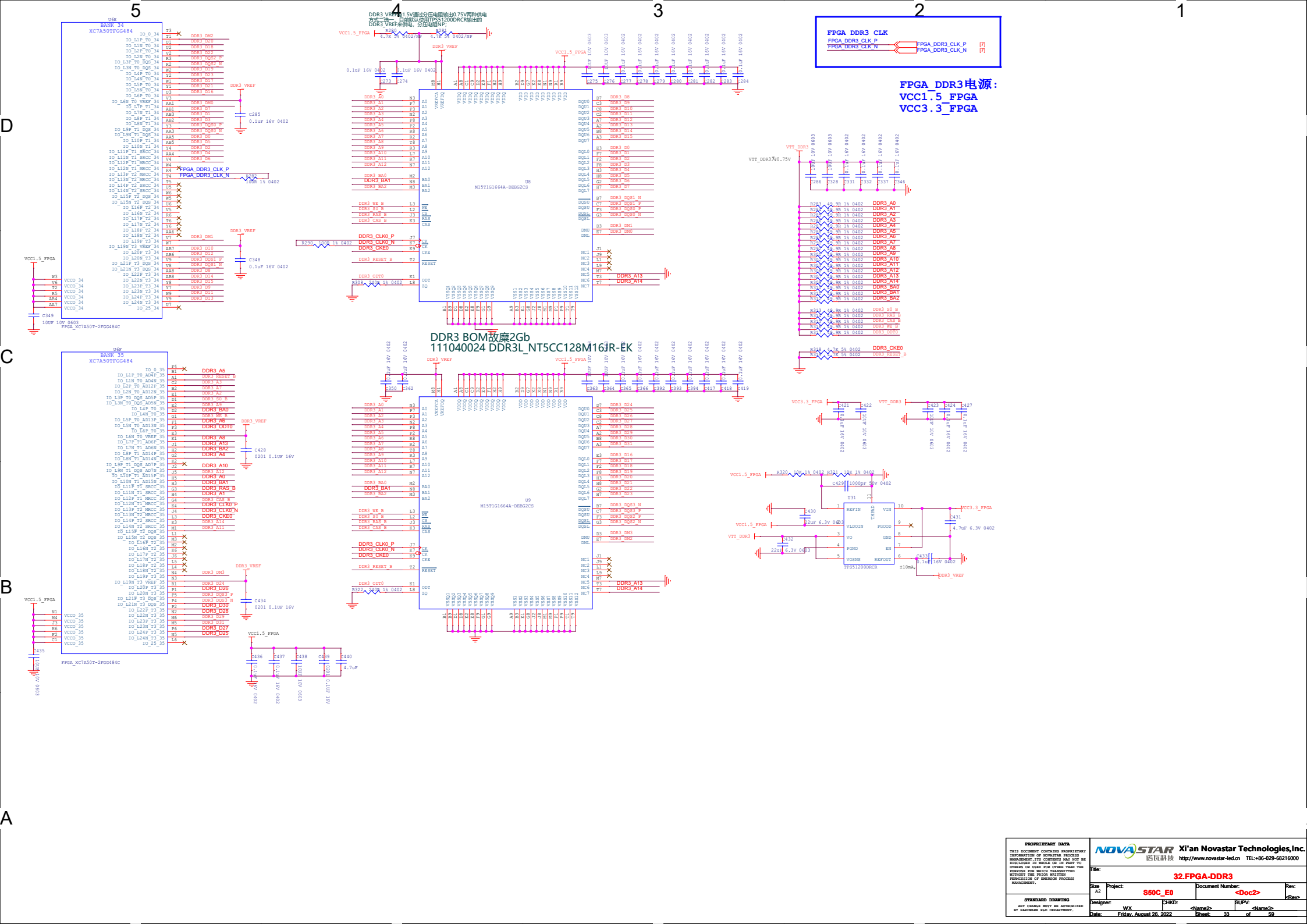
Title:	31.FPGA4O
Designer:	<Name1>
Board Name:	<Doc2>
Date:	Friday, February 18, 2022
Sheet:	32 of 59



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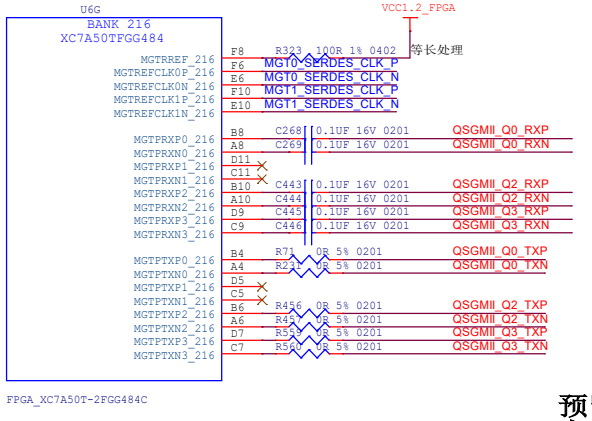
Title: 32.FPGA-DDR3

Size	Project	Document Number	Rev
A2	S50C_E0	<Doc2>	<Rev>

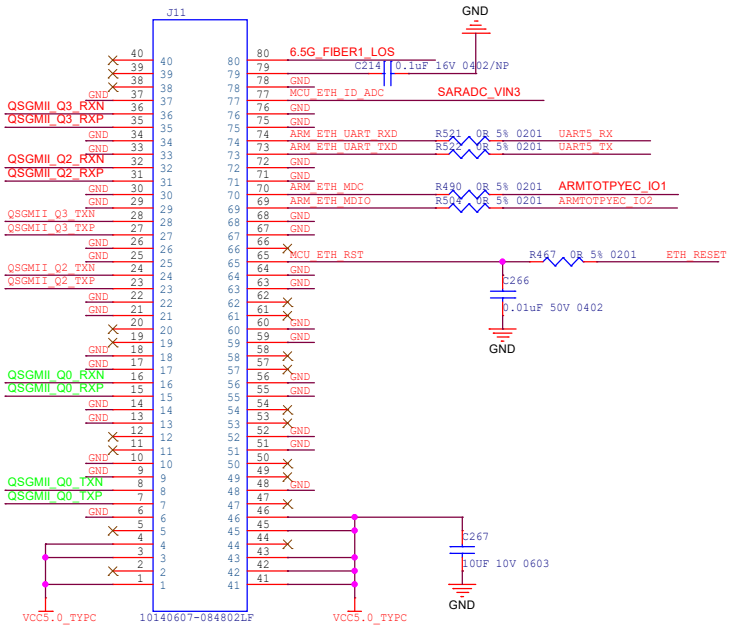
Designer	CHKD:	SUPV:
WX	<Name2>	<Name3>

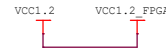
Date: Friday, August 26, 2022 Sheet: 33 of 59

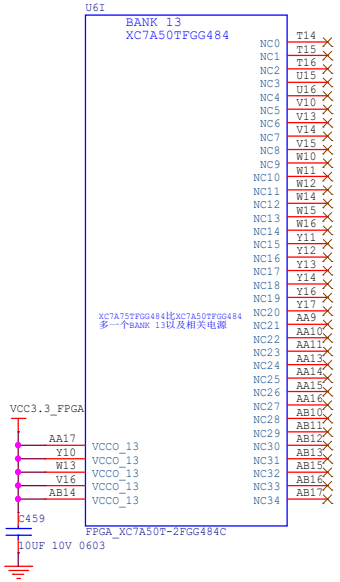
FPGA_SERDES电源：
VCC5.0_TYPC
VCC1.2_FPGA

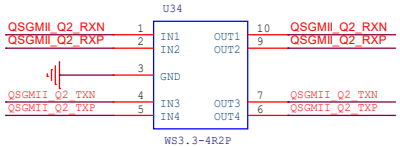


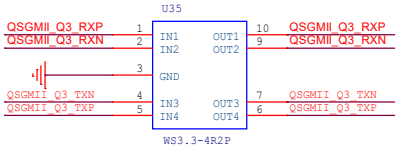
预留QSGMII接网口板上增加的6.5G光口

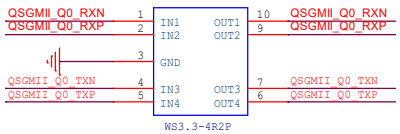


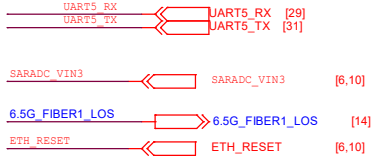












FPGA SERDES CLK

MGT0_SERDES_CLK_P	MGT0_SERDES_CLK_P [6,10]
MGT0_SERDES_CLK_N	MGT0_SERDES_CLK_N [6,10]
MGT1_SERDES_CLK_P	MGT1_SERDES_CLK_P [6,10]
MGT1_SERDES_CLK_N	MGT1_SERDES_CLK_N [6,10]

ARM IO

ARMTOTPYEC_IO1	ARMTOTPYEC_IO1 [6,10]
ARMTOTPYEC_IO2	ARMTOTPYEC_IO2 [6,10]

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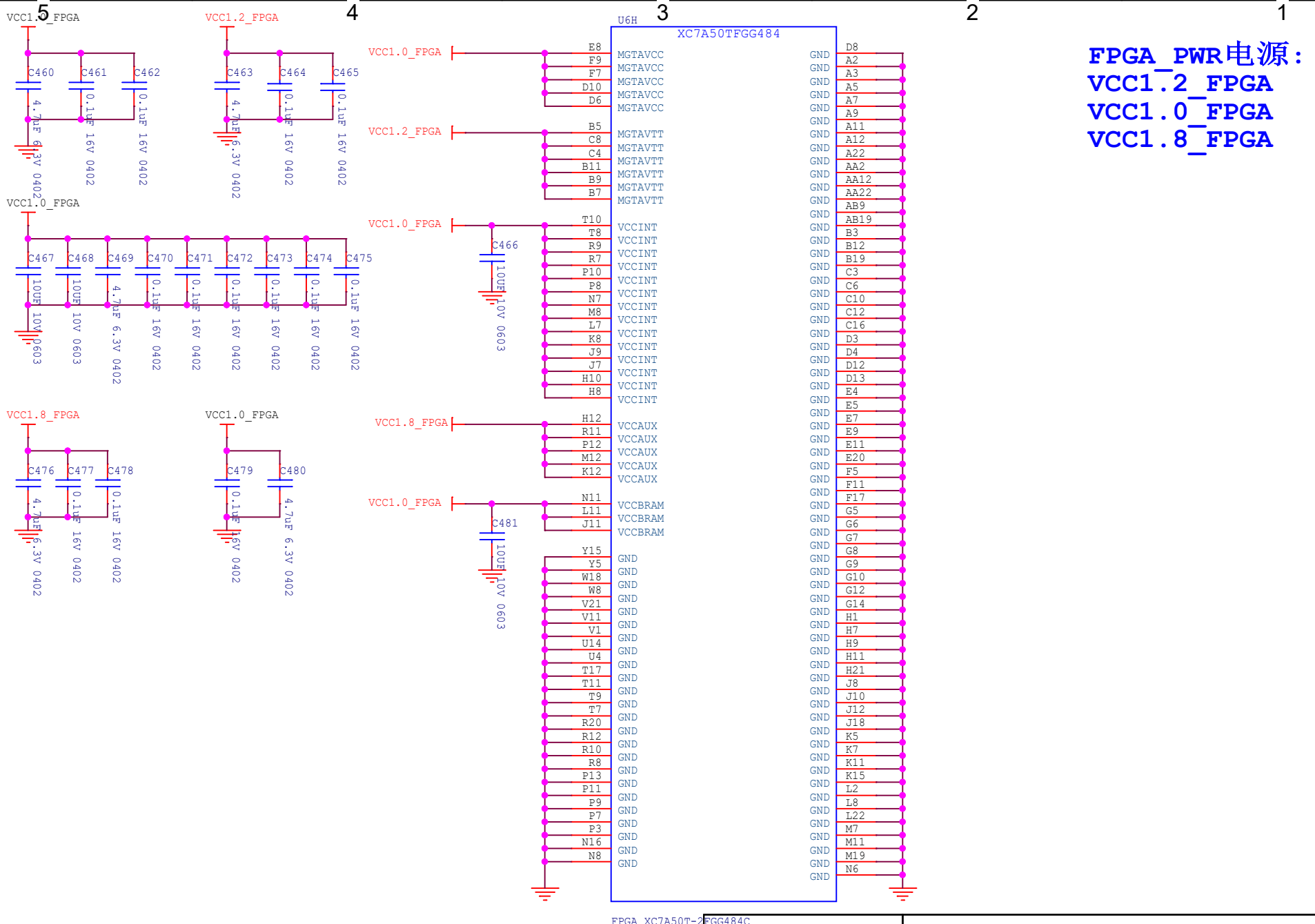
Title:	33.FPGA-SERDES
Designer:	<Name1>
Board Name:	<Doc2>
Date:	Friday, February 18, 2022
Sheet:	34 of 59



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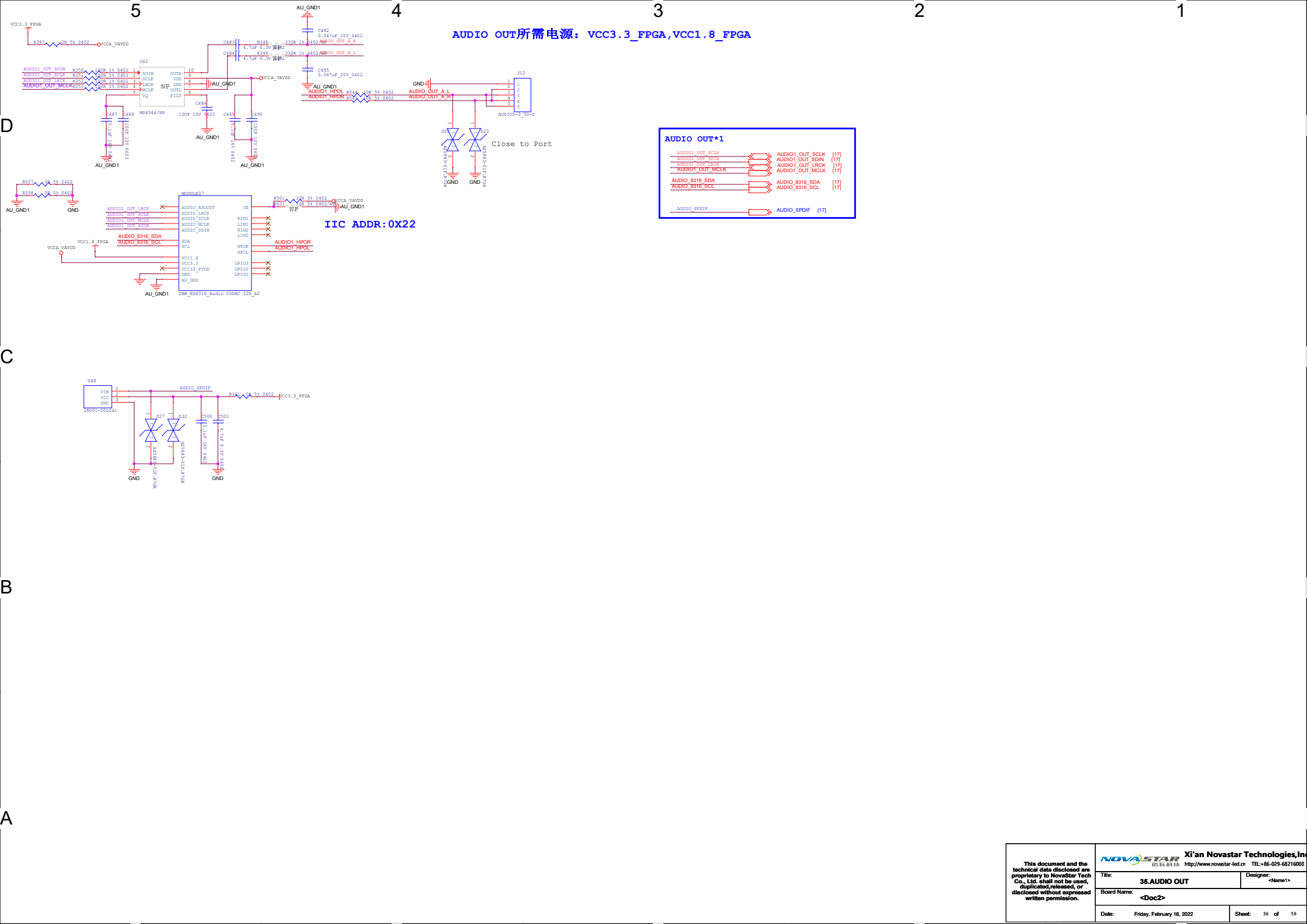
Title: 34.FPGA-PWR

Size	Project	Document Number	Rev
A4	S50C_E0	<Doc2>	<Rev>

Designer	CHKD	SUPV
WX	<Name2>	<Name3>

Date: Friday, August 26, 2022 Sheet: 35 of 59


AUDIO OUT所需电源：VCC3.3_FPGA,VCC1.8_FPGA
IIC ADDR:0X22
Close to Port
AUDIO OUT*1
AUDIO1_OUT_SCLK [17]
AUDIO1_OUT_SDIN [17]
AUDIO1_OUT_LRCK [17]
AUDIO1_OUT_MCLK [17]
AUDIO_8316_SDA [17]
AUDIO_8316_SCL [17]
AUDIO_SPDIF [17]
MS4344/NP
CBB_ES8316_Audio CODEC I2S_A0
28001-001041
AUDIO5-3_50-D
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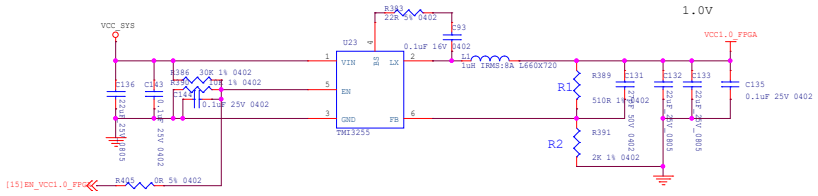
Title: 35.AUDIO OUT
Designer: <Name1>
Board Name: <Doc2>
Date: Friday, February 18, 2022
Sheet: 36 of 59

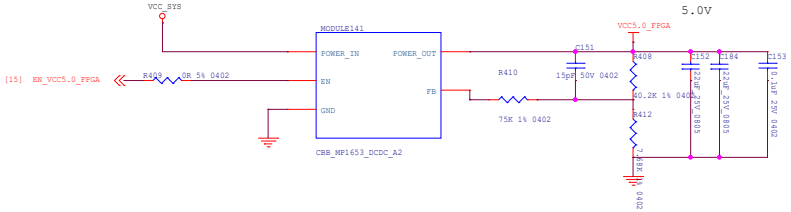
Vout==0.8* (1+R1/R2)

Imax==5A

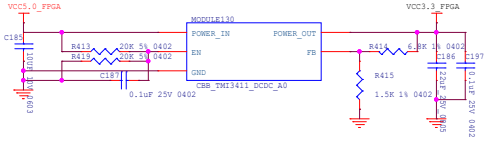
1.0V



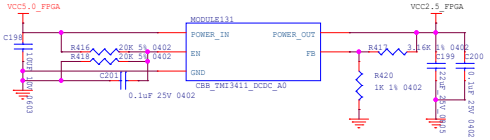
5.0V



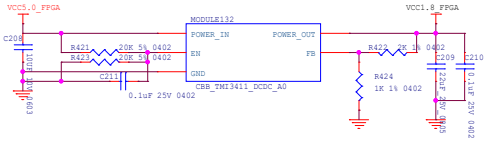
3.3V



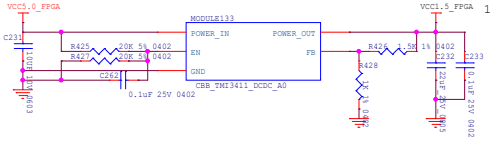
2.5V



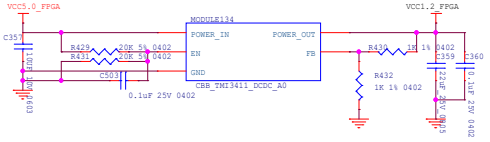
1.8V

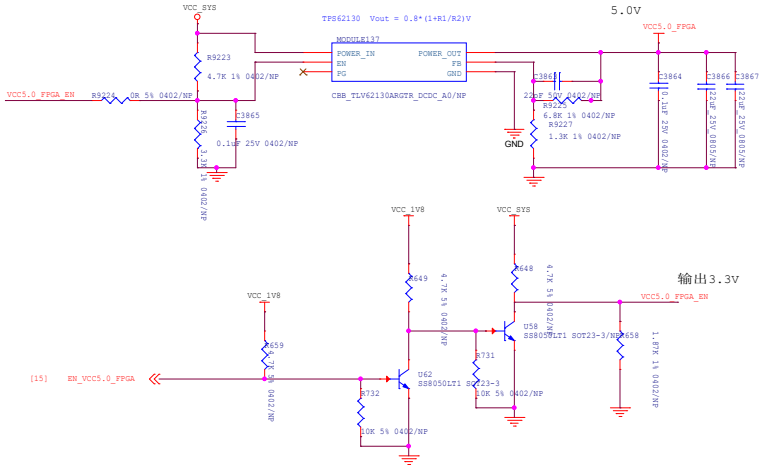


1.5V



1.2V





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Title: 36.FPGA-POWER	Designer: <Name1>
Board Name: <Doc2>	
Date: Friday, February 18, 2022	Sheet: 37 of 59