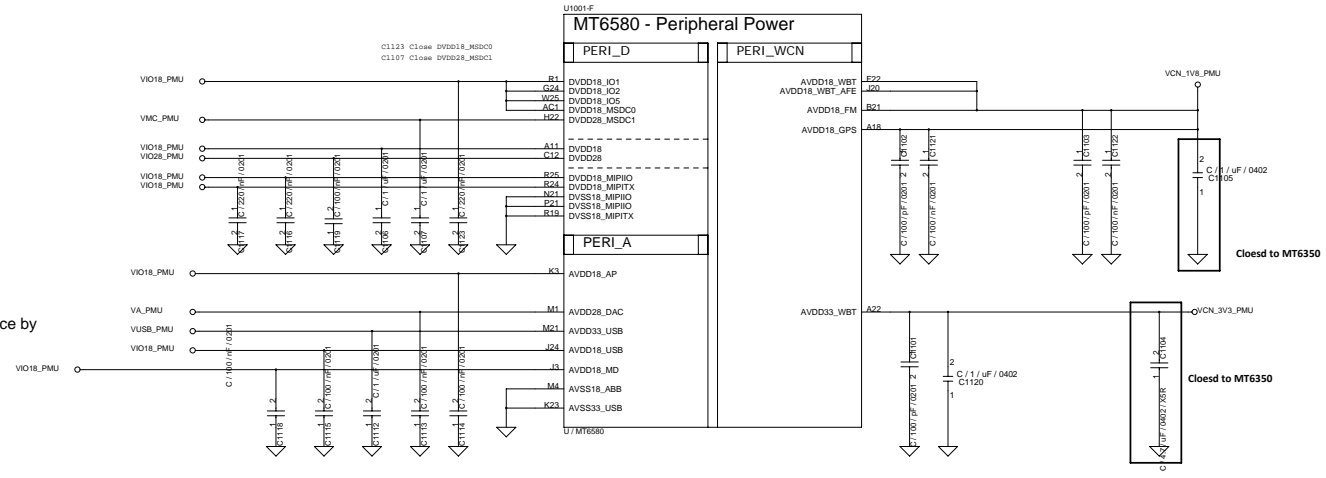
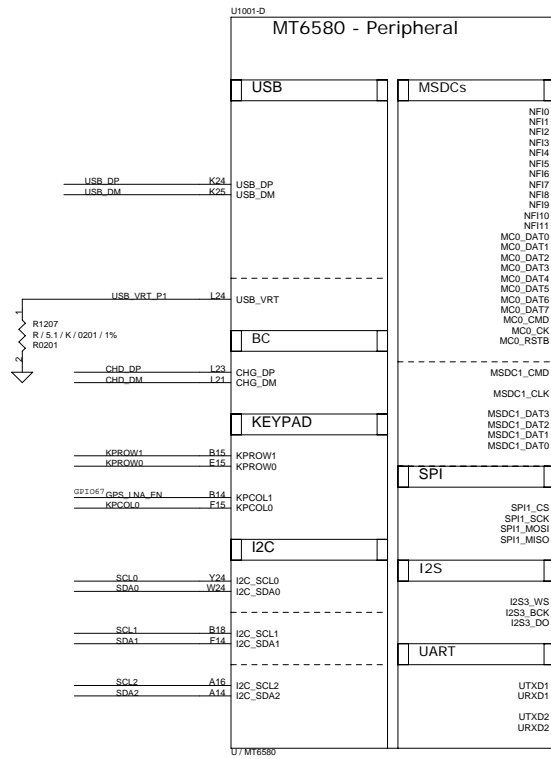


AVDD28_DAC change power source by "VA_PMU".

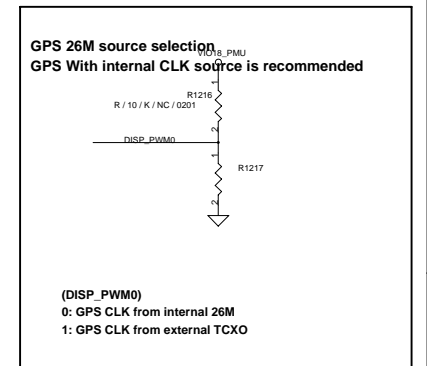
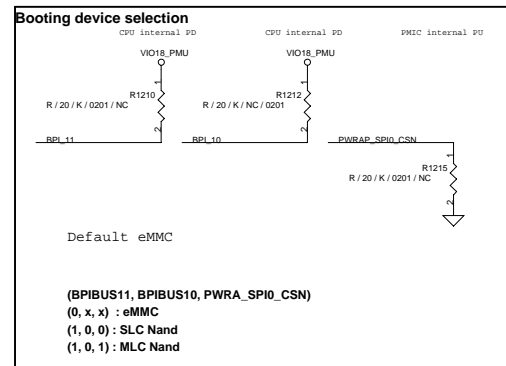


USB	(64) USB_DP << USB_DP (64) USB_DM << USB_DM
BC 1.1	(20) CHD_DM << CHD_DM (20) CHD_DP << CHD_DP
KP IF	(65) KPCOL0 << KPCOL0 (65) KPROW0 << KPROW0 (65) KPROW1 << KPROW1
I2C IF	(62) SCL0 << SCL0 (62) SDA0 << SDA0 (61) SCL1 << SCL1 (61) SDA1 << SDA1 (23,63) SCL2 << SCL2 (23,63) SDA2 << SDA2
eMMC	(40) MSDC0_CMD << MSDC0_CMD (40) MSDC0_RSTB << MSDC0_RSTB (40) MSDC0_CLK << MSDC0_CLK
MSDC IF	(41) MSDC1_CMD << MSDC1_CMD (41) MSDC1_CLK << MSDC1_CLK (41) MSDC1_DAT3 << MSDC1_DAT3 (41) MSDC1_DAT2 << MSDC1_DAT2 (41) MSDC1_DAT1 << MSDC1_DAT1 (41) MSDC1_DAT0 << MSDC1_DAT0
UART	
Camera IF	
Main Cam MIPSI_CSI	(62) RCP << RCP (62) RCN << RCN (62) RDP0 << RDP0 (62) RDNO << RDNO (62) RDP1 << RDP1 (62) RDN1 << RDN1 (62) RDP2 << RDP2 (62) RDN2 << RDN2 (62) RDN3 << RDN3
Main Cam control	(62) CAM_CLK0 << CAM_CLK0 (62) CAM_RST0 << CAM_RST0 (62) CAM_PDN0 << CAM_PDN0
Front Cam MIPSI_CSI	(62) RCP_A << RCP_A (62) RCN_A << RCN_A (62) RDP0_A << RDP0_A (62) RDNO_A << RDNO_A (62) RDP1_A << RDP1_A (62) RDN1_A << RDN1_A
Front Cam control	(62) CAM_CLK1 << CAM_CLK1 (62) CAM_RST1 << CAM_RST1 (62) CAM_PDN1 << CAM_PDN1

LCD IF	MIPSI_DSI (61) TCP << TCP (61) TCN << TCN (61) TDP0 << TDP0 (61) TDN0 << TDN0 (61) TDP1 << TDP1 (61) TDN1 << TDN1 (61) TDP2 << TDP2 (61) TDN2 << TDN2
Control interface	(65) LCM_RST << LCM_RST (61) DSI_TE << DSI_TE (23) DISP_PWM0 << DISP_PWM0
CTP IF	(61) CTP_RSTB << CTP_RSTB
LPDDR2 x32	
Data & Address	(40) ECKE << ECKE (40) EDCLK_B << EDCLK_B
Command	(40) ECKE << ECKE
Clock	(40) EDCLK << EDCLK (40) EDCLK_B << EDCLK_B
VREF	(40) EVREF << EVREF
Chip select	(40) ECS0_B << ECS0_B (40) ECS1_B << ECS1_B
DQM	(40) EDQM0 << EDQM0 (40) EDQM1 << EDQM1 (40) EDQM2 << EDQM2 (40) EDQM3 << EDQM3
DQS	(40) EDQS0 << EDQS0 (40) EDQS1 << EDQS1 (40) EDQS2 << EDQS2 (40) EDQS3 << EDQS3
DQS_B	(40) EDQS0_B << EDQS0_B (40) EDQS1_B << EDQS1_B (40) EDQS2_B << EDQS2_B (40) EDQS3_B << EDQS3_B
Interrupt	MEMS Sensor (63) EINT_PS << EINT_PS (63) EINT_GY << EINT_GY (63) EINT_MAG << EINT_MAG
Headphone plug	(60) EINT_EAR << EINT_EAR
CTP interrupt	(61) EINT_CTP << EINT_CTP
MSDC Card detect	(41) EINT_SD << EINT_SD
GPIO IF	GPS enable (50) GPS_LNA_EN << GPS_LNA_EN
Flash LED 5V Boost	(23) GPIO_FLASH_STB << GPIO_FLASH_STB (23) GPIO_FLASH_EN << GPIO_FLASH_EN



Note: 12-1



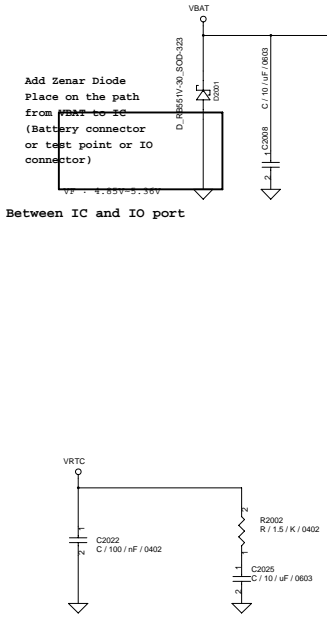
Schematic design notice of "12_BB_2" page.

- Note 12-1:
- Do not use UART1 as Power solution enable.
 - Do not use UART2 as power solution enable, if select UART1 as D/L or calibration path,

Audio IF	
Downlink	
(60) AU_SPKP	AU_SPKP
(60) AU_SPKN	AU_SPKN
(60) AU_HPL	AU_HPL
(60) AU_HPR	AU_HPR
(60) AU_HSP	AU_HSP
(60) AU_HSN	AU_HSN
Uplink	
(60) AU_VIND_P	AU_VIND_P
(60) AU_VIND_N	AU_VIND_N
(60) AU_VIN1_P	AU_VIN1_P
(60) AU_VIN1_N	AU_VIN1_N
(60) AU_VIN2_P	AU_VIN2_P
(60) AU_VIN2_N	AU_VIN2_N
HP detect	
(60) ACCDET	ACCDET
Vcore FB	
(10) VPROC_FB	VPROC_FB
(10) GND_VPROC_FB	GND_VPROC_FB
AP to PMIC IF	
Audio IF	
(11) AUD_CLK_MOSI	AUD_CLK_MOSI
(11) AUD_DAT_MOSI	AUD_DAT_MOSI
(11) AUD_DAT_MISO	AUD_DAT_MISO
PMIC_SPI IF	
(11) PWRAP_SPI_CS_N	PWRAP_SPI_CS_N
(11) PWRAP_SPI_CK	PWRAP_SPI_CK
(11) PWRAP_SPI_M0	PWRAP_SPI_M0
(11) PWRAP_SPI_M1	PWRAP_SPI_M1
Misc	
(11) SRCLENAG	SRCLENAG
(11) ENT_PMIC	ENT_PMIC
(11) WATCHDOG	WATCHDOG
(11) SYSRSTB	SYSRSTB
CLK	
(31) CLK4_AUDIO	CLK4_AUDIO
(11) CLK32K_BB	CLK32K_BB
(31) OUT_32K	OUT_32K
BC 1.1	
(12) CHD_DM	CHD_DM
(12) CHD_DP	CHD_DP
CO-TSX	
(20,21,31) AUXADC_REF	AUXADC_REF
(31) AUXADC_TSY	AUXADC_TSY
(31) GND_AUXADC	GND_AUXADC
SIM IF	
(11) SIM1_SCLK	SIM1_SCLK
(11) SIM1_SIO	SIM1_SIO
(11) SIM2_SCLK	SIM2_SCLK
(11) SIM2_SIO	SIM2_SIO
(65) SCLK1	SCLK1
(65) SIO1	SIO1
(65) SRST1	SRST1
(65) SCLK2	SCLK2
(65) SIO2	SIO2
(65) SRST2	SRST2
(65) PWRKEY	PWRKEY
Charger IF	
(21) CHR_LDO	CHR_LDO
(21) VCDT	VCDT
(21) VDRV	VDRV
(21) ISENSE	ISENSE
(21) BATSNS	BATSNS
(20,21,31)AUXADC_REF	AUXADC_REF
(21) BAT_ON	BAT_ON

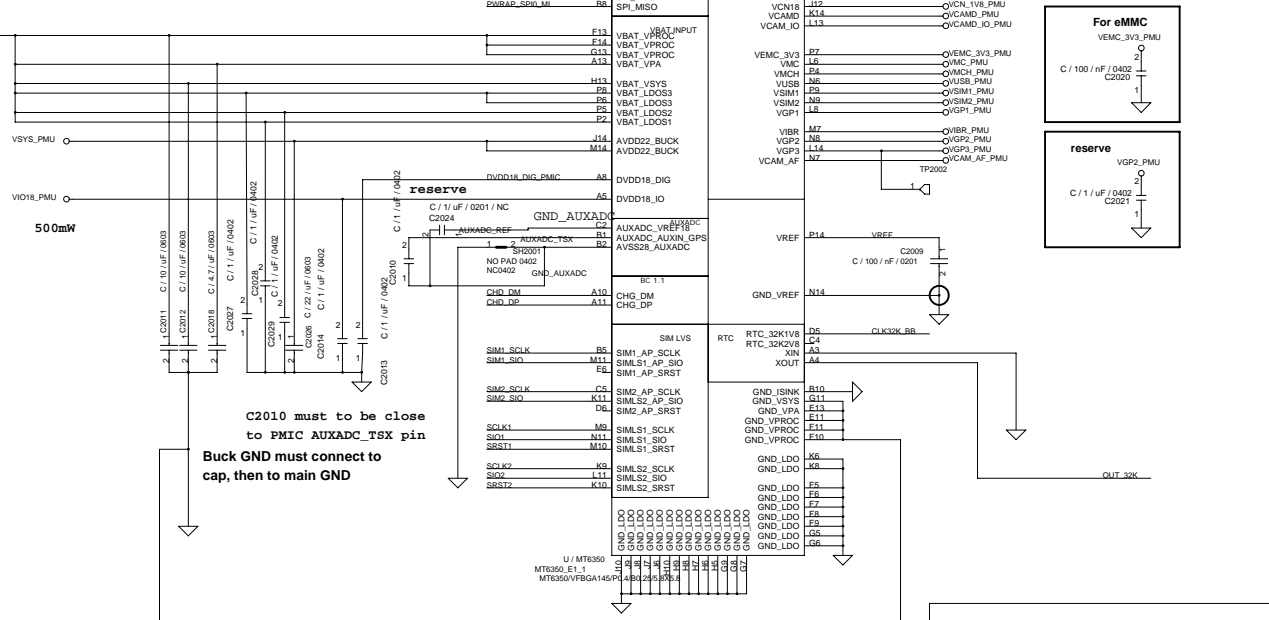
Add Zener Diode
Place on the path
from VBAT to IC
(Battery connector
or test point or IO
connector)

Between IC and IO port

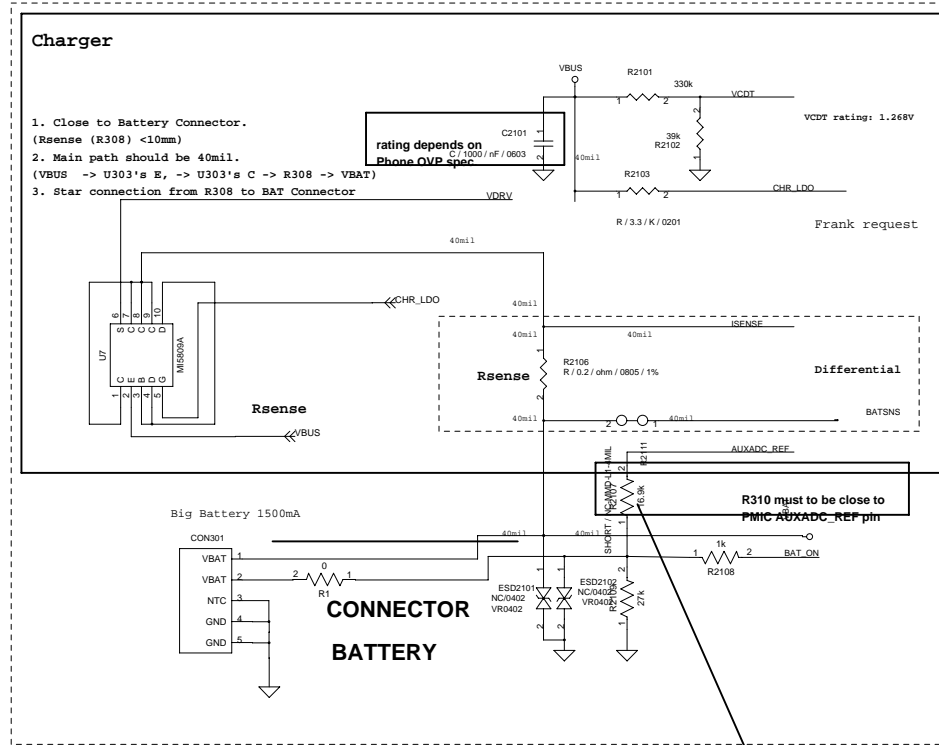
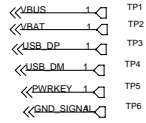
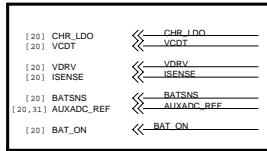


500mW

C2010 must be close
to PMIC AUXADC_TSY pin
Buck GND must connect to
cap, then to main GND



Charger IF



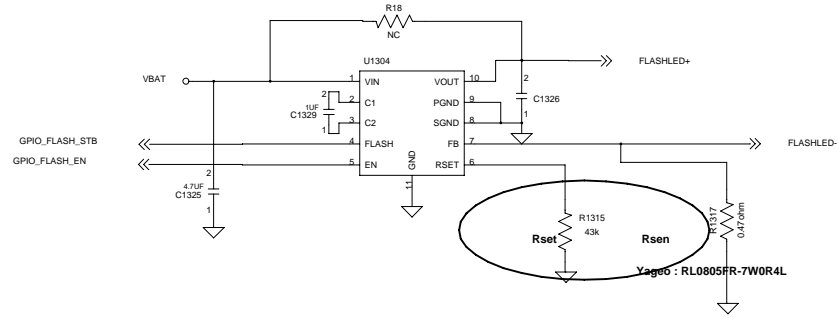
if battery NTC is 10kohm, R310=16.9K, R312=27K
 if battery NTC is 47kohm, R310=61.9K, R312=100K
 Refer to MT6350 HW design notice

Flash LED 5V Boost

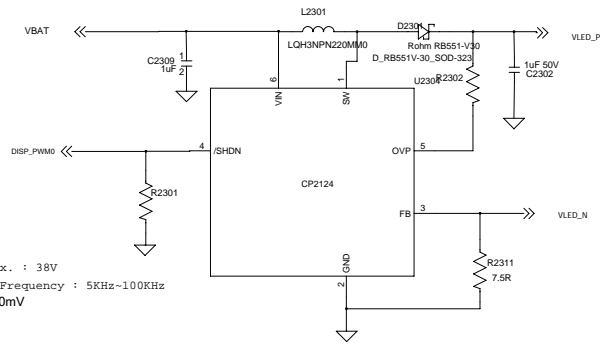
[12] GPIO_FLASH_STB << GPIO_FLASH_STB
 [12] GPIO_FLASH_EN << GPIO_FLASH_EN
 [12, #3] SCL2 << SCL2
 [12, #3] SDA2 << SDA2

LCM Backlight Driver

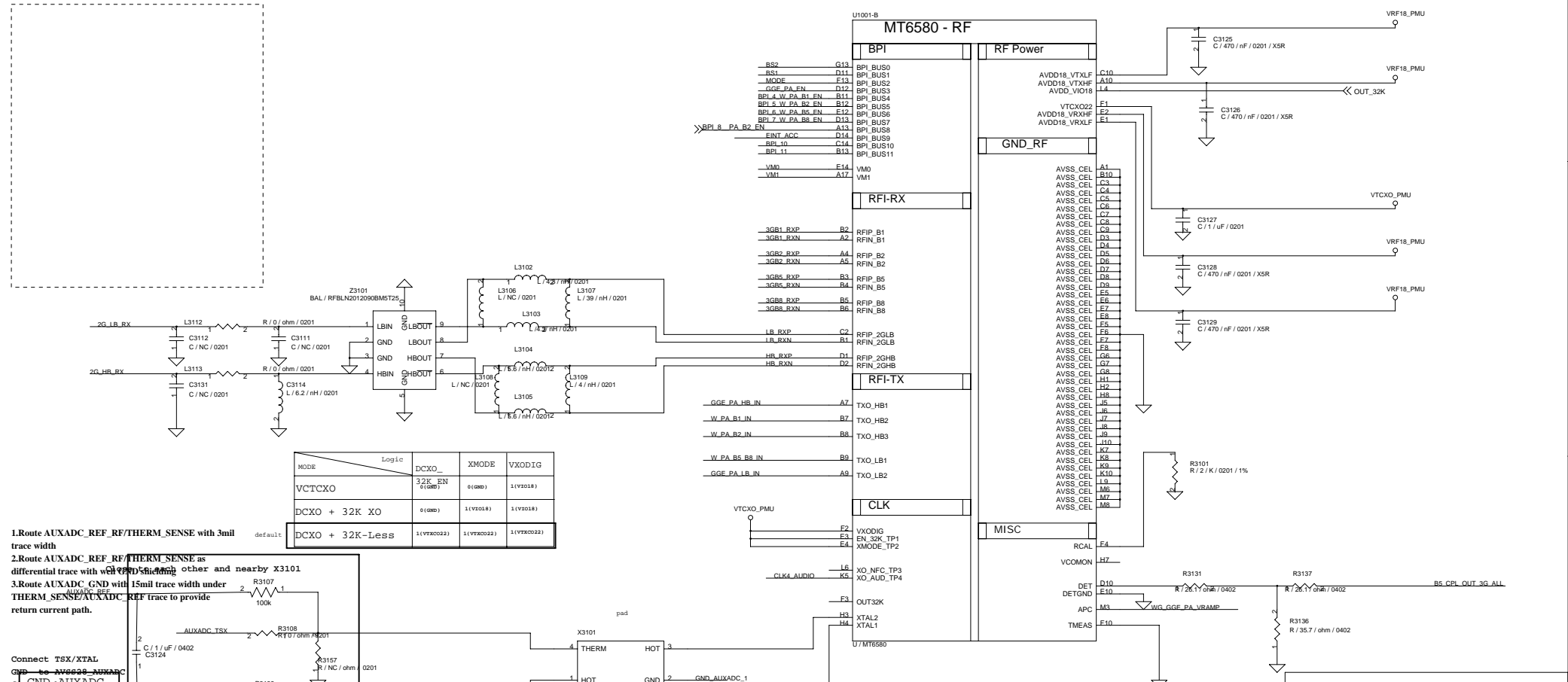
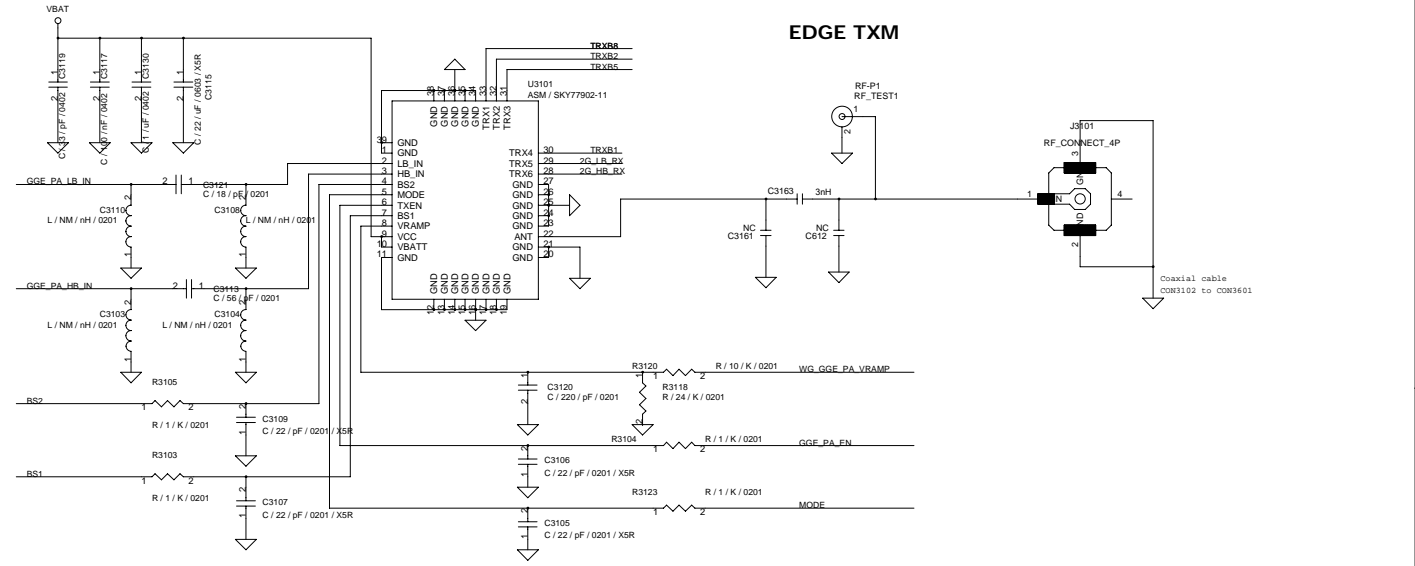
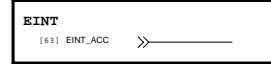
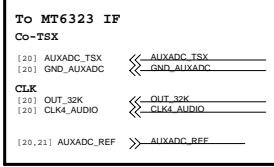
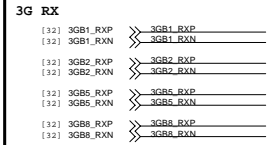
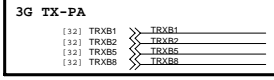
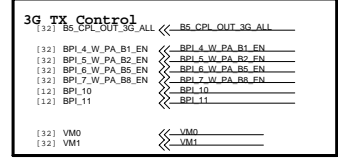
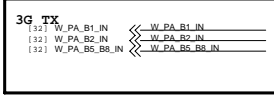
[61] LCM_LED_A << LCM_LED_A
 [61] LCM_LED_K << LCM_LED_K
 [12] DISP_PWM0 << DISP_PWM0



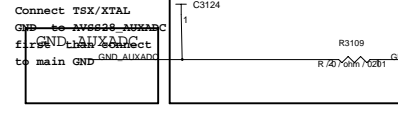
LCM Backlight LED Driver



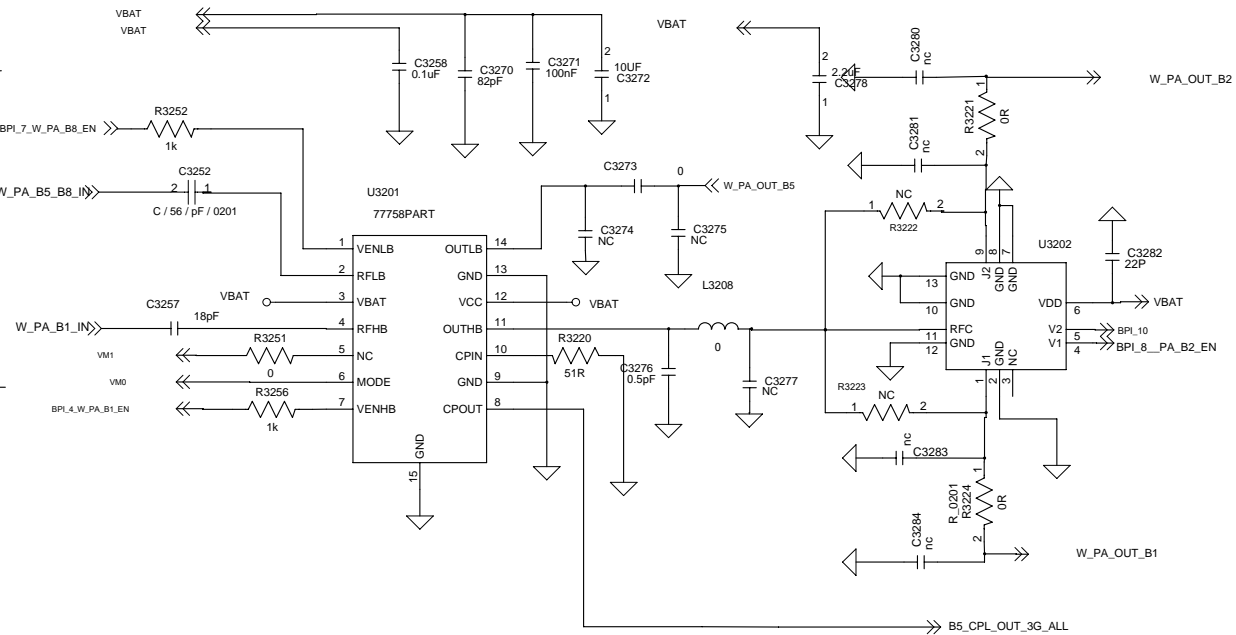
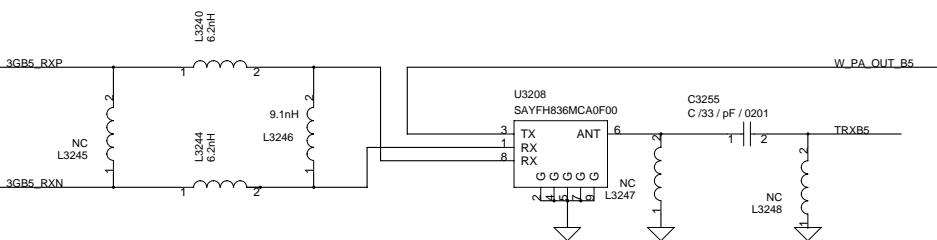
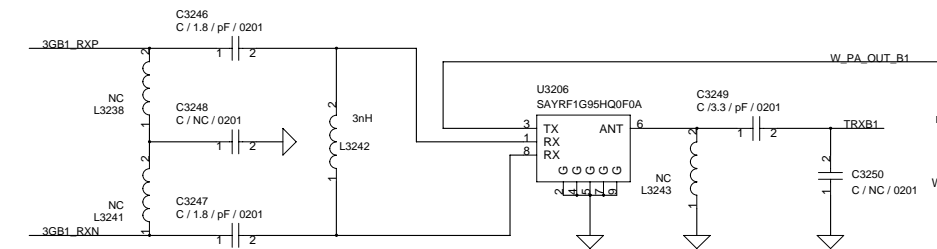
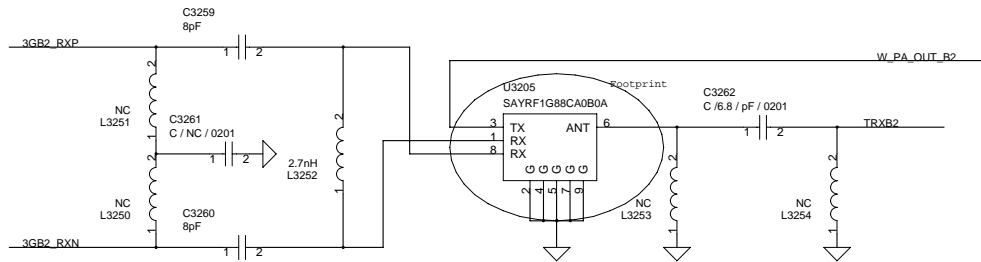
VOUT max. : 38V
 Switch Frequency : 5KHz-100KHz
 VFB : 300mV



- 1.Route AUXADC_REF_RF/THERM_SENSE with 3mil trace width
- 2.Route AUXADC_REF_RF/THERM_SENSE as differential trace with 15mil spacing other and nearby X3101
- 3.Route AUXADC_GND with 15mil trace width under THERM_SENSE/AUXADC_REF trace to provide return current path.



MODE	Logic	DCXO	XMODE	VXODIG
VTCXO	32K_EN 0 (GND)	0 (GND)	0 (GND)	1 (VDD18)
DCXO + 32K XO	0 (GND)	1 (VDD18)	1 (VDD18)	1 (VDD18)
DCXO + 32K-Less	1 (VDD18)	1 (VDD18)	1 (VDD18)	1 (VDD18)

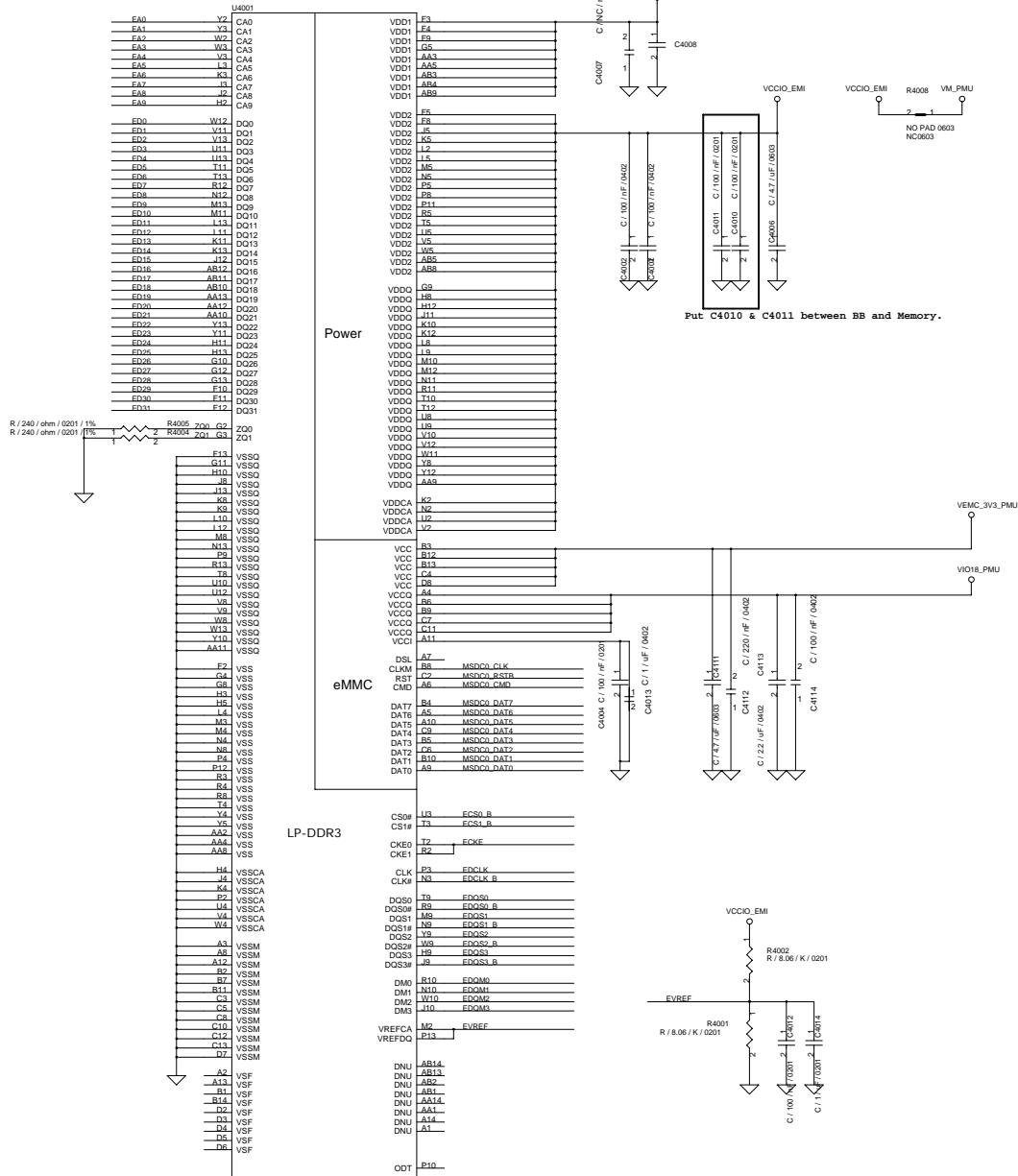
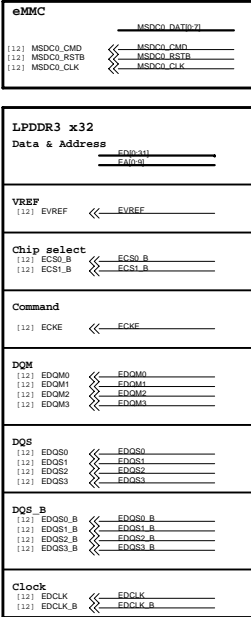


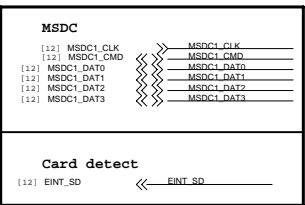
3G TX [32] W_PA_B1_IN << W_PA_B1_IN [32] [33] W_PA_B2_IN << W_PA_B2_IN [33] [34] W_PA_B5_B8_IN << W_PA_B5_B8_IN [34]		3G TX-PA TRXB1 << TRXB1 TRXB2 << TRXB2 TRXB5 << TRXB5 TRXB8 << TRXB8	
3G RX [31] 3GB1_RXP << 3GB1_RXP [31] [31] 3GB1_RXN << 3GB1_RXN [31]		3G TX Control B5_CPL_OUT_3G_ALL << B5_CPL_OUT_3G_ALL BPI_4_W_PA_B1_EN << BPI_4_W_PA_B1_EN BPI_5_W_PA_B2_EN << BPI_5_W_PA_B2_EN BPI_6_W_PA_B5_EN << BPI_6_W_PA_B5_EN BPI_7_W_PA_B8_EN << BPI_7_W_PA_B8_EN	
[31] 3GB2_RXP << 3GB2_RXP [31] [31] 3GB2_RXN << 3GB2_RXN [31]		VM0 << VM0 VM1 << VM1	
[31] 3GB5_RXP << 3GB5_RXP [31] [31] 3GB5_RXN << 3GB5_RXN [31]			
[31] 3GB8_RXP << 3GB8_RXP [31] [31] 3GB8_RXN << 3GB8_RXN [31]			

Main Antenna

Title	36_RF_AT
Size	MTK Confidential
Date:	Friday, January 30, 2015 12 of 22

eMMC+LPDDR3





Based on your system level design , if better ESD/desense performance is needed on your system.

Schematic design notice of "41_MEMORY_SD Card" page.

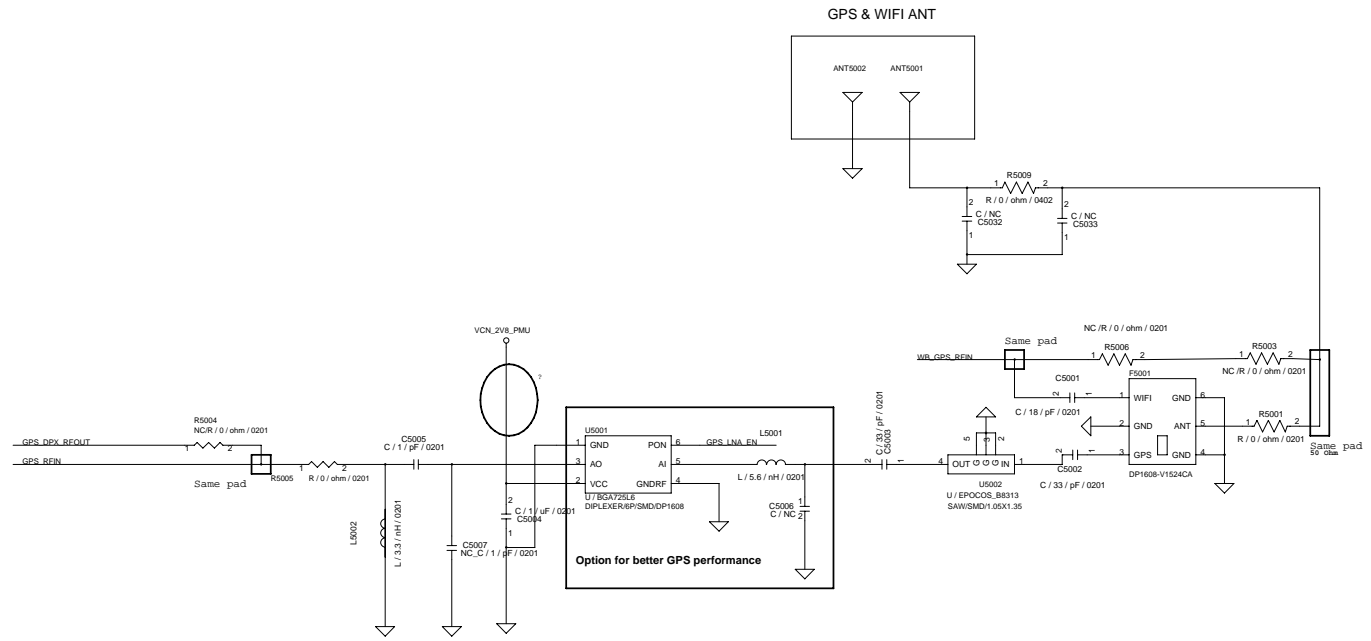
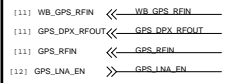
Note 41-1:

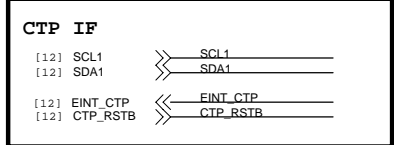
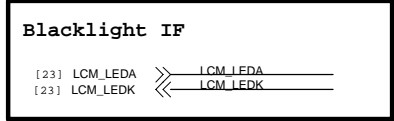
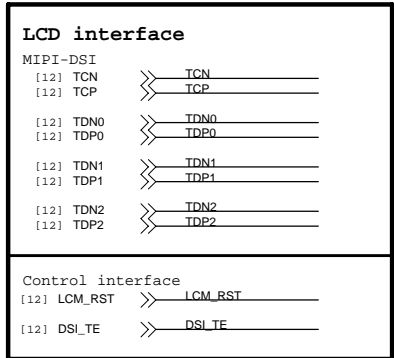
The equivalent capacitance of ESD protection device must be $\leq 1\text{pF}$
 -- otherwise it will result in NFC card mode function fail.

Note 41-2:

Depends on system design to add ESD protection component or not.

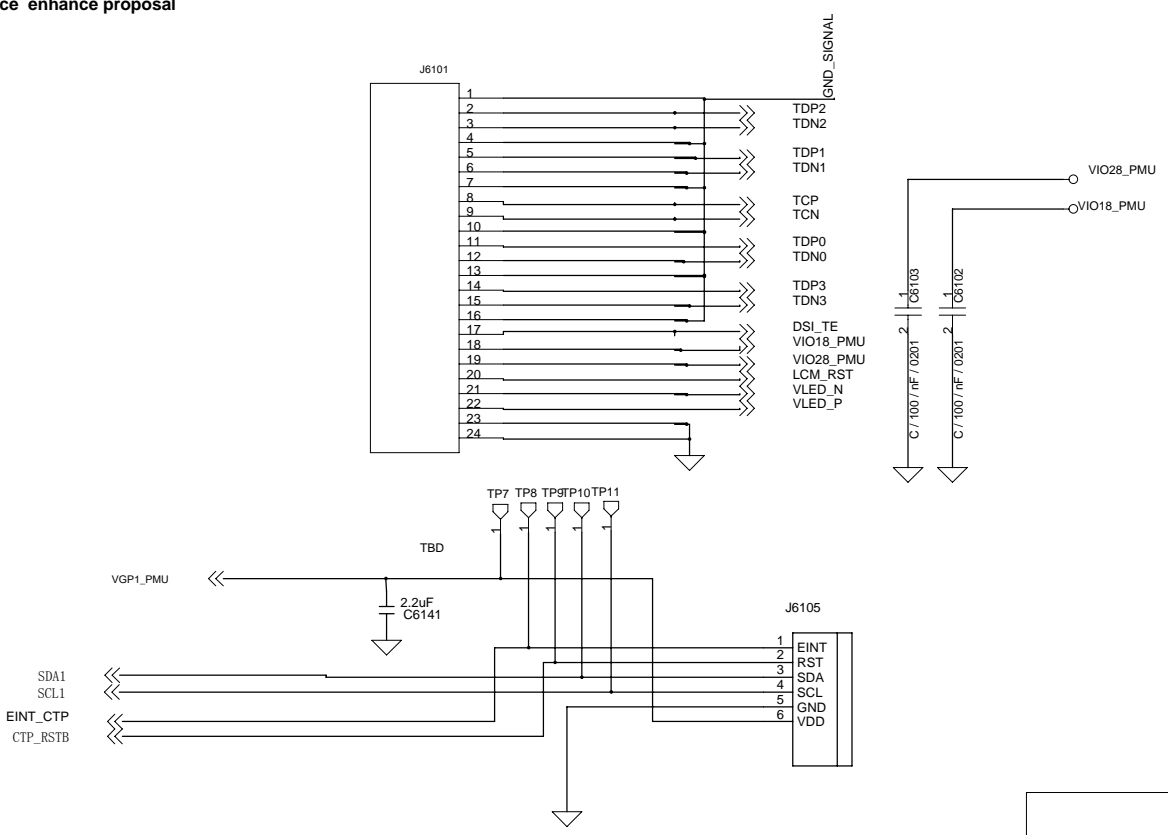
WCN RF Interface

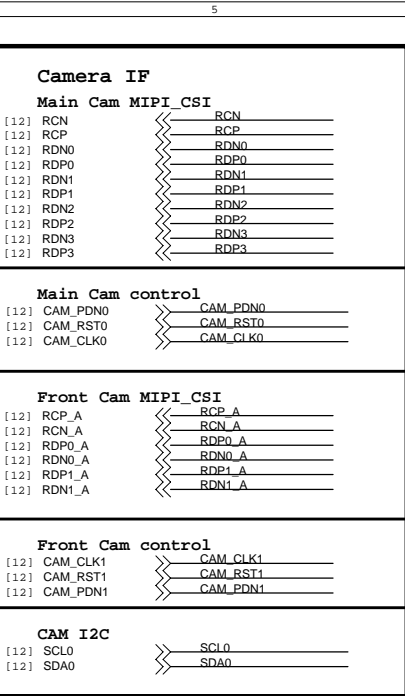




Based on your system level design , if better desense performance is needed on your system , please refer to desense performance enhance proposal

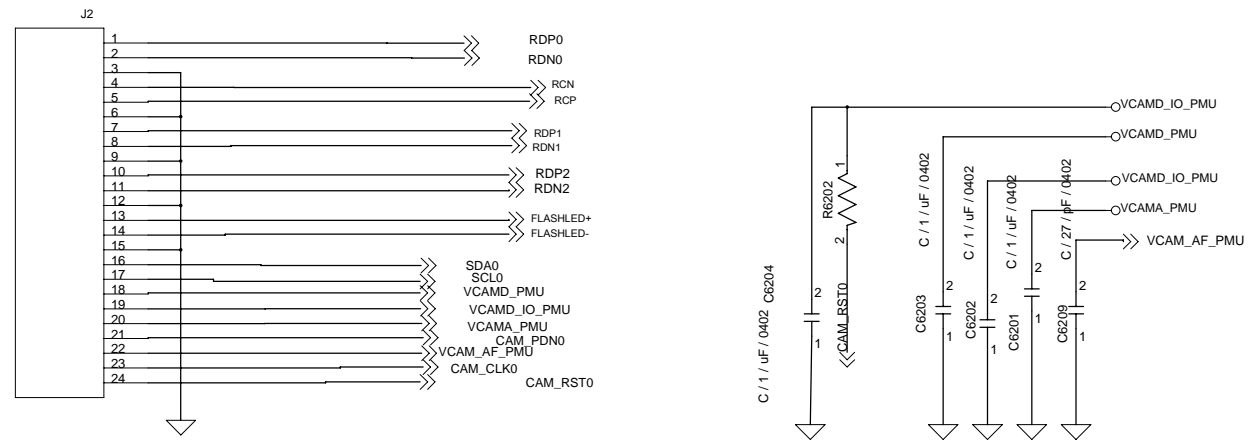
Main LCM





Rear Camera

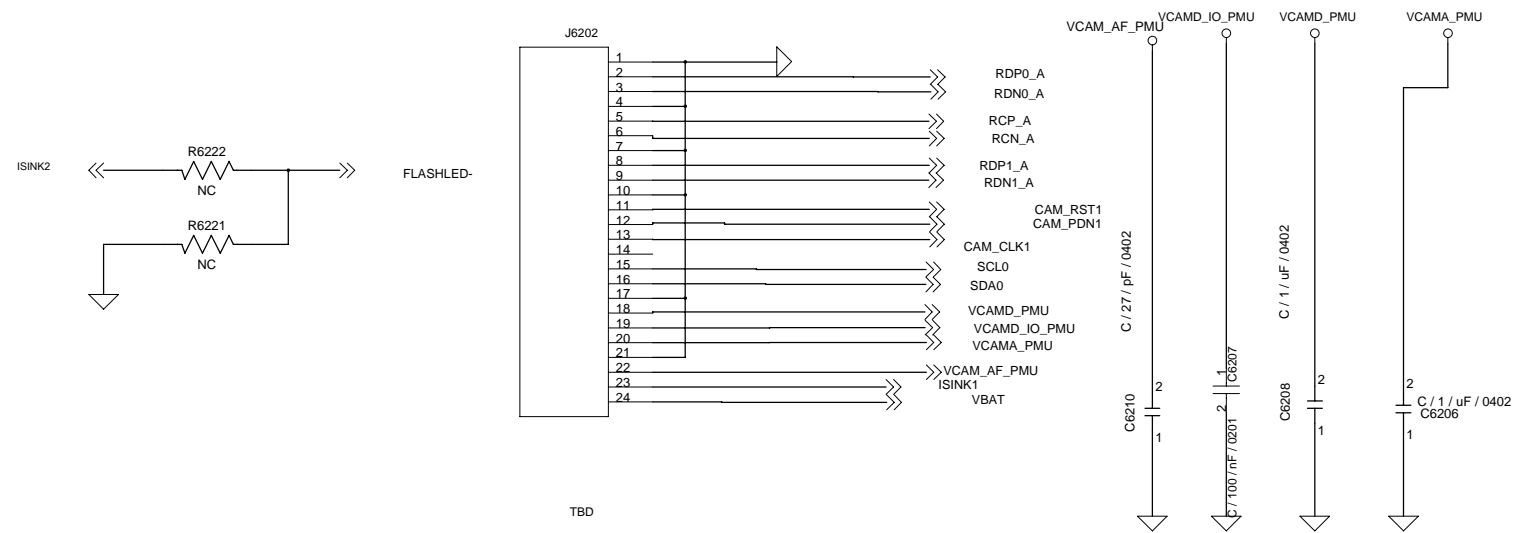
Rear camera (IMX179) I2C address: 0X10 (Write:0x20, Read:0x21)
 AF driver (F8N03C) I2C address: 0x0C (Write:0x18, Read:0x19)



TBD
 desense performance is needed on your system, please refer to desense performance enhance proposal

Front Camera

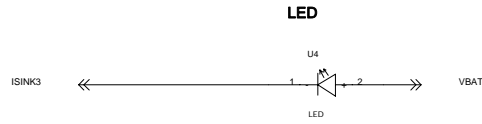
Front camera (OV5670) I2C address: 0X36 (Write:0x6C, Read:0x6D)



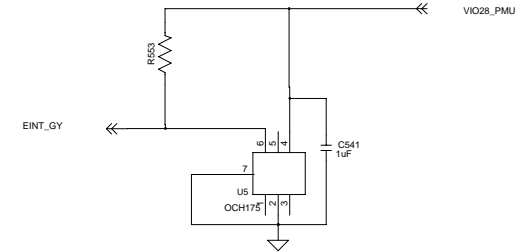
Title	62_PERI_CAMERA		
Size	C		
Date:	Friday, January 30, 2015	Sheet	18 of 22

Sensor Interrupt	
[12] EINT_MAG	← EINT_MAG
[12] EINT_GY	← EINT_GY
[12] EINT_PS	← EINT_PS
[31] EINT_ACC	← EINT_ACC
Tmp sensor	
[11,63] AUX_IN0_NTC	← AUX_IN0_NTC
control IF	
[12,23,63] SCL2	← SCL2
[12,23,63] SDA2	← SDA2

M-Sensor



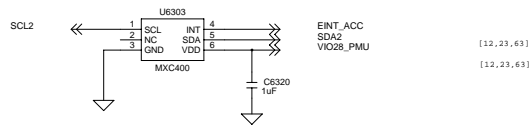
HALL



Accelerometer

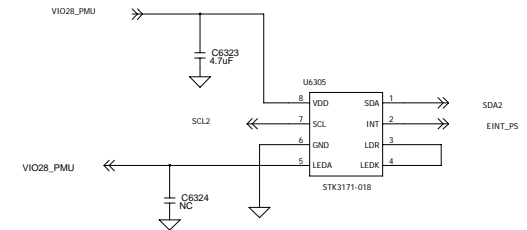
MC3410 / Accelerometer I2C address: 0x4C (Write:0x98, Read:0x99)

Reserve for open drain type : R6307

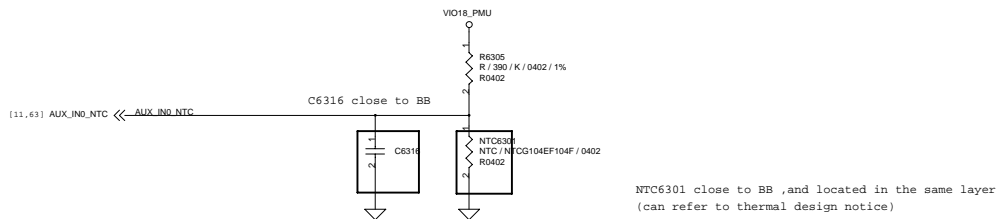


RGB & PS Sensor

CM36652 / RGB + PS I2C address: 0X60 (Write:0xC0, Read:0xC1)



Thermistor / To sense board level temperature



5

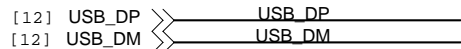
4

3

2

1

USB IF



D

D

C

C

B

B

A

A

Title		64_PERI_USB_MHL
Size	MTK Confidential	
C		
Date:	Friday, January 30, 2015	Sheet 20 of 22

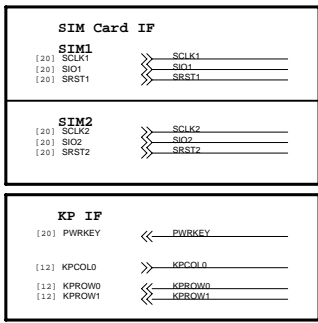
5

4

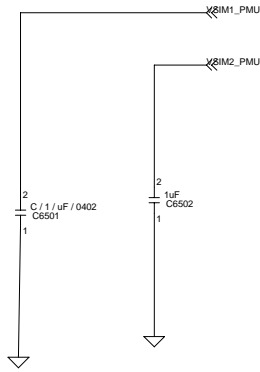
3

2

1

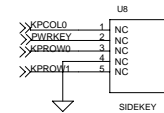
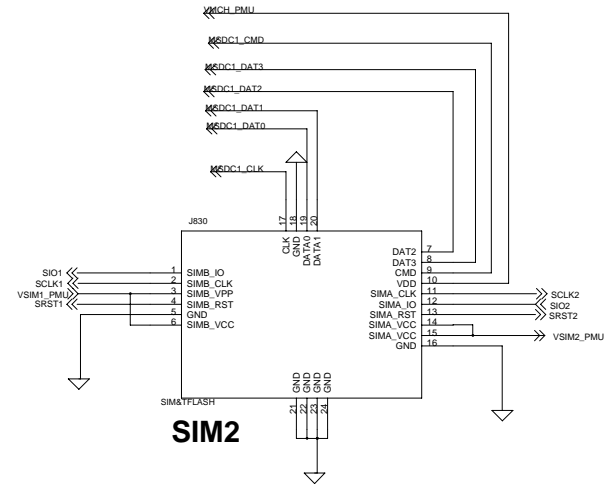
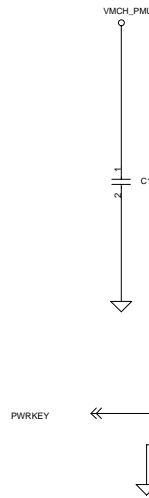


SIM1

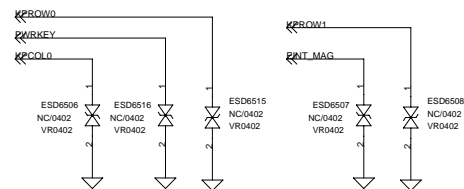


SIM & TFLASH

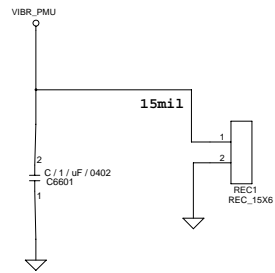
SIM2



	KCOL0	KCOL1
KROW0	Up	
KROW1	Down	



VIBRATOR



6

5

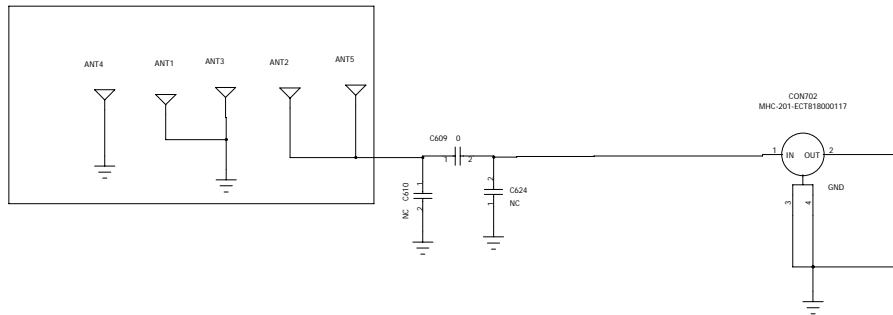
4

3

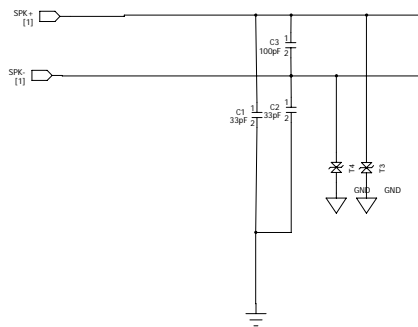
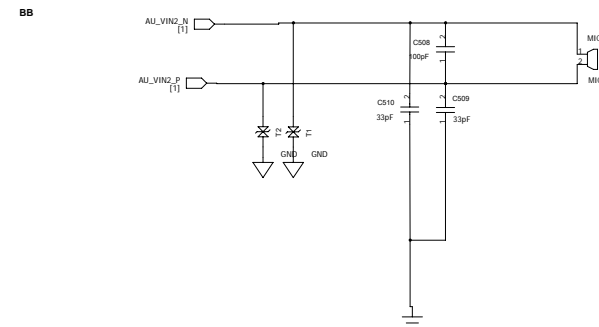
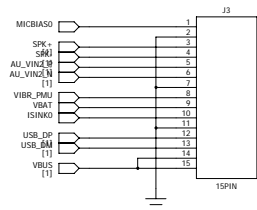
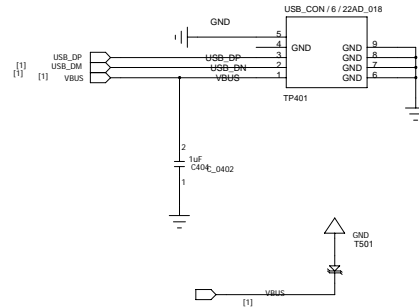
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GSM & WCDMA ANT



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY:

TITLE:

DRAWN:	DATED:
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

CODE:	SIZE:	DRAWING NO:	REV:
	C		
SCALE:			SHEET: 1