

Port2_20M_3560.01MHz_TM3.1a_CHL_CSE0a



Port2_20M_3560.01MHz_TM3.1a_CHL_CSE0b



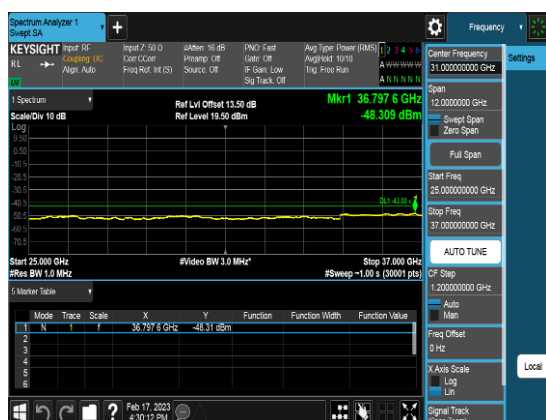
Port2_20M_3560.01MHz_TM3.1a_CHL_CSE1



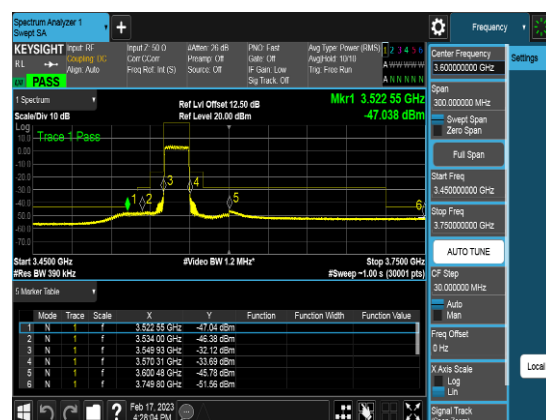
Port2_20M_3560.01MHz_TM3.1a_CHL_CSE2



Port2_20M_3560.01MHz_TM3.1a_CHL_CSE3



Port2_20M_3560.01MHz_TM3.1a_CHL_CSEpart 96



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Port2_20M_3624.99MHz_TM3.1a_CHM_CSE0a



Port2_20M_3624.99MHz_TM3.1a_CHM_CSE0b



Port2_20M_3624.99MHz_TM3.1a_CHM_CSE1



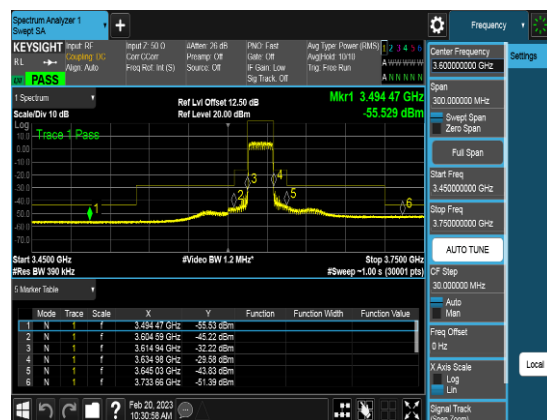
Port2_20M_3624.99MHz_TM3.1a_CHM_CSE2



Port2_20M_3624.99MHz_TM3.1a_CHM_CSE3



Port2_20M_3624.99MHz_TM3.1a_CHM_CSEpar 196



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Port2_20M_3690MHz_TM3.1a_CHH_CSE0a



Port2_20M_3690MHz_TM3.1a_CHH_CSE0b



Port2_20M_3690MHz_TM3.1a_CHH_CSE1



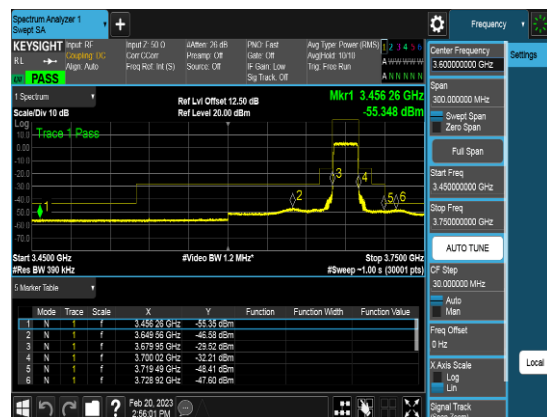
Port2_20M_3690MHz_TM3.1a_CHH_CSE2



Port2_20M_3690MHz_TM3.1a_CHH_CSE3



Port2_20M_3690MHz_TM3.1a_CHH_CSEpart96

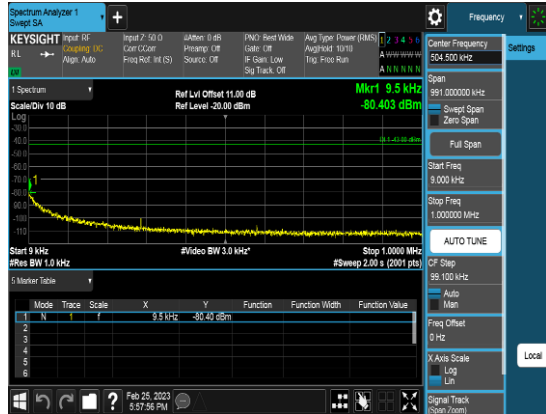


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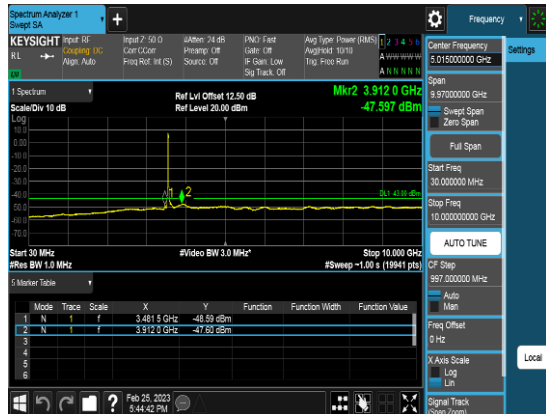
Port2_30M_3565.02MHz_TM3.1a_CHL_CSE0a



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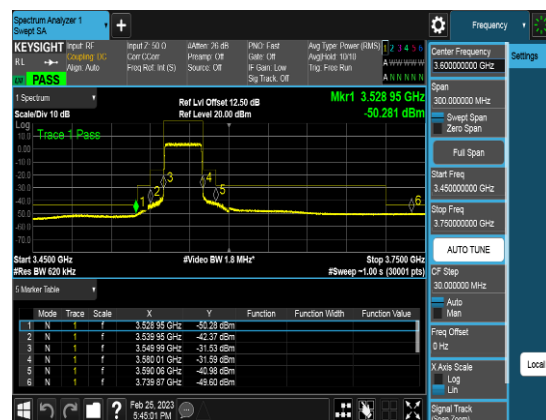
Port2_30M_3565.02MHz_TM3.1a_CHL_CSE2



Port2_30M_3565.02MHz_TM3.1a_CHL_CSE3



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Port2_30M_3624.99MHz_TM3.1a_CHM_CSE0a



Port2_30M_3624.99MHz_TM3.1a_CHM_CSE0b



Port2_30M_3624.99MHz_TM3.1a_CHM_CSE1



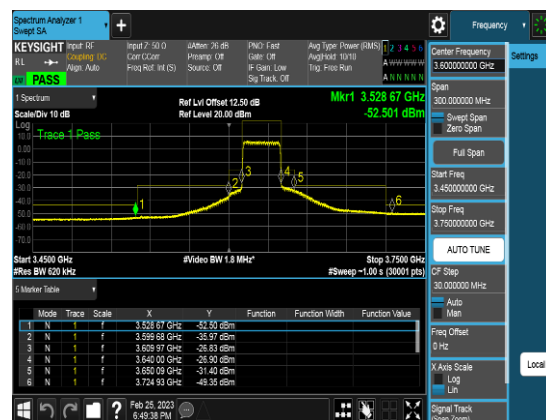
Port2_30M_3624.99MHz_TM3.1a_CHM_CSE2



Port2_30M_3624.99MHz_TM3.1a_CHM_CSE3



Port2_30M_3624.99MHz_TM3.1a_CHM_CSEpar 196



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Port2_30M_3684.99MHz_TM3.1a_CHH_CSE0a



Port2_30M_3684.99MHz_TM3.1a_CHH_CSE0b



Port2_30M_3684.99MHz_TM3.1a_CHH_CSE1



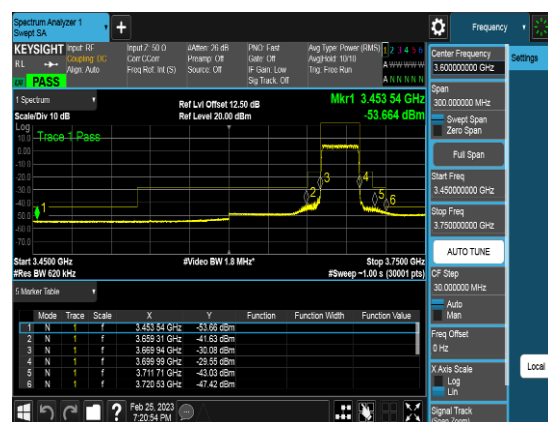
Port2_30M_3684.99MHz_TM3.1a_CHH_CSE2



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Port2_40M_3570MHz_TM3.1a_CHL_CSE0a



Port2_40M_3570MHz_TM3.1a_CHL_CSE0b



Port2_40M_3570MHz_TM3.1a_CHL_CSE1



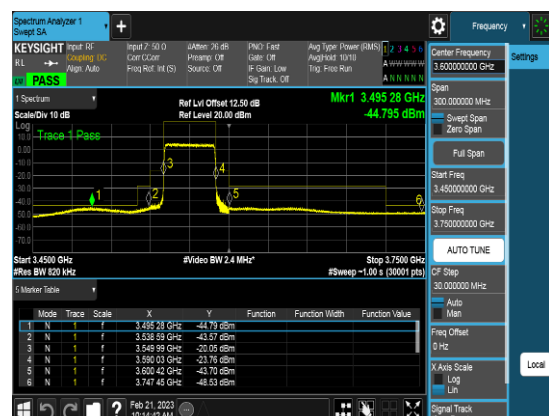
Port2_40M_3570MHz_TM3.1a_CHL_CSE2



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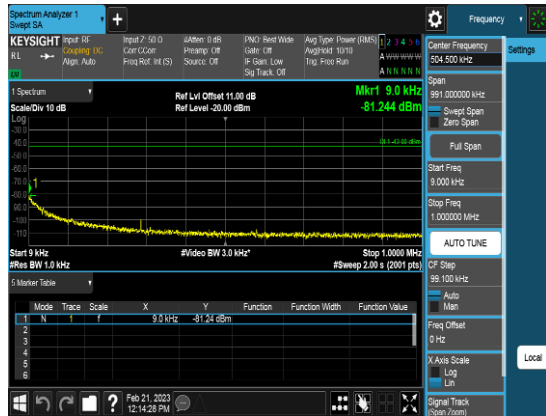
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Port2_40M_3624.99MHz_TM3.1a_CHM_CSE0b



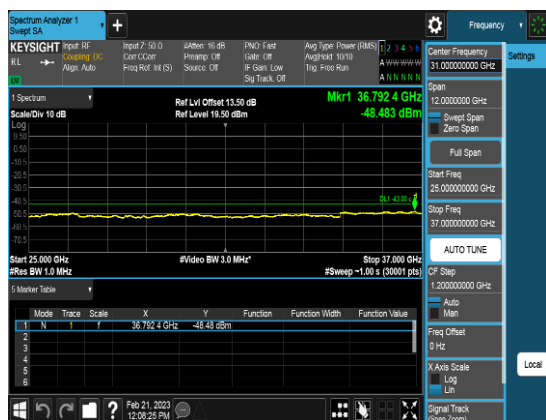
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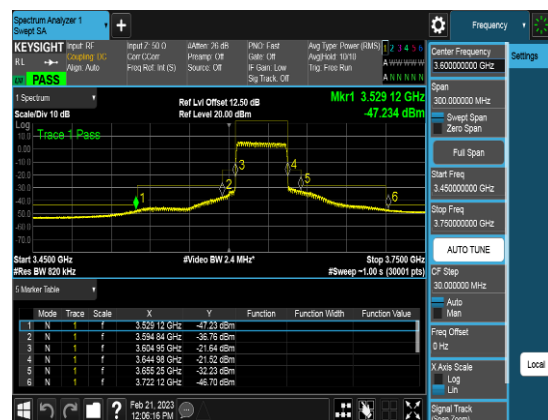
Port2_40M_3624.99MHz_TM3.1a_CHM_CSE2



Port2_40M_3624.99MHz_TM3.1a_CHM_CSE3



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Port2_40M_3679.98MHz_TM3.1a_CHH_CSE0b



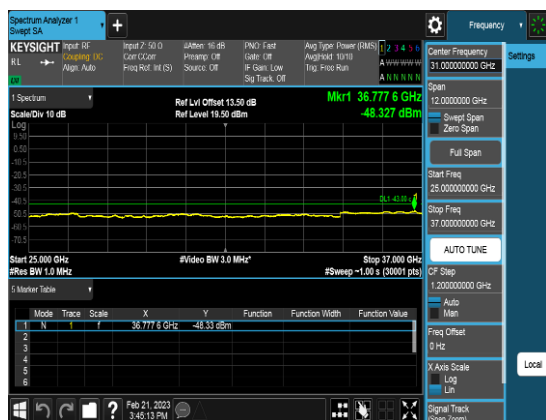
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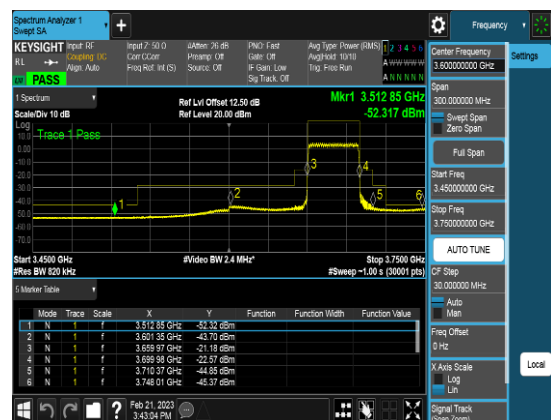
Port2_40M_3679.98MHz_TM3.1a_CHH_CSE2



Port2_40M_3679.98MHz_TM3.1a_CHH_CSE3



Port2_40M_3679.98MHz_TM3.1a_CHH_CSEpart 96



- End of the Appendix -



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