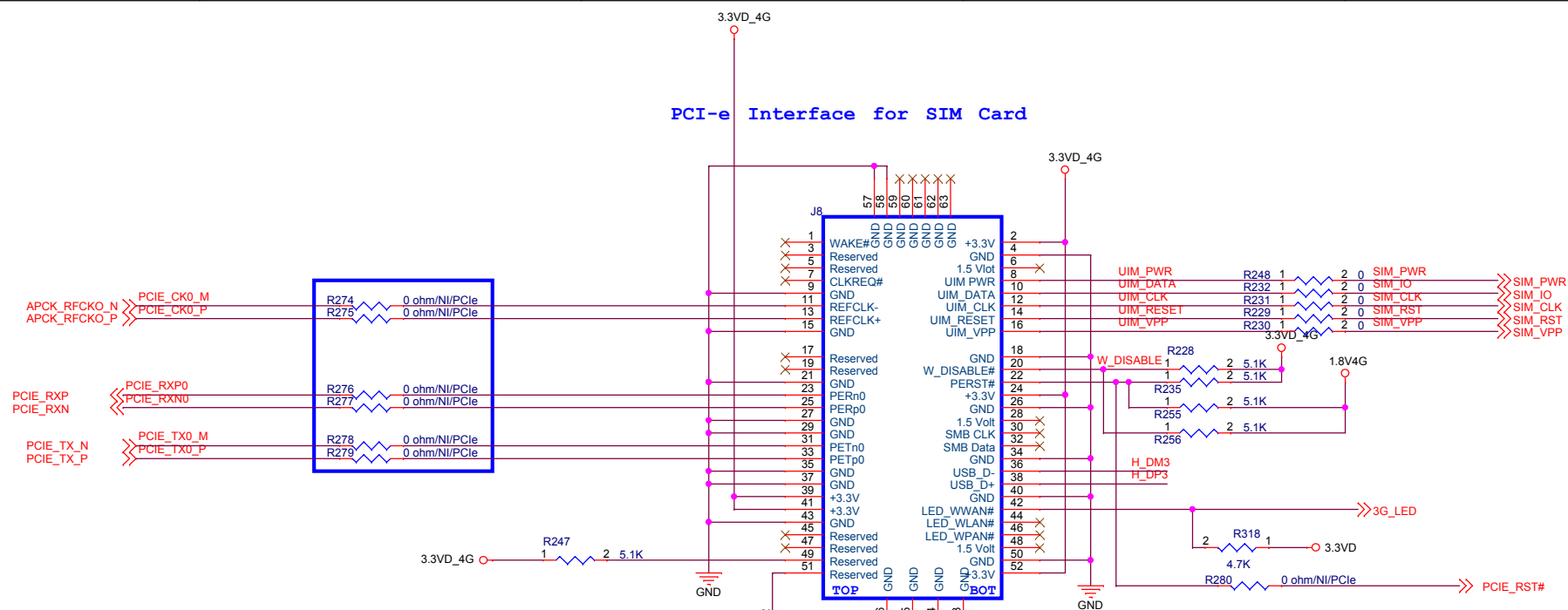
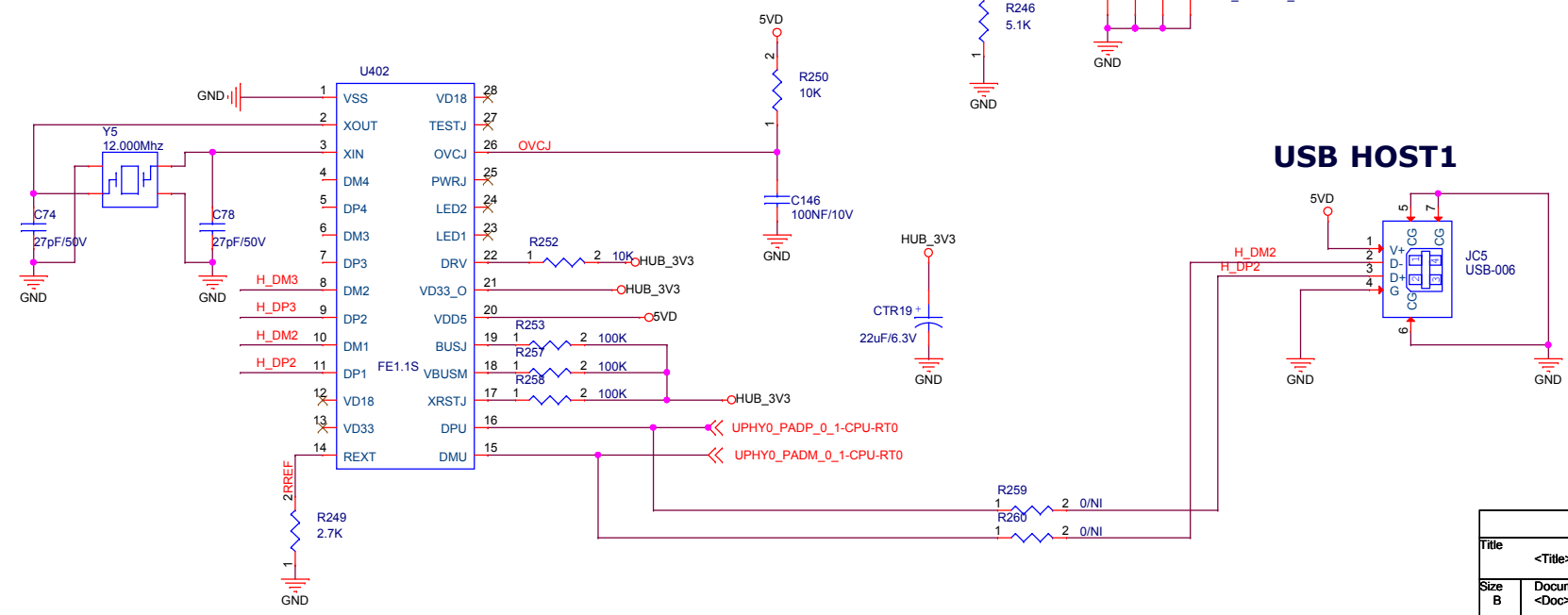


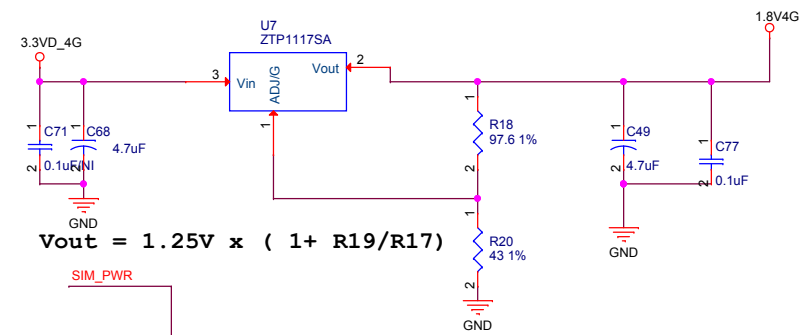
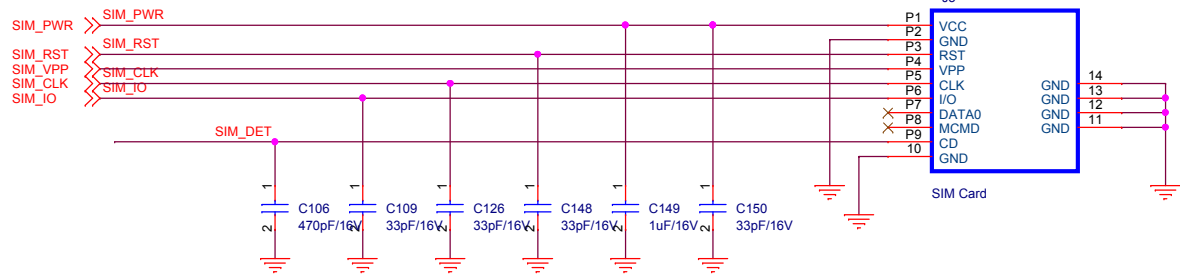
PCI-e Interface for SIM Card



USB HOST1

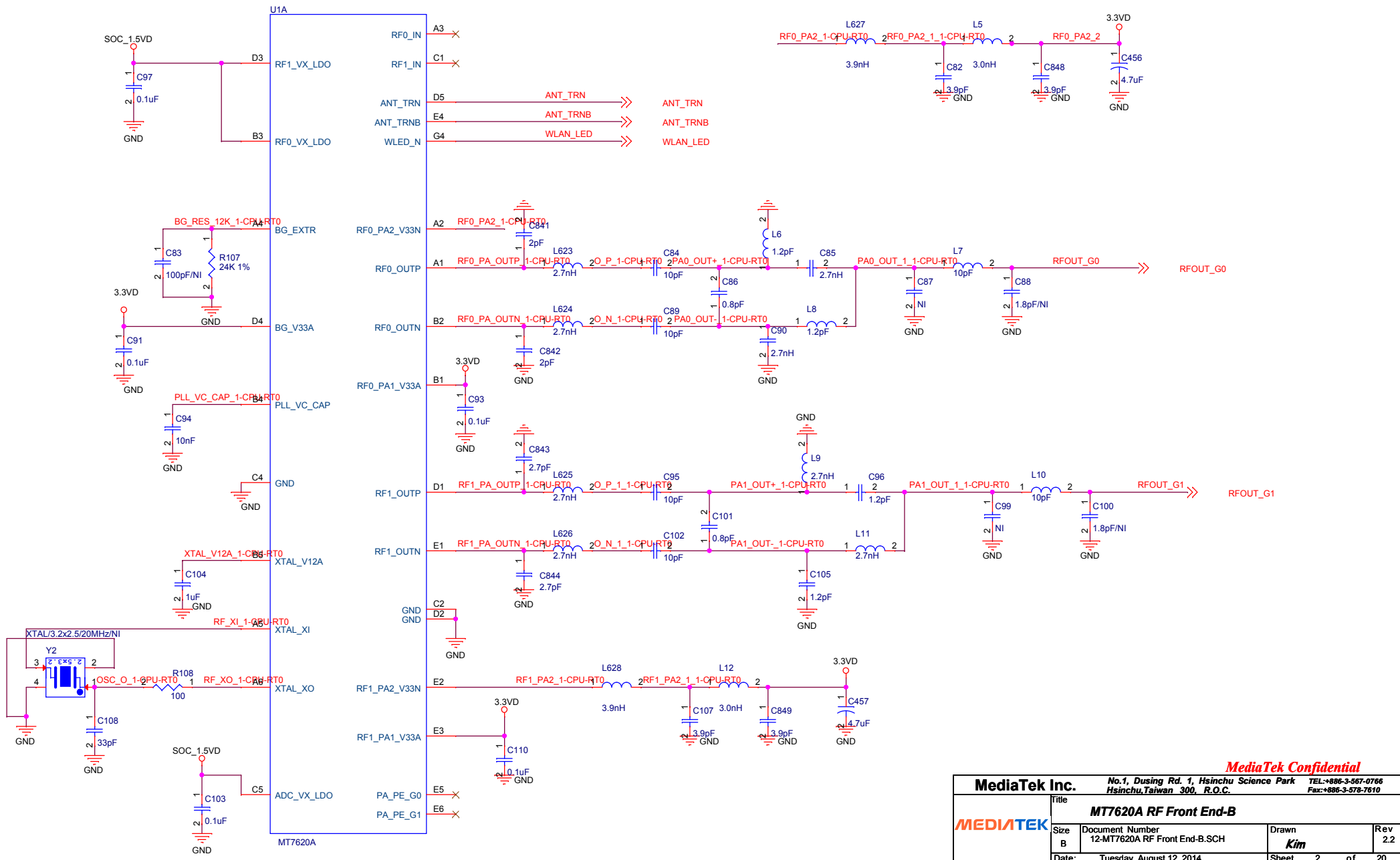


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Size B	Document Number	Rev
	<Doc>	<RevCode>
Date:	Tuesday, September 09, 2014	Sheet 1 of 1



$$V_{out} = 1.25V \times (1 + R19/R17)$$

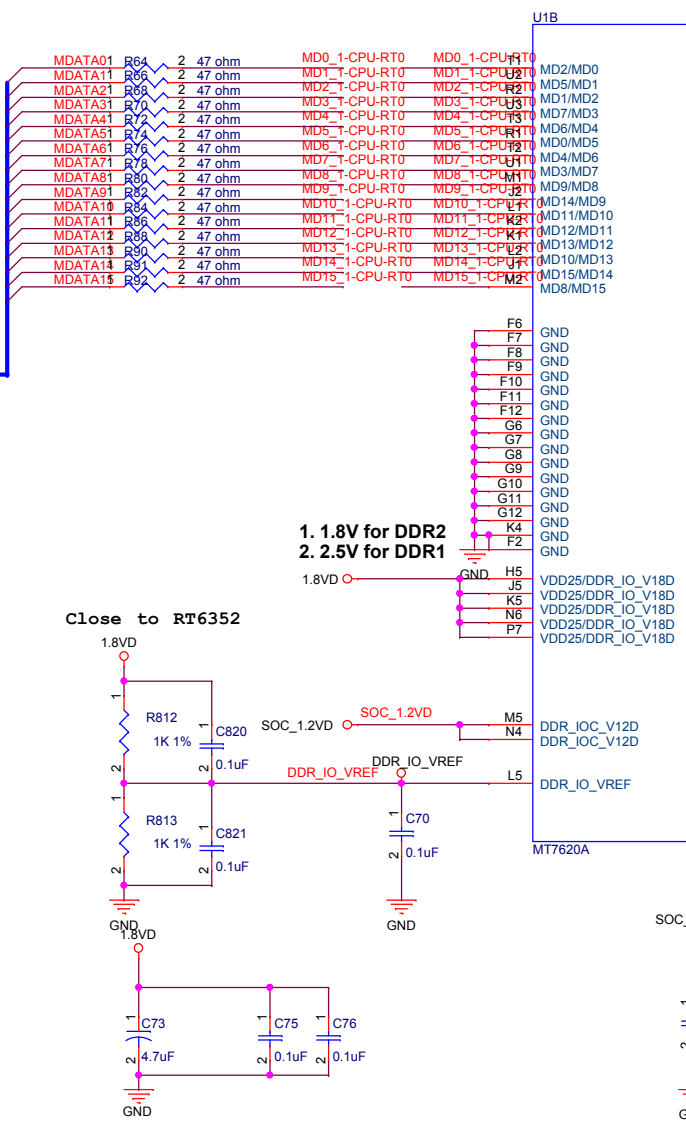
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Date:	Tuesday, August 12, 2014	Sheet 1 of 1



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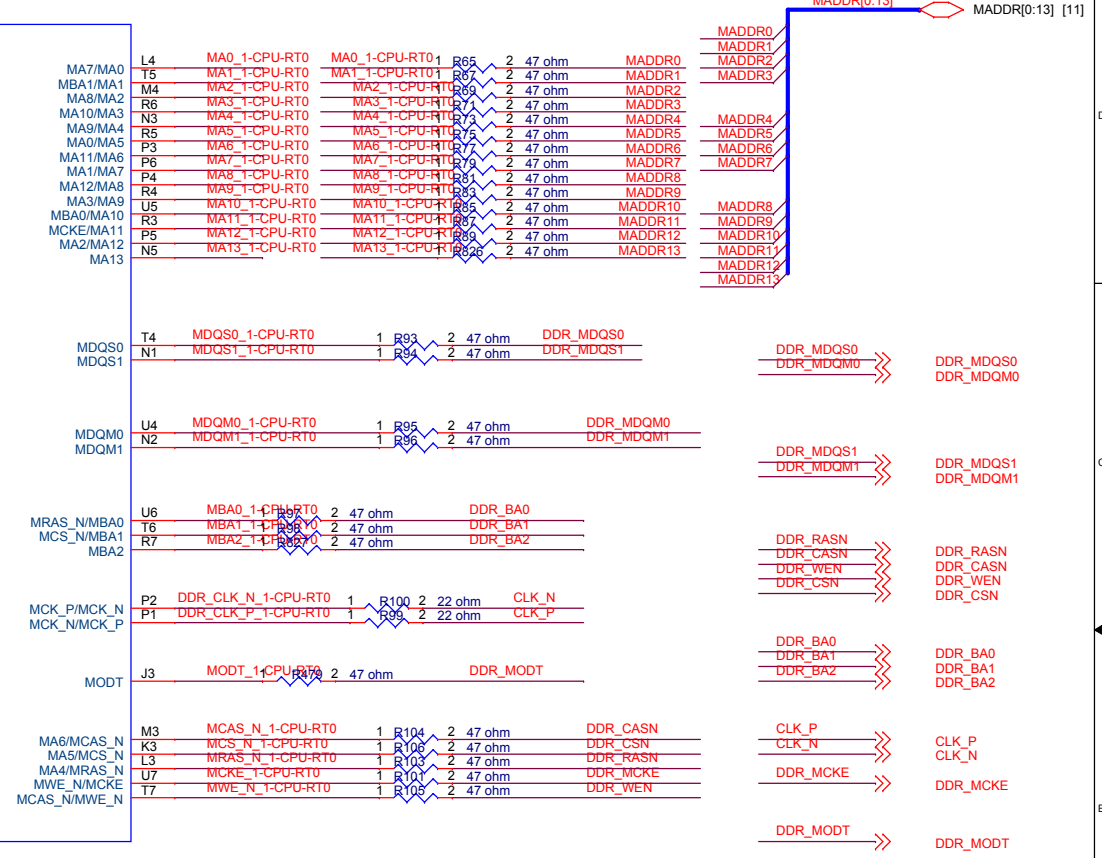
MediaTek Inc.		No.1, Dusing Rd. 1, Hsinchu Science Park Hsinchu, Taiwan 300, R.O.C.		TEL: +886-3-567-0766 Fax: +886-3-578-7610
MEDIATEK		Title MT7620A RF Front End-B		
		Size B	Document Number 12-MT7620A RF Front End-B.SCH	Drawn Kim
		Date: Tuesday, August 12, 2014	Sheet 2	Rev 2.2 of 20

[11] MDATA[0:15] MDATA[0:15]



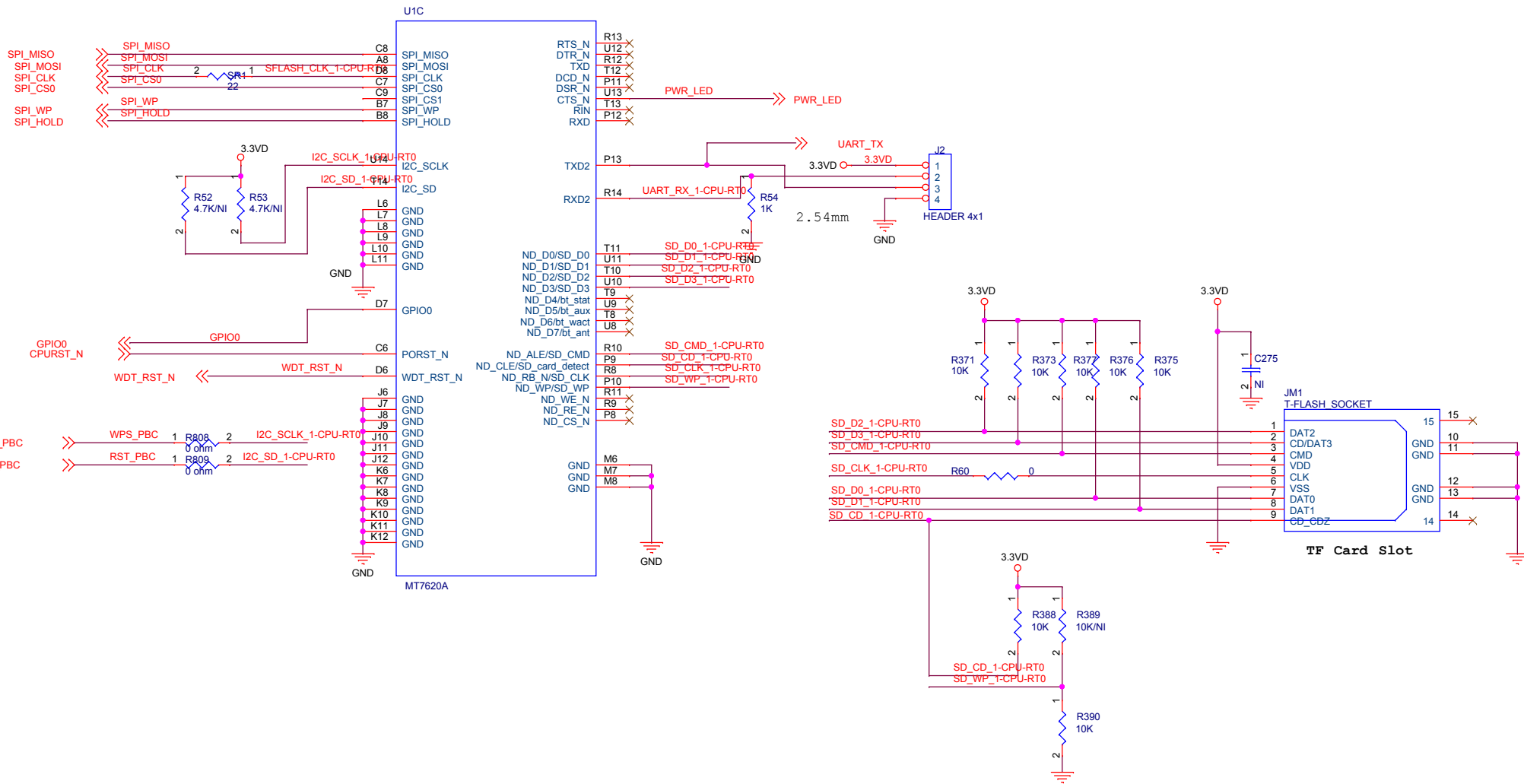
1. 1.8V for DDR2
2. 2.5V for DDR1

Close to RT6352



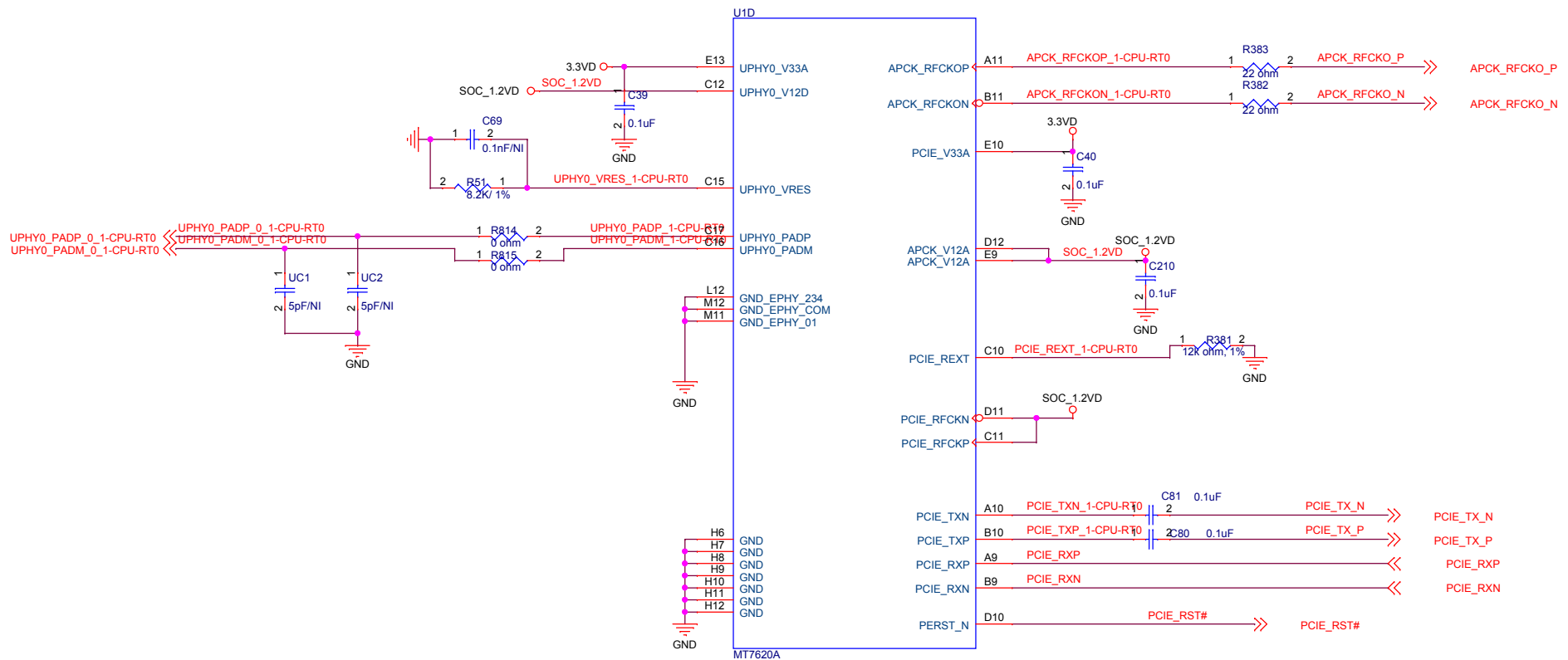
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Title MT7620A DDR I/F-C				
Size B	Document Number	Drawn	Rev	
	13-MT7620A DDR2 I/F-C.SCH	Kim	2.2	
Date:	Tuesday, August 12, 2014	Sheet	3	of 20



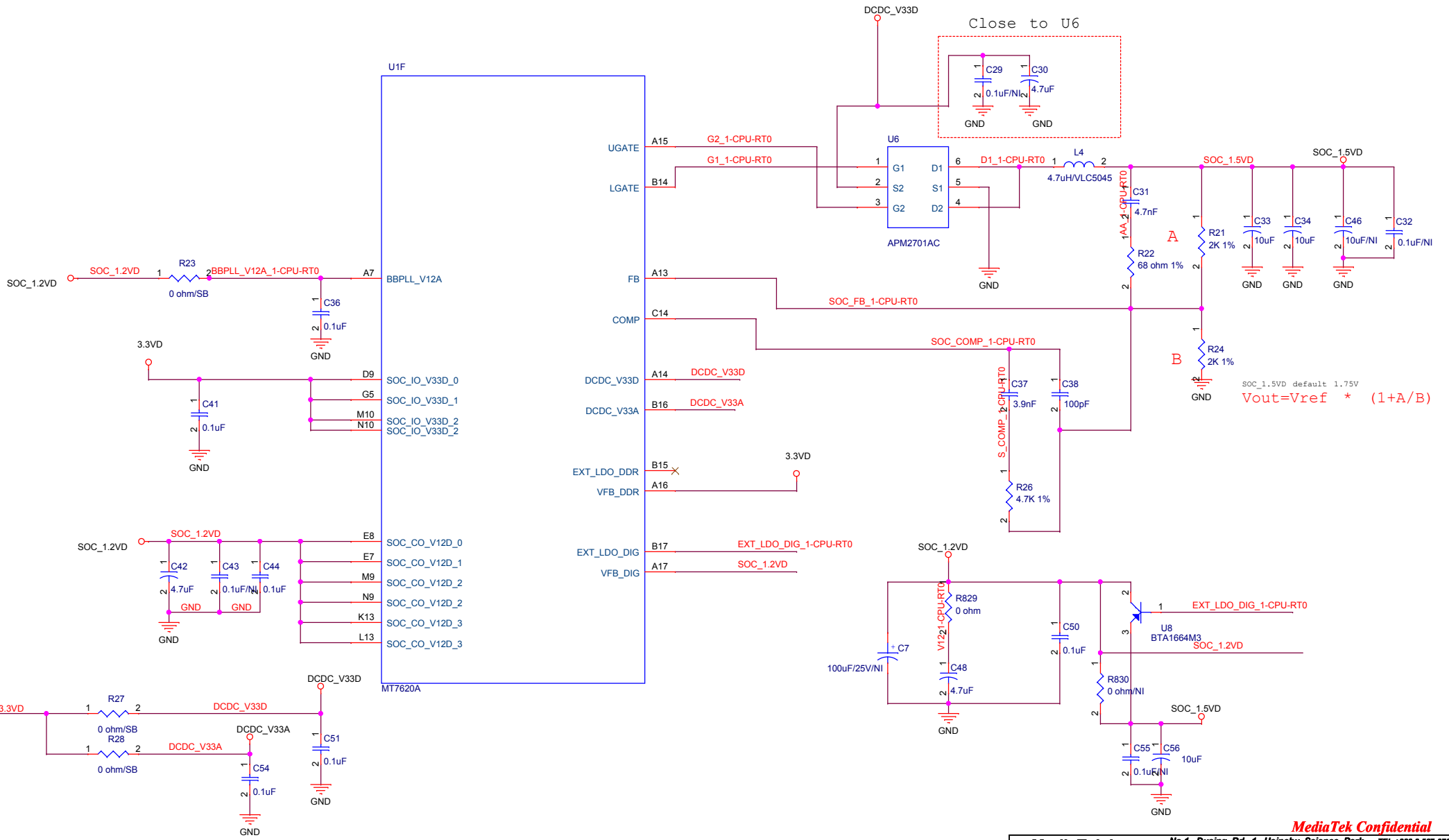
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MT7620A Pheripheral-C				
MEDIATEK	Size	Document Number	Drawn	Rev
	B	13-MT7620A Pheripheral-C.SCH	Kim	2.2
Date:	Friday, May 29, 2015	Sheet	4 of	20



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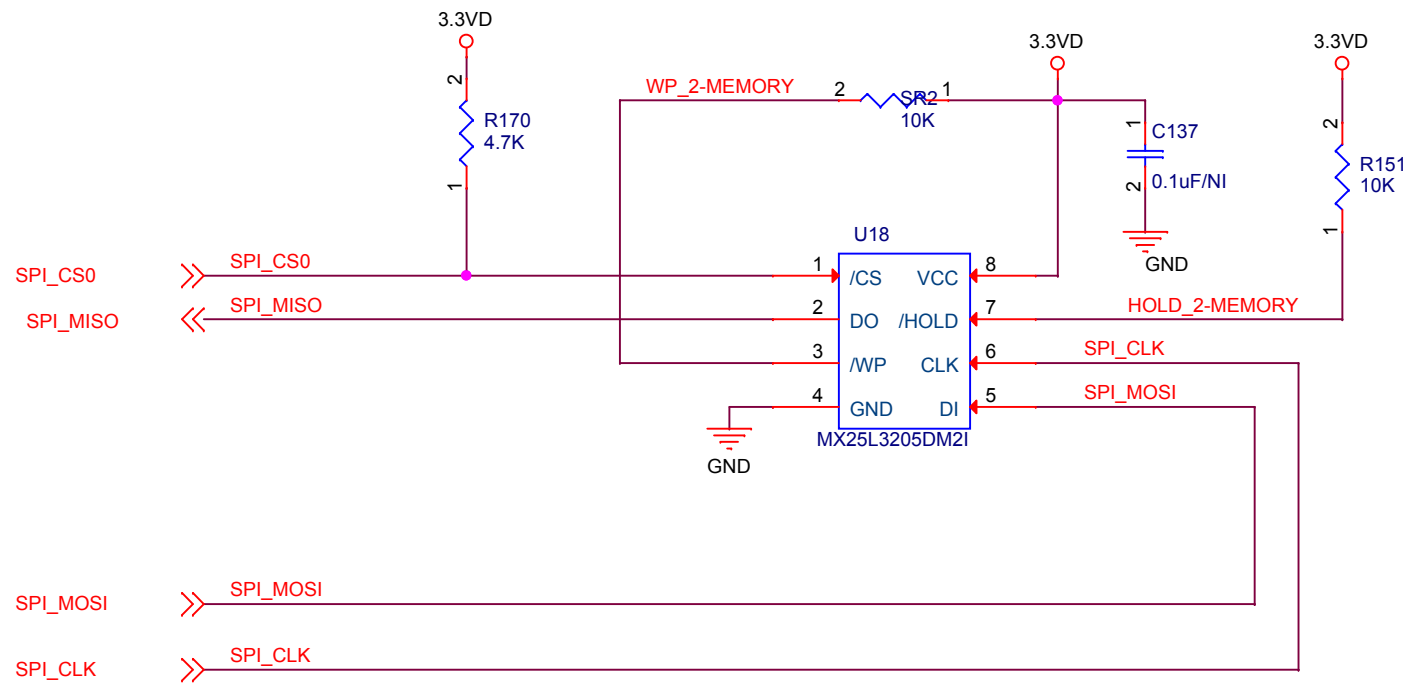
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		Title MT7620A USB-D		
		Size B	Document Number 14-MT7620A USB-D.SCH	Drawn Kim
Date: Tuesday, August 12, 2014		Rev 2.2		
		Sheet 5 of 20		




SOC_1.5VD default 1.75V
 $V_{out} = V_{ref} * (1 + A/B)$

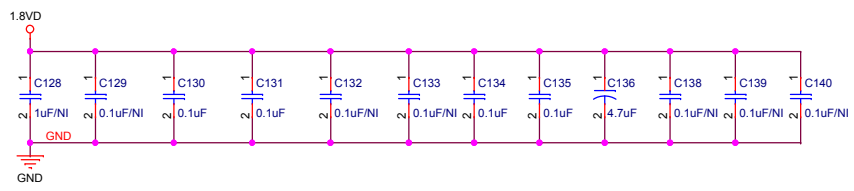
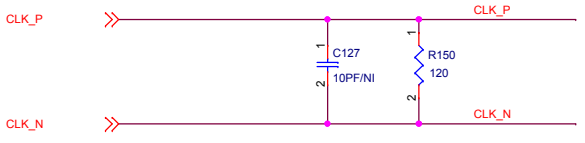
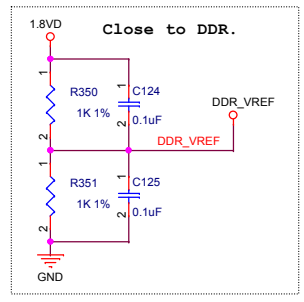
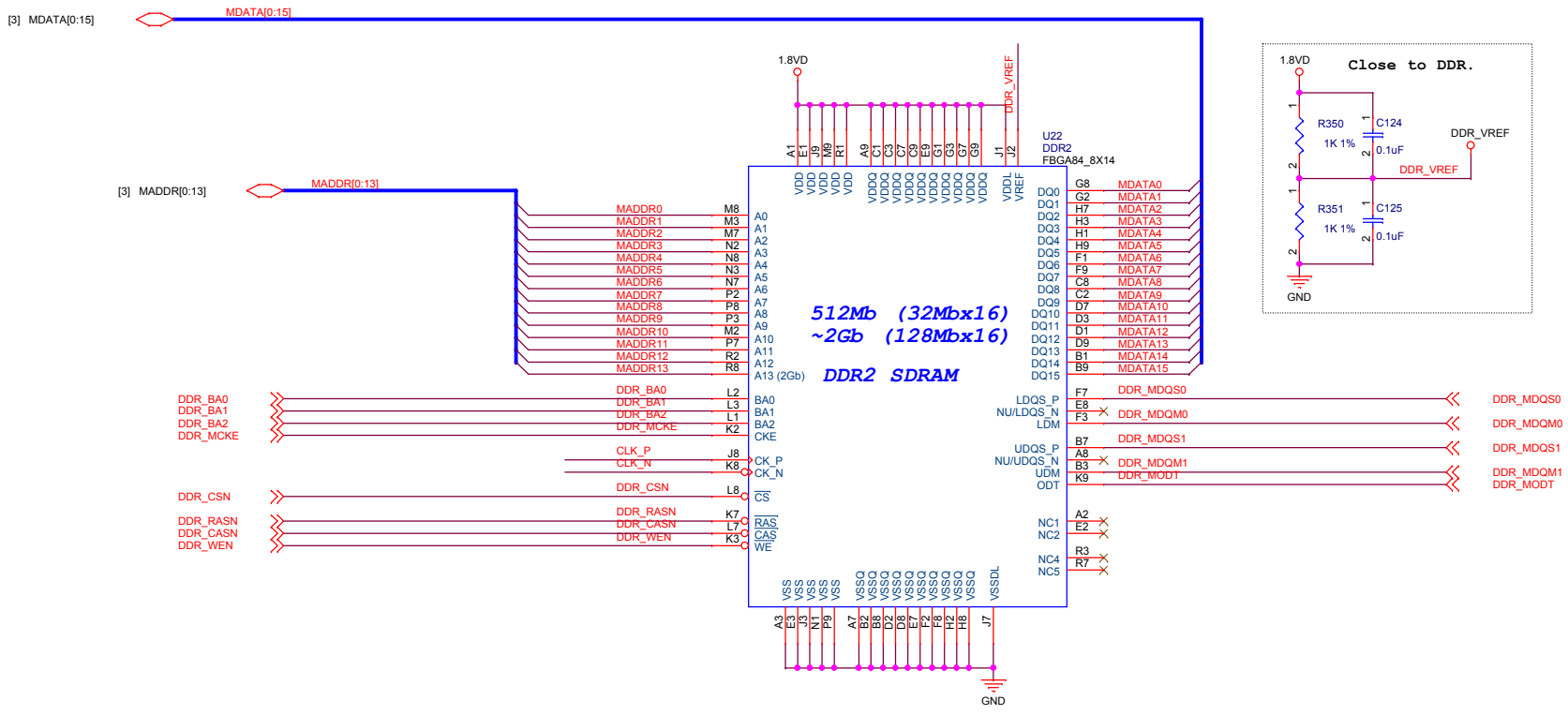
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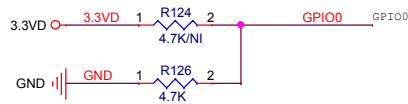
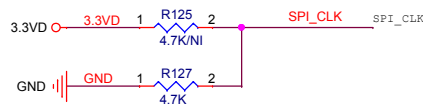
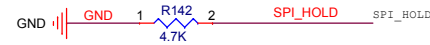
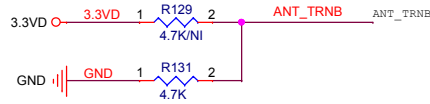
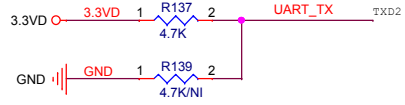
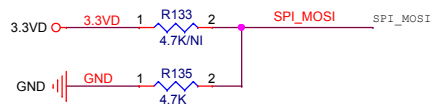
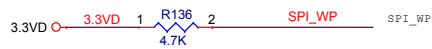
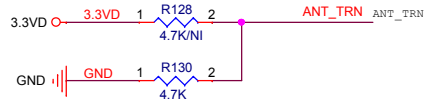
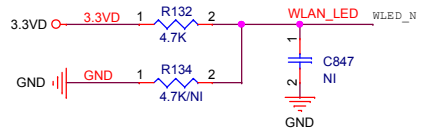
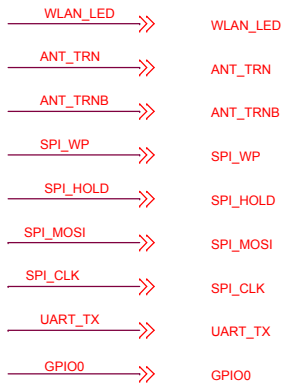
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MT7620A Power-F				
MEDIA/TEK	Size	Document Number	Drawn	Rev
	B	16-MT7620A Power-F.SCH	Kim	2.2
Date: Tuesday, August 12, 2014			Sheet	7 of 20



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	Title SPI Flash			
	Size A	Document Number 21-SPI Flash.SCH	Drawn Kim	Rev 2.2
	Date: Tuesday, August 12, 2014	Sheet 10 of 20		



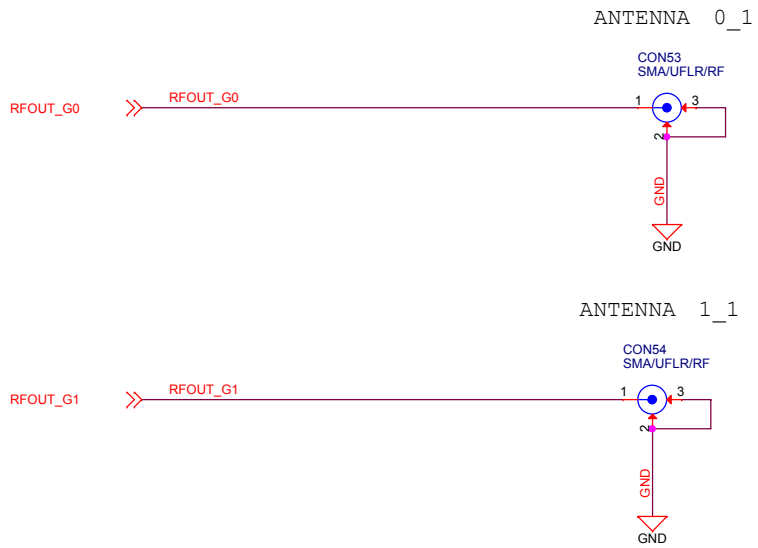


MT7620 Boot Up Strapping


Pin Name	Description	Value
WLED_N	DRAM_FROM_EE For non scan mode:	0: DRAM configuration from EEPROM 1: DRAM configuration from Auto Detect
ANT_TRN	DBG_JTAG_MODE	0: EPHY_LED 1: JTAG MODE
ANT_TRNB	XTAL_FREQ_SEL	0: 20MHz
{SPI_WP, SPI_HOLD}	DRAM_TYPE	01: DDR1 (CPU/3) TSOP 10: DDR2 (CPU/3) FBGA 11: SDRAM (CPU/5) (LVTTL 3.3 V) TSOP Package
{SPI_MOSI, SPI_HOLD, TXD2, GPIO0 }	CHIP_MODE[3:0]	<p>A vector to set chip function/test/debug modes. In non-test/debug operation,</p> <p>0001: Normal mode (boot from ROM+NAND flash 4 cycle address) 0010: Normal mode (boot from SPI 3Byte Addr) 0011: Normal mode (boot from SPI 4Byte Addr) 0100 :iNIC RGMII mode(boot from ROM) 0101: iNIC MII mode(boot from ROM) 0110: iNIC RVMII mode(boot from ROM) 0111: iNIC PHY mode(boot from ROM) 1000: iNIC USB mode(boot from ROM) 1001: iNIC PCIe mode(boot from ROM)</p>

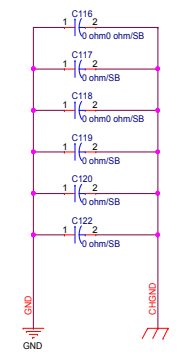
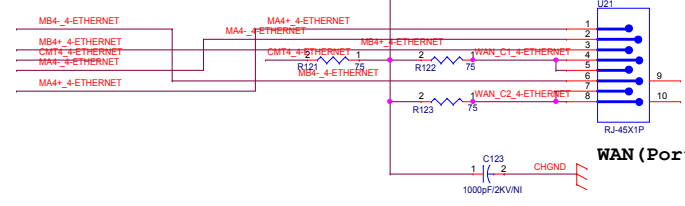
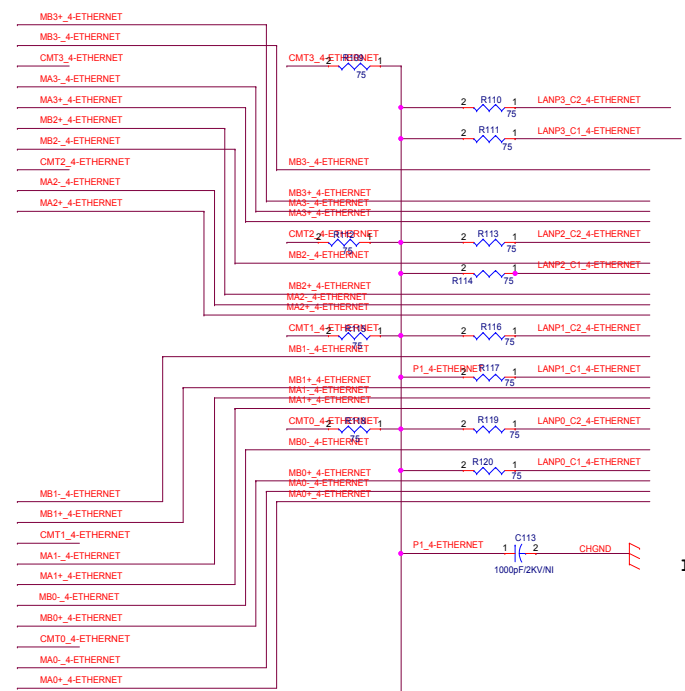
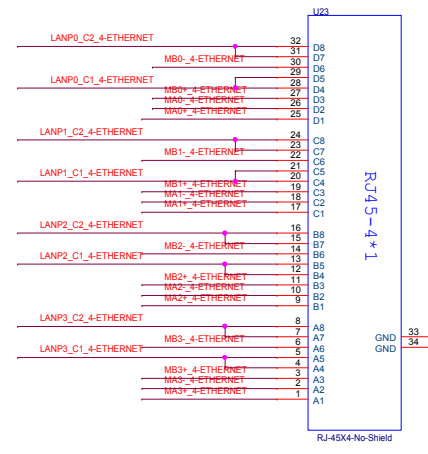
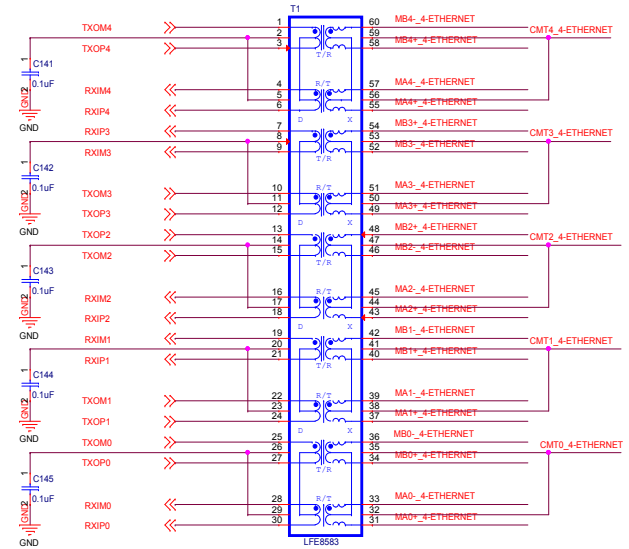
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MEDIATEK	Title Config			
	Size B	Document Number 23-Config.SCH	Drawn Kim	Rev 2.2
	Date:	Tuesday, August 12, 2014	Sheet	12 of 20



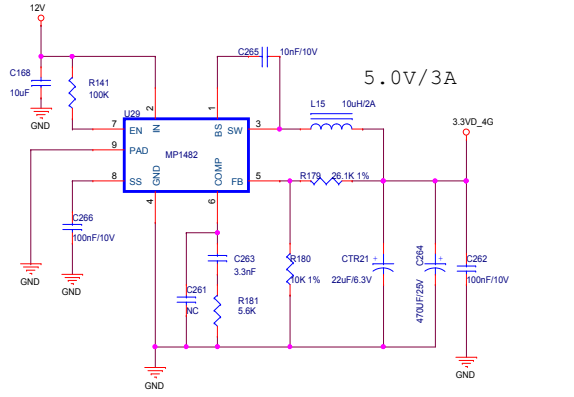
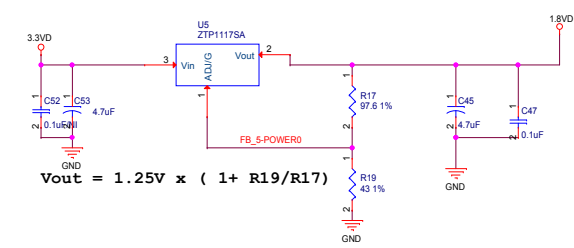
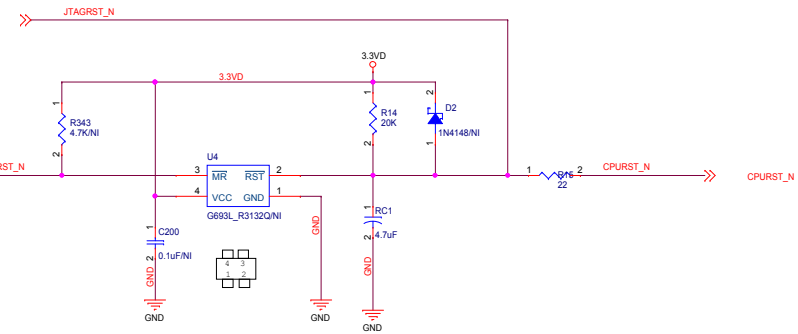
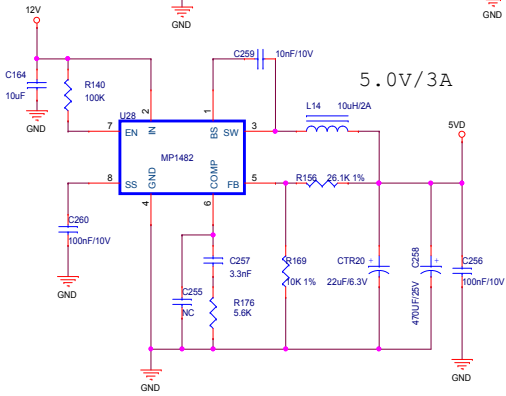
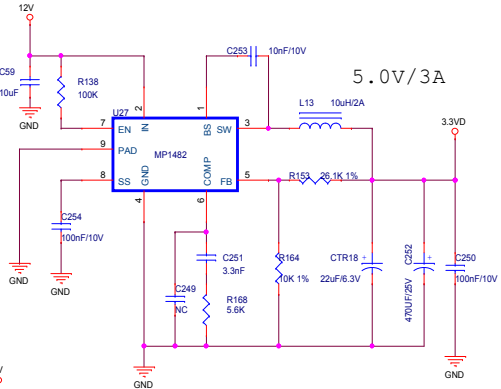
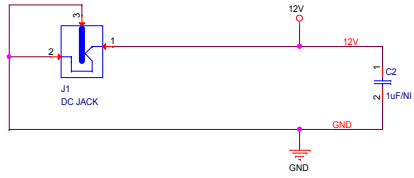
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		Title PA		
		Size B	Document Number 31-Antenna.SCH	Drawn Kim
		Date: Tuesday, August 12, 2014	Sheet 13 of 20	



Reset Circuit

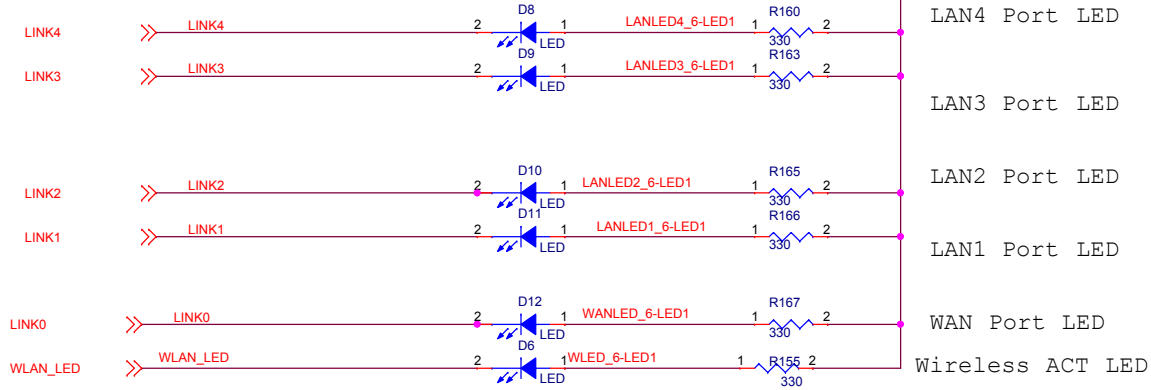
12V DC ADAPTER



GPIO13

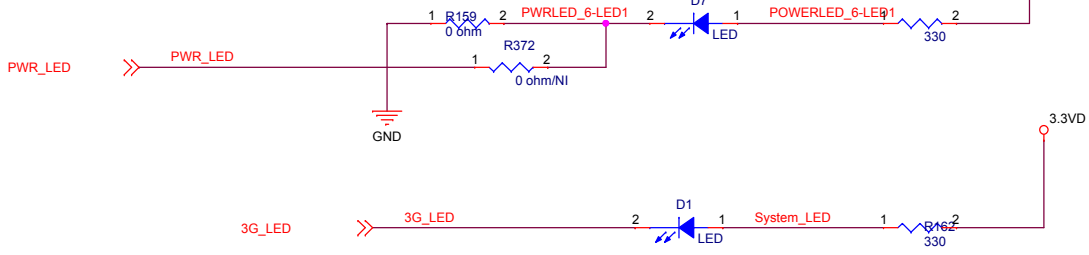
3.3VD

SMD LED



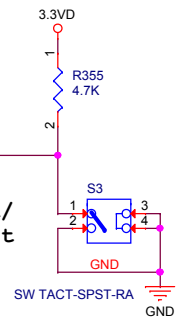
System/Power LED

3.3VD



GPIO1

Software Reset/
Factory Default



WPS PBC



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Title: LED				
Size: B	Document Number	Drawn	Rev	
	6-LED.SCH	Kim	2.2	
Date:	Wednesday, October 15, 2014	Sheet	19	of 20