

DRAM STRAP

DRAM CONFIG	DDR4	LPDDR4
M_DDR4	1	0
M_LPDDR4	0	1

Note: Pull-up to VDDIO_MEM_S3

Madigi

Design Title: **Barcelo**

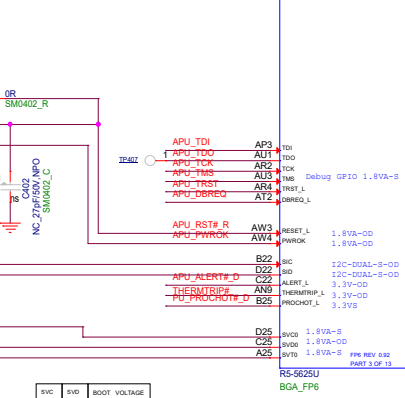
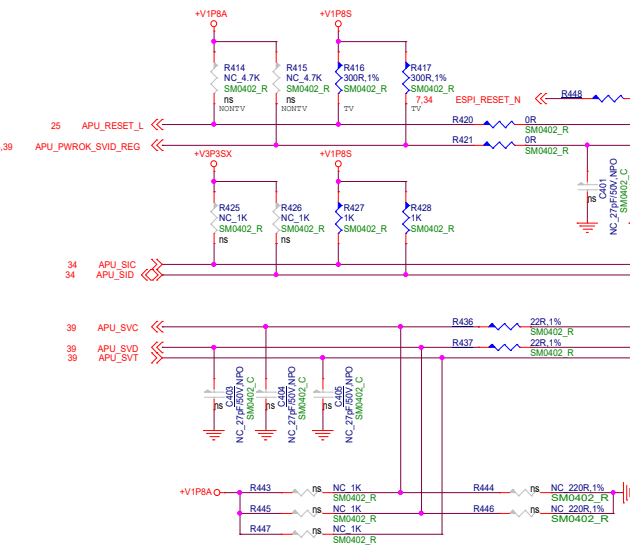
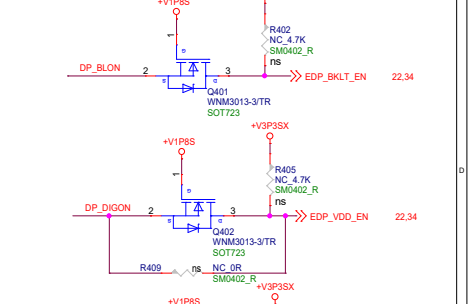
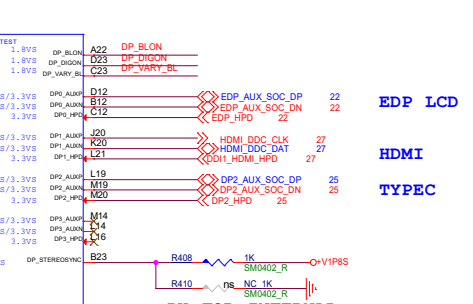
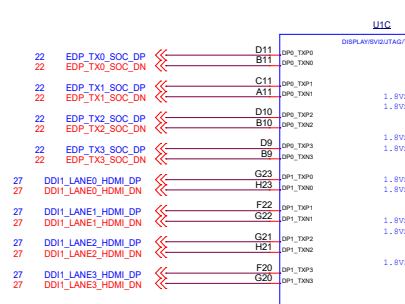
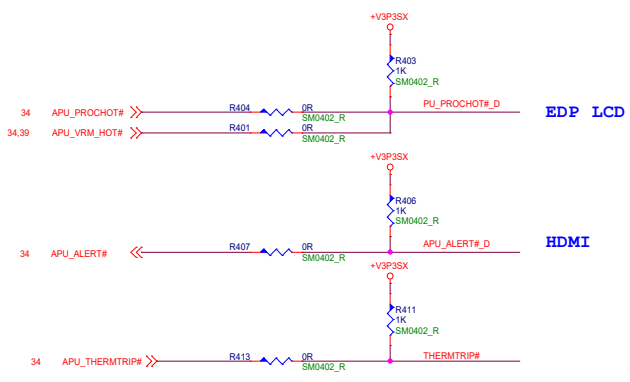
Project Name: N156EBL01

Document Number: Page Name: **SOC_A(DDR CHANNEL A)**

Design Date: Monday, April 17, 2023 Author: Java

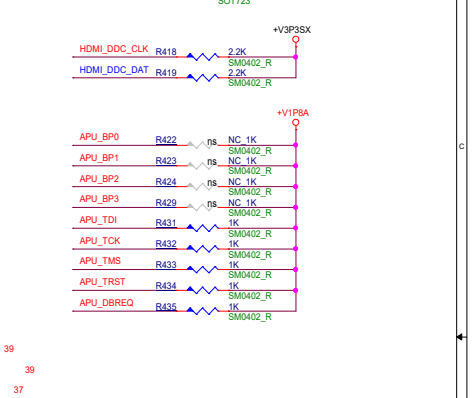
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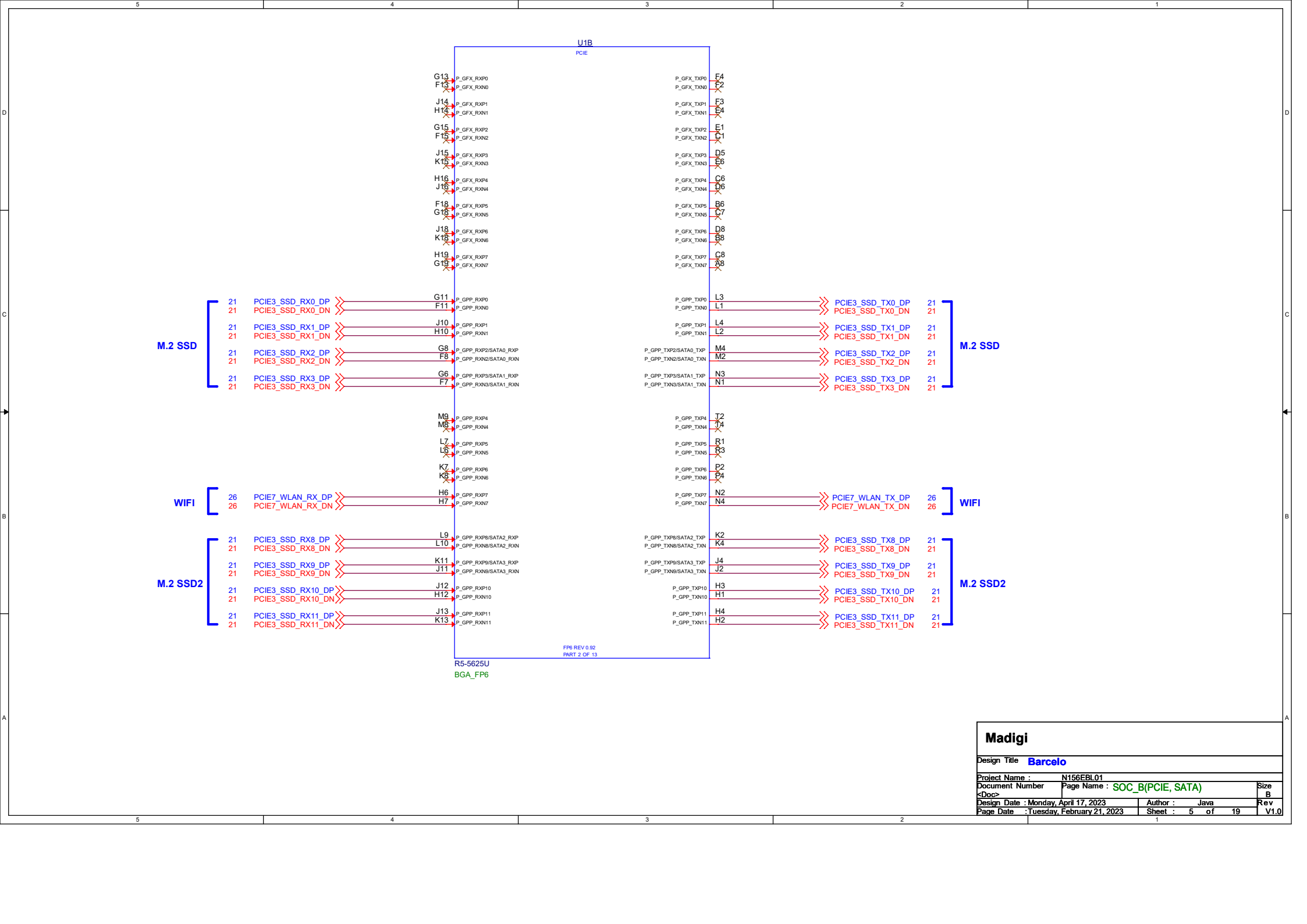
R5-5825U BGA_FP6
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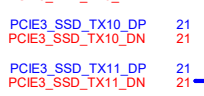
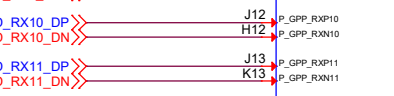
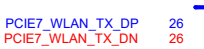
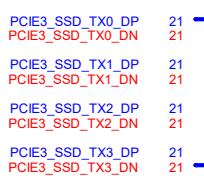
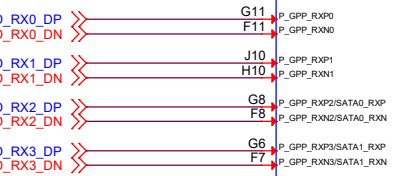
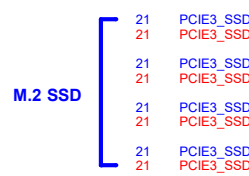
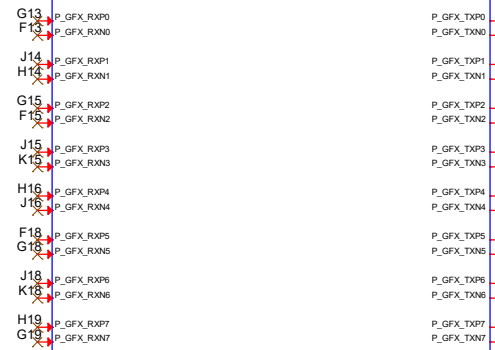
SVC	SVID	BOOT	VOLTAJE
0	0	0	1.1
0	1	1	1.6
1	0	0	0.6
1	1	0	0.6

For normal operation system all switches





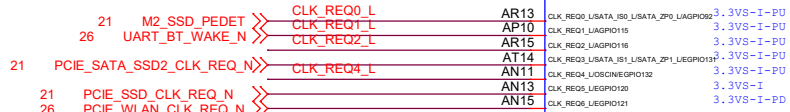
U1B
PCIE



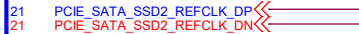
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R5-5625U
BGA_FP6

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Document Number		Page Name : SOC_B(PCIE, SATA)	
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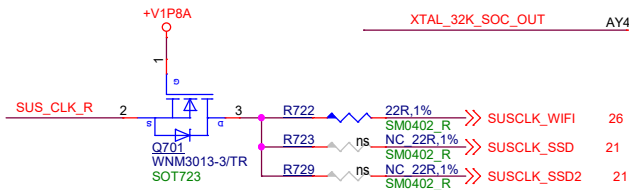
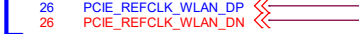
SSD2



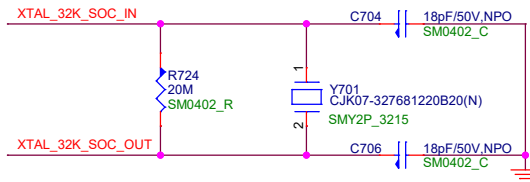
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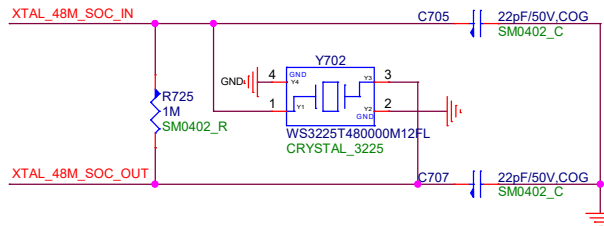
WIFI



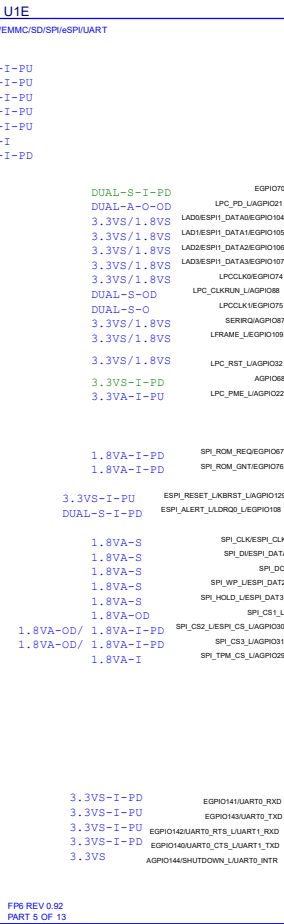
32.768-kHz XTAL(± 10PPM)
Typically 15 pF capacitor
The maximum ESR of the XTAL is 65 kΩ .



48MHz XTAL(± 10PPM)
typically 22 pF capacitor



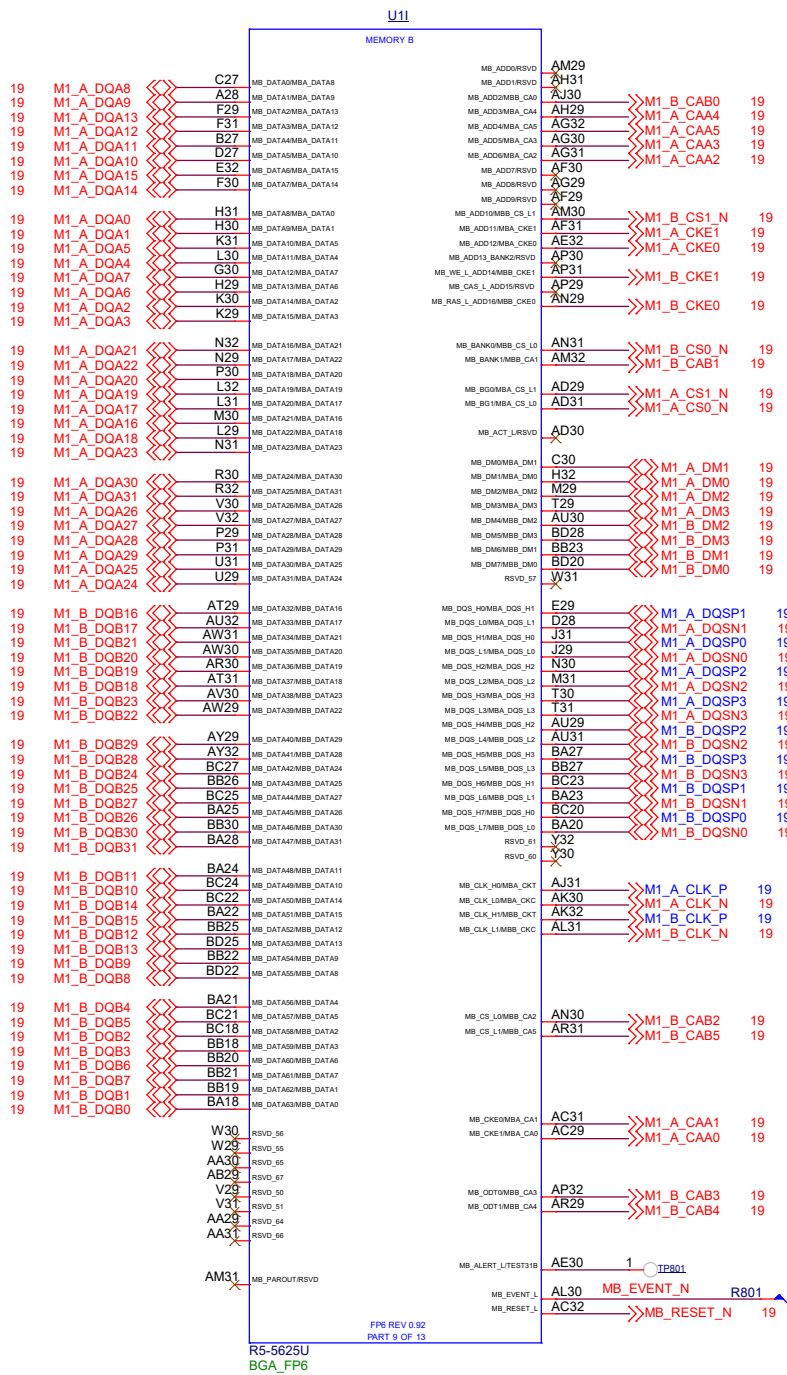
R5-5625U
BGA_FPB6



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STRAP	DEFINITION
SPI_CLK	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS (DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY

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USB3.0 TYPEC

USB3.0 CN_USB1

USB3.0 FP_IO1

USB3.0 FP_IO2

USB3.0 TYPEC

USB3.0 CN_USB1

FingerPrint

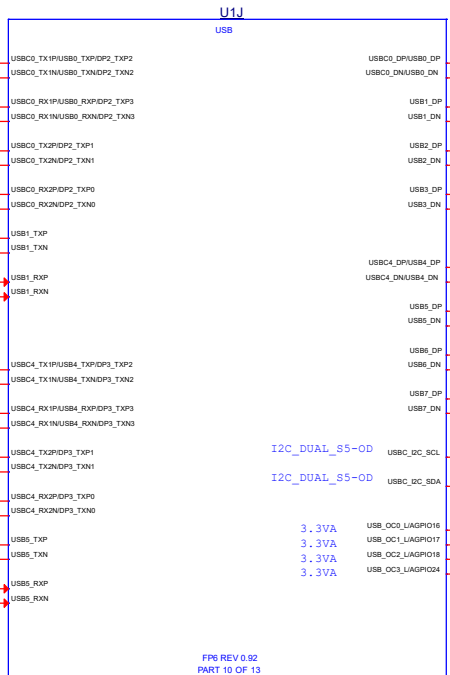
camera EDPCON

USB3.0 FP_IO1

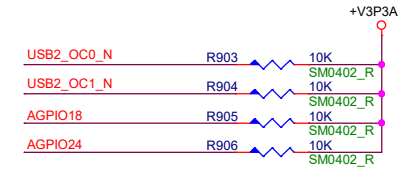
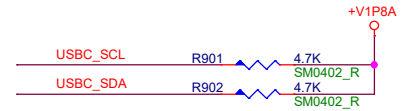
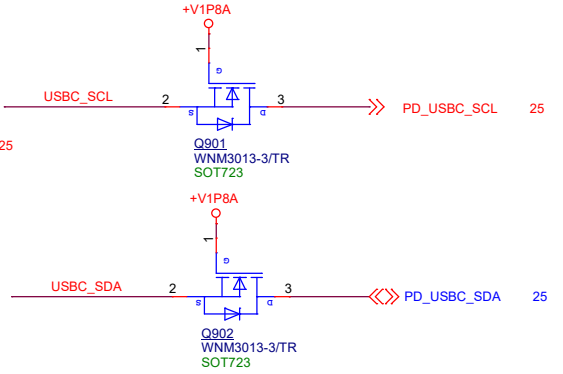
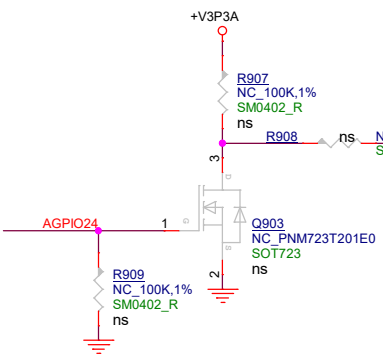
USB3.0 FP_IO2

CardReader

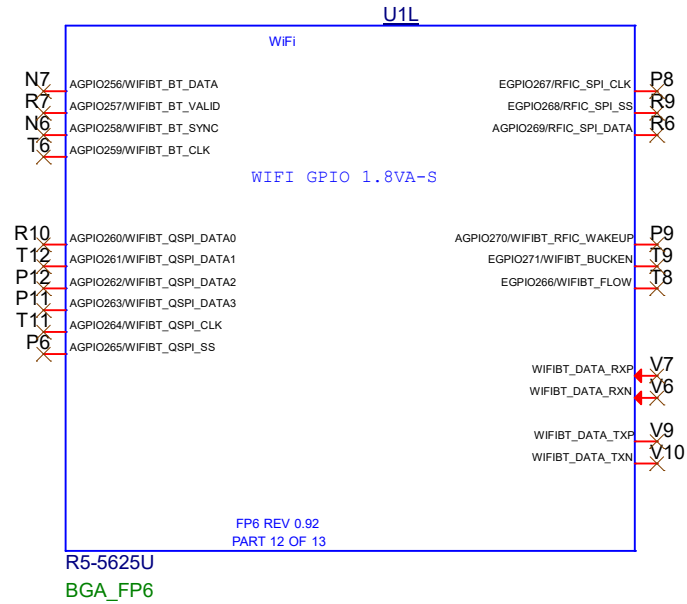
WIFI module BT



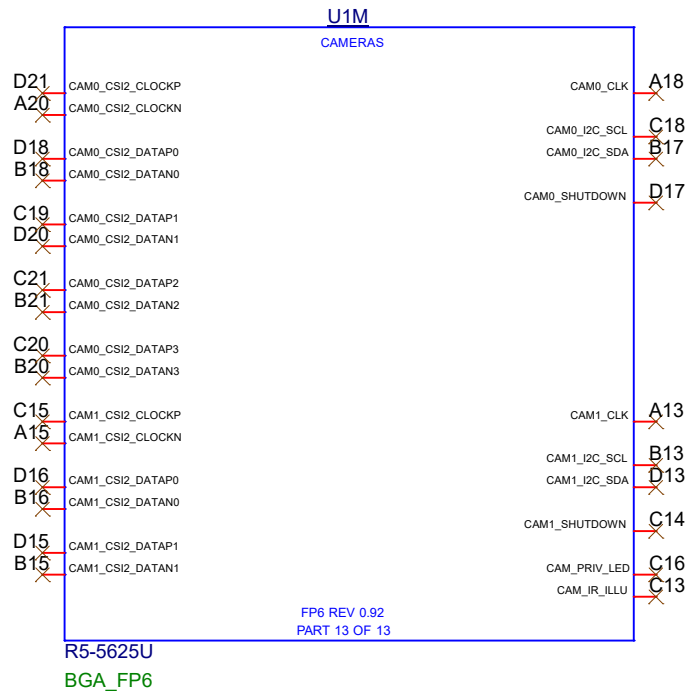
R5-5625U BGA_FP6



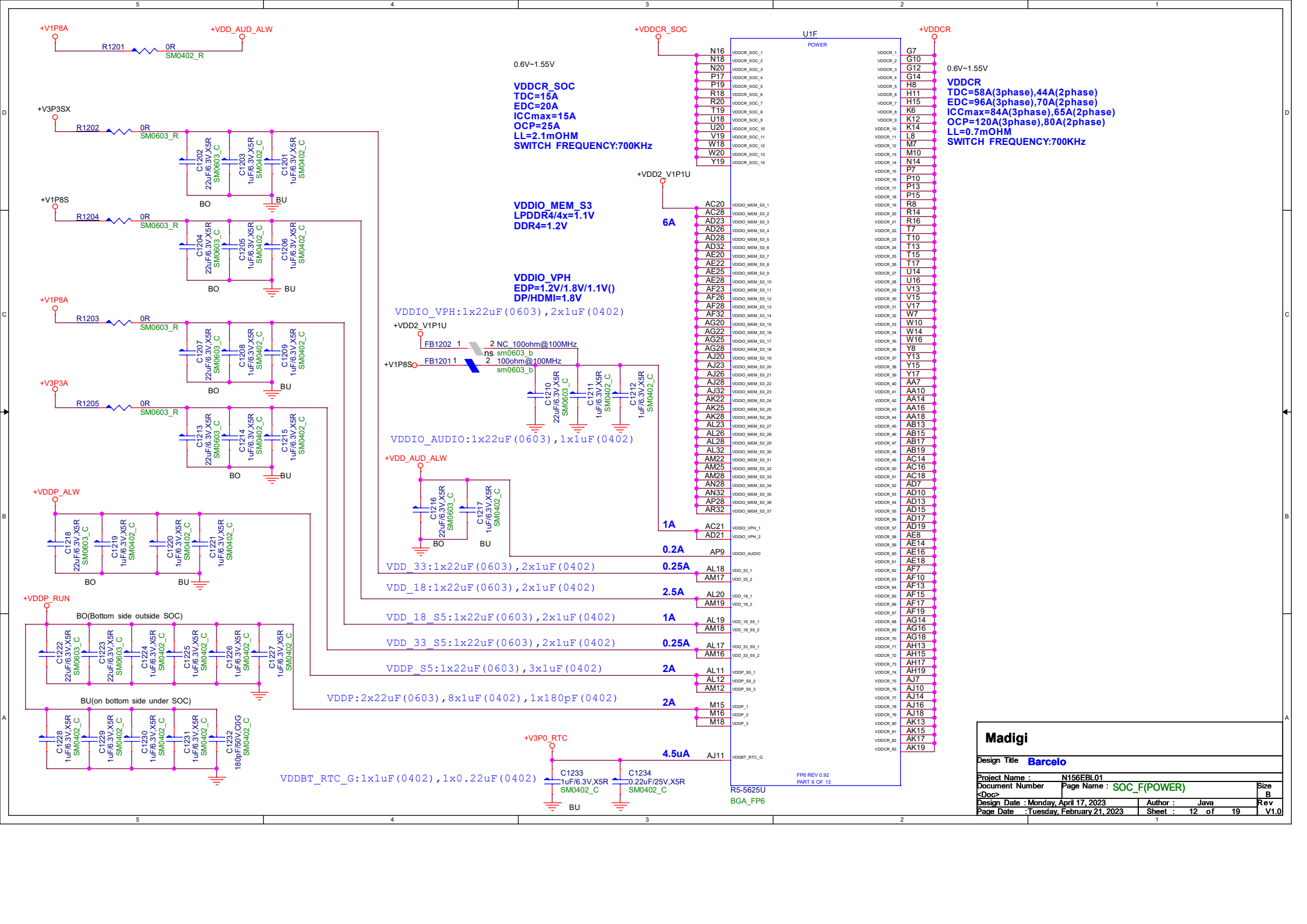
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0.6V-1.55V
VDDCR_SOC
 TDC=15A
 EDC=20A
 ICmax=15A
 OCP=25A
 LL=2.1mOHM
 SWITCH FREQUENCY:700KHz

VDDIO_MEM_S3
 LPDDR4/4x=1.1V
 DDR4=1.2V

VDDIO_VPH
 EDP=1.2V/1.8V/1.1V()
 DP/HDMI=1.8V

0.6V-1.55V
VDDCR
 TDC=58A(3phase),44A(2phase)
 EDC=96A(3phase),70A(2phase)
 ICmax=84A(3phase),65A(2phase)
 OCP=120A(3phase),80A(2phase)
 LL=0.7mOHM
 SWITCH FREQUENCY:700KHz

VDDIO_VPH:1x22uF(0603), 2x1uF(0402)

+VDD2_V1P1U

+V1P8S

VDDIO_AUDIO:1x22uF(0603), 1x1uF(0402)

+VDD_AUD_ALW

VDD_33:1x22uF(0603), 2x1uF(0402)

VDD_18:1x22uF(0603), 2x1uF(0402)

VDD_18_S5:1x22uF(0603), 2x1uF(0402)

VDD_33_S5:1x22uF(0603), 2x1uF(0402)

VDDP_S5:1x22uF(0603), 3x1uF(0402)

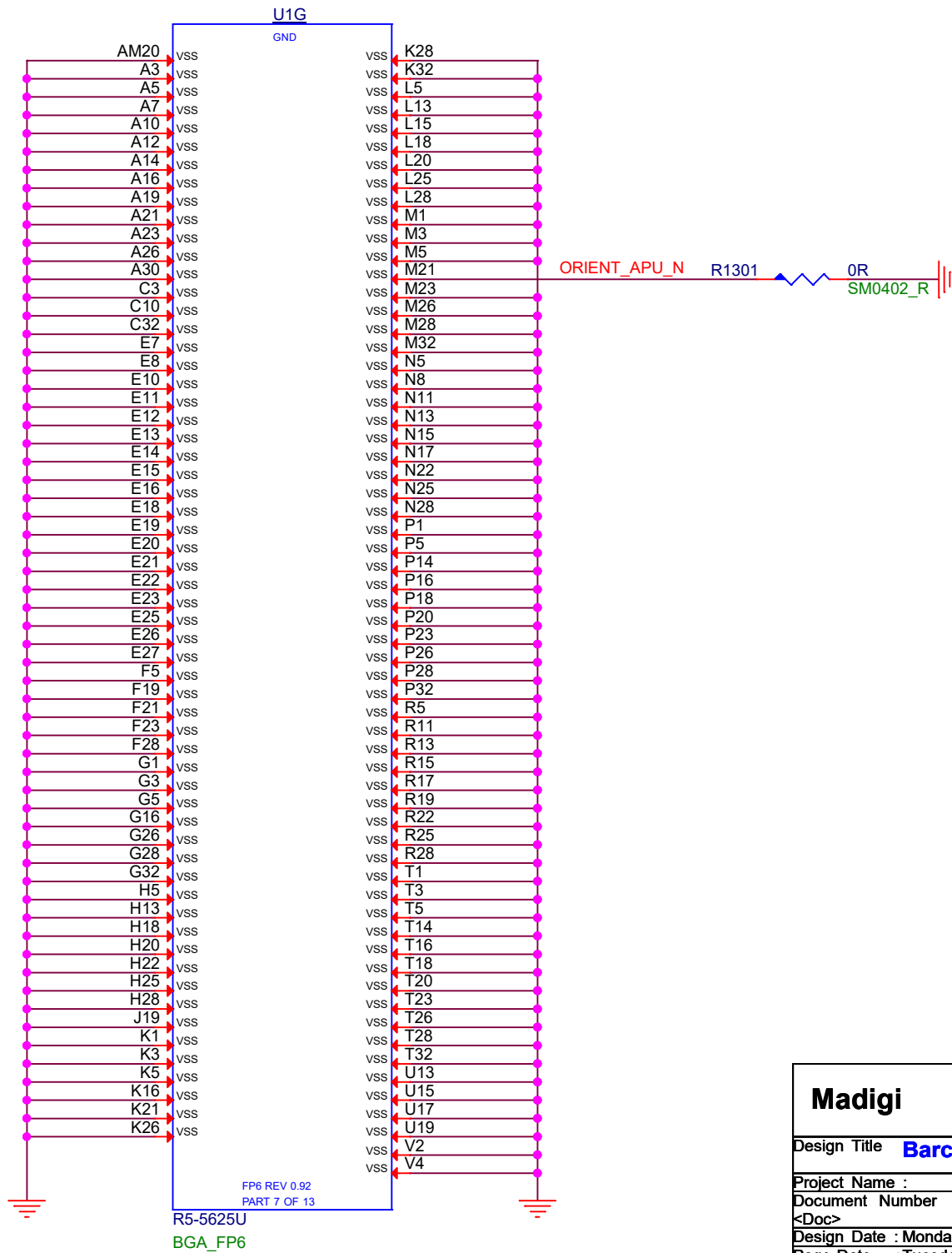
VDDP:2x22uF(0603), 8x1uF(0402), 1x180pF(0402)

VDDBT_RTC_G:1x1uF(0402), 1x0.22uF(0402)

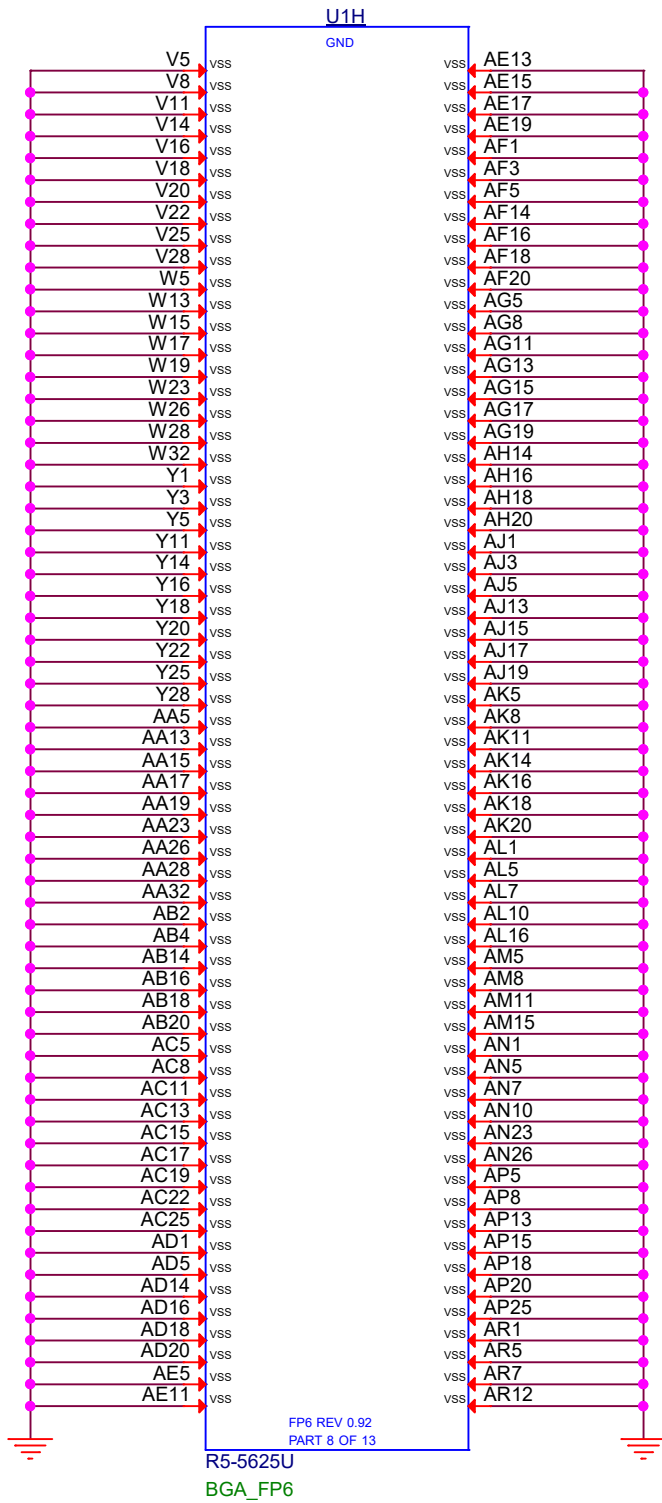
- POWER
- N16 VDDCR_SOC_1
 - N18 VDDCR_SOC_2
 - N20 VDDCR_SOC_3
 - P17 VDDCR_SOC_4
 - P19 VDDCR_SOC_5
 - R18 VDDCR_SOC_6
 - R20 VDDCR_SOC_7
 - T19 VDDCR_SOC_8
 - U18 VDDCR_SOC_9
 - U20 VDDCR_SOC_10
 - V19 VDDCR_SOC_11
 - W18 VDDCR_SOC_12
 - W20 VDDCR_SOC_13
 - Y19 VDDCR_SOC_14
- 6A
- AC20 VDDIO_MEM_S3_1
 - AC28 VDDIO_MEM_S3_2
 - AD23 VDDIO_MEM_S3_3
 - AD26 VDDIO_MEM_S3_4
 - AD28 VDDIO_MEM_S3_5
 - AD32 VDDIO_MEM_S3_6
 - AE20 VDDIO_MEM_S3_7
 - AE22 VDDIO_MEM_S3_8
 - AE25 VDDIO_MEM_S3_9
 - AE28 VDDIO_MEM_S3_10
 - AF23 VDDIO_MEM_S3_11
 - AF26 VDDIO_MEM_S3_12
 - AF28 VDDIO_MEM_S3_13
 - AF32 VDDIO_MEM_S3_14
 - AG20 VDDIO_MEM_S3_15
 - AG22 VDDIO_MEM_S3_16
 - AG25 VDDIO_MEM_S3_17
 - AG28 VDDIO_MEM_S3_18
 - AJ20 VDDIO_MEM_S3_19
 - AJ23 VDDIO_MEM_S3_20
 - AJ26 VDDIO_MEM_S3_21
 - AJ28 VDDIO_MEM_S3_22
 - AJ32 VDDIO_MEM_S3_23
 - AK22 VDDIO_MEM_S3_24
 - AK25 VDDIO_MEM_S3_25
 - AK28 VDDIO_MEM_S3_26
 - AL23 VDDIO_MEM_S3_27
 - AL26 VDDIO_MEM_S3_28
 - AL28 VDDIO_MEM_S3_29
 - AL32 VDDIO_MEM_S3_30
 - AM22 VDDIO_MEM_S3_31
 - AM25 VDDIO_MEM_S3_32
 - AM28 VDDIO_MEM_S3_33
 - AN28 VDDIO_MEM_S3_34
 - AN32 VDDIO_MEM_S3_35
 - AP28 VDDIO_MEM_S3_36
 - AR32 VDDIO_MEM_S3_37
- 1A
- AC21 VDDIO_VPH_1
 - AD21 VDDIO_VPH_2
- 0.25A
- AL18 VDD_33_1
 - AM17 VDD_33_2
- 2.5A
- AL20 VDD_18_1
 - AM19 VDD_18_2
- 1A
- AL19 VDD_18_S5_1
 - AM18 VDD_18_S5_2
- 0.25A
- AL17 VDD_33_S5_1
 - AM16 VDD_33_S5_2
- 2A
- AL11 VDDP_S5_1
 - AM12 VDDP_S5_2
- 2A
- M15 VDDP_1
 - M16 VDDP_2
 - M18 VDDP_3
- 4.5uA
- AJ11 VDDBT_RTC_G
- R5-5625U
 BGA_FP6

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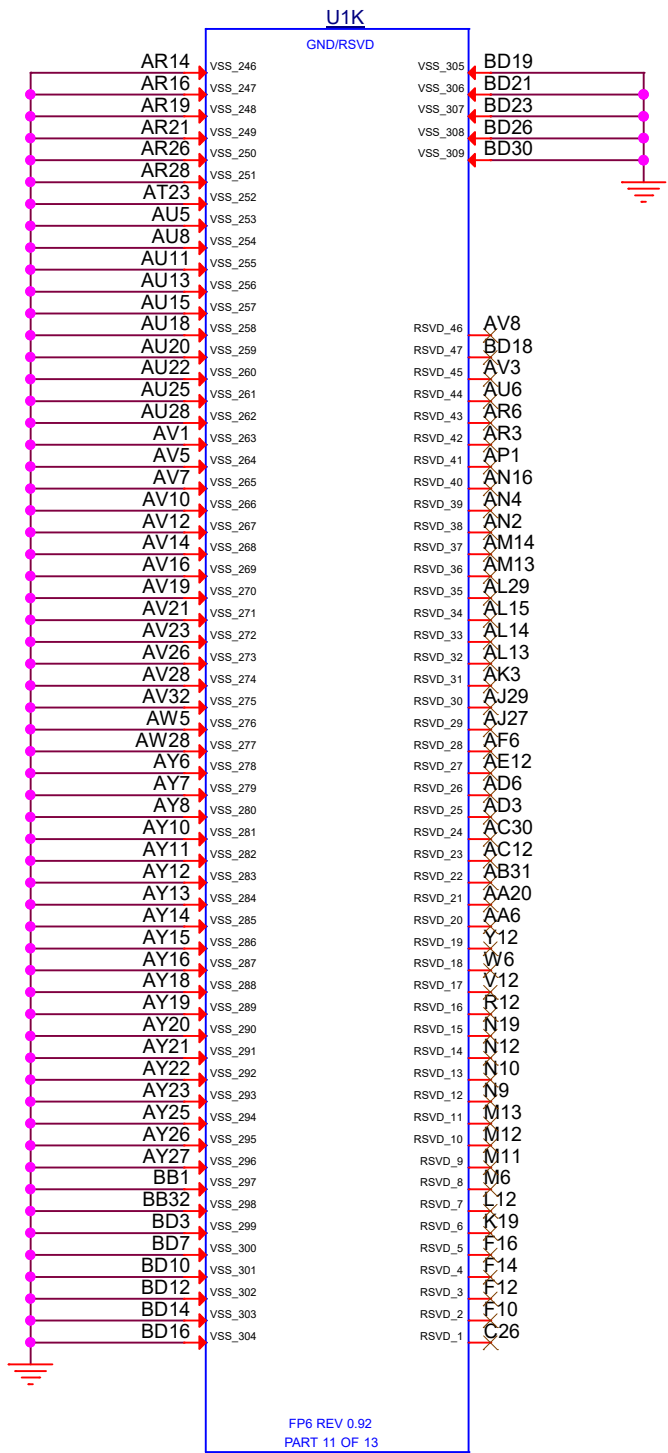
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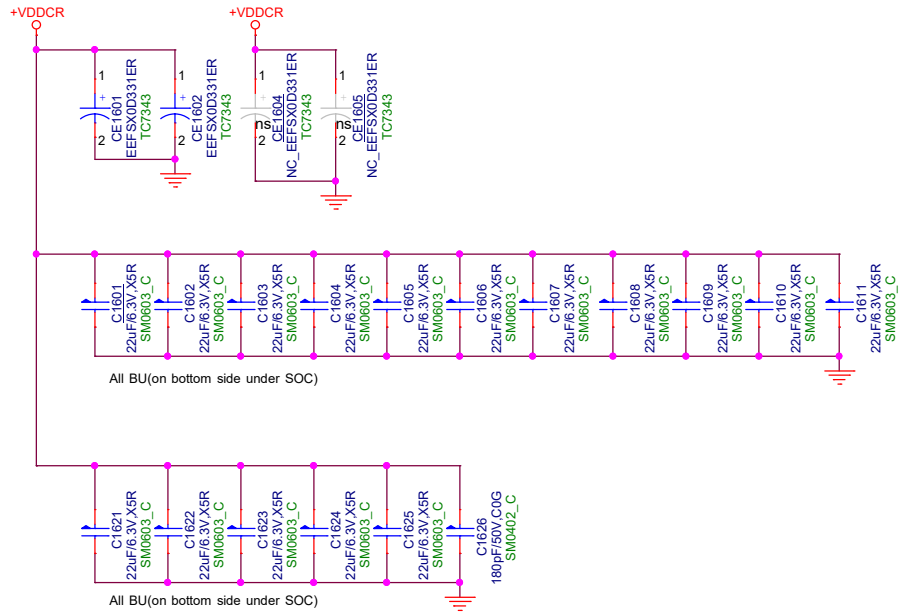


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BGA_FP6

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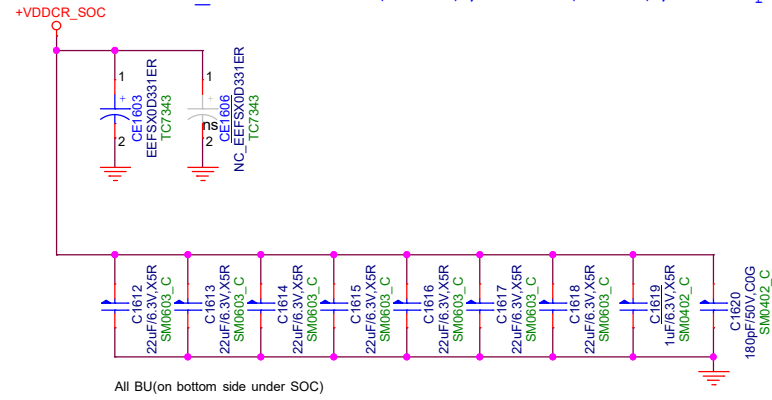
VDDCR: 16x22uF (0603), 1x180pF (0402)



All BU(on bottom side under SOC)

All BU(on bottom side under SOC)

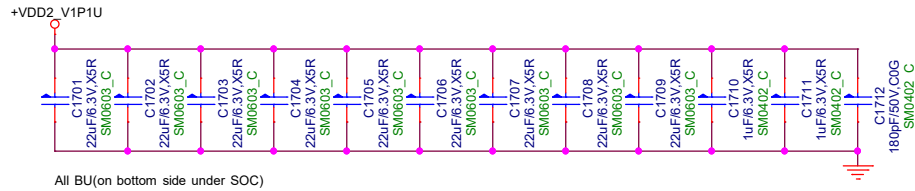
VDDCR_SOC: 7x22uF (0603), 1x1uF (0402), 1x180pF (0402)



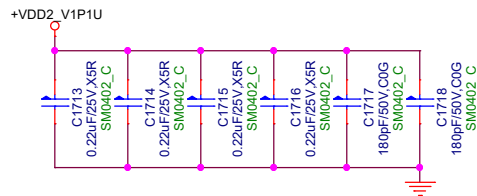
All BU(on bottom side under SOC)

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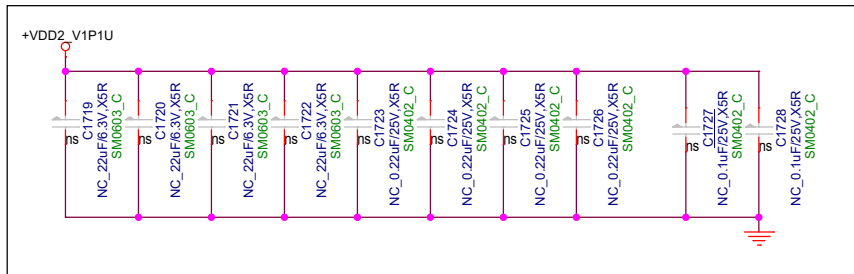
VDDIO_MEM_S3: 9x22uF (0603), 2x1uF (0402), 4x0.22uF (0402), 1x180pF (0402)



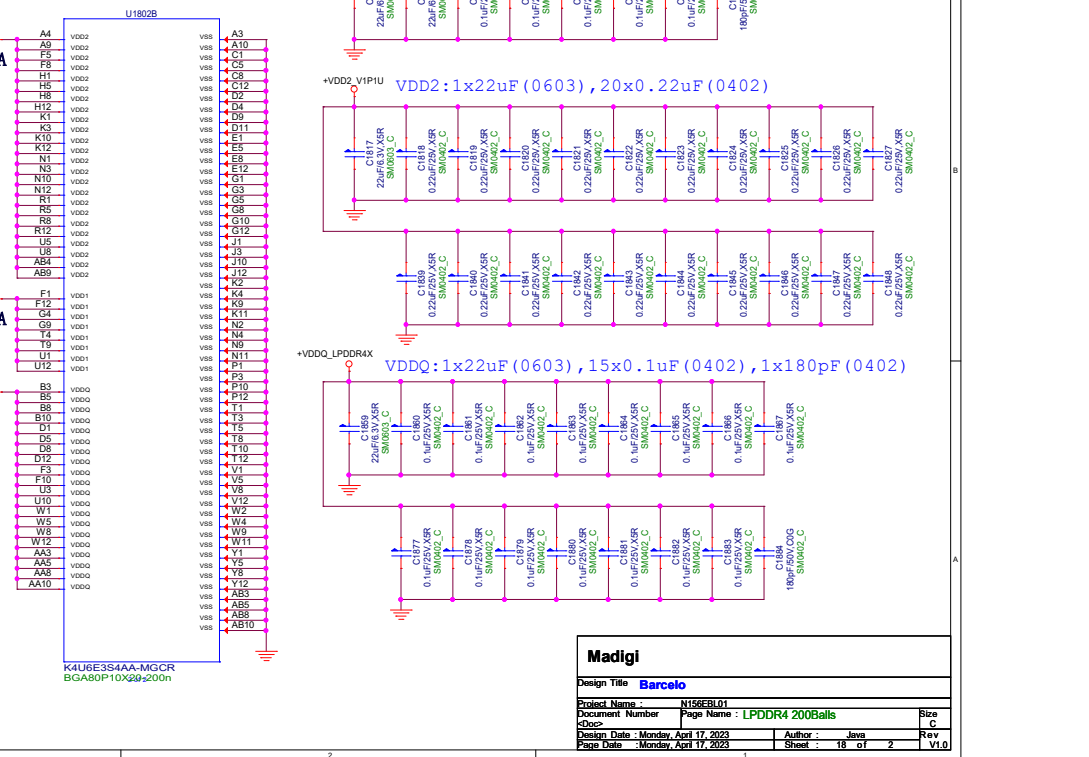
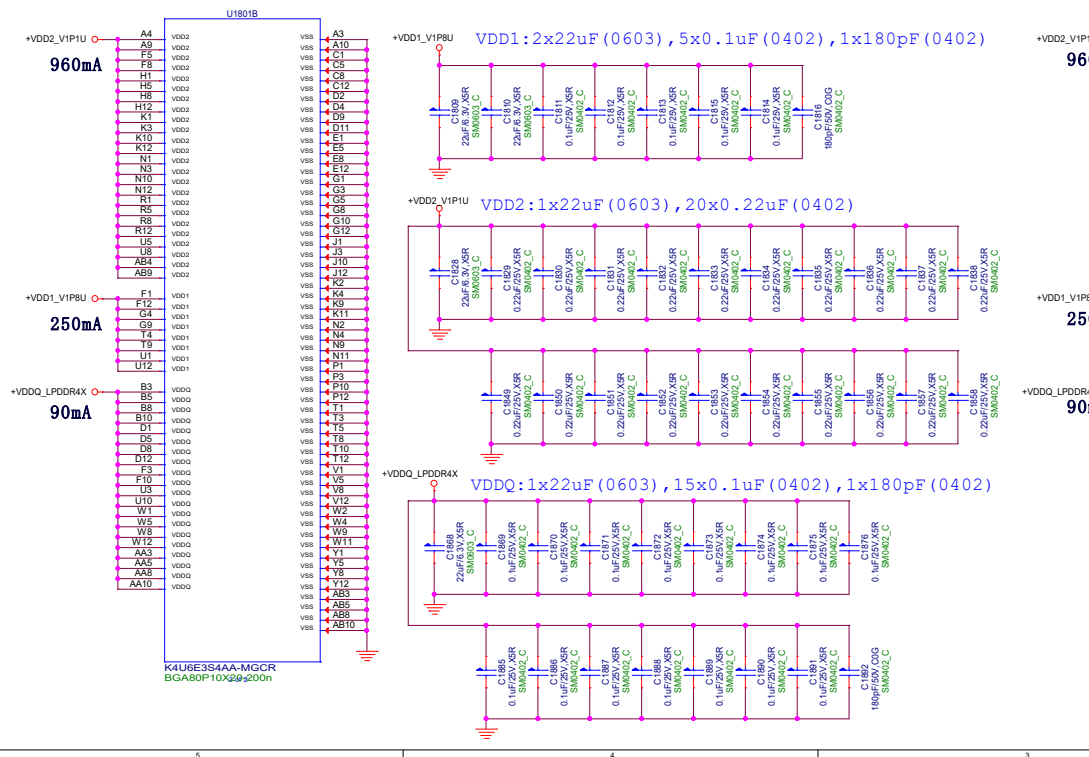
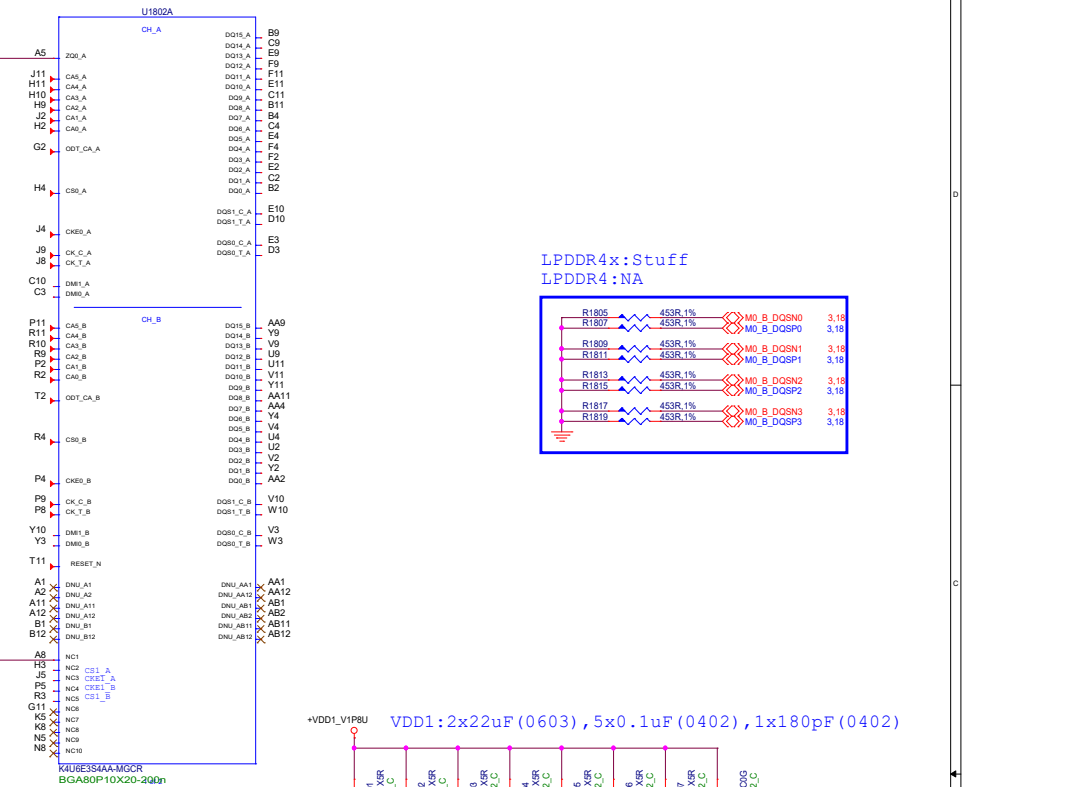
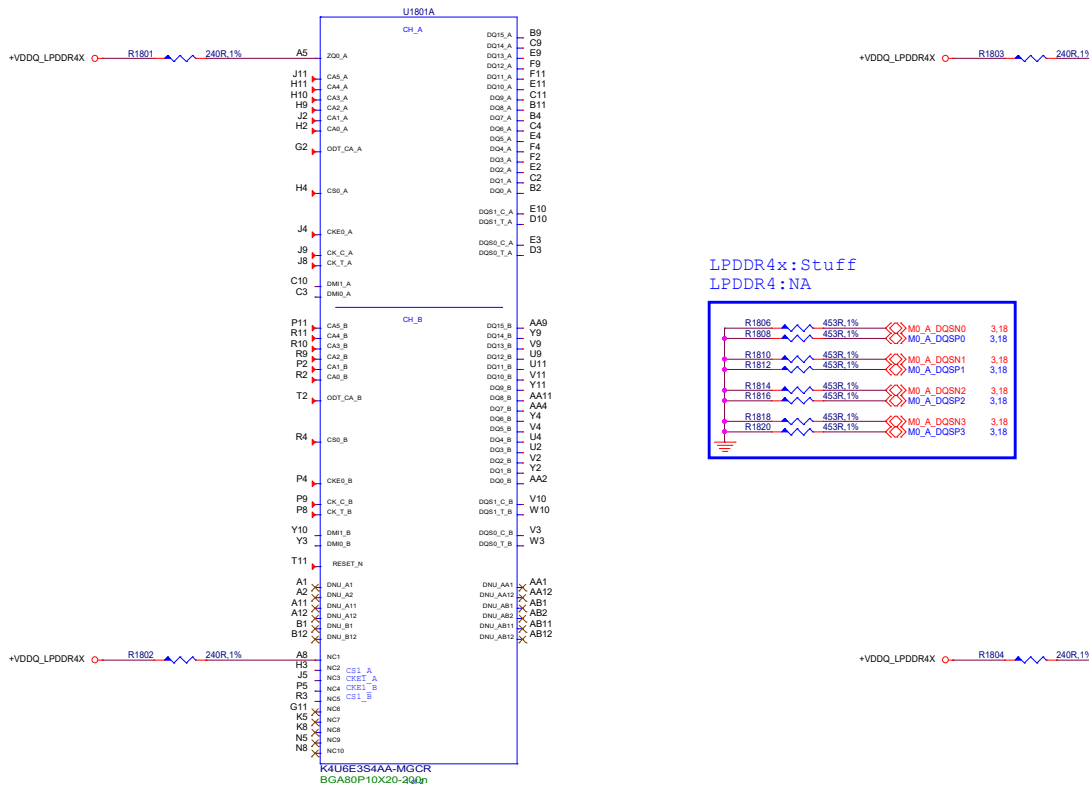
All BU(on bottom side under SOC)

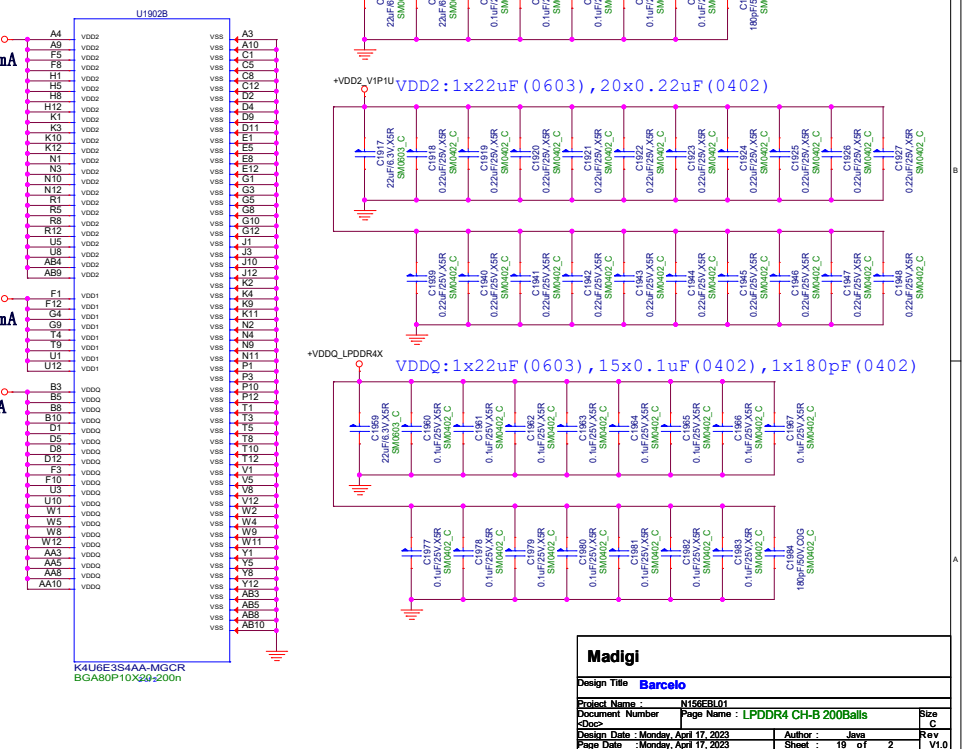
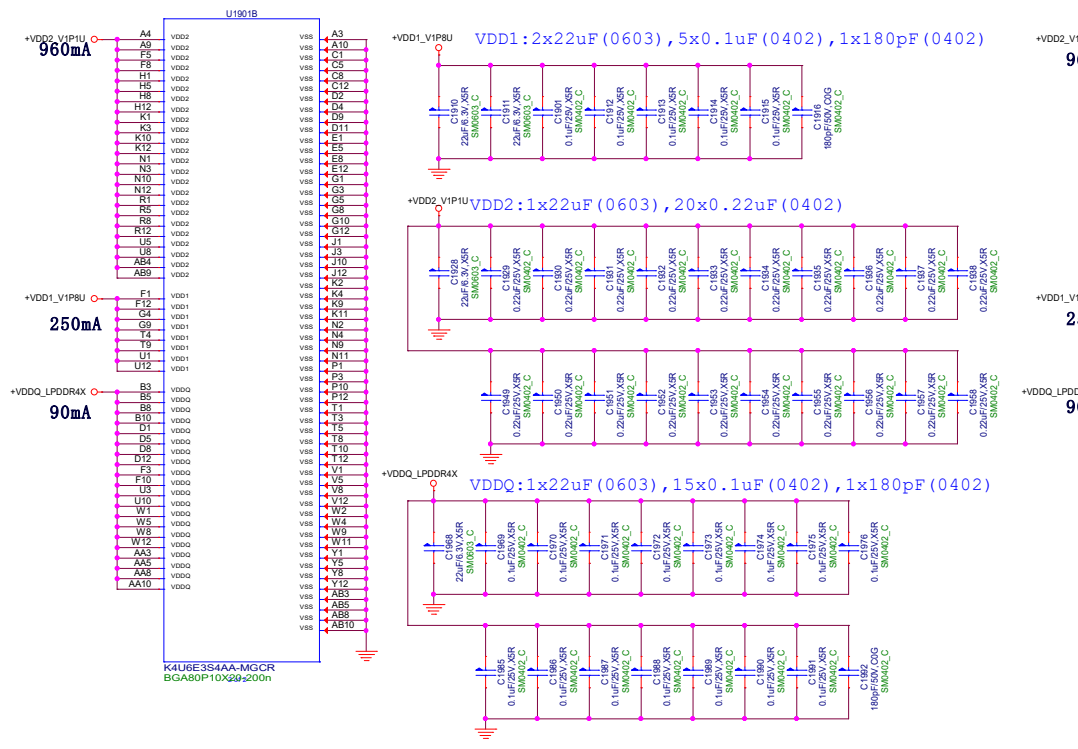
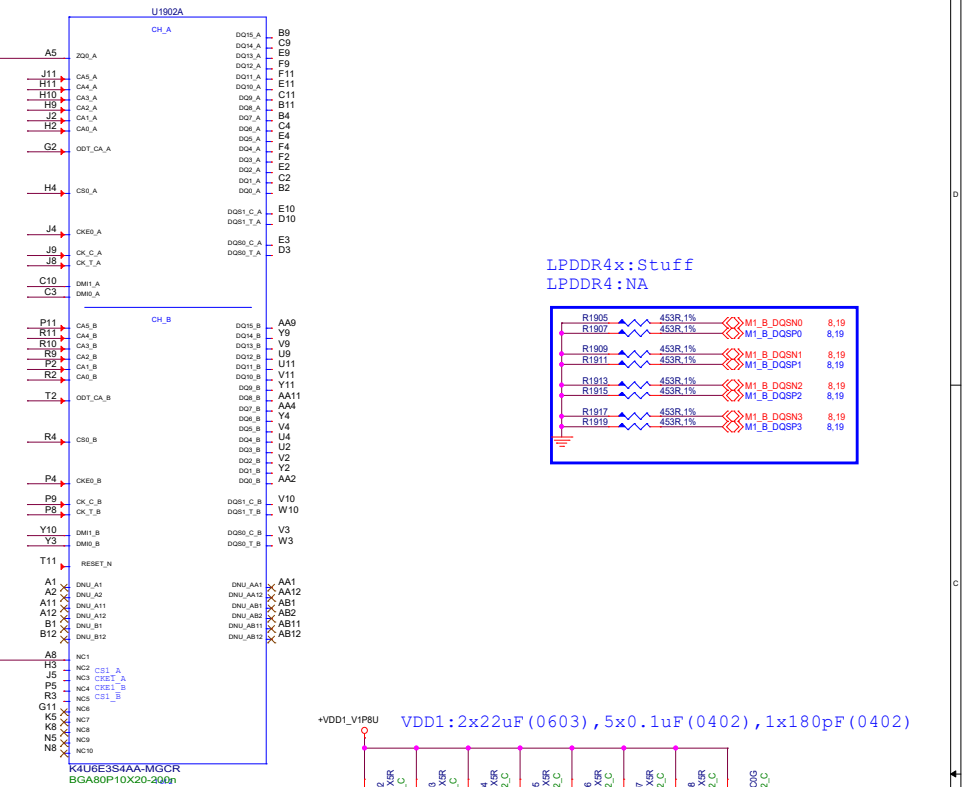
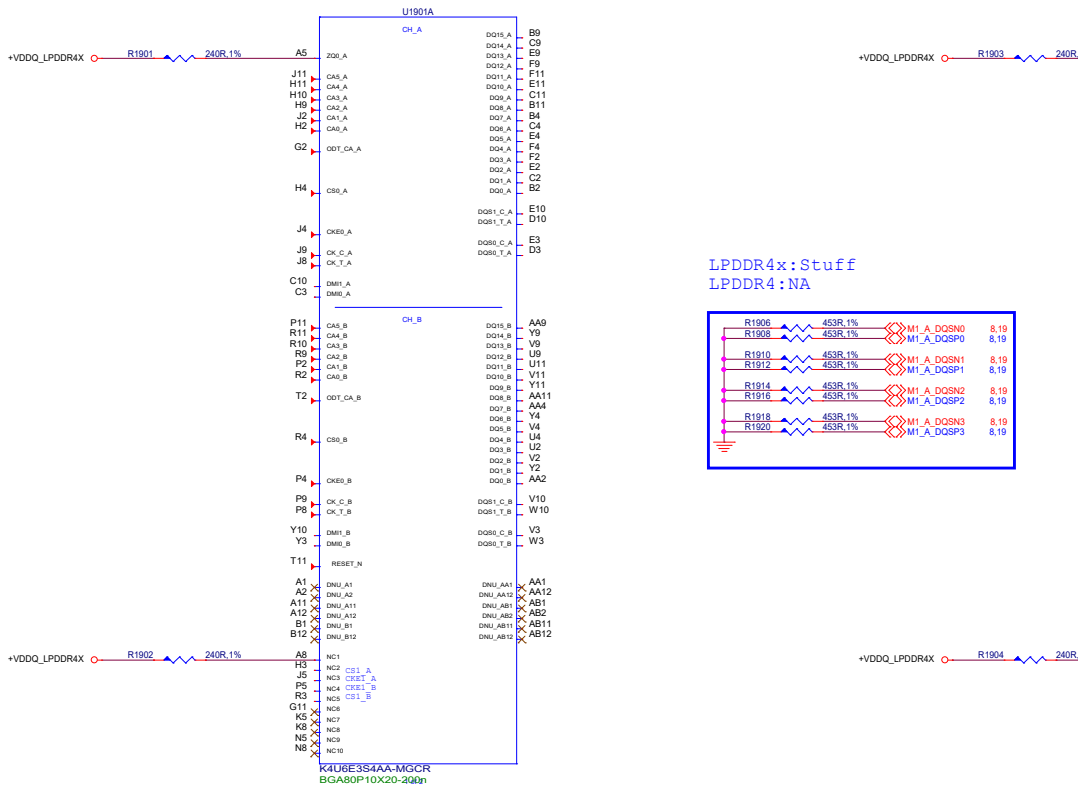


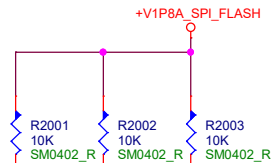
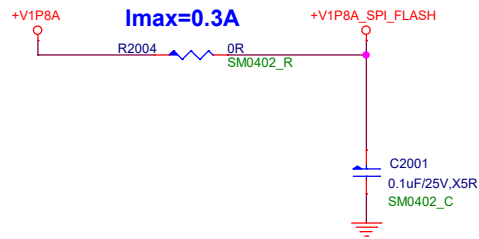
VDDIO_MEM_S3(place hole): 4x22uF (0603), 4x0.22uF (0402), 2x0.1uF (0402)



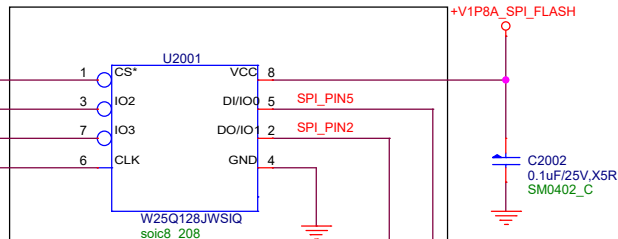
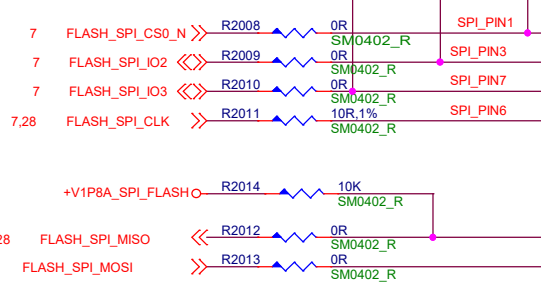
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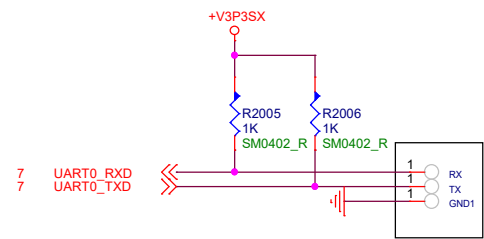
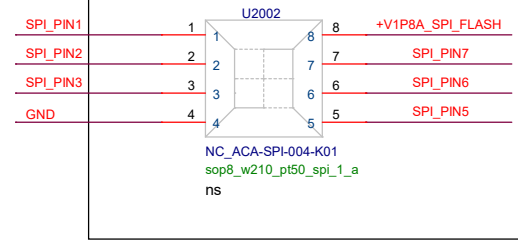


SYSTEM FLASH



DVT/PVT/MP Stuff U2001
EVT Stuff U2002

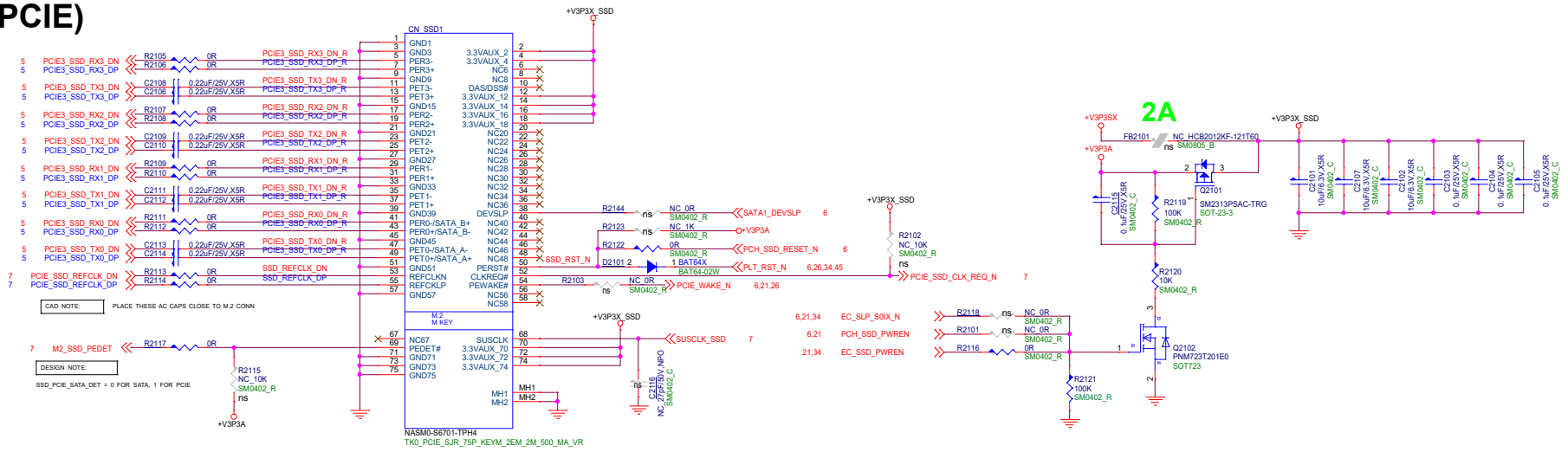
CO-LAY



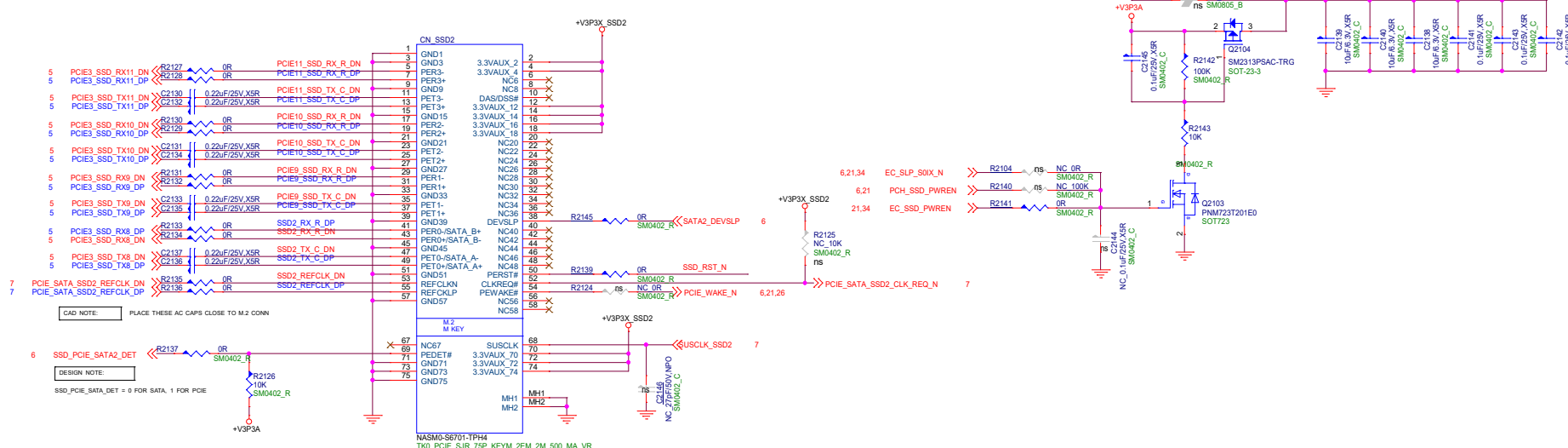
Testpoint place top side

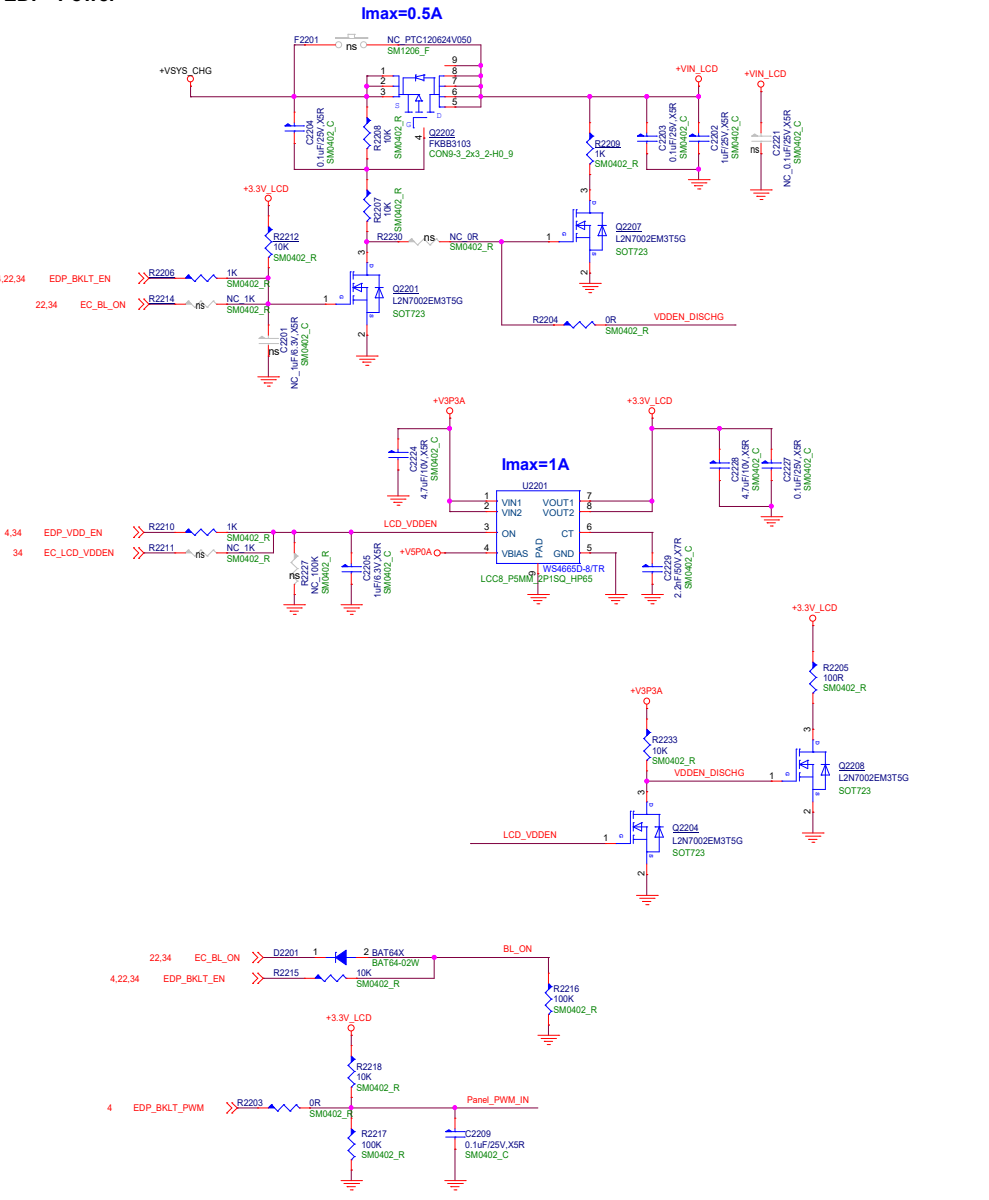
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Design Title Barcelo			
Project Name : N156EBL01		Size B	
Document Number		Page Name : SYSTEM FLASH	Rev B
Design Date : Monday, April 17, 2023		Author : Java	Rev
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M.2 SSD(PCIE)

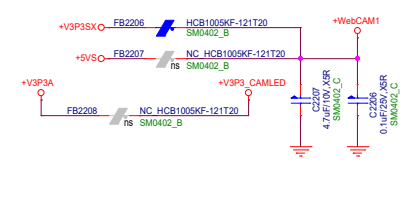


M.2 SSD(SATA or PCIE)

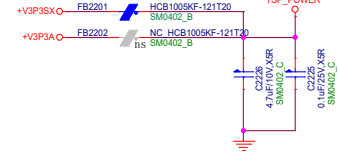




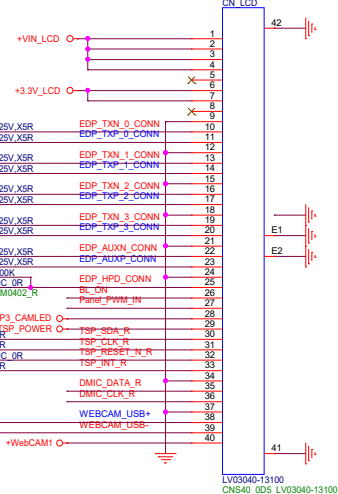
Imax=0.5A CAM Power



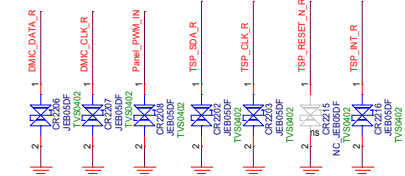
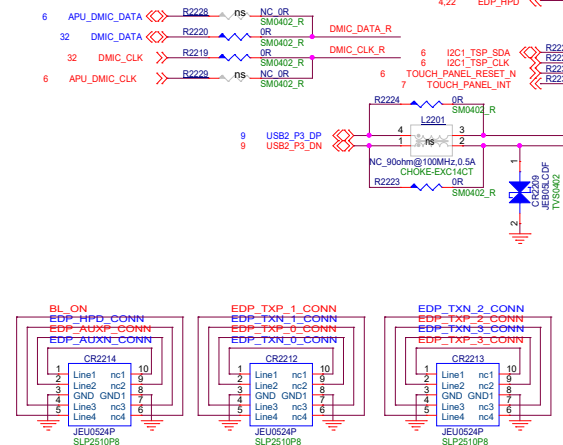
TouchPanel Power



EDP CONN1



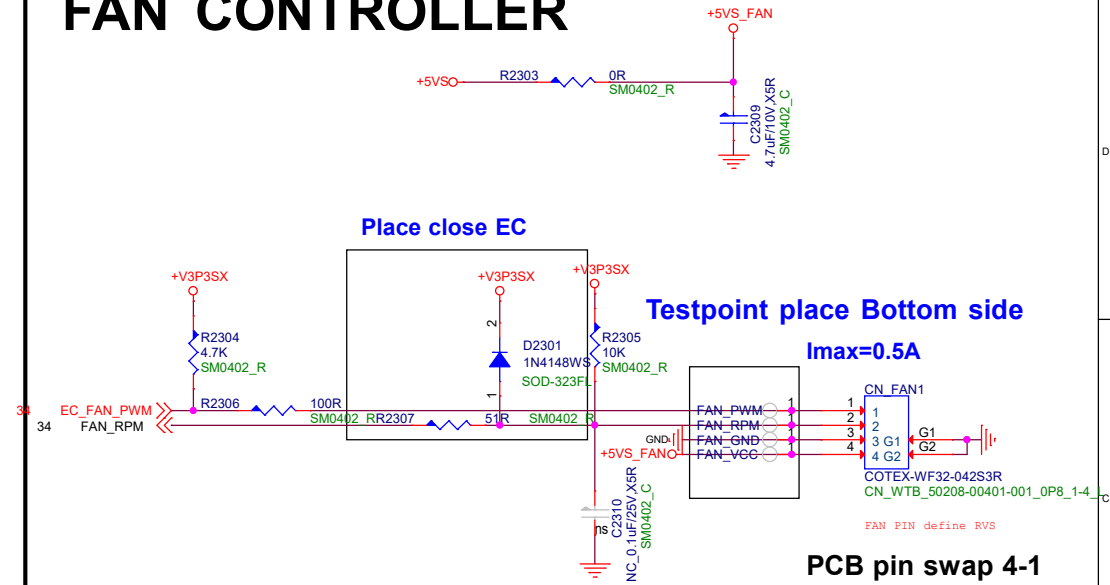
DMIC



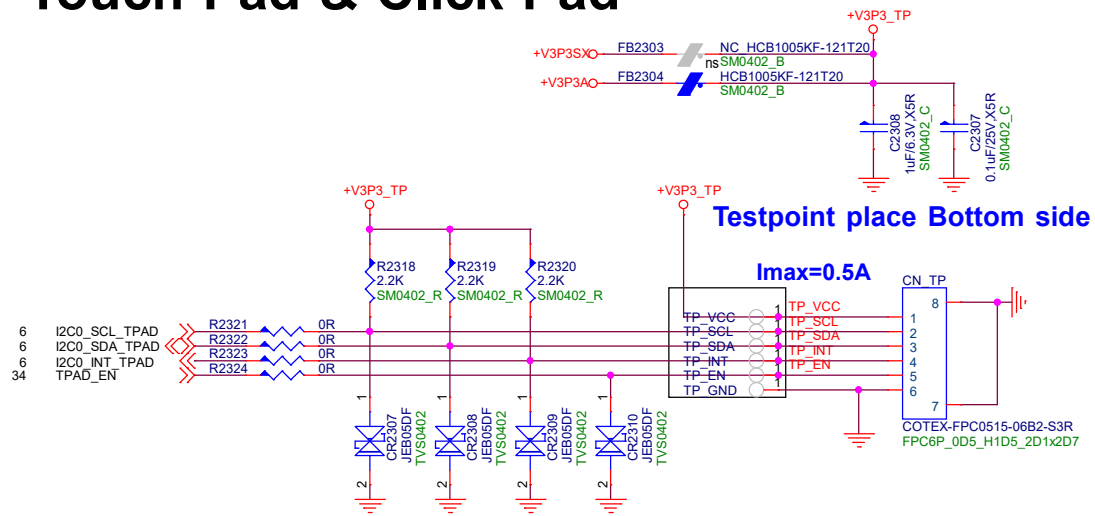
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Project Name	N156EBL01		
Document Number	Page Name : eDP CONN/CAMERA		
Design Date	Monday, April 17, 2023	Author	Java
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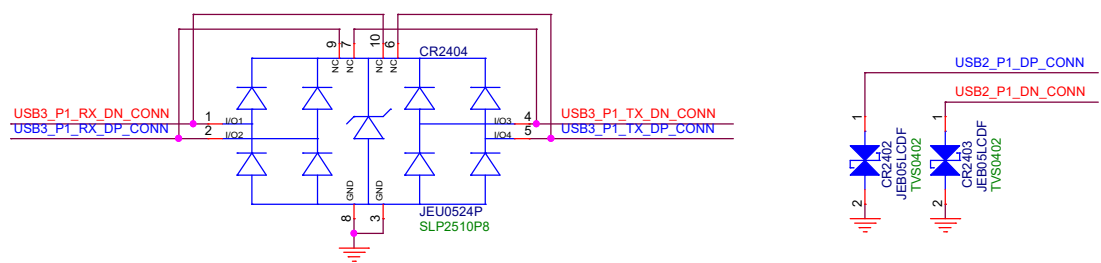
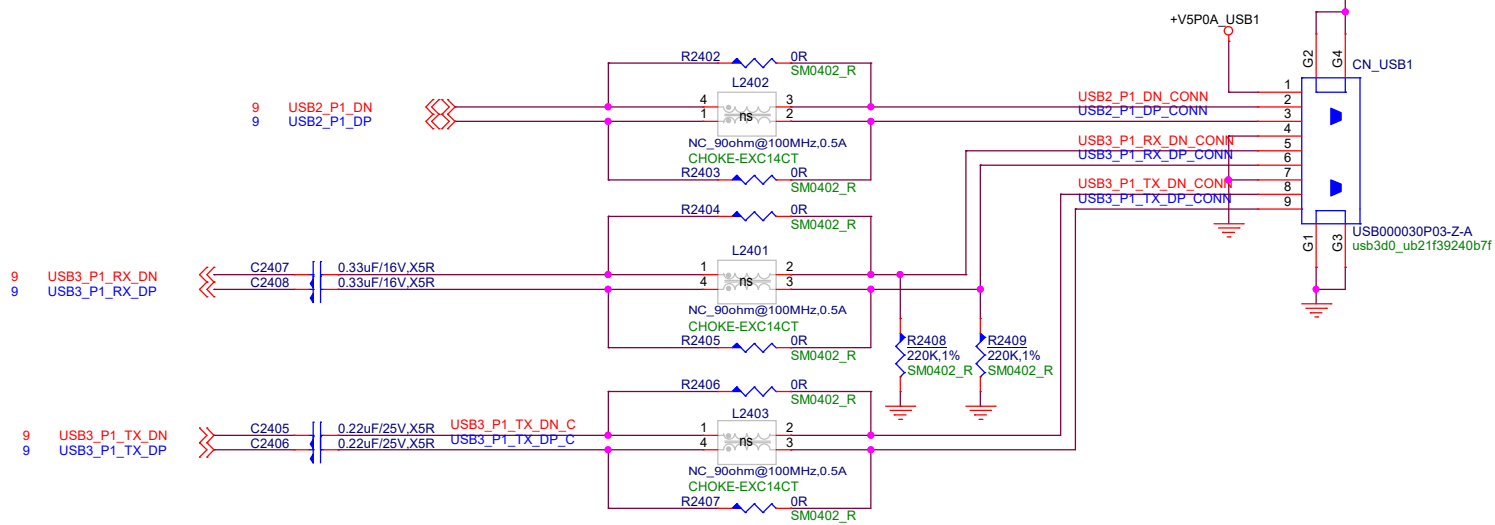
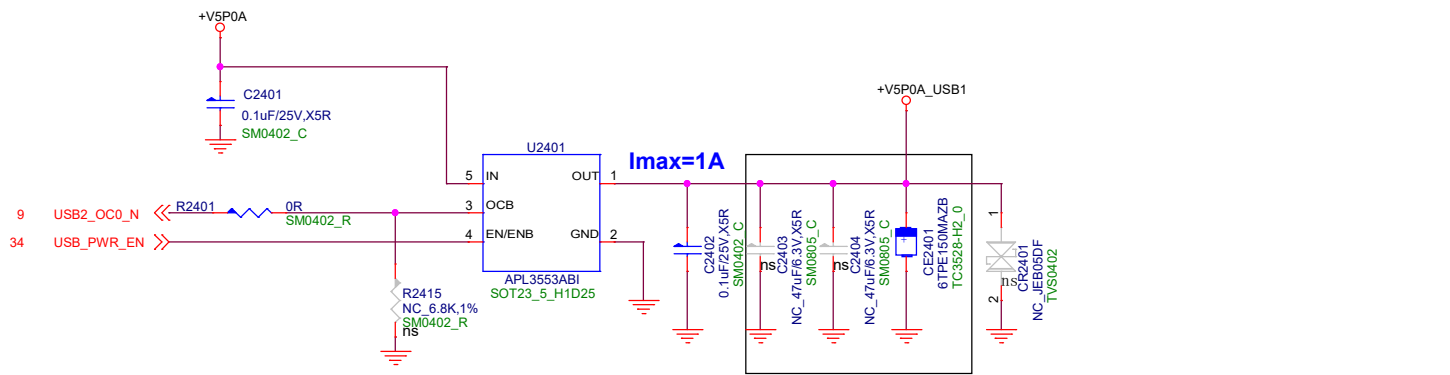
FAN CONTROLLER



Touch Pad & Click Pad

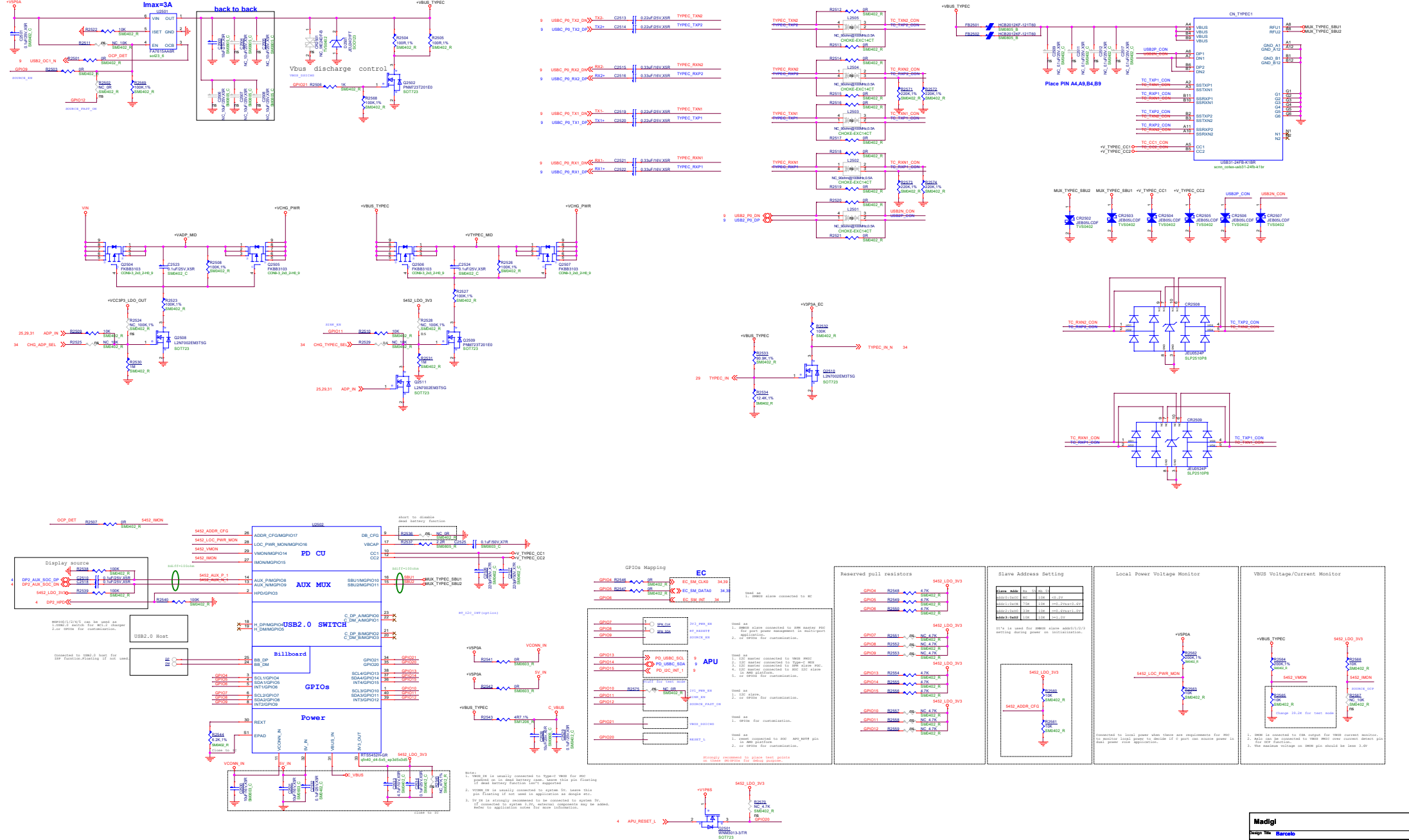


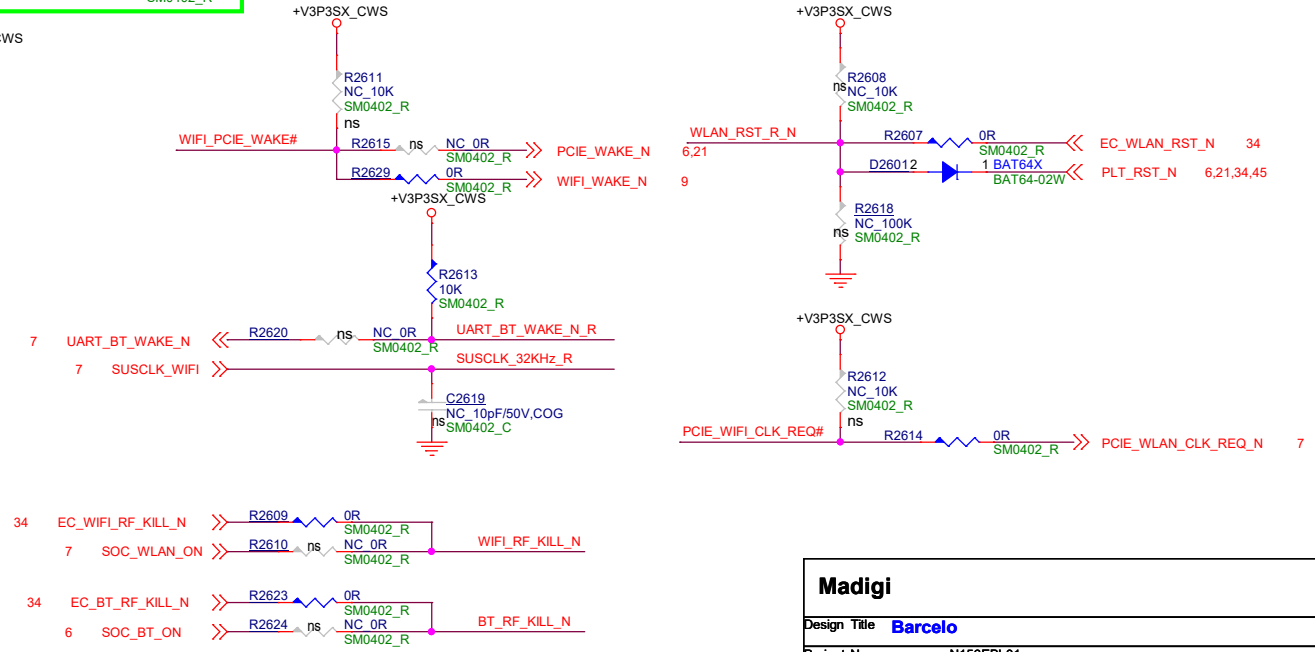
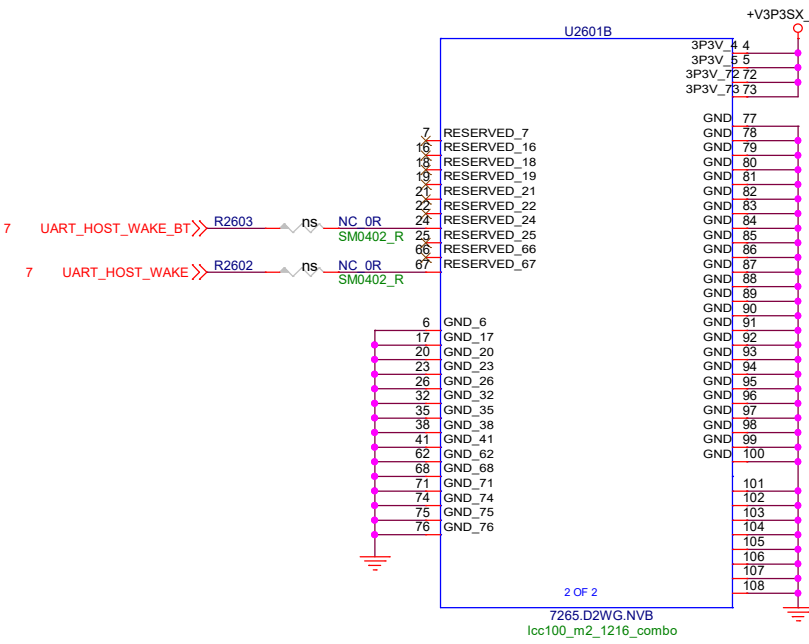
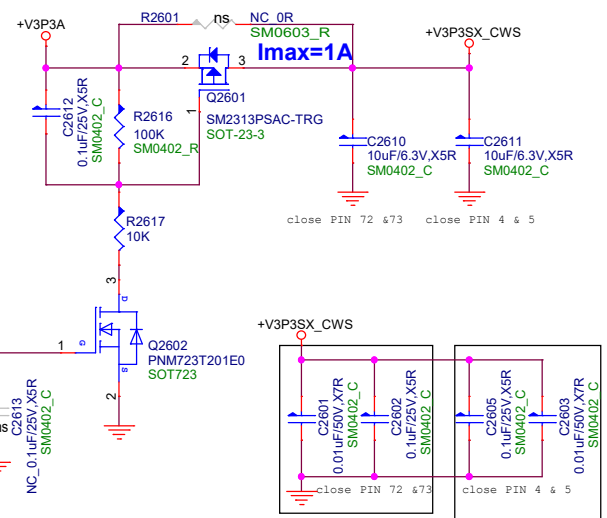
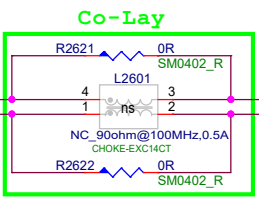
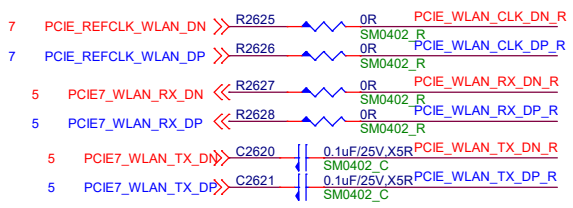
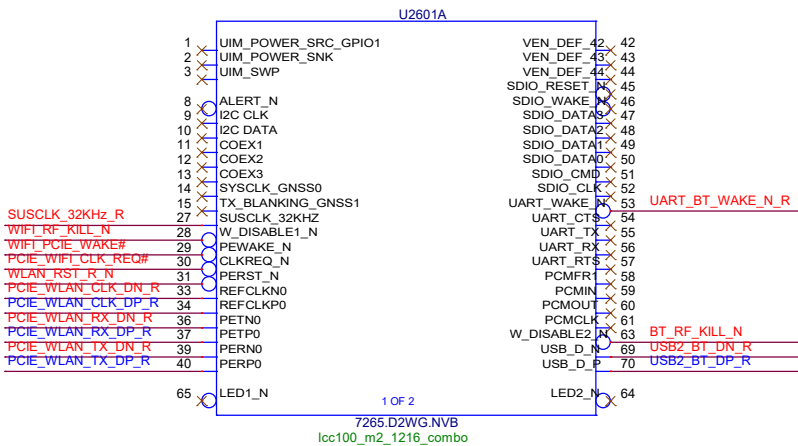
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Project Name	N156EBL01		
Document Number	Page Name	TPAD/FP/FAN	Size
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Madigi			
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Docp	USB3.0 CONN		B
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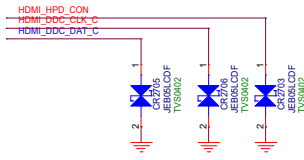
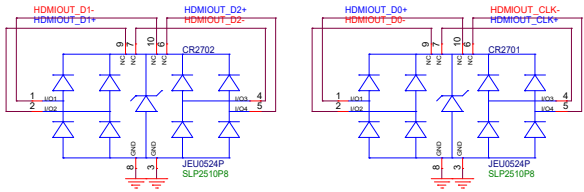
FA7615AA6R(Active High,Auto Discharge 100R)
FA7615CA6R(Active High,no discharge)
I_{max}=3A



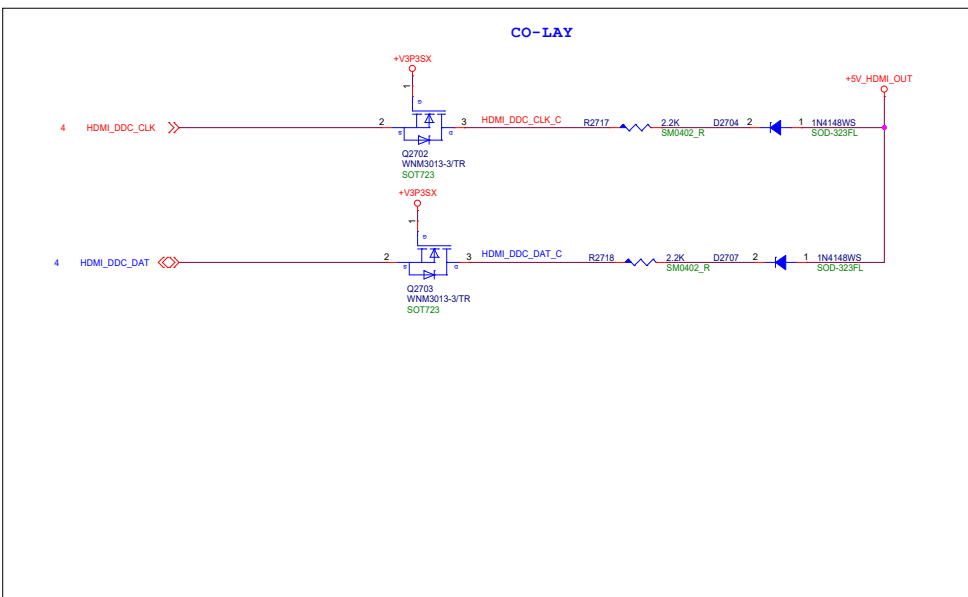
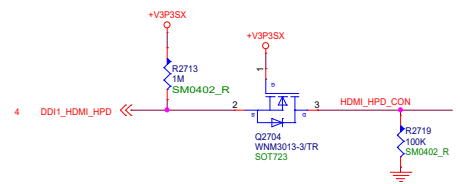
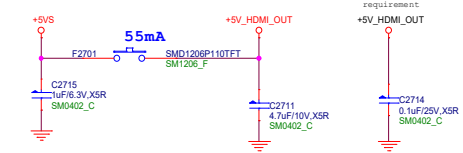
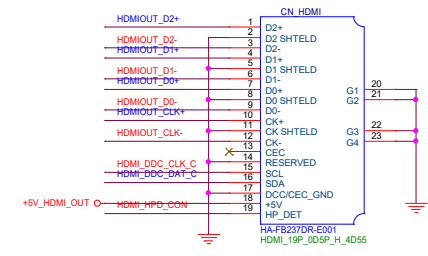
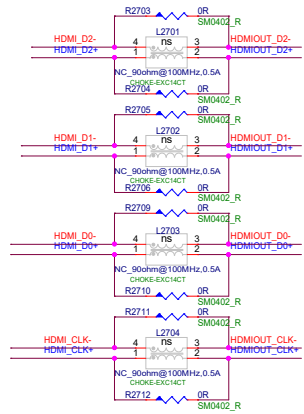
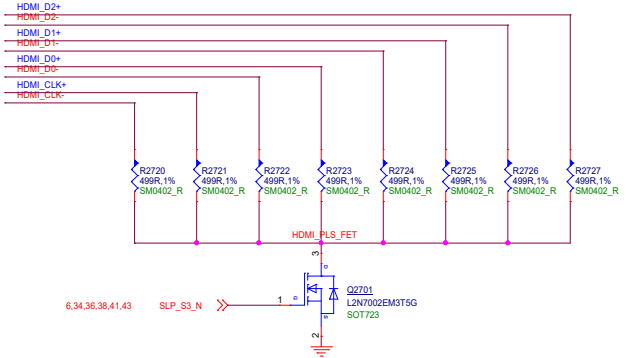


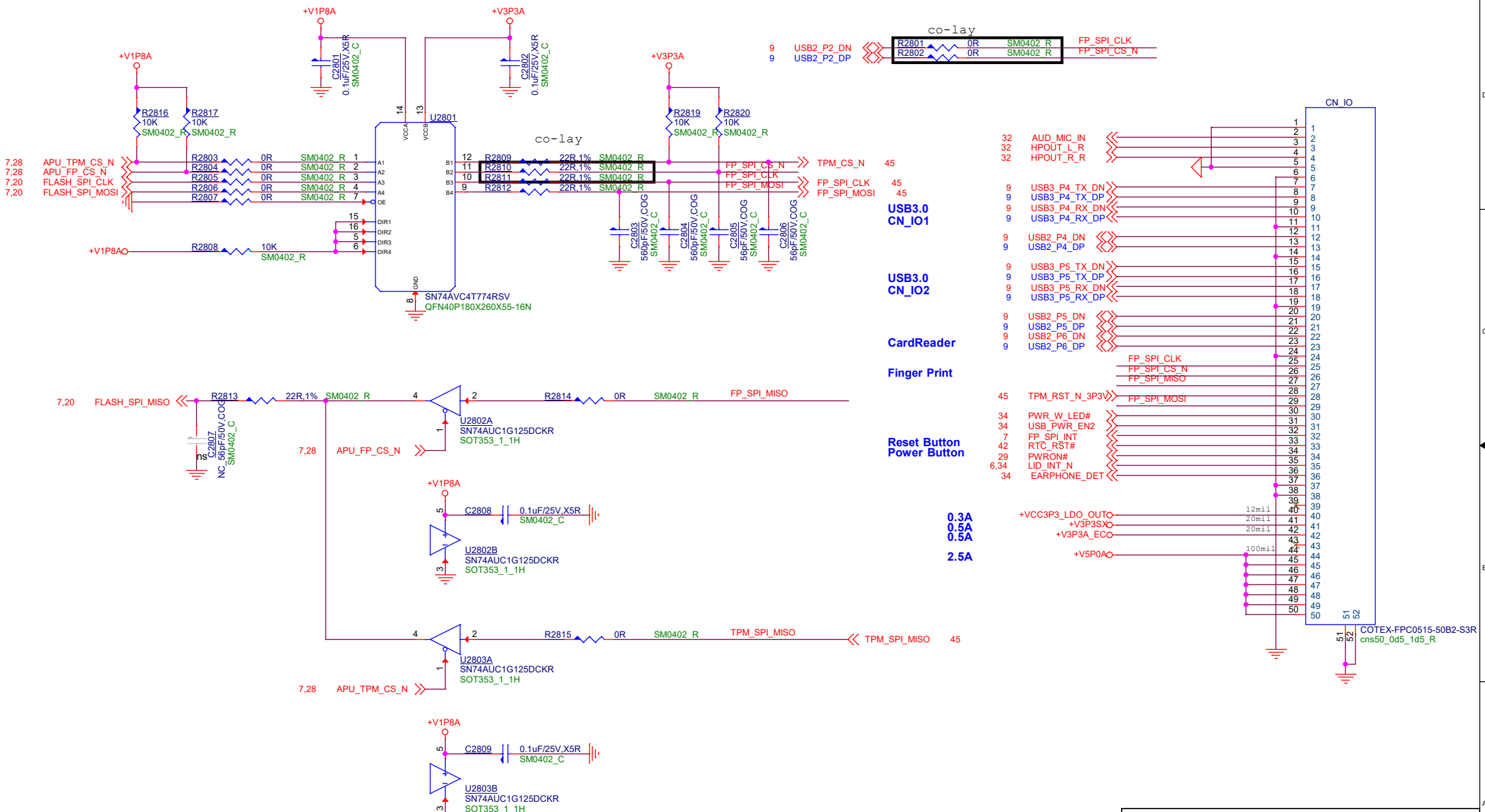
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HDMI



4	DDI1_LANE3_HDMI_DP	>>	C2708	0.1uF/25V X5R	HDMI_CLK+
4	DDI1_LANE3_HDMI_DN	>>	C2707	0.1uF/25V X5R	HDMI_CLK-
4	DDI1_LANE2_HDMI_DP	>>	C2706	SM0402_C	HDMI_D0+
4	DDI1_LANE2_HDMI_DN	>>	C2705	0.1uF/25V X5R	HDMI_D0-
4	DDI1_LANE1_HDMI_DP	>>	C2704	SM0402_C	HDMI_D1+
4	DDI1_LANE1_HDMI_DN	>>	C2703	0.1uF/25V X5R	HDMI_D1-
4	DDI1_LANE0_HDMI_DP	>>	C2702	SM0402_C	HDMI_D2+
4	DDI1_LANE0_HDMI_DN	>>	C2701	0.1uF/25V X5R	HDMI_D2-



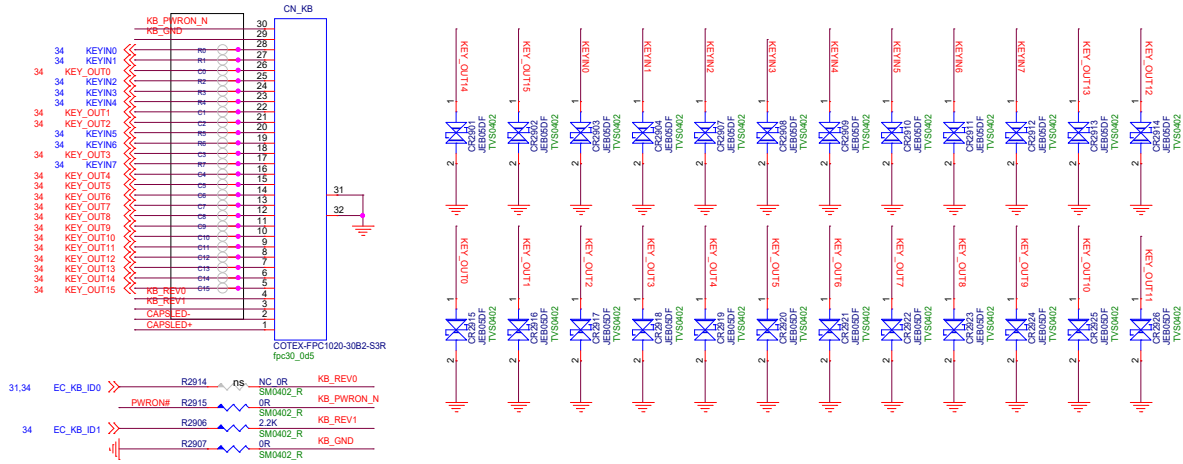


Pin	Function	Pin	Function
1		1	
2		2	
3	AUD_MIC_IN	3	
4	HPOUT_L_R	4	
5	HPOUT_R_R	5	
6		6	
7		7	
8		8	
9	USB3_P4_TX_DN	9	
9	USB3_P4_TX_DP	9	
9	USB3_P4_RX_DN	9	
9	USB3_P4_RX_DP	9	
9	USB2_P4_DN	9	
9	USB2_P4_DP	9	
9	USB3_P5_TX_DN	9	
9	USB3_P5_TX_DP	9	
9	USB3_P5_RX_DN	9	
9	USB3_P5_RX_DP	9	
9	USB2_P5_DN	9	
9	USB2_P5_DP	9	
9	USB2_P6_DN	9	
9	USB2_P6_DP	9	
24		24	
25	FP_SPI_CLK	25	
26	FP_SPI_CS_N	26	
27	FP_SPI_MISO	27	
28		28	
29	TPM_RST_N_3P3	29	
30		30	
31	PWR_W_LED#	31	
32	USB_PWR_EN2	32	
33	FP_SPI_INT	33	
34	RTC_RST#	34	
35	PWRON#	35	
36	LID_INT_N	36	
37	EARPHONE_DET	37	
38		38	
39		39	
40	+VCC3P3_LDO_OUTO	40	
41	+V3P3SXO	41	
42	+V3P3A_ECO	42	
43		43	
44	+V5P0AO	44	
45		45	
46		46	
47		47	
48		48	
49		49	
50		50	
51		51	
52		52	

Madigi	
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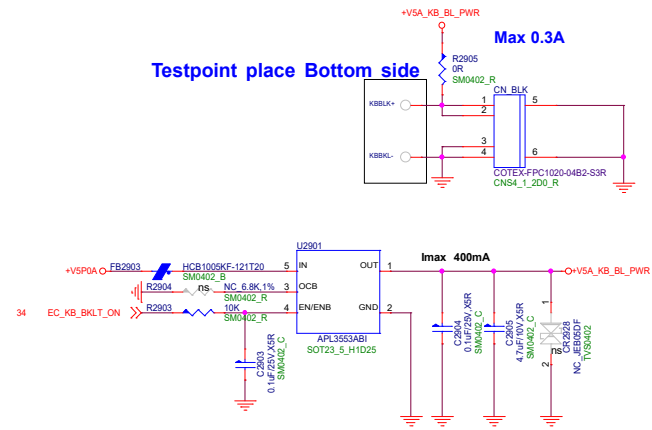
KEYBOARD CONN

Testpoint place Bottom side

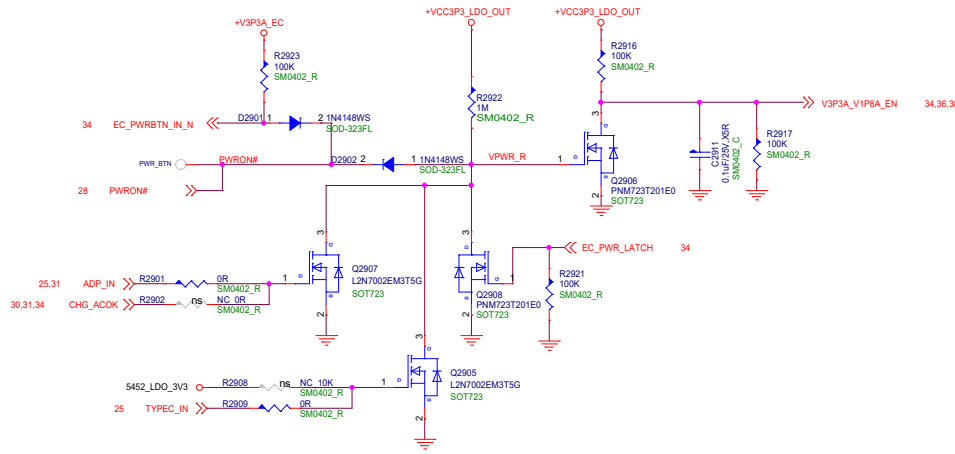


Keyboard Backlight

Testpoint place Bottom side

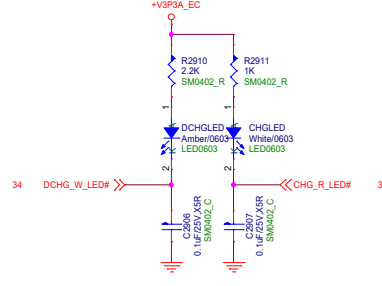


PWR SW

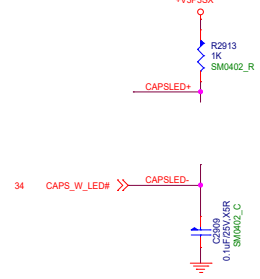


POWER LED

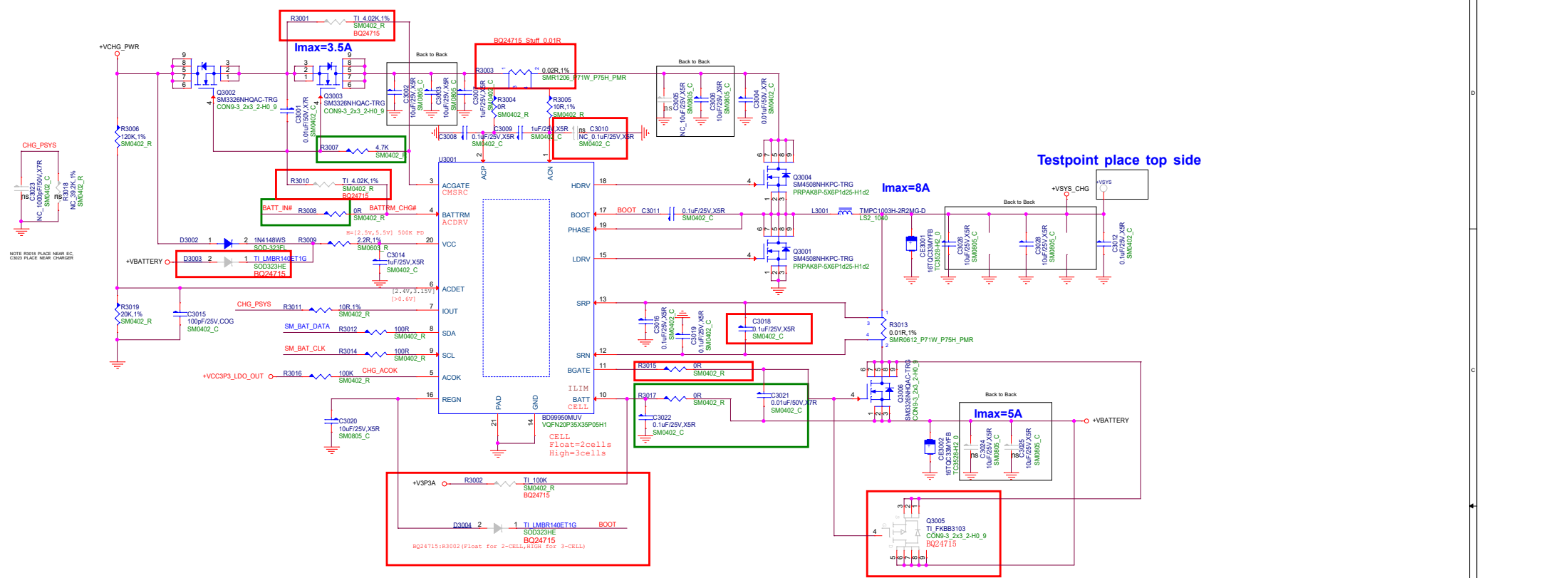
CHARGE LED



CAPS LED



BATTERY CHARGER



Register Address	Func	Value	Descrip
0x12	Charge Option	0xF302	DEFAULT
0x14	Charge Current	0x0640	1600mA
0x15	Charge Voltage	0x3300 0x2200	1305mV 8708mV
0x3E	Min Sys Voltage	0x2340 0x17C0	9024mV 6080mV
0x3F	Input Current	0x0800	2048mA

RED - 3Cell
BLUE - 2Cell

Chip Address	BD99950
Chip Address + R	0x13
Chip Address + W	0x12

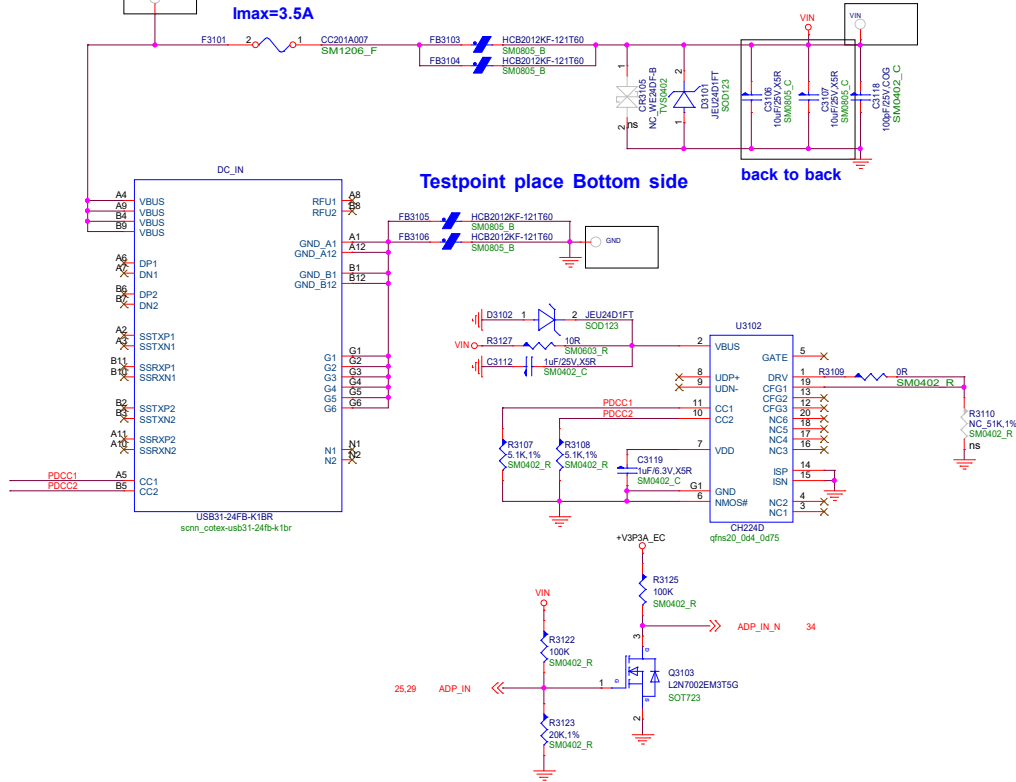
Net Interface
34 CHG_PSYS <<< CHG_PSYS
31,34 SM_BAT_DATA <<> SM_BAT_DATA
31,34 SM_BAT_CLK <<> SM_BAT_CLK
31,34 CHG_ACOK <<< CHG_ACOK
31,34 BATT_IN# <<> BATT_IN#

DC

Testpoint place Bottom side

Adapter:19V/3.42A, 65W

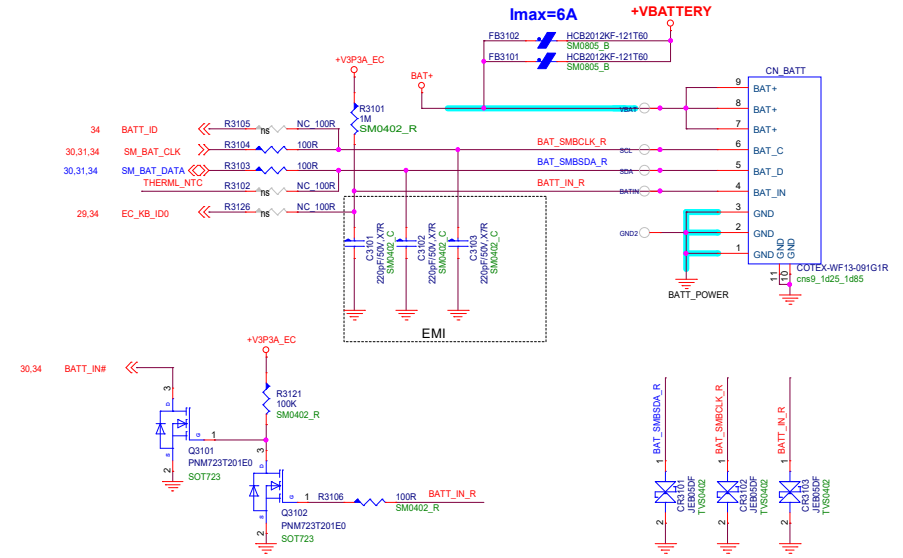
Testpoint place top side



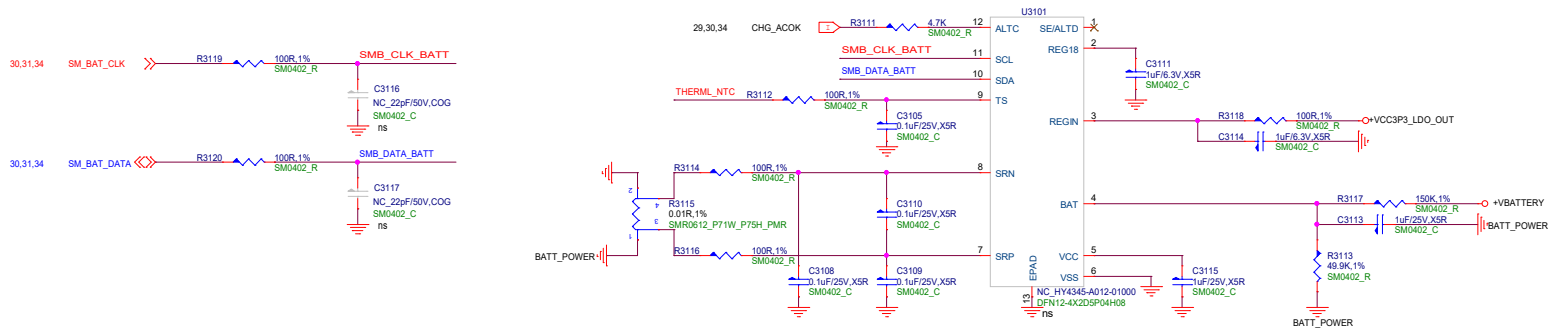
BATTERY

Note:
Smart Battery: Stuff R3103, R3104; Unstuff U3101, R3119, R3120
Dummy Battery: Stuff U3101, R3119, R3120, R3102; Unstuff R3103, R3104

Battery: 3Cell (11.55V 6A)

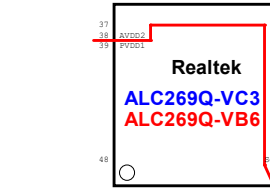
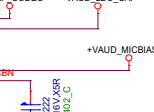
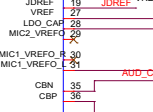
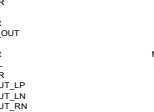
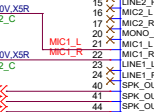
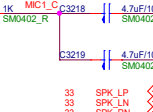
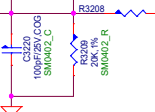
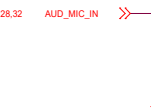
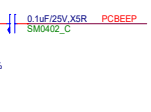
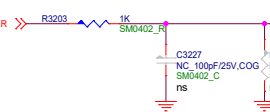
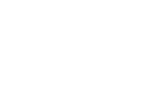
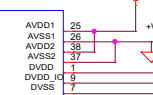
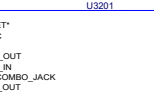
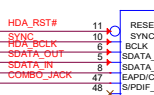
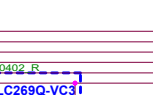
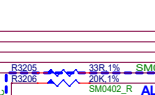
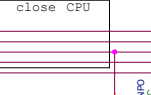
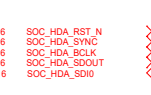
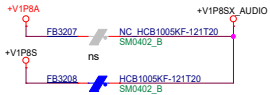
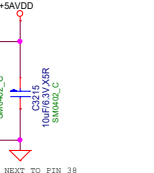
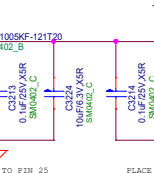
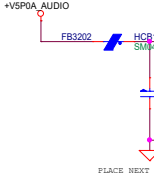
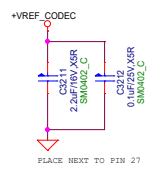
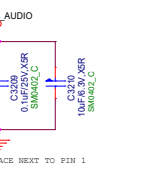
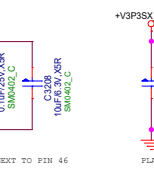
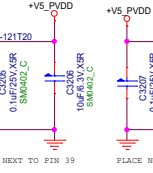
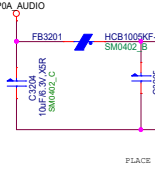
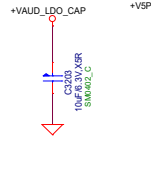
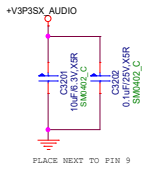
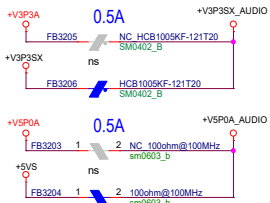
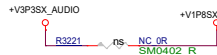


Fuel Gauge

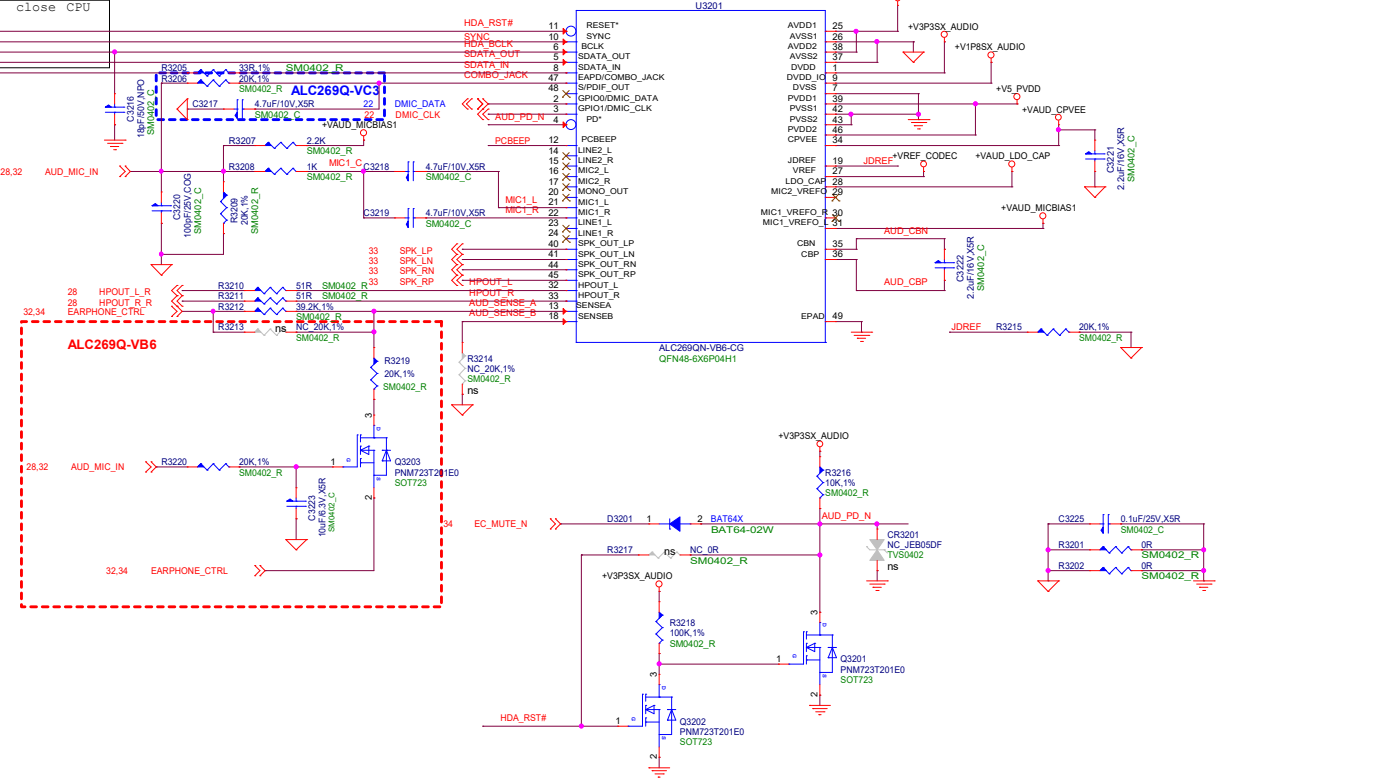


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CODEC

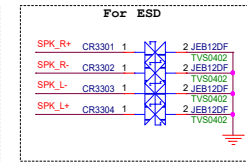
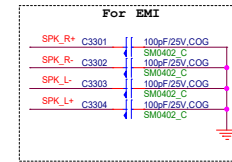
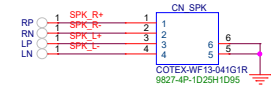
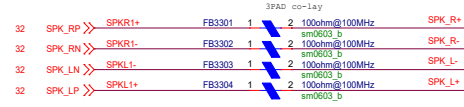


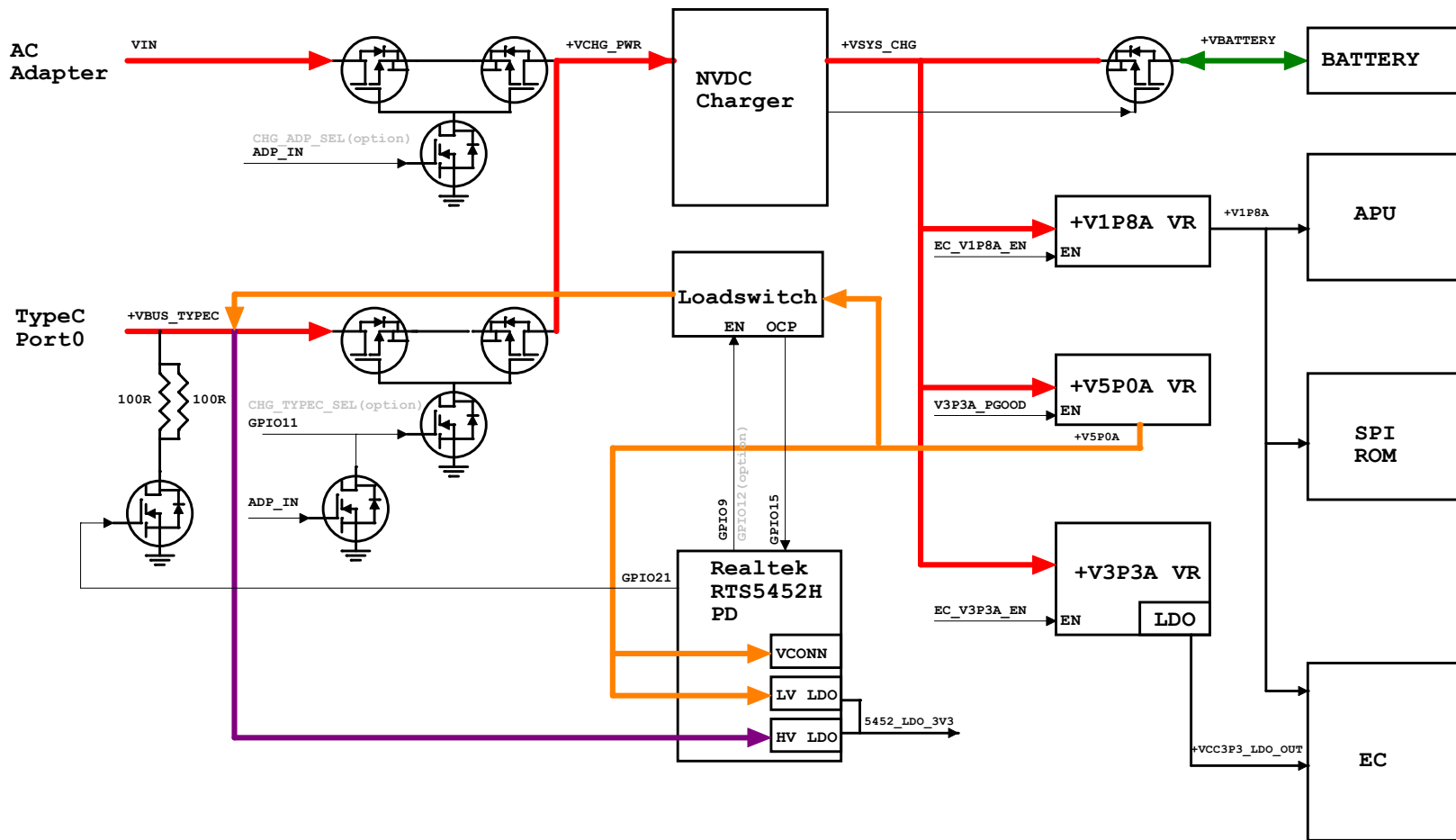
DIGITAL ANALOG
Moat

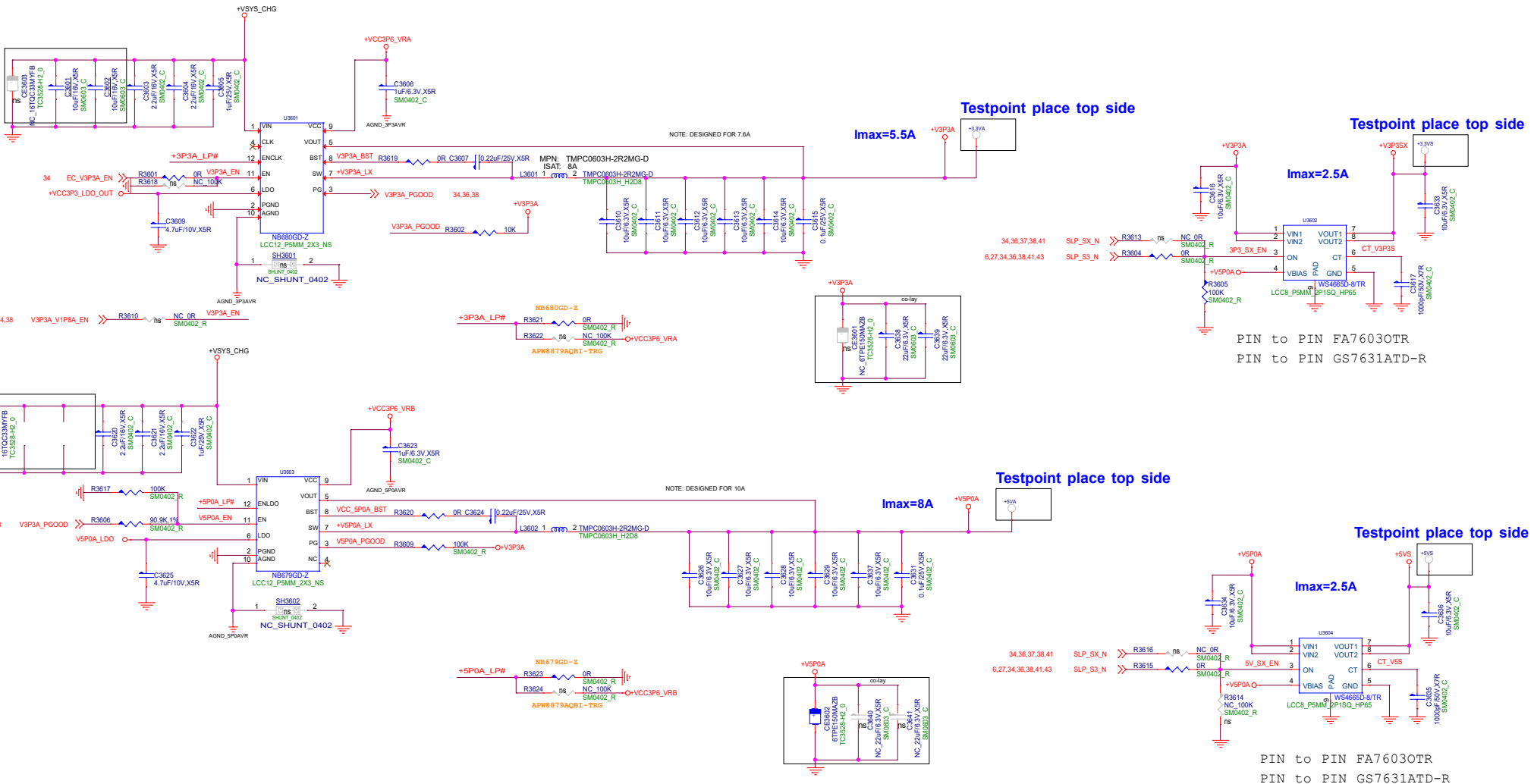


INT_SPEAKER

SPEAK: 2 W 4 Ω



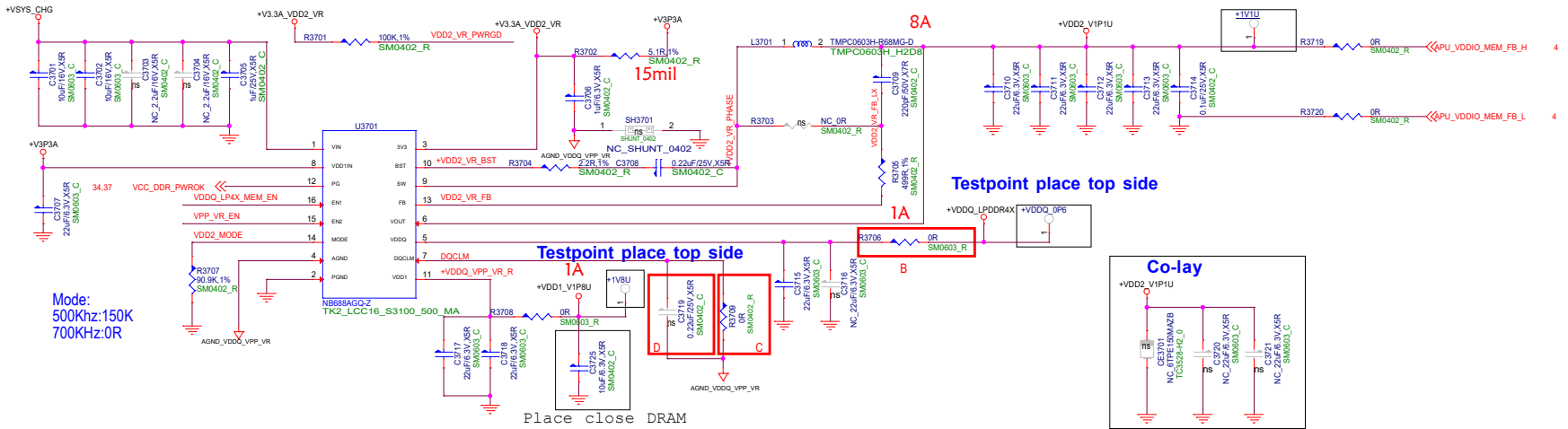




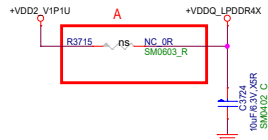
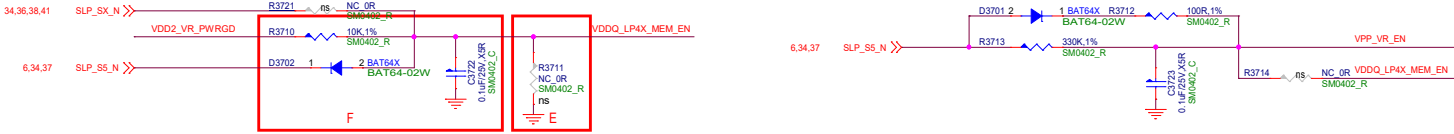
PIN to PIN FA7603OTR
PIN to PIN GS7631ATD-R

PIN to PIN FA7603OTR
PIN to PIN GS7631ATD-R

DESIGN NOTE:
PLACE C29
CLOSE TO FN 8



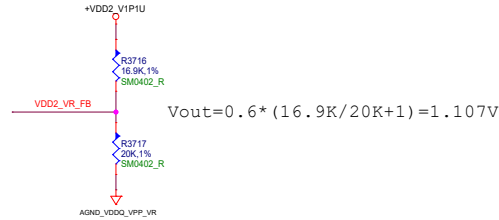
Mode:
500Khz:150K
700Khz:0R



Note:
LPDDR4:Stuff R3715,Unstuff R3706
LPDDR4X:Stuff R3706,Unstuff R3715

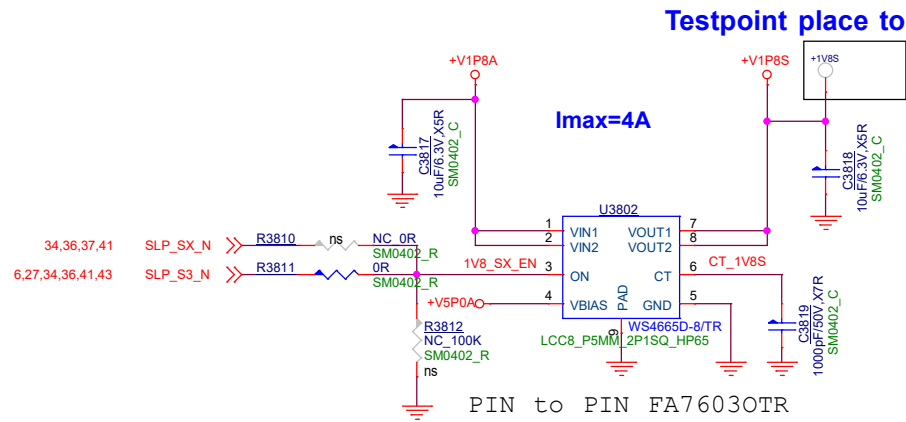
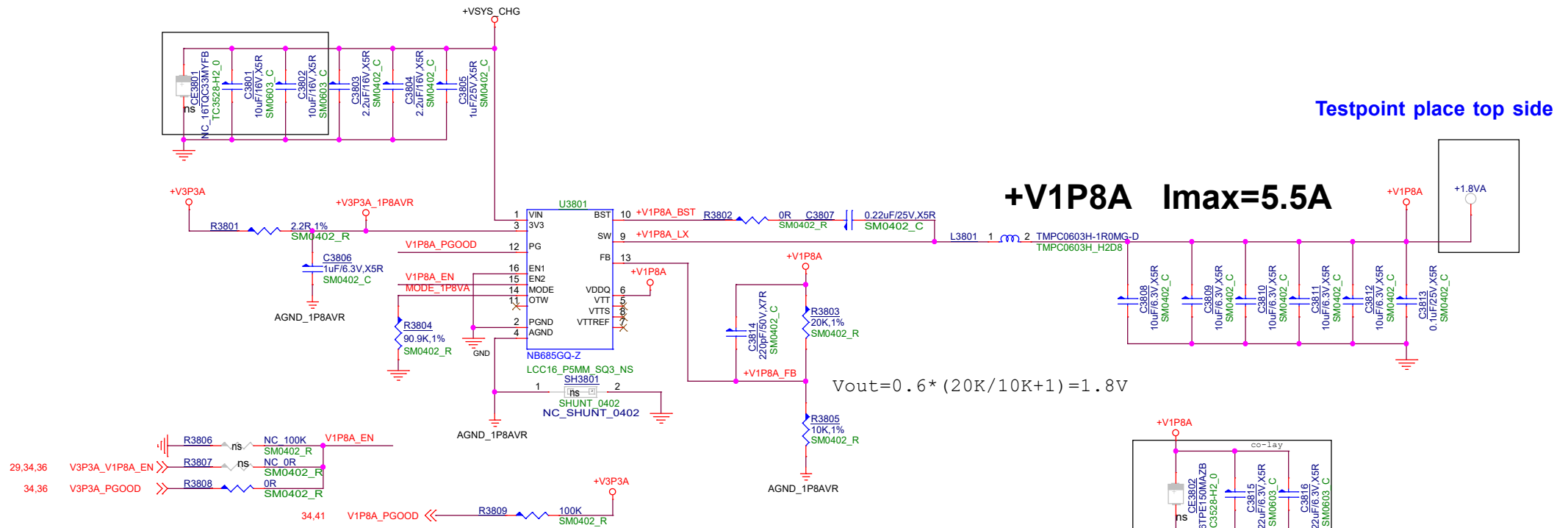
DESIGN NOTE:

PARAMETER	SETTING
OUTPUT VOLTAGE	1.1V
LOAD CURRENT	9A
OCP	11.25A
FREQUENCY	700 KHZ
SOFT START	2.8 MLLI SEC



DESIGN NOTE:

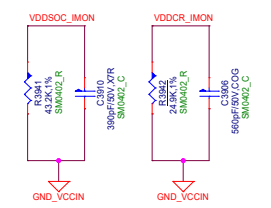
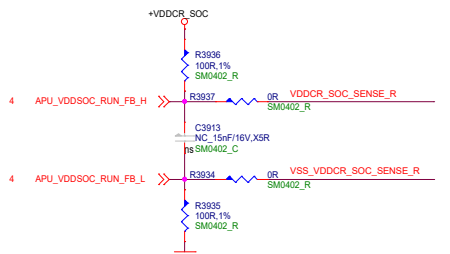
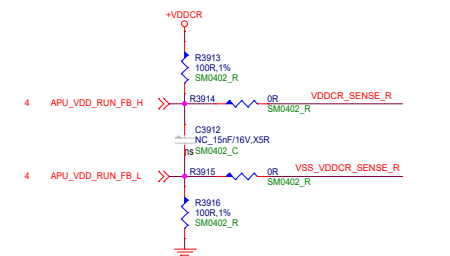
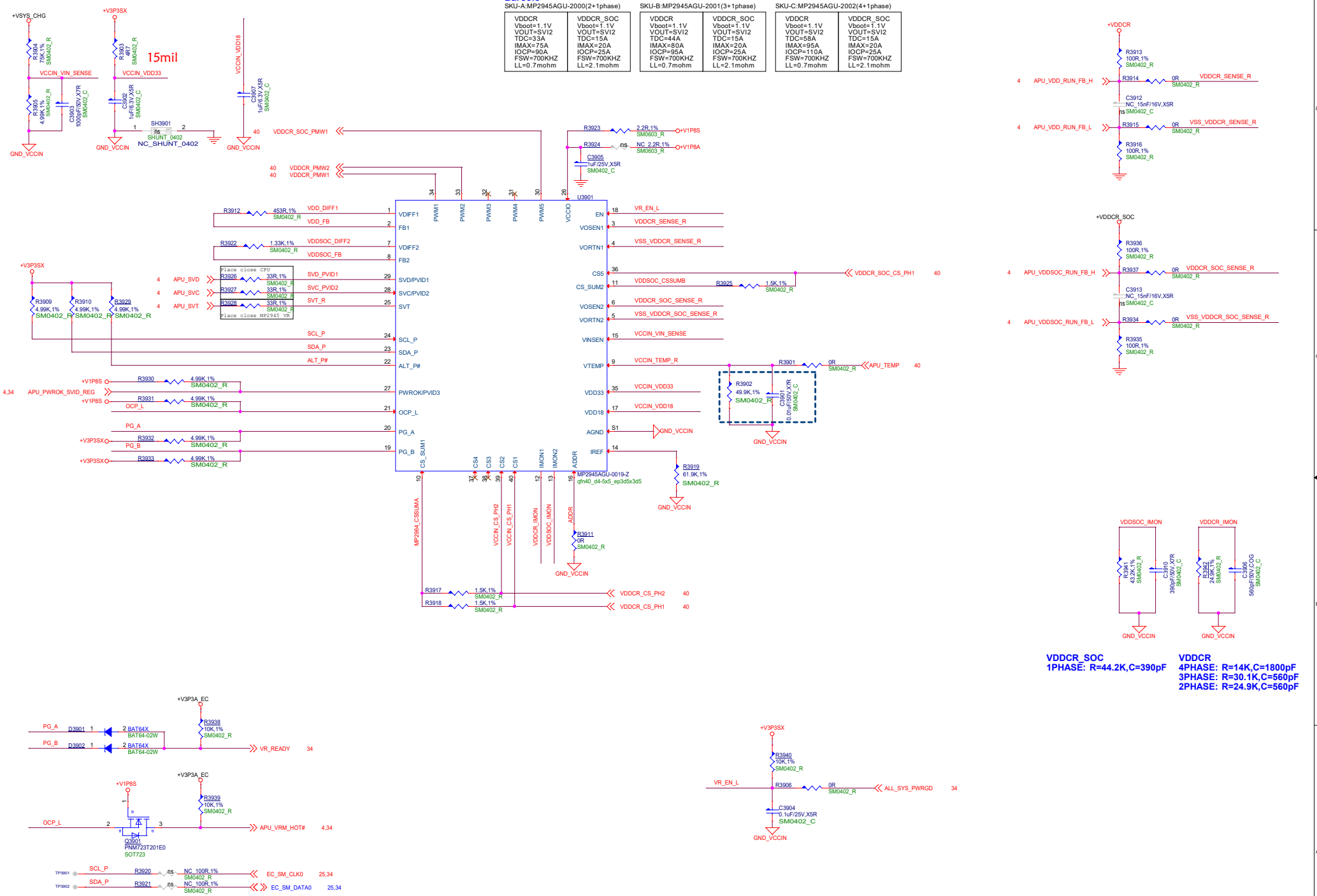
LPDDR4X	LPDDR4
A TO BE EMPTY	A TO BE STUFF R2416
B TO BE STUFF	B TO BE EMPTY
C TO BE STUFF	C TO BE EMPTY
D TO BE EMPTY	D TO BE STUFF
E TO BE EMPTY	E TO BE STUFF
U401-NB688A	U4001-NB688
F TO BE STUFF	F TO BE EMPTY



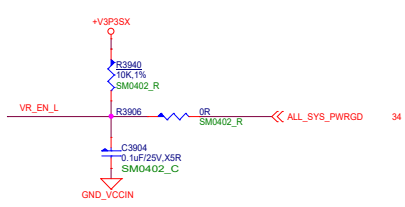
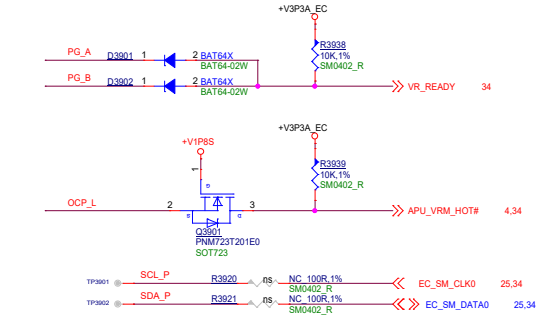
Madigi			
Design Title		Barcelo	
Project Name		N156EBL01	
Document Number	Page Name	POWER 1.8VA/S	Size B
Design Date	Monday, April 17, 2023	Author	Java
Page Date	Tuesday, February 21, 2023	Sheet	38 of 48
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Barcelo

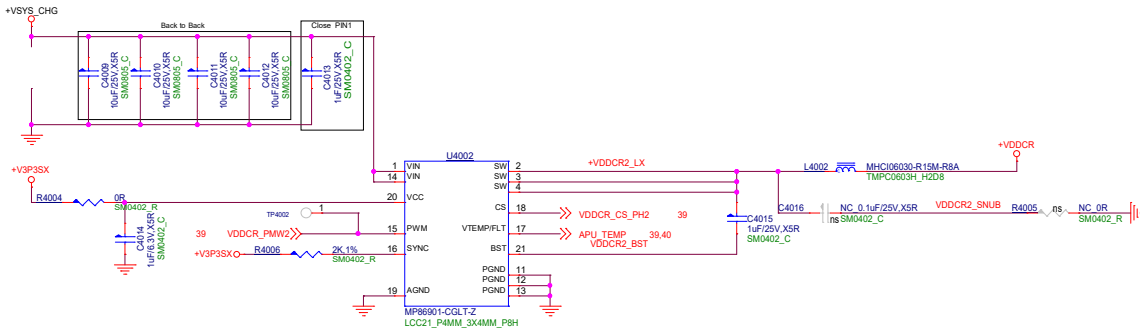
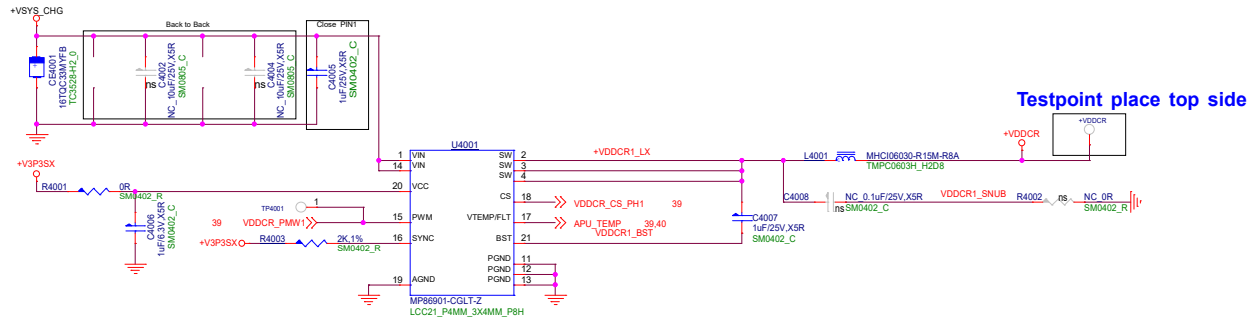
SKU-A:MP2945AGU-2000(2+1phase)	SKU-B:MP2945AGU-2001(3+1phase)	SKU-C:MP2945AGU-2002(4+1phase)
VDDCR Vboot=1.1V VOUT=SVI2 TDC=33A IMAx=75A IOCP=25A FSW=700KHZ LL=0.7mohm	VDDCR_SOC Vboot=1.1V VOUT=SVI2 TDC=15A IMAx=20A IOCP=25A FSW=700KHZ LL=2.1mohm	VDDCR Vboot=1.1V VOUT=SVI2 TDC=44A IMAx=80A IOCP=95A FSW=700KHZ LL=0.7mohm
	VDDCR_SOC Vboot=1.1V VOUT=SVI2 TDC=15A IMAx=20A IOCP=25A FSW=700KHZ LL=2.1mohm	VDDCR Vboot=1.1V VOUT=SVI2 TDC=58A IMAx=95A IOCP=25A FSW=700KHZ LL=0.7mohm
		VDDCR_SOC Vboot=1.1V VOUT=SVI2 TDC=15A IMAx=20A IOCP=25A FSW=700KHZ LL=2.1mohm



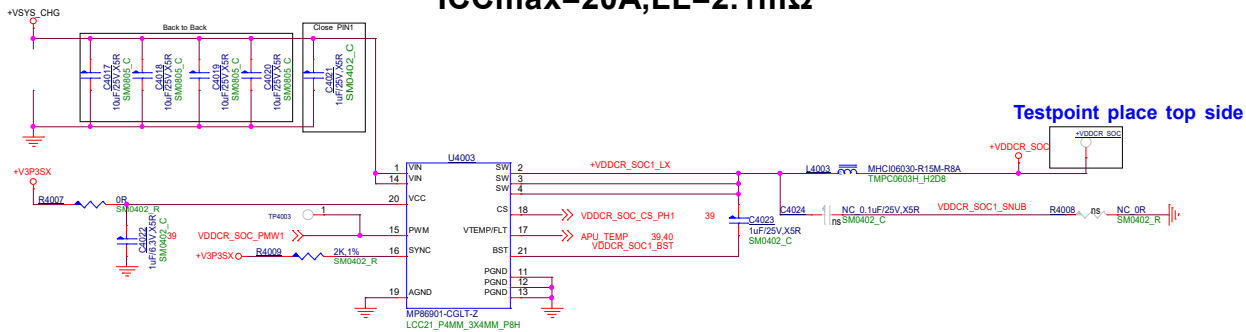
VDDCR_SOC
1PHASE: R=44.2K,C=390pF
VDDCR
4PHASE: R=14K,C=1800pF
3PHASE: R=30.1K,C=560pF
2PHASE: R=24.9K,C=560pF

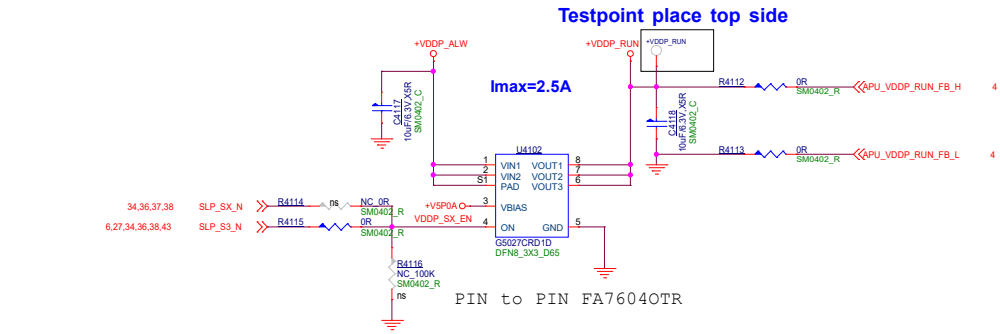
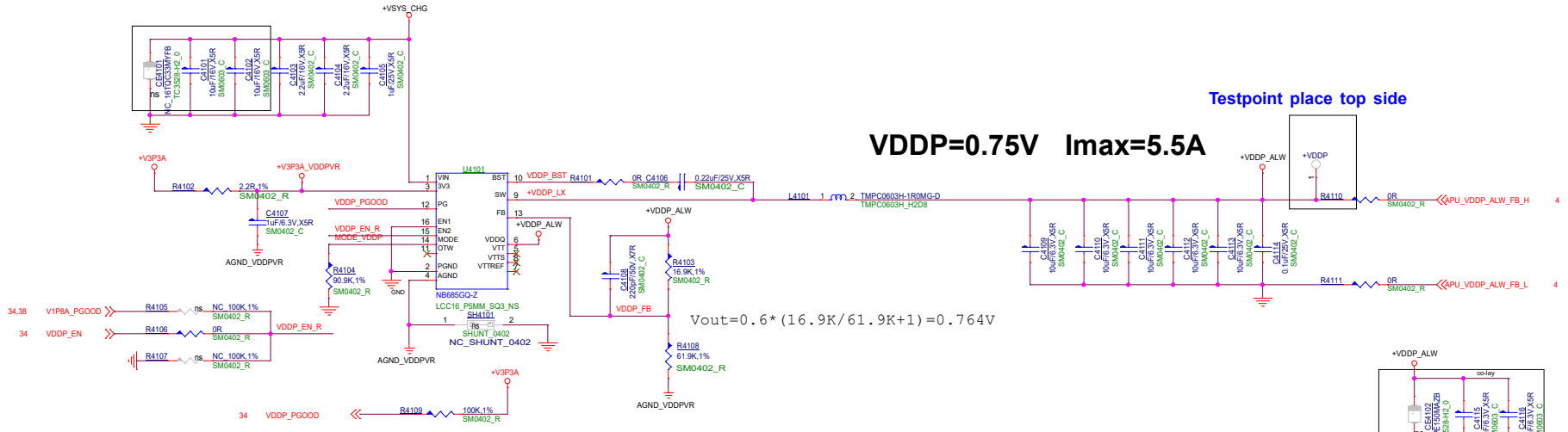


**+VDDCR(Itdc=44A)
ICCmax=65A,LL=0.7mΩ**

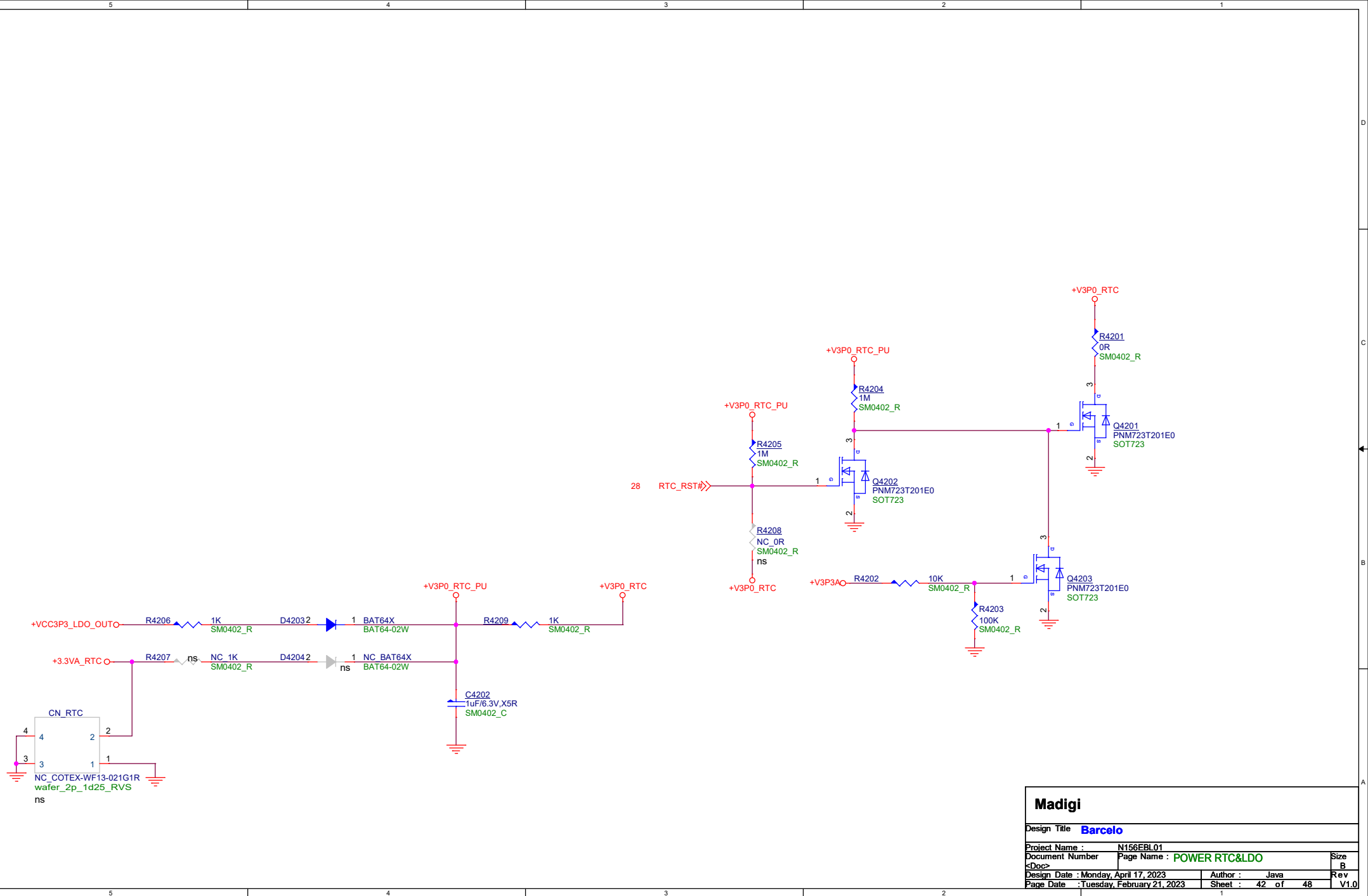


**+VDDCR_SOC(Itdc=15A)
ICCmax=20A,LL=2.1mΩ**



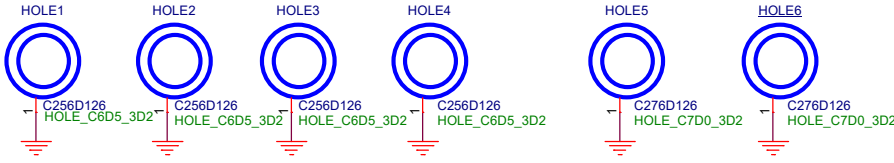


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Project Name	N156EBL01		
Document Number	Page Name	POWER VDDP/S	Size
Doc#			C
Design Date	Monday, April 17, 2023	Author	Java
Page Date	Tuesday, February 21, 2023	Sheet	41 of 48
		Rev	V1.0

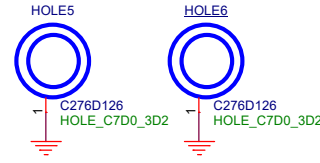


Madigi			
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Project Name : N156EBL01		Size B	
Document Number	Page Name : POWER RTC&LDO	Rev	
Docp	Design Date : Monday, April 17, 2023	Author : Java	Rev
Design Date	Page Date : Tuesday, February 21, 2023	Sheet : 42 of 48	V1.0

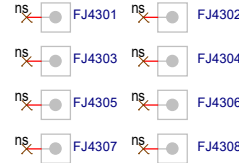
CPU & GPU HEATSINK



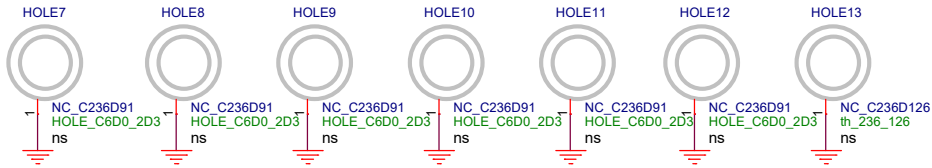
SSD1 SSD2



Mark Point EMI CAP



SCREW HOLE



DRAM shielding



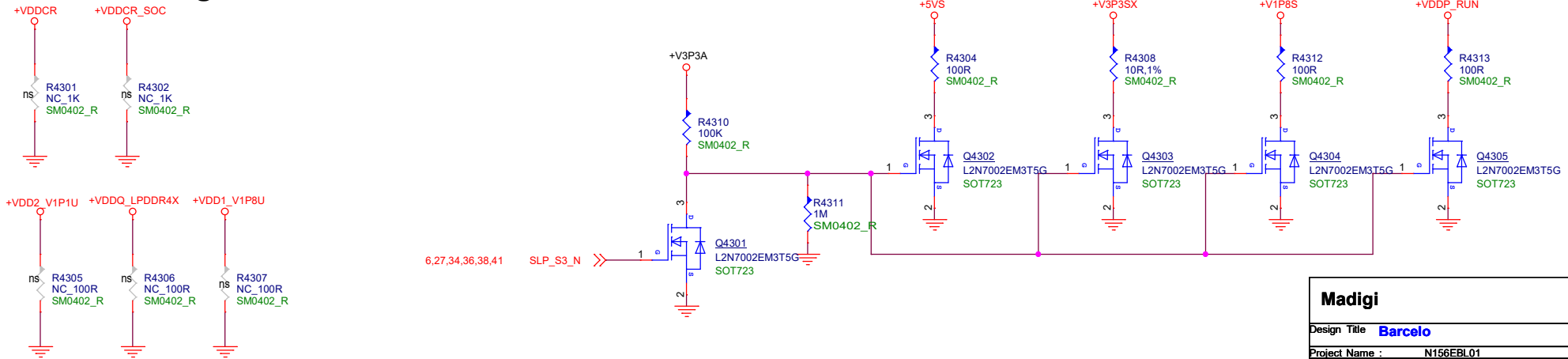
PCB
N156EBC01_MB_V11

S/N :
SN NC_Seril Number
ns



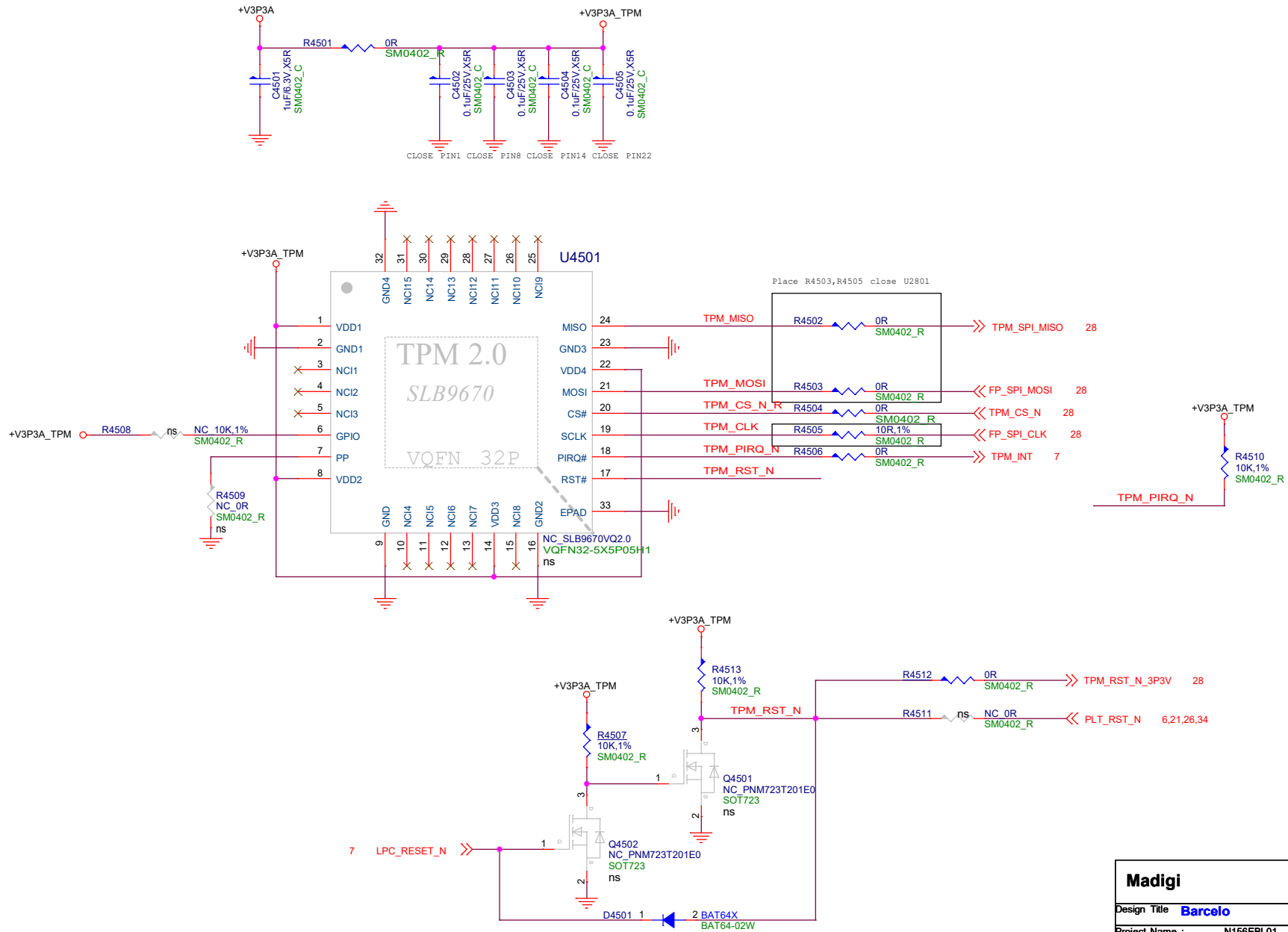
RTC_BATT
NC_CR2030 3.3V
ns

Discharge Resistor

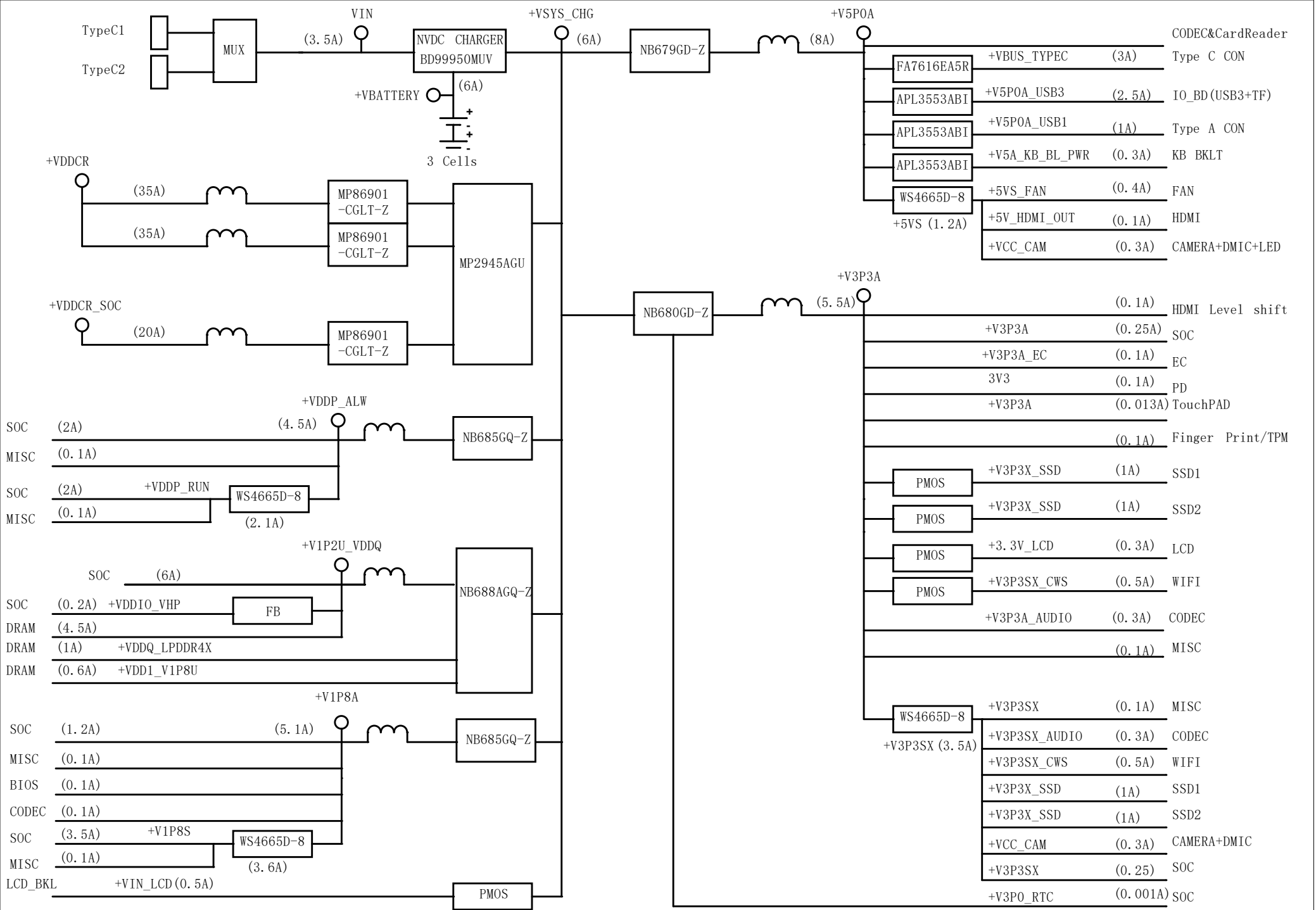


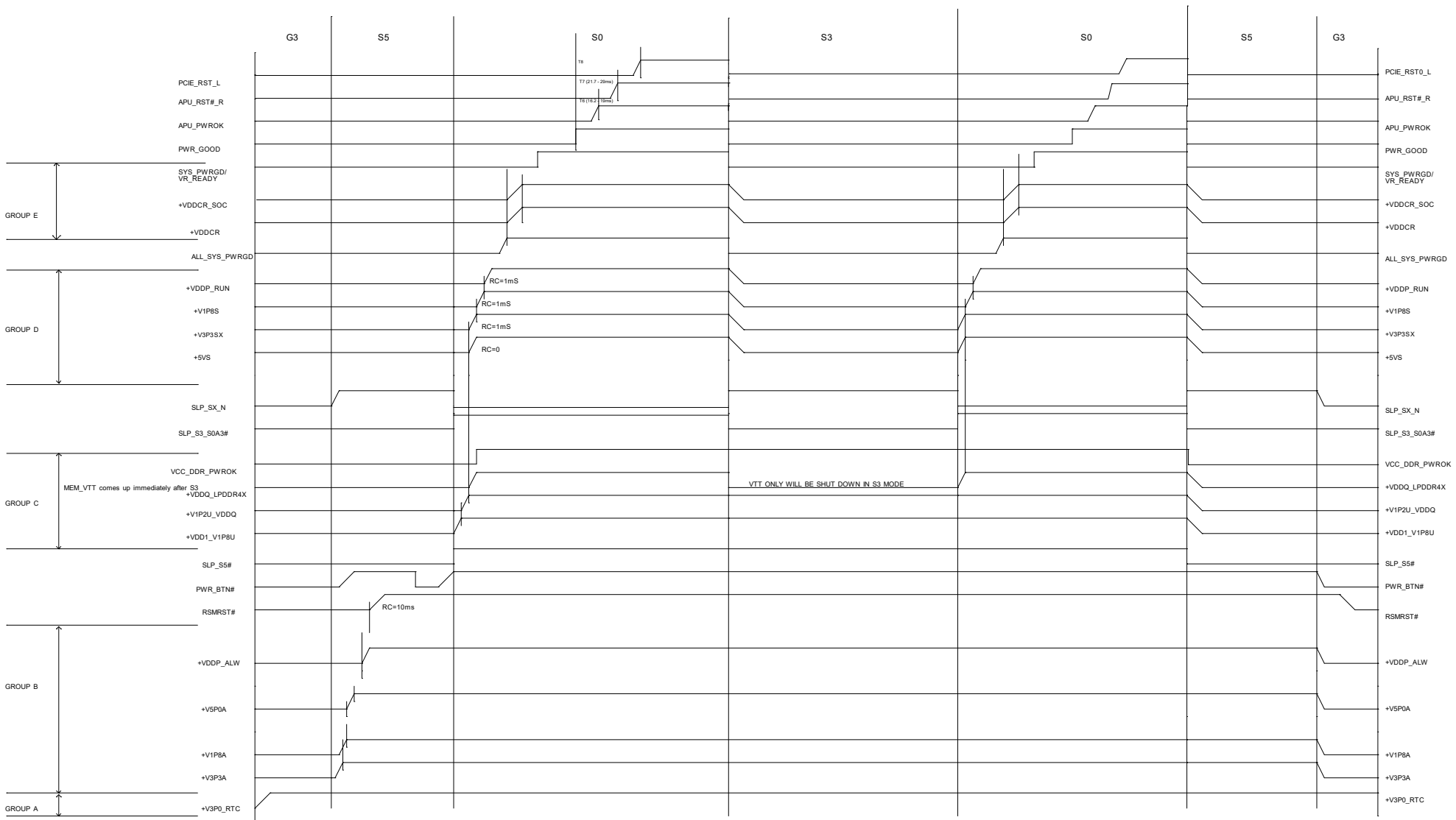
Madigi		
Design Title	Barcelo	
Project Name	N156EBL01	
Document Number	Page Name	Size
eDoc	Discharge/HOLE	B
Design Date	Author	Rev
Tuesday, April 17, 2023	Java	
Page Date	Sheet	
Tuesday, February 28, 2023	43 of 48	V1.0

Madigi			
Design Title	Barcelo		
Project Name	NT56E9101		
Document Number	Page Name	BLANK	Size
<Doc>			L
Design Date	Monday, April 17, 2023	Author	Jims
Page Date	Tuesday, February 21, 2023	Sheet	44 of 48
			Rev V1.0



Madigi	
Design Title	Barcelo
Project Name	N156EBL01
Document Number	Page Name : TPM
Docp	Size B
Design Date : Monday, April 17, 2023	Author : Java
Page Date : Tuesday, February 21, 2023	Sheet : 45 of 48
	Rev V1.0



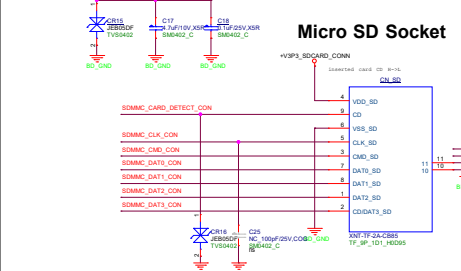
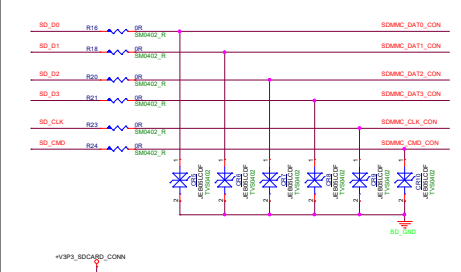
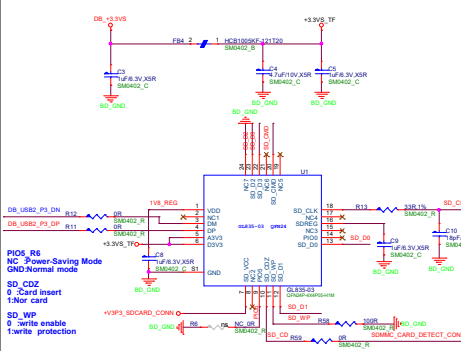


Power on Sequence required:

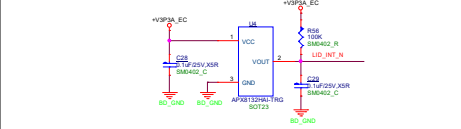
1. There is no sequencing requirement between power supplies within the individual power groups.
2. All power supplies in Group A must be stable and within specifications for 5 seconds before any power supply in Power sequencing Group B is greater than 10% of its specified minimum operating voltage.
3. All power supplies in Group B must be stable and within specifications before any power supply in Power sequencing Group C is greater than 10% of its specified minimum operating voltage.
4. All power supplies in Group C must be stable and within specifications before any power supply in Power sequencing Group D is greater than 10% of its specified minimum operating voltage.

Madigi				
Design Title	Barcelo			
Project Name	NT569101			
Document Number	Page Name	Power Sequence	Size	C
Design Date	Monday, April 17, 2023	Author	Jims	Rev
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SD CardReader



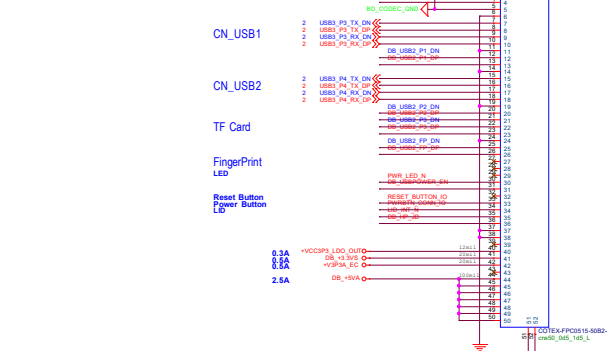
LID Sensor



FAN2



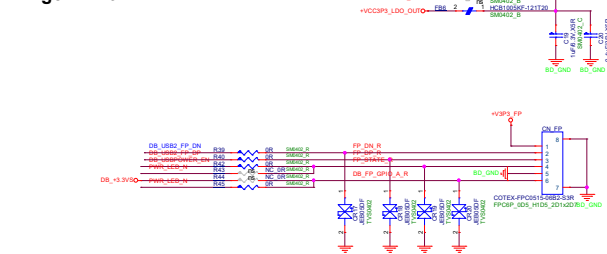
IO CONNECTOR



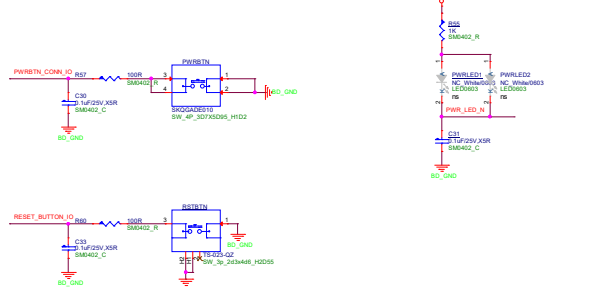
Screw Hole



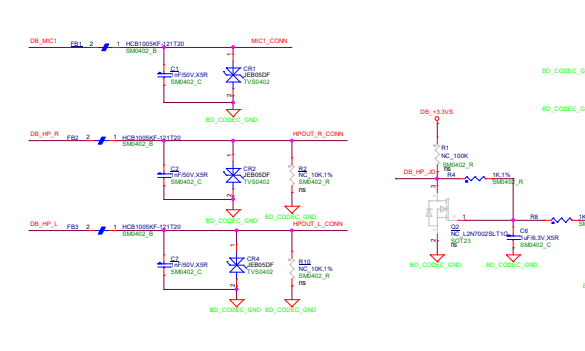
FingerPrint



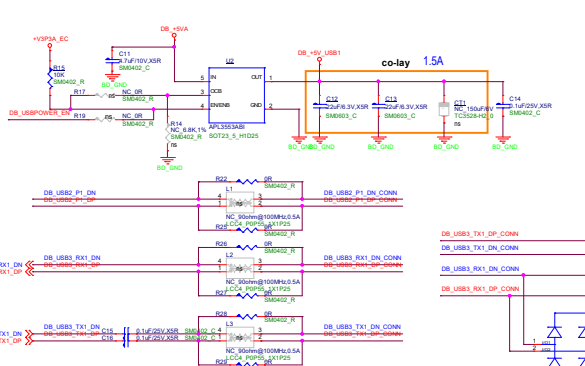
Button & LED



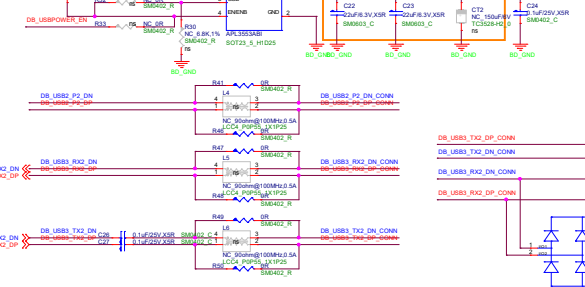
Headset



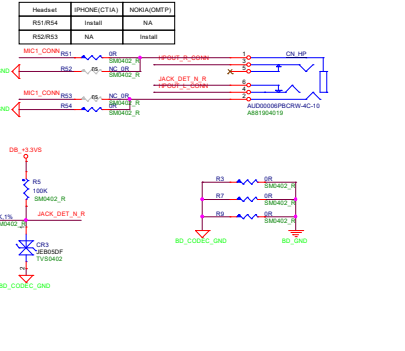
USB3 TypeA



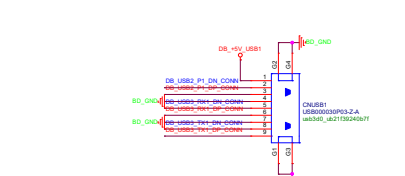
USB3 TypeA



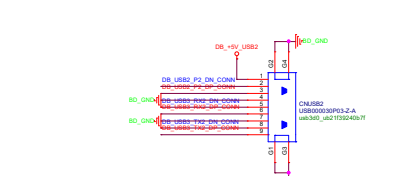
Audio Jack

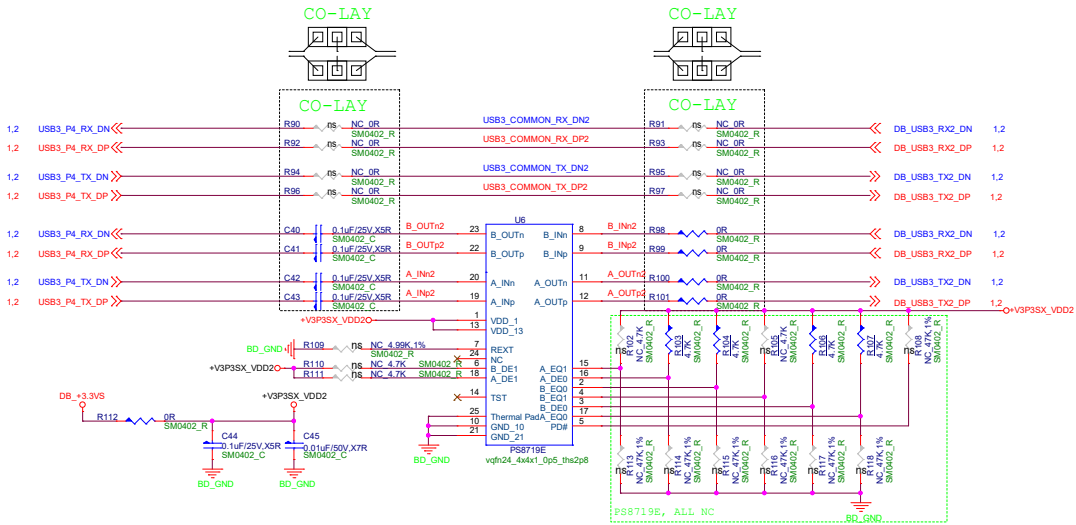
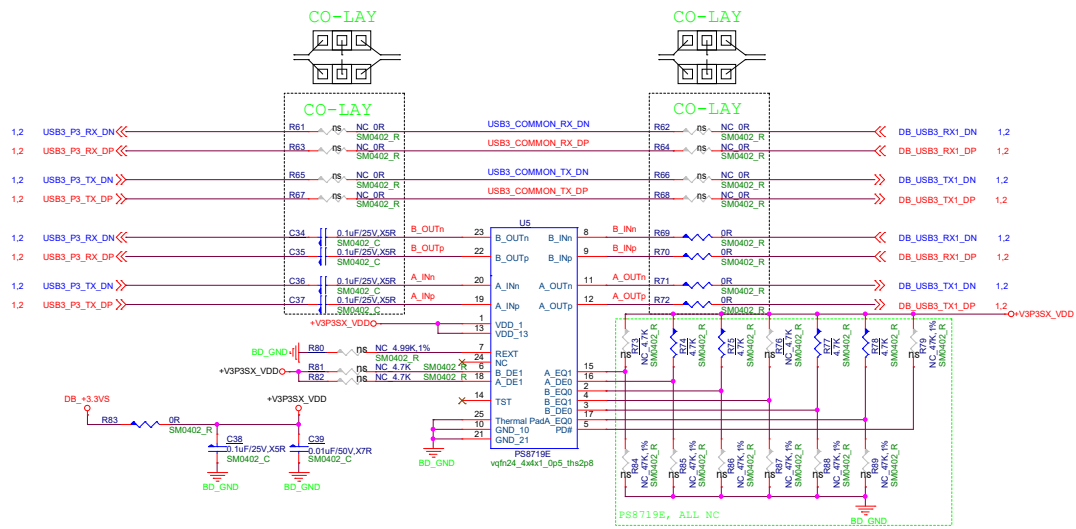


USB3 Jack



USB3 Jack





RX Receiver

TX Driver

Equalizer control and program for Channel A
 3.3V tolerant.Integrated pulleddown 150K resistors.
 [A_EQ1,A_EQ0]==[PIN15,PIN17]
 LL = program EQ for channel loss up to 9.5dB(default)
 LH = program EQ for channel loss up to 13dB
 HL = program EQ for channel loss up to 4.5dB
 HH = program EQ for channel loss up to 7.5dB

Programmable output de-emphasis level setting for Channel A
 3.3V tolerant.Integrated pulleddown 150K resistors.
 [A_DE1,A_DE0]==[PIN18,PIN16]
 LL = 3.5dB de-emphasis(default)
 LH = 0dB de-emphasis
 HL = 2.7dB de-emphasis
 HH = 5dB de-emphasis

Equalizer control and program for Channel B
 3.3V tolerant.Integrated pulleddown 150K resistors.
 [B_EQ1,B_EQ0]==[PIN4,PIN2]
 LL = program EQ for channel loss up to 9.5dB(default)
 LH = program EQ for channel loss up to 13dB
 HL = program EQ for channel loss up to 4.5dB
 HH = program EQ for channel loss up to 7.5dB

Programmable output de-emphasis level setting for Channel B
 3.3V tolerant.Integrated pulleddown 150K resistors.
 [B_DE1,B_DE0]==[PIN6,PIN3]
 LL = 3.5dB de-emphasis(default)
 LH = 0dB de-emphasis
 HL = 2.7dB de-emphasis
 HH = 5dB de-emphasis