QCA4004 Low-Energy Wi-Fi Dual-Band 802.11a/b/g/n SoC

Data Sheet

80-Y5035-2 Rev. F

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Revision history

Revision	Date	Description
A	May 2013	Initial release
B	July 2013	■ Table 3-3: Updated DC Electrical Characteristics for Digital I/Os
C	October 2013	■ Table 3-2 :Updated Recommended Operating Conditions. ■ Tables 3-9 through 3-15: Updated Radio Rx and Tx Characteristics. ■ Table 3-16: Updated Typical Current Consumption: Low Power States at 3.3 V Operation. ■ Section 4.4: Added Power Up Sequence.
D	January 2014	■ Section 2.3: Updated GPIO. ■ Chapter 7: Added industrial temperature part ordering information.
E	March 2014	■ Table 4-1: Updated CK1 ■ Table 3-5: Updated Crystal Value Configuration ■ Section 3.5.1: Added Internal Bias ■ Section 3.5.4: Added 1.8 V Regulator Configuration ■ Tables 3-7,Table 3-8, Table 5-2, Table 5-3: Updated GPIO information ■ Table 5-1: Updated RFIN2P1_ANT* pin description
F	August 2014	■ Section 7: Updated ordering number for chip revision B. ■ Section 8: Added chip reliability data.

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Contents

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1 Introduction

1.1 General Description

The QCA4004 is an intelligent platform for the Internet of Everything that contains a low-power Wi-Fi connectivity solution on a single chip. It includes a number of TCP/IP-based connectivity protocols along with SSL, enabling a low-cost, low-complexity system to obtain full-featured internet connectivity and reliable information exchange.

The QCA4004 provides two interfaces for connecting to local system controllers. A UART-based host interface can be used for rapid development and deployment of simple data streams between the local device and the internet cloud. An SPI slave interface is available for applications that require more advanced connectivity to the network.

The QCA4004 Wi-Fi link is a full-featured, dual-band, single stream 802.11n solution. The Wi-Fi link is highly integrated, and includes an energy efficient on-board power amplifier and LNA. For the 2.4 GHz band, RF switches are also integrated. The QCA4004 Wi-Fi link is optimized for low system cost, and minimizes the number and cost of any components required to achieve a reliable Wi-Fi link.

1.2 Features

Wi-Fi link

- Support for IEEE 802.11a/b/g/n
- Single stream 1 × 1
- Dual-band 2.4 GHz/5 GHz
- Integrated PA, LNA, with support for external PA and external LNA
- Single or dual Rx front end for antenna diversity
- Green Tx power saving mode
- Low power listen mode
- Data rates up to 150 Mbps
- Full security support: WPS, WPA, WPA2, WAPI, WEP, TKIP

System cost optimization

- Highly-Integrated Wi-Fi solution that requires only a single crystal, antenna, and antenna matching components to complete the RF link.
- Integrated IPv4/IPv6 TCP/IP stack

- Integrated Network services such as HTTP, DNS, FTP
- 8 mm x 8 mm, 68-pin QFN package
- QCA4004 patch firmware is stored and automatically loaded from a low cost serial flash memory

Manufacturing interface

- USB 2.0 device interface, providing a simplified, high-speed, and scalable manufacturing test and configuration interface for QCA4004-based systems, using an integrated controller and PHY

Host interfaces

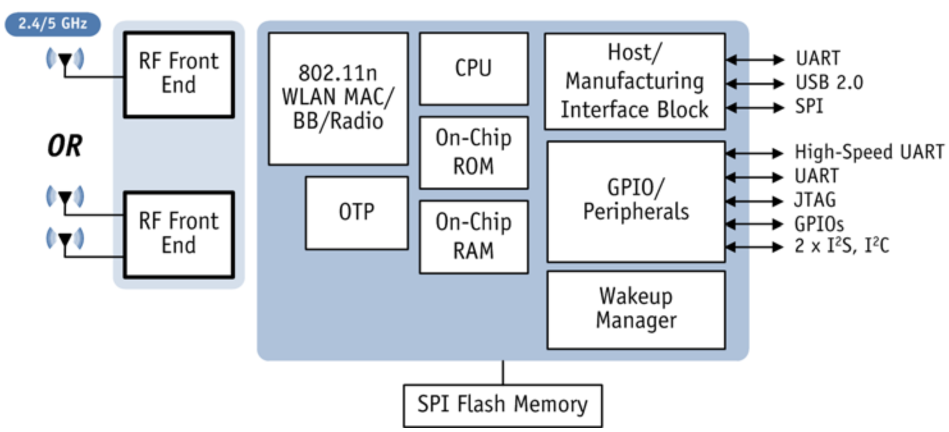
- SPI slave interface

  Allows for simplified connection to local host microcontrollers.
  Host driver source code and programming APIs are available.
- UART/SPI host interface allows simple interfacing to microcontrollers.
- UART with an AT style command set

Wakeup manager

- Non-volatile 8 KB RAM
- Suspend/resume timer

1.3 QCA4004 System Block Diagram



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2 Functional Description

2.1 Overview

The QCA4004 is a single chip, system-on-a-chip, 1x1 802.11 a/b/g/n device optimized for low-power embedded applications with single-stream capability for both transmit and receive. It has an integrated network processor with a large set of TCP/IP with IPv4/IPv6 based services. These services can be accessed via a serial SPI link connected external host CPU.

2.2 Integrated Network Processor

The QCA4004 includes a network processor that provides IP services and manages Wi-Fi link operations. The network processor code is loaded automatically from ROM off-chip serial flash memory. The flash memory is also used to store system configuration and persistent data sets. The network processor is optimized for energy efficient communications and includes multiple power states (see section 2.6). Customers can use the integrated network processor to implement application-specific solutions. This customized code is stored on an off-chip serial flash.

2.3 GPIO

The QCA4004 GPIO pins are fully configurable. They are shared with other interfaces, such as I^2C, SPI, and serial flash. Table 5-2 and Table 5-3 provides the set of pin configurations options. Each of the GPIO pins supports these configuration options:

- Internal pull-up/down options
- API to read the current pin state
- API signals host CPU when a GPIO pin transaction is detected
- Trigger an exit from the Sleep state when a pin event is detected
- Open-drain or push-pull output driver
- Output source from a software register or the hardware pulse-width modulation (PWM)

2.4 Serial Interface

The QCA4004 includes two high-speed Universal Asynchronous Receiver/Transmitter (UART) interfaces, which may be configured to serve as either a host interface link or a debug message console.

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2.5 Reset and Startup Sequence

The QCA4004 CHIP_PWD_L pin can be used to completely reset the entire chip. After this signal has been de-asserted, if configured for SPI slave operation, the QCA4004 waits in a low-power state until communication from the host, indicating that the Wi-Fi and the network services should be started. When configured for UART host mode, the QCA4004 begins its boot up process and starts network services as soon as CHIP_PWD_L is deasserted.

2.5.1 Wakeup Manager

The wakeup manager enables use of the QCA4004 in low power environments with no external host CPU. To achieve the lowest average power profile, the QCA4004 must be placed in suspend mode for the majority of the time. While in suspend state, the QCA4004 shuts down all circuits except a few critical blocks needed to resume operation after suspend; these include I/O pads to detect a wakeup request, a sleep timer to detect a synchronous wakeup event, and a small RAM that stores state information spanning a suspend-resume cycle.

To enter SUSPEND state, QCA4004 firmware saves state in the on-chip non-volatile RAM (NVRAM) and configures wakeup timers. Firmware then triggers the suspend operation, which turns on isolation circuits and turns off voltage regulators to the QCA4004 main core block.

Only the wakeup manager block and PMU circuits remain powered in suspend mode. When a wakeup event is detected, the device exits suspend back to active state. Wakeup events include synchronous wakeup, which occurs when the sleep timer in the wakeup manager expires, and asynchronous wakeup, which occurs when a pin event is detected on the wakeup pin.

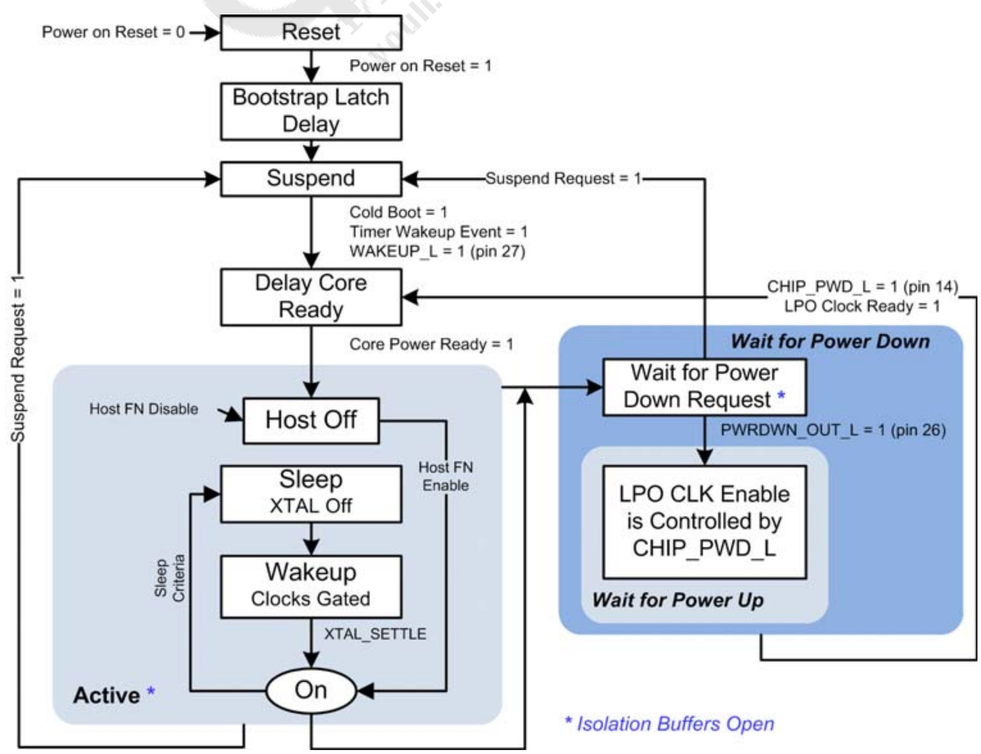

Figure 2-1 Wakeup Manager

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2.5.2 Detailed SPI Slave Startup Sequence

After a COLD_RESET event (e.g., the host toggles CHIP_PWD_L), the QCA4004 enters the HOST_OFF state and awaits communication from the host indicating that Wi-Fi and network services should be started. When configured for UART host mode, the QCA4004 begins its boot up process and starts network services as soon as CHIP_PWD_L pin is deasserted.

- When the host is ready to use the QCA4004, it initiates communication via SPI slave and enables network services by writing to a specific register via the SPI slave interface.
- When the QCA4004 enters the WAKEUP state for some duration and transits to the ON state, the on-chip network processor configures the QCA4004 functions and interfaces, as per the configuration and customization data set provided by the serial flash memory. When the QCA4004 is ready to receive commands from the host, it sets a specific flag that is accessible from the Host CPU via the SPI slave interface.
- The host reads the ready bit and can now send function commands to the QCA4004.

2.5.3 Power Management Unit

The QCA4004 has an integrated power management unit (PMU) that generates all the power supplies required by its internal circuitry either from an external battery or a 3.3 V supply.
The main components of the PMU include:

- A switching regulator (SWREG) that produces a 1.2 V supply from the 3.3 V supply.
- A linear regulator (SREG) which converts the host I/O supply to a 1.2 V supply for some small control blocks which are turned on when CHIP_PWD_L is de-asserted.
- A linear regulator which produces a 1.2 V supply from a 3.3 V supply (can be used instead of the SWREG to reduce the BOM cost).

2.6 Power Transition

The QCA4004 provides integrated power management and control functions and extremely low power operation for maximum battery life across all operational states by:

- Gating clocks for logic when not needed
- Shutting down unneeded high speed clock sources
- Reducing voltage levels to specific blocks in some states

2.6.1 Sleep State Management

SLEEP state minimizes power consumption while network services are not required, yet the system must remain ready for use within a short time. In SLEEP state, all high speed clocks are gated off and the external reference clock source is powered off. The network processor and Wi-Fi link are also suspended and not operational. All state information in the network processor (and its memory) and the Wi-Fi link are preserved to allow a fast resume to full network services.

The system remains in sleep state until a wakeup event causes the system to enter the WAKEUP state. Once WAKEUP state is entered, the QCA4004 restores all voltage levels and clocks, then

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automatically moves to the ON state. This wakeup event can be either a pin event or internal timer based event. The pin event may be triggered by the host CPU, or some system level event.

2.6.2 Hardware Power States

Table 2-1 describes the top level hardware power states in the QCA4004.

Table 2-1 Power Management States

State	Description
POWER_ DOWN	CHIP_PWD_L pin assertion immediately brings the chip to this state.
	Sleep clock is disabled.
	No state is preserved.
SUSPEND	While in suspend state, the chip shuts down all circuits except a few critical blocks needed to resume operation after suspend.
HOST_OFF	Network services and WLAN are off. Only the SPI host interface is powered on, the rest of the chip is power gated (off).
	The host can transition QCA4004 to WAKEUP (followed by ON) at any time by writing a register in the host interface domain.
	WLAN and CPU states are not retained.
	For UART hosted, or USB manufacturing configurations, this state is bypassed by pulling GPIO0 low at the deassertion of CHIP_PWD_L. This state applies only to SPI designs.
SLEEP	Only the sleep clock is operating.
	The crystal or oscillator is disabled.
	Any wakeup events (MAC, host, LF timer, GPIO interrupt force a transition to WAKEUP.
	All internal states are maintained.
	Host interface is idle (USB is in SUSPEND).
WAKEUP	The system transition from sleep OFF states to ON.
	The high frequency clock is gated off as the oscillator is brought up and the PLL is enabled.
	WAKEUP duration is less than 2 ms.
ON	The high speed clock is operational.
	Lower-level clock gating is implemented at the block level, including the CPU, which can be gated off using WAITI instructions while the system is on.

Figure 2-2 depicts the USB and UART power state transition diagrams.

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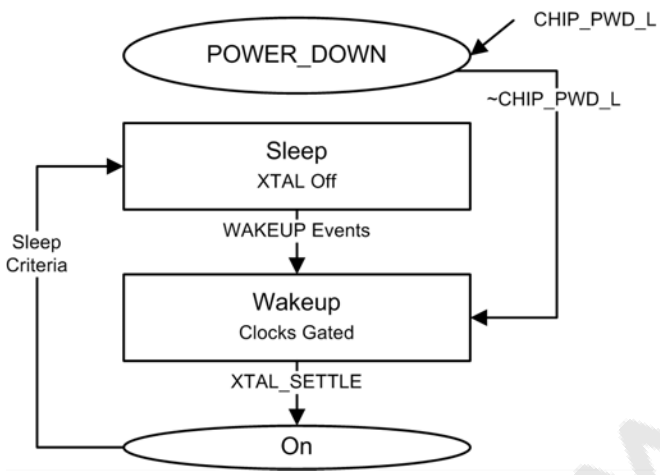

Figure 2-2 QCA4004 Power State: USB and UART Host Modes or Hostless Systems

2.7 System Clocking (RTC Block)

The QCA4004 has an RTC block which controls the clocks and power going to other internal modules. Its inputs consist of sleep requests from these modules and its outputs consist of clock enable and power signals which are used to gate the clocks going to these modules. The RTC block also manages resets going to other modules with the device. The QCA4004's clocking is grouped into two types:

- High-speed
- Low-speed

2.7.1 High Speed Clocking

The reference clock source drives the PLL and RF synthesizer within the QCA4004. It can be either an external crystal or oscillator. To minimize power consumption, the reference clock source is powered off in SLEEP, HOST_OFF, POWER_DOWN and after HOST_OFF states. For an external crystal, the QCA4004 disables the on-chip oscillator driver. For an external oscillator, the QCA4004 de-asserts its CLK_REQ signal to indicate that a reference clock is not needed.

When exiting SLEEP state, the QCA4004 waits in WAKEUP state for a programmable duration. During this time, the CLK_REQ signal is asserted to allow for the reference clock source to settle. The CLK_REQ signal remains asserted in ON state.

The QCA4004 supports reference clock sharing in all power states. For an external crystal, the on-chip oscillator driver drives a reference clock output whenever an external clock request signal is asserted. For an external oscillator, the external clock request signal is forwarded on the CLK_ REQ signal, and the input clock is passed along to the reference clock output.

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2.7.2 Low-Speed Clocking

The QCA4004 has eliminated the need for an external sleep clock source thereby reducing system cost. Instead, an internal ring oscillator is used to generate a low frequency sleep clock. It is also used to run the state machines and counters related to low power states.

The QCA4004 has an internal calibration module which produces a 32.768 KHz output with minimal variation. For this, it uses the reference clock source as the golden clock. As a result, the calibration module adjusts for process and temperature variations in the ring oscillator when the system is in ON state.

2.7.3 Interface Clock

The host interface clock represents another clock domain for the QCA4004. This clock comes from the host and is completely independent from the other internal clocks. It drives the host interface logic as well as certain registers which can be accessed by the host in HOST_OFF and SLEEP states.

2.7.4 Wakeup Manager Clock

The QCA4004 includes a dedicated always-on clock oscillator. In the SUSPEND state, this clock oscillator is the only clock that continues to run. This clock is used to calculate the resume from SUSPEND time interval. The QCA4004 has an option for using an external 32-KHz oscillator instead of the onboard low-power oscillator.

2.8 Front End Control

For applications that use external front-end components, the QCA4004 provides the ability to control them with four antenna switch control outputs named:

- ANTA
- ANTB
- ANTC
- ANTD

A programmable switch table indexed by transceiver state offers flexibility for various front-end configurations. The QCA4004 supports antenna sharing with another wireless chip in all power states by using ANTD to control the shared antenna switch.

2.9 MAC Block

The QCA4004 Wireless MAC consists of these major blocks:

- Host interface unit (HIU) for bridging to the AHB for bulk data accesses and APB for register accesses
- 10 queue control units (QCU) for transferring Tx data

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- 10 DCF control units (DCU) for managing channel access
- Protocol control unit (PCU) for interfacing to baseband
- DMA receive unit (DRU) for transferring Rx data
- Supports Rx diversity

2.10 Baseband Block

The QCA4004 baseband (BB) module is the physical layer controller for the 1x1 802.11a/b/g/n air interface. It is responsible for modulating data packets in the transmit direction, and detecting and demodulating data packets in the receive direction. It has a direct control interface to the radio to enable hardware to adjust analog gains and modes dynamically.

2.11 Active Power Save

2.11.1 Low Power Listen (LPL)

To minimize active current consumption, the QCA4004 firmware will set the receiver in a low power listen mode, thus saving active power in between frames, when the transceiver is awaiting frames, as well as during active reception. It can be enabled in most conditions with minimal performance impact, between 1 and 2 dB. If harsh channel conditions require it, firmware will automatically revert to full power mode.

2.11.2 Green Tx

To minimize active current consumption during transmission, the QCA4004 will utilize Green Tx. This feature allows the device to save power when communicating with a nearby station or access point when high output power is not required to sustain reliable communications. In such cases, the transmitter will reduce the transmit power to obtain current saving, while maintaining its high uplink throughput.

2.12 IPv4/IPv6 Networking

The QCA4004 includes a TCP/IP and UDP offload capability. This capability can reduce Flash requirements on a host MCU by up to 100 KBytes and also free up CPU cycles. The IP stack is a simultaneous IPv4/IPv6 stack with a BSD-like interface to simplify porting and integration with common embedded operating systems. The supported features of the QCA4004 (support for DHCP, multicast, and ARP) include:

- ARP
- Forwarding
- Fragmentation/reassembly (supported with limitation)
- IPv4/v6 header processing

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- UDP/TCP socket support
- DHCP v4
- Neighbor discovery
- Broadcast/multicast
- Path MTU discovery
- Address auto-configuration
- Multicast
- TCP zero-copy feature
- HTTP/SSL client/server feature

The QCA4004 supports many key IPv4 and IPv6 RFCs as shown in Table 2-2 and Table 2-3.

Table 2-2 QCA4004 IPv4 Supported RFCs

IPv4 RFC Number
RFC1122: TCP Timeout/retransmission
RFC1122: TCP Keep-alive
RFC1122: TCP Zero-Window-Probe
RFC1122: TCP Sliding window protocol

Table 2-3 QCA4004 IPv6 Supported RFCs

IPv6 RFC Number
RFC2464:Transmission of IPv6 packets over Ethernet networks
RFC2460: Internet Protocol version 6
RFC2462: Duplicate Address Detection (DAD)
RFC2463: ICMPv6
RFC3513: IP version 6 addressing architecture
RFC3484: Default Address Selection
RFC2461: Neighbour discovery for IPv6 host
RFC4862: Stateless Address Auto-configuration

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3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 summarizes the absolute maximum ratings and Table 3-2 lists the recommended operating conditions for the QCA4004. Absolute maximum ratings are those values beyond which damage to the device can occur.

Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

NOTE Maximum rating for signals follows the supply domain of the signals.

Table 3-1 Absolute Maximum Ratings

Symbol (Domain)	Description	Max Rating	Unit
VDDIO_GPIO	I/O supply for GPIO15-GPIO31 pins	-0.3 to 4.0	V
VDDIO_HOST	I/O supply for GPIO0-GPIO13 pins	-0.3 to 4.0	V
DVDD12	Digital 1.2 V supply[1]	-0.3 to 1.32	V
SWREG_FB_VDD12			
VDD12_BB_PLL	1.2 V supply for analog BB PLL	-0.3 to 1.32	V
VDD12_RF	1.2 V supply for analog RF	-0.3 to 1.32	V
VDD12_SYNTH	1.2 V supply for analog SYNTH	-0.3 to 1.32	V
VDD33_ANT	Antenna control I/O supply	-0.3 to 4.0	V
VDD33_RF	3.3 V supply for analog RFs	-0.3 to 4.0	V
VDD33_SYNTH	3.3 V supply for analog SYNTH	-0.3 to 4.0	V
VDD33	3.3 V supply for switching regulator/PMU	-0.3 to 4.0	V
SWREG_IN			
VDD33_PLL_XTAL	3.3 V supply for XTAL/PLL	-0.3 to 4.0	V
VDD33_USB	3.3 V supply for USB	-0.3 to 4.0	V
V_{IH} MIN	Minimum Digital I/O Input Voltage for 1.8 V or 3.3 V I/O Supply	-0.3	V
3.3 V I/O V_{IH} MAX	Maximum Digital I/O Input Voltage for 3.3 V I/O Supply	V_{dd} +0.3	V
RF_{in}	Maximum RF input (reference to 50-Ω input)	+10	dBm
T_{store}	Storage Temperature	-45 to 135	°C
T_j	Junction Temperature	125	°C

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Table 3-1 Absolute Maximum Ratings

ESD-HBM	Electrostatic Discharge Tolerance under Human Body Model, all pins	2000	V
ESD-CDM	Electrostatic Discharge under Charged Device Model, all pins except RF pins	500	
ESD-CDM-RF	Electrostatic Discharge under Charged Device Model, for the RFIN and RFOUT pins	400	

1. DVDD12 and SWREG_FB are connected through an external LC filter to the SWREG_OUT pin. See Figure 3-1.

3.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
VDDIO_GPIO	I/O supply for GPIO15-GPIO21 pins	1.71	–	3.46	V
VDDIO_HOST	I/O supply for GPIO0-GPIO13 pins	3.0	–	3.6	V
VBATT_3P3	I/O supply for GPIO31 pin	3.14	–	3.46	V
DVDD12	Digital 1.2 V supply[1]	1.20	1.26	1.32	V
SWREG_FB_VDD12					
VDD12_BB_PLL, VDD12_SYNTH, VDD12_RF	Analog 1.2 V supplies	1.20	1.26	1.32	V
VDD33	Internal switching regulator supply	3.14	3.3	3.46	V
SWREG_IN					
VDD33_ANT	Antenna control I/O supply	3.14	3.3	3.46	V
VDD33_RF, VDD33_SYNTH, VDD33_PLL_XTAL, VDD33_USB	Analog 3.3 V supplies	3.14	3.3	3.46	V
T_{case}	Standard case temperature	0	–	85	°C
	Industrial case temperature	-40	–	85	° C
Psi_{JT}	Thermal parameter[2]	–	3	–	°C/W

1. DVDD12 and SWREG_FB_VDD12 are connected through an external LC filter to the SWREG_OUT pin. See Figure 3-1.
2. The thermal parameter is for the8 mm x 8 mm, 68-pin QFN package.

3.3 General DC Electrical Characteristics

These conditions apply to all DC characteristics unless otherwise specified:

T_{amb} = 25 °C, V_{dd33}= 3.3 V

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Table 3-3 DC Electrical Characteristics for Digital I/Os

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	1.8	–	3.6	V
V_{IL}	Low Level Input Voltage	-0.3	–	0.3	V
V_{OH}	High Level Output Voltage	2.2	–	3.3	V
V_{OL}	Low Level Output Voltage	0	–	0.4	V
I_{IH}	High Level Input Current	–	–	0.1	µA
I_{IL}	Low Level Input Current	–	–	0.1	µA
I_{OH}	High Level Output Current for GPIO0 to GPIO13	–	–	20	mA
	High Level Output Current for GPIO15 to GPIO31	–	–	20	
I_{OL}	Low Level Output Current for GPIO0 to GPIO13	–	–	20	mA
	Low Level Output Current for GPIO15 to GPIO31	–	–	20	
C_{IN}	Input Capacitance for GPIO0 to GPIO13	–	5	–	pF
	Input Capacitance for GPIO15 to GPIO31	–	3	–	

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3.4 Internal Voltage Regulator

The QCA4004 supports two regulator modes for its on-chip 1.2 V regulator; see section 3.5.4 for more information.

3.4.1 Switching 1.2 V Regulator

Figure 3-1 depicts the switching 1.2 V switching power supply regulated by the QCA4004. Refer to the reference design schematics for details.

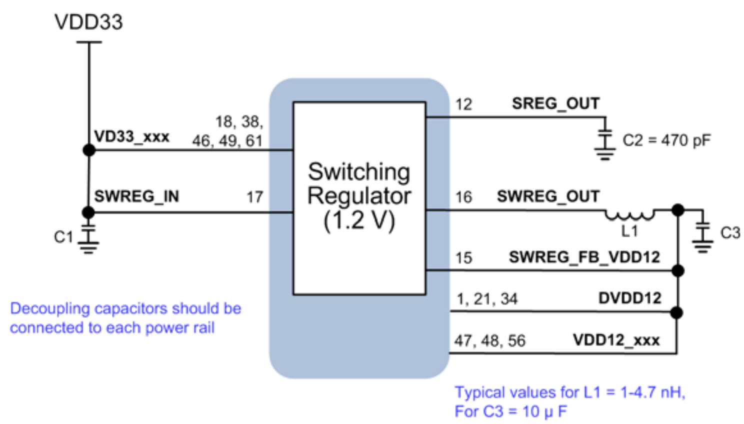

Figure 3-1 1.2 V Switching Power Supply Regulated by the QCA4004

3.4.2 Linear 1.2 V Regulator

Figure 3-2 depicts the switching 1.2 V linear power supply regulated by the QCA4004. Refer to the reference design schematics for details.

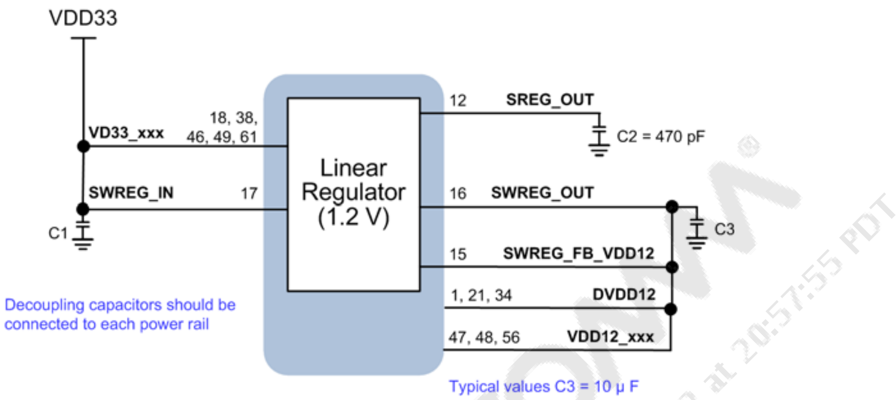

Figure 3-2 1.2 V Linear Power Supply Regulated by the QCA4004

3.5 Bootstrap Modes and Pins

Certain pins in the QCA4004 are sampled at startup, and these sampled values are used to select among various bootstrap modes and chip configurations.

3.5.1 Internal Bias

Table 3-4 shows the pins biased by chip hardware during power down. After startup, chip firmware may change the bias.

Table 3-4 Internal Bias During Power Down

GPIO	Internal Bias
GPIO6	Pull-Down
GPIO11	
GPIO20	Pull-Up
GPIO30	
GPIO31	

3.5.2 Host Mode Configuration

Table 3-5 lists the QCA4004 bootstrap pins that select the interface used to communicate with the external host CPU. Host mode selection affects pin behavior of host interface pins as well as bootup processes in the PCM state machine. It informs the QCA4004 about the presence of an external CPU (referred to as the host controller) and the interface used to exchange messages.

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Table 3-5 Host Mode Configuration

Pin Name	Bootstrap Function Name	On Chip Biasing	GPIO [0,2]	Description
GPIO0, GPIO2	hostmode	—	00	QCA4004 CPU bootup is under control of the host CPU via the USB interface. The external CPU is required and the host interface is USB.
			01	No host required at startup time. The QCA4004 CPU self boots and firmware may configure any of the available interfaces. No external CPU is required.
			10	The QCA4004 CPU bootup is under control of host CPU via SPI Slave interface. The external CPU is required and the SPI interface is the host interface.
			11	Reserved

3.5.3 Crystal Value Configuration

Table 3-6 shows the bootstrap pin to configure the crystal value.

Table 3-6 Crystal Value Configuration

Pin Name	Bootstrap Function Name	On Chip Biasing	Description	
GPIO20	xtal_freq[0]	–	0	Reserved
			1	40 MHz

3.5.4 1.2 V Regulator Configuration

The QCA4004 supports two regulator modes for its on-chip 1.2 V regulator: switching and linear. Linear mode requires fewer board-level components, but at a slightly higher power consumption than switching mode. Table 3-7 shows the bootstrap pin to configure the 1.2 V regulator.

Table 3-7 Host Mode Configuration

Pin Name	Bootstrap Function Name	On Chip Biasing	Description	
GPIO13	en_linear	–	0	Switching regulator
			1	Linear regulator

3.5.5 1.8 V Regulator Configuration

The QCA4004 supports a regulator mode for its on-chip 1.8 V regulator.

Table 3-8 Host Mode Configuration

Pin Name	Bootstrap Function Name	On Chip Biasing	Description	
GPIO31	1p8_reg_enable	Pull Up	Enable for on chip 1.8 V regulator	
			0	1.8 V regulator is disabled
			1	1.8 V regulator is enabled

3.5.6 Test Mode Configuration

Table 3-9 shows the bootstrap pin to configure the test mode. GPIO11 has an on-chip pull down.

Table 3-9 Test Mode Configuration

Bootstrap Function Name	Description	
Normal Function Mode	GPIO11	0
	WAKEUP_L	1
	GPIO3 GPIO4 GPIO5 GPIO6 GPIO12	Does not care
JTAG Function Mode	GPIO3	Does not care
	GPIO4	1
	GPIO5	0
	GPIO6	Does not care
	GPIO11	1
	GPIO12	0

GPIO31 is enabled for on-chip 1.8 V regulator whose output is on VDD_1P8_OUT (pin 23).

3.5.7 JTAG Pins

When the bootstrap power up is configured for JTAG mode, the QCA4004 will connect its TAP controller to the pins shown in Table 3-10.

Table 3-10 JTAG Mode

Pin Name	Bootstrap Function Name
GPIO6	TDI
GPIO10	TMS
GPIO12	TCK
GPIO13	TDO
GPIO25	TRST

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3.6 Radio Rx Characteristics

This section summarizes the QCA4004 Rx characteristics.

Table 3-11 Rx Characteristics for 2.4 GHz Operation

Symbol	Parameter	Conditions[1 2]	Min	Typ[3]	Max	Unit
F_{rx}	Rx input frequency range	–	2.412	–	2.484	GHz
S_{rf}	Sensitivity					
	CCK	1 Mbps	–	-95.7	–	dBm
		2 Mbps	–	-92.7	–	
		5.5 Mbps	–	-90.7	–	
		11 Mbps	–	-87.7	–	
	OFDM	6 Mbps	–	-92.7	–	
		9 Mbps	–	-91.7	–	
		12 Mbps	–	-89.7	–	
		18 Mbps	–	-87.7	–	
		24 Mbps	–	-85.7	–	
		36 Mbps	–	-82.7	–	
		48 Mbps	–	-78.7	–	
		54 Mbps	–	-75.7	–	
	HT20	MCS0	–	-92.7	–	
		MCS1	–	-89.7	–	
		MCS2	–	-86.7	–	
		MCS3	–	-82.7	–	
		MCS4	–	-80.7	–	
		MCS5	–	-76.7	–	
		MCS6	–	-74.7	–	
		MCS7	–	-72.7	–	
	HT40	MCS0	–	-90.7	–	
		MCS1	–	-87.7	–	
		MCS2	–	-84.7	–	
		MCS3	–	-80.7	–	
		MCS4	–	-78.7	–	
		MCS5	–	-73.7	–	
		MCS6	–	-72.7	–	
		MCS7	–	-69.7	–	

1. In LPL mode, sensitivity will be degraded by 1-2 dB.
2. As measured on the RFIN2N1 and RFIN2P1 pins.
3. Performance measured at the balun.

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Table 3-12 Adjacent Channel Rejection for 2.4 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
r_{adj}	***Adjacent channel rejection***					
	CCK	2 Mbps	–	43	–	dB
	CCK	11 Mbps	–	37	–	dB
	OFDM	6 Mbps	–	37	–	dB
	OFDM	54 Mbps	–	21	–	dB
	HT20	MCS0	–	36	–	dB
	HT20	MCS7	–	20	–	dB
	HT40	MCS0	–	27	–	dB
	HT40	MCS7	–	7	–	dB

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Table 3-13 Rx Characteristics for 5 GHz Operation

Symbol	Parameter	Conditions [1 2]	Min	Typ	Max	Unit
F_{rx}	Receive input frequency range		4.90	–	5.925	GHz
S_{rf}	Sensitivity					
	OFDM	6 Mbps	–	-94.5	–	dBm
		9 Mbps	–	-92.5	–	
		12 Mbps	–	-89.5	–	
		18 Mbps	–	-87.5	–	
		24 Mbps	–	-85.5	–	
		36 Mbps	–	-82.5	–	
		48 Mbps	–	-78.5	–	
		54 Mbps	–	-77.5	–	
	HT20	MCS0	–	-94.5	–	
		MCS1	–	-92.5	–	
		MCS2	–	-87.5	–	
		MCS3	–	-82.5	–	
		MCS4	–	-81.5	–	
		MCS5	–	-78.5	–	
		MCS6	–	-76.5	–	
		MCS7	–	-74.5	–	
	HT40	MCS0	–	-91.5	–	
		MCS1	–	-88.5	–	
		MCS2	–	-86.5	–	
		MCS3	–	-83.5	–	
		MCS4	–	-80.5	–	
		MCS5	–	-75.5	–	
		MCS6	–	-74.5	–	
		MCS7	–	-71.5	–	

1. In LPL mode, sensitivity will be degrade by 1-2 dB.
2. Performance measured at the balun.

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Table 3-14 Adjacent Channel Rejection for 5 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{adj}	Adjacent channel rejection					
	OFDM	6 Mbps	–	26	–	dB
	OFDM	54 Mbps	–	12	–	
	HT20	MCS0	–	25	–	
	HT20	MCS7	–	7	–	
	HT40	MCS0	–	25	–	
	HT40	MCS7	–	8	–	

3.7 Radio Tx Characteristics

This section summarizes the QCA4004 Tx characteristics.

Table 3-15 Tx Characteristics for 2.4 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Tx output frequency range	–	2.412	–	2.484	GHz
P_{out}	Output power[1,2]					
	802.11b mask compliant	1 Mbps	–	20.7	–	dBm
	802.11g mask compliant	6 Mbps	–	20.7	–	
	802.11g EVM compliant	54 Mbps	–	18.8	–	
	802.11n HT20 mask compliant	MCS0	–	20.7	–	
	802.11n HT40 mask compliant	MCS0	–	18.5	–	
	802.11n HT20 EVM compliant	MCS7	–	18	–	
	802.11n HT40 EVM compliant	MCS7	–	18.4	–	
A_{pc}	Accuracy of power control	–	–	±1.5	–	dB

1. Refer to IEEE 802.11 specification for Tx spectrum limits:
   - 802.11b mask (18.4.7.3)
   - 802.11g mask (19.5.4)
   - 802.11g EVM (17.3.9.6.3)
   - 802.11n HT20 mask (20.3.21.1)
   - 802.11n HT20 EVM (20.3.21.7.3)
2. Performance calculated at the balun. Loss from balun to antenna connector in the test board is 0.7 dB (2 GHz) or 1.5 dB (5 GHz).

Table 3-16 Tx Characteristics for 5 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Tx output frequency range	–	4.90	–	5.925	GHz

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Table 3-16 Tx Characteristics for 5 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_{out}	Output power[1]					
	802.11a mask compliant	6 Mbps	–	20	–	dBm
	802.11a EVM compliant	54 Mbps	–	17.3	–	
	802.11n HT20 mask compliant	MCS0	–	19.7	–	
	802.11n HT40 mask compliant	MCS0	–	20.1	–	
	802.11n HT20 EVM compliant	MCS7	–	16.4	–	
	802.11n HT40 EVM compliant	MCS7	–	16.8	–	
Apc	Accuracy of power control	–	–	±2.0	–	dB

1. Performance measured at the balun.

3.8 QCA4004 Synthesizer Characteristics

This section summarizes the synthesizer characteristics for the QCA4004.

Table 3-17 Synthesizer Composite Characteristics for 2.4 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_c	Center channel frequency	Center frequency at 5 MHz spacing	2.412	–	2.484	GHz
F_{ref}	Reference oscillator frequency	±20 ppm	–	40	–	MHz
F_{step}	Frequency step size (at RF)	–	–	1	–	MHz

Table 3-18 Synthesizer Composite Characteristics for 2.4 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_c	Center channel frequency	Center frequency at 5 MHz spacing	4.90	–	5.925	GHz
F_{ref}	Reference oscillator frequency	±20 ppm	–	40	–	MHz
F_{step}	Frequency step size (at RF)	–	–	5	–	MHz

3.9 Power Consumption Performance

3.9.1 Measurement Conditions for Low Power States

- T_ambient = 25°C
- All I/O pins except CHIP_PWD_L are maintained at their default polarities (I/Os without default internal pulls are pulled low). See Table 3-19.

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Table 3-19 Typical Current Consumption: Low Power States at 3.3 V Operation

Mode	State	Typical Current Consumption for SPI/UART at 3.3 V				
Standby	CHIP_PWD	5 µA				
	SUSPEND	10 µA				
	HOST_OFF	50 µA				
	SLEEP	130 µA				
PS (2.4 GHz) (without LPL enabled)[1]	**DTIM Period**	**Current Consumption (µA)**	**T1 (ms)**	**T2 (ms)**	**Tbeacon (ms)**	**T3 (ms)**
	DTIM 1	1,090	2.01	0.36	0.99	0.39
	DTIM 3	473	1.99	0.32	1.06	0.41
	DTIM 5	335	1.99	0.30	1.01	0.41
	DTIM 10	258	1.97	0.43	0.97	0.47

1. Numbers are for switcher mode.

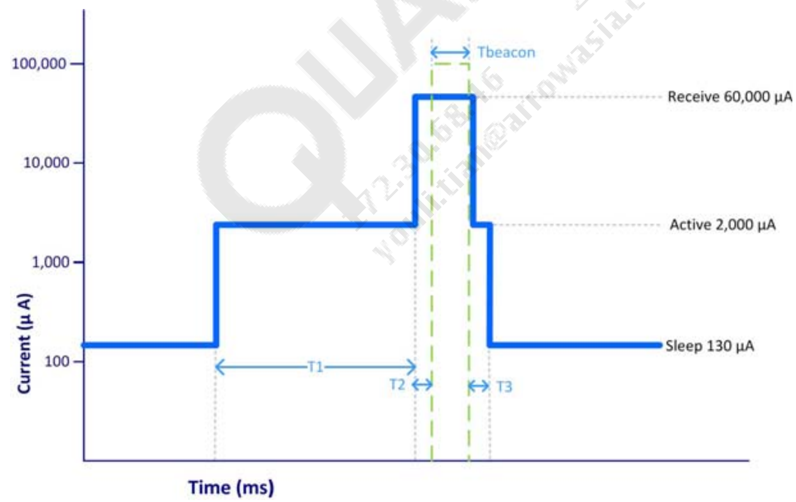

Figure 3-3 IEEE Sleep Power Profile

3.9.2 Measurement Conditions for Continuous Rx (2.4 GHz Operation)

Table 3-20 Typical Current Cons. (2.4 GHz): SW Regulator Continuous Rx at 3.3 V Operation[1]

Mode/Rate (Mbps)	SPI/UART		SW Regulator (mW)	Total Power (mW)
	3.3 V Circuits Power Consumption (mW)	1.2 V Circuits Power Consumption (mW)		
RX 11 Mbps	76.89	113.28	10.47	200.64
RX 54 Mbps	76.89	120	12	208.89
RX HT20 MCS0	76.89	116.88	11.16	204.93
RX HT20 MCS7	79.53	120.24	9.78	209.55
RX HT40 MCS0	80.52	140.88	14.22	235.62
RX HT40 MCS7	80.52	140.88	18.51	239.91

1. Insertion loss: Rx: 5 GHz = 1.6 dB, 2 GHz = 1.2 dB

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Table 3-21 Typical Current Cons. (2.4 GHz): SW Regulator Continuous Rx at 3.3 V Operation[1]

Mode/Rate (Mbps)	SPI/UART		SW Regulator (mW)	Total Power (mW)
	3.3 V Circuits Power Consumption (mW)	1.2 V Circuits Power Consumption (mW)		
RX 11 Mbps	77.6	116.5	189.7	383.8
RX 54 Mbps	77.6	124.4	201.6	403.6
RX HT20 MCS0	77.6	120.6	195.5	393.7
RX HT20 MCS7	77.6	124.9	200.1	402.6
RX HT40 MCS0	78.2	147.1	240.6	466.0
RX HT40 MCS7	78.2	150.6	246.7	475.5

1. Insertion loss: Rx: 5 GHz = 1.6 dB, 2 GHz = 1.2 dB

3.9.3 Measurement Conditions for Continuous Tx (2.4 GHz Operation)

- T_ambient = 25°C

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Table 3-22 Typical Current Cons. (2.4 GHz): SW Regulator Continuous Tx at 3.3 V Operation [1 2 3]

Mode/Rate (Mbps)	Target Output Power (dBm)	SPI/UART		SW Regulator (mW)	Total Power (mW)
		3.3 V Circuits Power Consumption (mW)	1.2 V Circuits Power Consumption (mW)		
Tx 1 Mbps	19.0	697.95	94.68	25.11	817.74
Tx 6 Mbps	19.0	671.22	101.76	39.48	812.46
Tx 11 Mbps	19.0	695.64	95.64	4.68	795.96
Tx 54 Mbps	18.0	577.17	105.84	12.3	695.31
Tx HT20 MCS0	20.0	723.36	102.24	42.63	868.23
Tx HT20 MCS7	17.0	590.37	102.96	23.43	716.76
Tx HT40 MCS0	17.0	582.78	116.52	32.31	731.61
Tx HT40 MCS7	14.0	510.51	118.56	16.41	645.48

1. Insertion loss: Rx: 5 GHz = 1.6 dB, 2 GHz = 1.2 dB
2. Tx Power is on the RF balun
3. Measured on a QCA4002 with DB142

Table 3-23 Typical Current Cons. (2.4 GHz): LDO Continuous Tx at 3.3 V Operation [1 2 3]

Mode/Rate (Mbps)	Target Output Power (dBm)	SPI/UART		LDO (mW)	Total Power (mW)
		3.3 V Circuits Power Consumption (mW)	1.2 V Circuits Power Consumption (mW)		
Tx 1 Mbps	19.0	697.95	94.68	147.54	940.17
Tx 6 Mbps	19.0	671.22	101.76	172.8	945.78
Tx 11 Mbps	19.0	695.64	95.64	159.78	951.06
Tx 54 Mbps	18.0	577.17	105.84	184.89	867.9
Tx HT20 MCS0	20.0	723.36	102.24	178.59	1004.19
Tx HT20 MCS7	17.0	590.37	102.96	169.95	863.28
Tx HT40 MCS0	17.0	582.78	116.52	196.32	895.62
Tx HT40 MCS7	14.0	510.51	118.56	190.65	819.72

1. Insertion loss: Rx: 5 GHz = 1.6 dB, 2 GHz = 1.2 dB
2. Tx Power is on the RF balun
3. Measured on a QCA4002 with DB142

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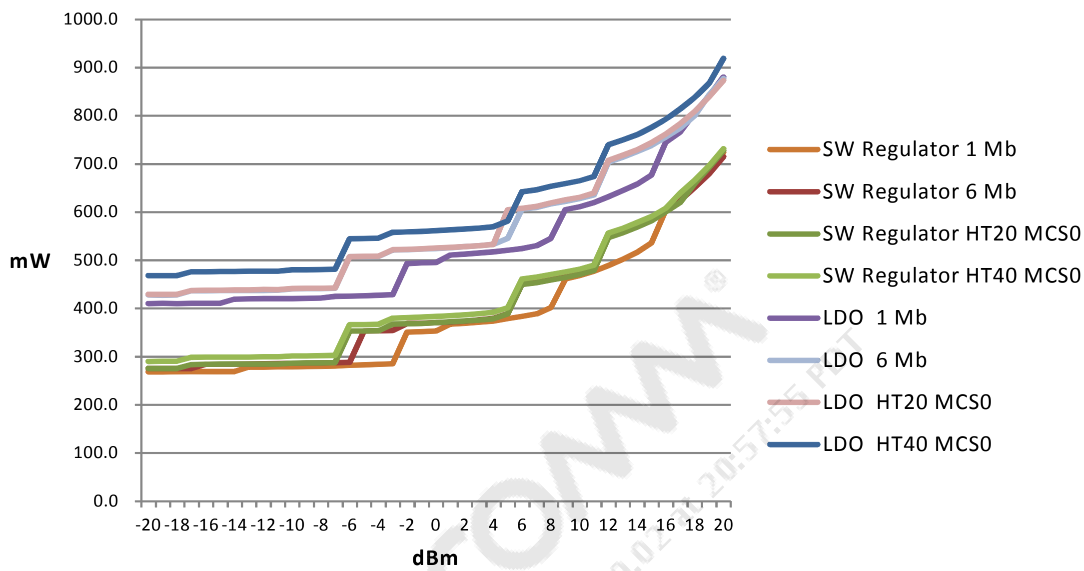

Figure 3-4 Total Chip Power vs. Tx Power: 2.4 GHz TX99 (in mW)

3.9.4 Measurement Conditions for Continuous Rx (5 GHz Operation)

- T_ambient = 25°C

Table 3-24 Typical Current Cons. (5 GHz): SW Regulator Continuous Rx at 3.3 V Operation[1]

Mode/Rate (Mbps)	SPI/UART		SW Regulator	Total Power
	3.3 V Circuits Power Consumption (mW)	1.2 V Circuits Power Consumption (mW)		
Rx 54 Mbps	80.19	129.84	7.77	217.8
Rx HT20 MCS0	80.19	126.72	7.59	214.5
Rx HT20 MCS7	80.19	130.32	5.97	216.48
Rx HT40 MCS0	87.45	148.32	8.76	244.53
Rx HT40 MCS7	87.45	151.2	9.51	248.16

1. Insertion loss:
   Rx: 5 GHz = 1.6 dB, 2 GHz = 1.2 dB

Table 3-25 Typical Current Cons. (5 GHz): LDO Continuous Rx at 3.3 V Operation[1]

Mode/Rate (Mbps)	SPI/UART		LDO	Total Power
	3.3 V Circuits Power Consumption (mW)	1.2 V Circuits Power Consumption (mW)		
Rx 54 Mbps	77.9	133.1	219.0	430.0

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Table 3-25 Typical Current Cons. (5 GHz): LDO Continuous Rx at 3.3 V Operation[1]

Rx HT20 MCS0	77.9	131.3	212.3	421.4
Rx HT20 MCS7	77.9	135.0	218.4	431.3
Rx HT40 MCS0	78.5	154.1	252.5	485.1
Rx HT40 MCS7	78.5	157.1	258.1	493.7

1. Insertion loss: Rx: 5 GHz = 1.6 dB, 2 GHz = 1.2 dB

3.9.5 Measurement Conditions for Continuous Tx (5 GHz Operation)

- T_ambient = 25°C

Table 3-26 Typical Current Cons. (5 GHz): SW Regulator Continuous Tx at 3.3 V Operation [1] [2] [3]

Mode/Rate (Mbps)	Target Output Power (dBm)	SPI/UART		SW Regulator	Total Power (mW)
		3.3 V Circuits Power Consumption (mW)	1.2 V Circuits Power Consumption (mW)		
OFDM 6 Mbps	17.0	644.16	95.64	28.77	768.57
OFDM 54 Mbps	15.0	545.82	100.08	29.94	675.84
HT20 MCS0	18.0	702.57	95.88	24.57	823.02
HT20 MCS7	10.5	494.34	96.48	11.1	601.92
HT40 MCS0	14.0	542.85	108.6	21.75	673.2
HT40 MCS7	10.5	491.7	110.64	18.39	620.73

1. Insertion loss: Rx: 5 GHz = 1.6 dB, 2 GHz = 1.2 dB
2. Tx Power is on the RF balun
3. Measured on a QCA4002 with DB142

Table 3-27 Typical Current Cons. (5 GHz): LDO Continuous Tx at 3.3 V Operation [1] [2] [3]

Mode/Rate (Mbps)	Target Output Power (dBm)	SPI/UART		LDO	Total Power (mW)
		3.3 V Circuits Power Consumption (mW)	1.2 V Circuits Power Consumption (mW)		
OFDM 6 Mbps	17.0	644.16	95.64	166.71	906.51
OFDM 54 Mbps	15.0	545.82	100.08	155.67	801.57
HT20 MCS0	18.0	702.57	95.88	152.61	951.06
HT20 MCS7	10.5	494.34	96.48	157.62	748.44
HT40 MCS0	14.0	542.85	108.6	185.76	837.21
HT40 MCS7	10.5	491.7	110.64	186.36	788.7

1. Insertion loss: Rx: 5 GHz = 1.6 dB, 2 GHz = 1.2 dB
2. Tx Power is on the RF balun
3. Measured on a QCA4002 with DB142

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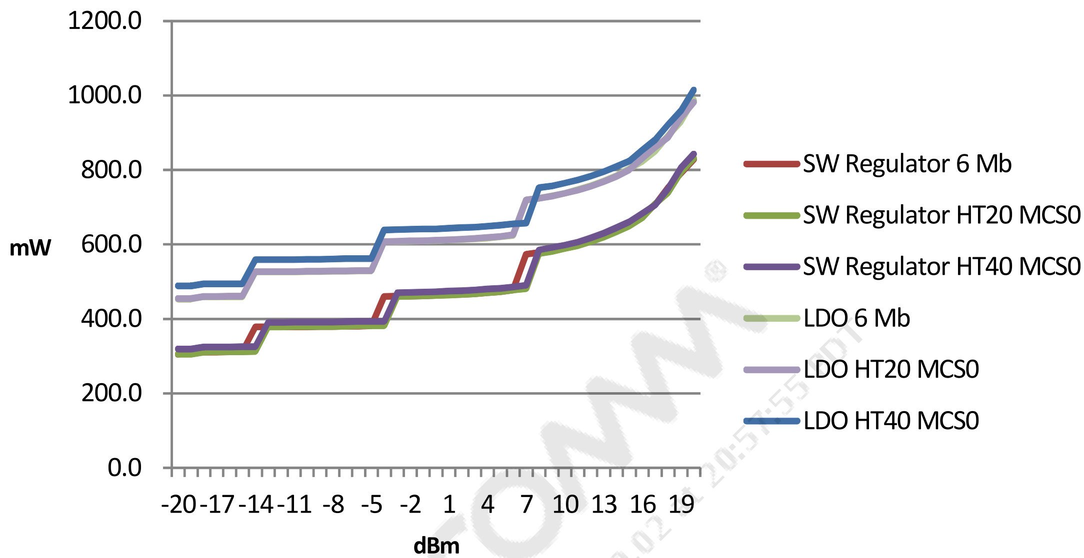

Figure 3-5 Total Chip Power vs. Tx Power: 5 GHz TX99 (in mW)

4 AC Specifications

4.1 External Reference Input Clock Timing

Figure 4-1 and Table 4-1 show the external 40 MHz reference input clock timing requirements.

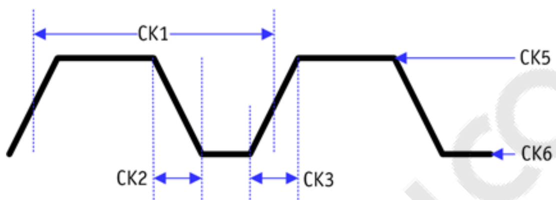

Figure 4-1 External Reference Input Clock Timing

Table 4-1 External 40 MHz Reference Input Clock Timing

Symbol	Description	Min	Typ	Max	Unit
CK1	Frequency accuracy	-20	–	20	ppm
	Frequency	–	40	–	MHz
CK2	Fall time	–	–	0.1 x period	ns
CK3	Rise time	–	–	0.1 x period	ns
CK4	Duty cycle (high-to-low ratio)	40	–	60	%
CK5	Input high voltage	0.75	–	1.26	V
CK6	Input low voltage	-0.55	–	0.3	V

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4.2 SPI Slave Interface Timing

Figure 4-2 shows the write timing for SPI slave style transactions.

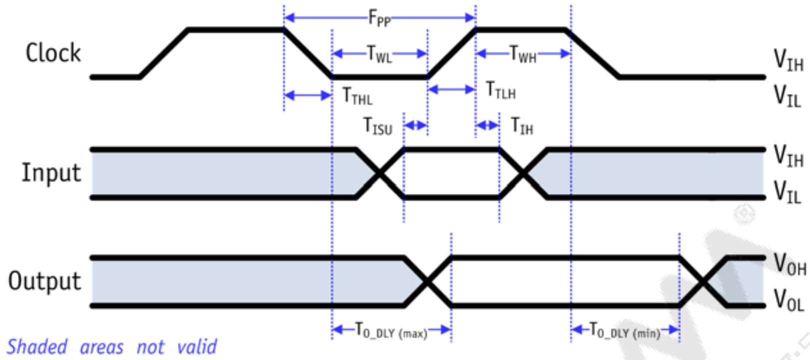

Figure 4-2 SPI Slave Timing

Table 4-2 shows the values for timing constraints for SPI slave.

Table 4-2 SPI Slave Timing Constraints

Parameter	Description	Min	Max	Unit
f_{PP}	Clock frequency	0	48	MHz
t_{WL}	Clock low time	8.3	–	ns
t_{WH}	Clock high time	8.3	–	ns
t_{TLH}	Clock rise time	–	2	ns
t_{THL}	Clock fall time	–	2	ns
t_{ISU}	Input setup time	5	–	ns
t_{IH}	Input hold time	5	–	ns
t_{O_DLY}	Output delay	0	5	ns

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4.3 SPI Master Interface Timing

Figure 4-3 shows the write timing for SPI master style transactions.

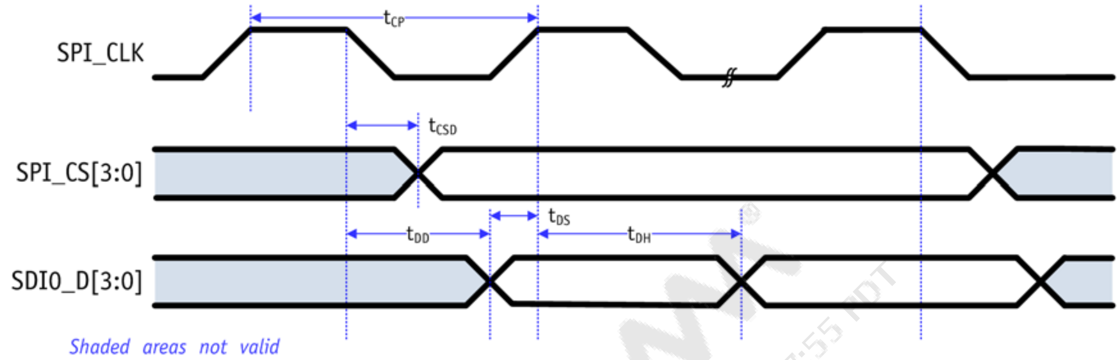

Figure 4-3 SPI Master Timing

Table 4-2 shows the values for timing constraints for SPI master.

Table 4-3 SPI Master Timing Constraints

Parameter	Description	Min	Max	Unit
t_{CP}	Clock period	30.7	1000	ns
t_{CSD}	Chip select valid delay	-5.5	5	ns
t_{DD}	Data valid delay	-5.5	5	ns
t_{DS}	Data setup	3	–	ns
t_{DH}	Data hold	0	–	ns

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4.4 Power Up Sequence

If a host processor controls the QCA4004 CHIP_PWD_L reset pin, then all supplies should be stable for a minimum of 5 µS before CHIP_PWD_L is deasserted (that is, is greater than V_{IL} for VDDIO_SDIO).

In the case where CHIP_PWD_L is not driven, but is a delayed version of VDD33 (power-on reset), the timing diagram in Figure 4-4 applies.

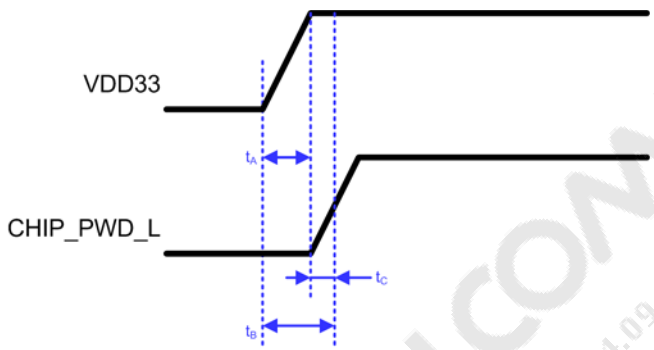

Figure 4-4 Power-On-Reset Timing

Table 4-4 shows the values for timing for power on reset.

Table 4-4 Power-On-Reset Timing

Parameter	Description	Min	Max	Unit
t_A	Rise time of VDD33 to 90% of 3.3 V	—	25	mS
t_C	Time from VDD33 reaching 90% of 3.3 V to the level of CHIP_PWD_L going above 0.5 * VDD33	5	—	µS
t_B	The value is $t_A + t_C$; during this time, the level of CHIP_PWD_L should stay below 0.5 × VDD33			

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5 Pin Descriptions

This section contains both a package pinout and tabular listings of the signal descriptions.

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types:

IA	Analog input signal
I	Digital input signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
I/O	A digital bidirectional signal
OA	An analog output signal
O	A digital output signal
P	A power or ground signal

Figure 5-1 shows the QCA4004 pinout.

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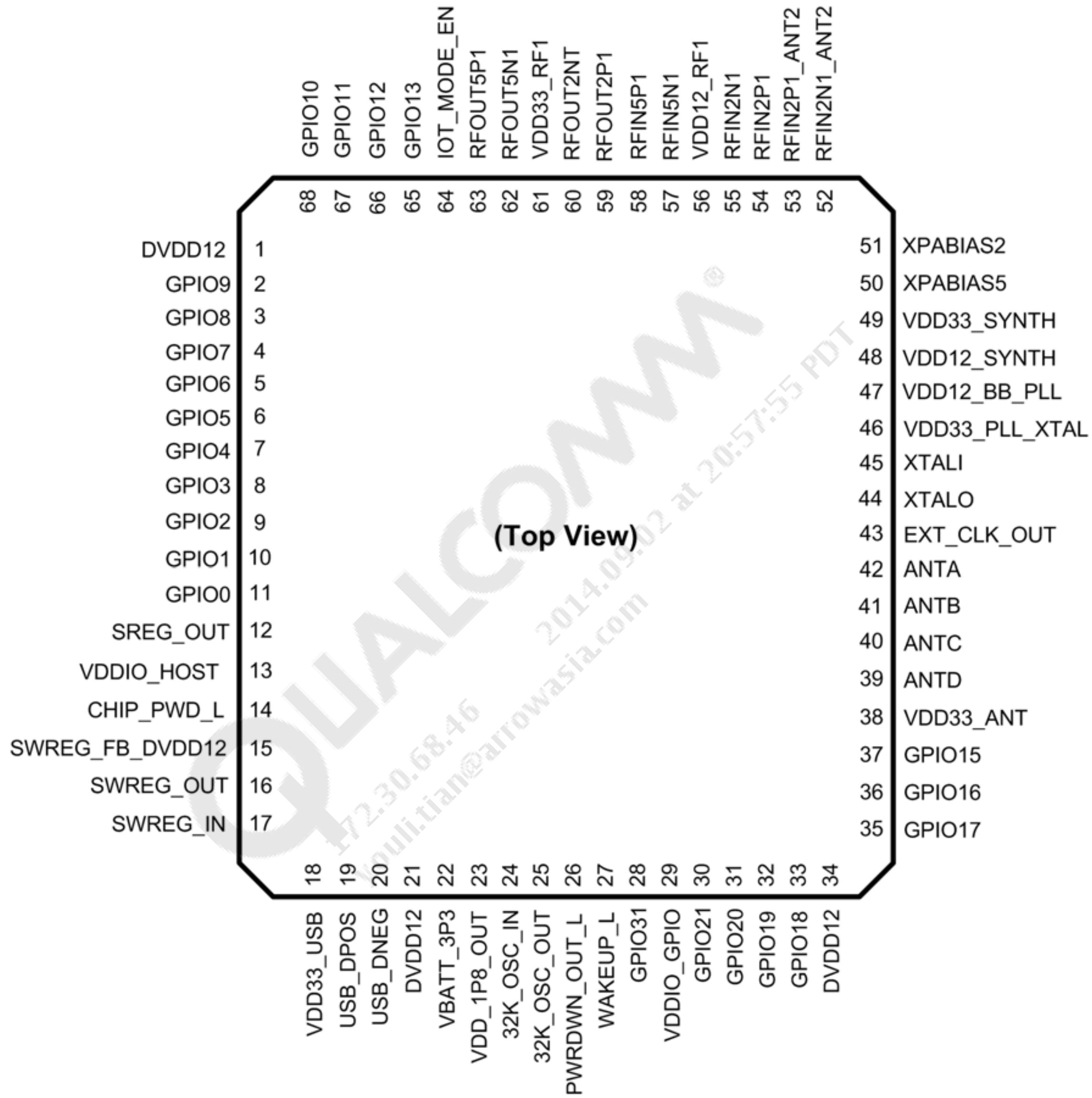

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Figure 5-1 QCA4004 Package Pinout

Table 5-1 provides the signal-to-pin relationship information for the QCA4004.

Table 5-1 Signal to Pin Relationships and Descriptions

Signal Name	Pin	Type	Description
General			
EXT_CLK_OUT	43	O	External clock out: 40 or 26 MHz; its corresponding half rate is available when configured.
XTALI	45	I/O	Supports 40 MHz or 26 MHz crystal. When an external reference clock is used, connect the clock signal to the XTALO pin and ground the XTALI pin.
XTALO	44	I	
Radio			
CHIP_PWD_L	14	I	Chip power-down control

Table 5-1 Signal to Pin Relationships and Descriptions (cont.)

Signal Name	Pin	Type	Description
RFIN2N1	55	IA	The first differential RF inputs
RFIN2P1	54	IA	
RFIN5N1	57	IA	
RFIN5P1	58	IA	
RFOUT2N1	60	OA	The first differential RF outputs
RFOUT2P1	59	OA	
RFOUT5N1	62	OA	
RFOUT5P1	63	OA	
RFIN2P1_ANT2	53	IA	The second differential RF inputs for 2.4 GHz Rx/LNA diversity using two antennas; can be left open if not in use
RFIN2N1_ANT2	52	IA	
Analog Interface			
XPABIAS2	51	OA	Bias for optional external power amplifier in 2.4 GHz
XPABIAS5	50	OA	Bias for optional external power amplifier in 5 GHz
External Switch Control			
ANTA	42	O	External RF switch control
ANTB	41	O	
ANTC	40	O	
ANTD	39	O	
USB			
USB_DPOS	19	IA/OA	USB D+ signal; carries USB data to and from the USB 2.0 PHY
USB_DNEG	20	IA/OA	USB D- signal; carries USB data to and from the USB 2.0 PHY
Internal Switching Regulator			
SREG_OUT	12	P	1.2 V regulator output, connect to a 470 pF bypass capacitor on the board
SWREG_OUT	16	P	Output of the switching regulator to an LC filter or the LDO
SWREG_IN	17	P	3.3 V input to the internal switching regulator or LDO
Wakeup Manager			
IOT_MODE_EN	64	I	Power island isolation setting. This pin should be tied to the VBATT_3P3 signal. When this pin is low, the internal signal connections between pins 23 through 28 are isolated from rest of the chip. When this pin is high, internal connections are enabled, and pins 23 through 28 can be used.
32K_OSC_IN	24	IA	32 KHz crystal oscillator input
32K_OSC_OUT	25	OA	32 KHz crystal oscillator output
PWRDWN_OUT_L	26	O	Suspend Control signal. This pin is driven low by the QCA4004 when the wakeup manager power island is requesting a power down of the top level power island (SUSPEND state). This pin is driven high by the QCA4004 when the wakeup manager power island is requesting a resume to active to the top level power island.

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Table 5-1 Signal to Pin Relationships and Descriptions (cont.)

Signal Name	Pin	Type	Description
WAKEUP_L	27	I	Wakeup Control. While in SUSPEND state, the QCA4004 monitors this pin, and if a falling edge or rising edge is detected, the resume from SUSPEND sequence is started.
GPIO			
GPIO0	11	I/O	General purpose input/output. The QCA4004 supports a USB interface as well as an RGMII interface. The QCA4004 can be configured to support any of these interfaces by tying certain inputs externally. See Interface Selection by GPIO Bootstrap Pins (GPIO0-GPIO5) for more information on GPIOs and interface options.
GPIO1	10	I/O	
GPIO2	9	I/O	
GPIO3	8	I/O	
GPIO4	7	I/O	
GPIO5	6	I/O	
GPIO6	5	I/O	
GPIO7	4	I/O	
GPIO8	3	I/O	
GPIO9	2	I/O	
GPIO10	68	I/O	
GPIO11	67	I/O	
GPIO12	66	I/O	
GPIO13	65	I/O	
GPIO15	37	I/O	
GPIO16	36	I/O	
GPIO17	35	I/O	
GPIO18	33	I/O	
GPIO19	32	I/O	
GPIO20	31	I/O	
GPIO21	30	I/O	
GPIO31	28	I/O	
DVDD12	1, 21, 34	P	Digital 1.2 V power supply, should be connected to the SWREG_FB pin.
SWREG_FB_ DVDD12	15	P	Reference feedback voltage to the internal switching regulator or LDO
VBATT_3P3	22	P	Connect to 3.3 V host IO supply
VDD_1P8_OUT	23	P	1.8 V LDO output, connect to a > 1 µF bypass capacitor on the board
VDD12_BB_PLL	47	P	Analog 1.2 V power supply, should be connected to the SWREG_FB pin.
VDD12_RF1	56	P	
VDD12_SYNTH	48	P	

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Table 5-1 Signal to Pin Relationships and Descriptions (cont.)

Signal Name	Pin	Type	Description
VDD33_ANT	38	P	Analog 3.3 V power supply
VDD33_RF1	61	P	
VDD33_PLL_XTAL	46	P	
VDD33_SYNTH	49	P	
VDD33_USB	18	P	
VDDIO_HOST	13	P	Connect to 3.3 V host IO supply
VDDIO_GPIO	29	P	Connect to 3.3 V host IO supply or 1.8 V peripheral IO supply
Ground			
GND	–	P	Exposed ground pad (Package Dimensions)

Interface Selection

The QCA4004 supports multiple interfaces including SPI, I^2S, I^2C, UART, debug UART, and JTAG. It is possible to configure the QCA4004 to support these interfaces by connecting certain inputs externally. See section 3.5 for information on bootstrap modes and pins.

Table 5-2 and Table 5-3 illustrate examples interface selection by GPIO bootstrap pins.

Table 5-2 Interface Selection by GPIO Bootstrap Pins (GPIO0-GPIO5)

GPIO	Bootstrap [GPIO2, GPIO0]=01 SPI Function Enabled	Bootstrap [GPIO2, GPIO0]=00 USB Function Enabled
GPIO0	SPI_CS	GPIO0
GPIO1	SPI_MOSI	GPIO1/I2S_BCLK1
GPIO2	GPIO/LED	GPIO2/I2S_SDI1
GPIO3	SPI_INT	GPIO3/I2S_SDO1
GPIO4	SPI_MISO	GPIO4/I2S_WS1
GPIO5	SPI_CLK	GPIO5/I2S_MCLK1

Table 5-3 Interface Selection by Firmware Configuration

GPIO	Alternate Function	Alternate Function	Alternate Function	Alternate Function
GPIO6	GPIO6	–	I2C_DATA	TDI
GPIO7	GPIO7	UART0_TXD	–	–
GPIO8	GPIO8	UART0_RTS	–	–
GPIO9	GPIO9	UART0_CTS	–	–
GPIO10	GPIO10	UART1_RXD	I2S0_MCK	TMS
GPIO11	GPIO11	UART1_TXD	I2S0_BCK	TM
GPIO12	GPIO12	–	I2C_CLK	TCK

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Table 5-3 Interface Selection by Firmware Configuration

GPIO	Alternate Function	Alternate Function	Alternate Function	Alternate Function
GPIO13	GPIO13	–	–	TDO
GPIO15	GPIO15	UART0_RXD	–	–
GPIO16	GPIO16	–	–	–
GPIO17	GPIO17	–	–	–
GPIO18	GPIO18	–	–	–
GPIO19	GPIO19	–	I2S0_SDI	–
GPIO20	GPIO20	–	I2S0_SDO	–
GPIO21	GPIO21	–	I2S0_WS	TRST
GPIO30	GPIO30	WAKEUP	–	–
GPIO31	GPIO31	–	–	–

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6 Package Dimensions

The QCA4004 is packaged in a QFN package. The body size is 8 mm by 8 mm. The package drawings and dimensions are provided in Figure 6-1 and Table 6-1.

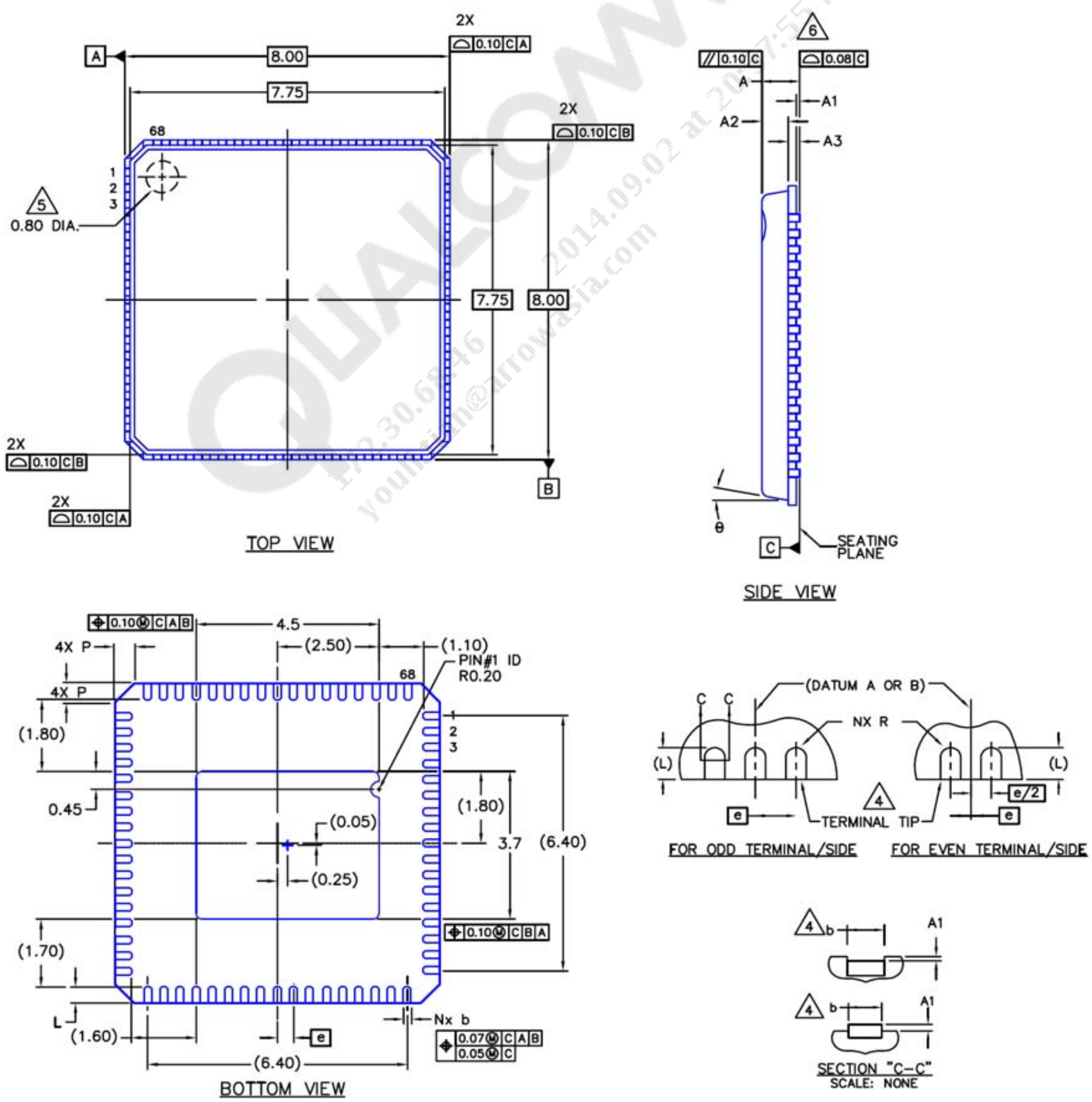

Figure 6-1 QCA4004 Package Drawing

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Table 6-1 Package Dimensions

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	0.80	0.85	0.90	mm	0.315	0.335	0.354	inches
A1	0.00	0.01	0.05	mm	0.000	0.001	0.002	inches
A2	0.60	0.65	0.70	mm	0.236	0.256	0.276	inches
A3	0.20 REF			mm	0.008 REF			inches
θ	0	—	12	°	0	—	12	°
P	0.24	0.42	0.60	mm	0.094	0.165	0.236	inches
e	0.40 BSC			mm	0.157 BSC			inches
L	0.30	0.40	0.50	mm	0.118	0.157	0.197	inches
b	0.15	0.20	0.25	mm	0.059	0.079	0.098	inches

1. Controlling dimension: Millimeters
2. Reference document: 483287PO

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7 Ordering Information

The order number QCA4004X-AL3A specifies a lead-free halogen-free standard-temperature version of the QCA4004.

The ordering number QCA4004X-AL3B specifies a lead-free halogen-free industrial-temperature version of the QCA4004.

The order number QCA4004X-BL3A specifies a lead-free halogen-free standard-temperature version of the QCA4004.

The ordering number QCA4004X-BL3B specifies a lead-free halogen-free industrial-temperature version of the QCA4004.

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8 Part Reliability

8.1 Reliability qualifications summary

Table 8-1 QCA4004 reliability evaluation

Reliability tests, standards, and conditions	Sample # Lots	Result	Assembly1	Assembly2
Average failure rate (AFR) in FIT (λ) **Failure in billion device-hours** Functional HTOL: JESD22-A108	231 3 lots	λ = 20 FIT	–	–
ESD – (HBM) human body model rating JESD22-A114-B	3	Pass ±2000 V, all pins	–	–
ESD – (CDM) charge device model rating JESD22-C101-C	3	Pass ±500 V, all pins except RFIN2P1 and RFIN2N1 pass ±400 V	–	–
Latch-up (Overcurrent test): EIA/JESD78 Trigger current: ±200 mA; temperature: 25°C	6 1 lot	Pass	–	–
Latch-up (Overvoltage test): EIA/JESD78 Trigger voltage: 1.6 x Vnom; temperature: 25°C	6 1 lot	Pass	–	–
High Temperature Storage Life (HTSL) JESD-22 A104, -50 to +150°C, 1000 hrs	462 3 + 3 lots	–	Pass	Pass
Moisture/Reflow Sensitivity Classification: MSL3; JSTD-020D, (30C/60% RH, 192 hrs, 3 x IR @ 260°C)	1078 3 + 3 lots	–	Pass	Pass
Temperature cycle: JESD22-A104 Temperature: -65 to +150 °C Number of cycles: 1000 Min soak time at min/max temperature: 5 minutes Cycle rate: 2 cycles per hour (cph) **Prerequisite:** All samples subjected to preconditioning MSL 3 and reflow (260°C) 3X prior to TC	462 3 + 3 lots	–	Pass	Pass
Highly accelerated stress test, unbiased (HAST) JESD22-A118 **Prerequisite**: All samples subjected to preconditioning MSL 3 and reflow (260°C) 3X prior to HAST	474 3 + 3 lots	–	Pass	Pass

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Table 8-1 QCA4004 reliability evaluation

Reliability tests, standards, and conditions	Sample # Lots	Result	Assembly1	Assembly2
Highly accelerated stress test, biased (bHAST) JESD22-A118 **Prerequisite**: All samples subjected to preconditioning MSL 3 and reflow (260°C) 3X prior to HAST	158 1 + 1 lots	–	Pass	Pass
Die shear (5 kg)	5	–	Pass	Pass

8.2 Qualification sample description

- Device name: QCA4004
- Package type: QFN 68L
- Package body size: 8 mm × 8 mm × 0.85 mm
- Lead count: 68
- Lead pitch: 0.4 mm

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