# Exhibit 11

**SECTION 2.1033(c) (16) DETAILED DESCRIPTION OF THE MODULATION SYSTEM**

**SECTION 2.1033(c) (16)**

For equipment employing digital modulation techniques, a detailed description of the modulation system to be use, including response characteristics of any filters provided, and a description of the modulating wave train, shall be submitted for the maximum rated conditions under which the equipment will be operated.

**Response**

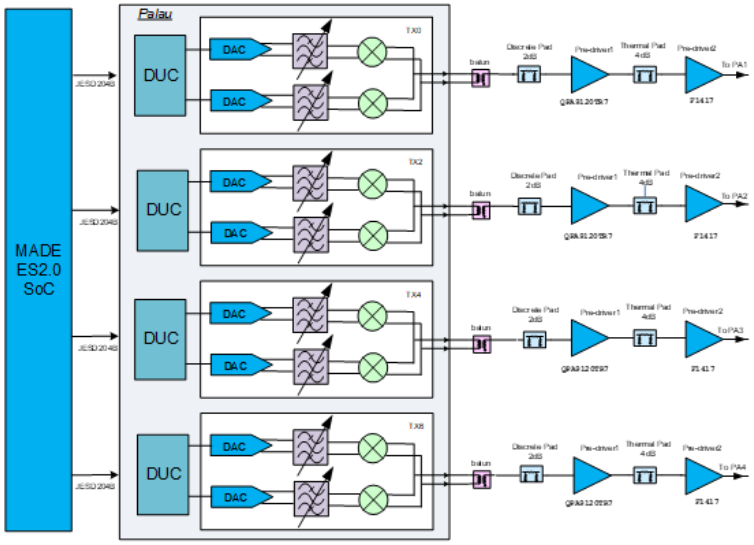
The Nokia (AWHQU) supports NR and LTE radio access technology. A Made chip are used as DFE to support 4 TRX. DUC/DDC/CFR/DPD are al integrated Made. L1-low function such as FFT/IFFT is also integrated in Made to provide less data transmission rate.

ADI RFIC is used as transceiver component, to provide analog TRX path for signal chain. It converts digital I/Q-data to RF frequency and then up-converted to CBRS B48 frequency band in the range of 3550-3700MHz. RFIC can support 4 TRX and 1 Feedback, with dedicated FB function to calibration LO leakage and IQ imbalance.

A PA (power amplifier) is used to provide final output of each TX path. The PAR for LTE or NR one carrier should be 7.8dB@0.01%. For 150M IBW, possible to be 8.3dB@0.01%. A cavity filter is used to implement the tight requirement of spurious emission for B48 band (3550~3700MHz).

A SoC chip (Made2) provides all the digital processing for the downlink path and then presents them to the transceiver IC. It converts digital I/Q-data to RF frequency and then up-converted to CBRS B48 frequency band in the range of 3550-3700MHz.

The transmitter chain RRH Radio block diagram is provided below.




The SoC performs channel filtering with a series of filters and signal conditioning stages. The overall response incorporates the necessary amplitude and phase equalization to meet the requirements of the 3GPP NR and LTE standards.

Digital Pre-distortion performs amplitude sensitive adjustments to the signal in anticipation of power- amplifier non-linearity distortions and cancels out the distortion effects of the power amplifier. The ACL block detects if the average power exceeds a set threshold and adjusts the power of the output signal. The Digital Gain Compensation block dynamically measures the DC offset and DC gain contained in the signal and autonomously removes them. The Equalization block anticipates RF path propagation distortions and eliminates them with adjustments to the signal.

The SoC also includes a peak limiting block, which removes samples above a predetermined threshold without detrimental effects on the EVM (Error Vector Magnitude) metric. This enables the peaks of the baseband signal to be limited to obtain the desired peak to average ratio (PAR) in the output waveform. The overall response achieves pulse shaping and equalization which meets the transmitted signal Rho and EVM requirements when demodulated with the appropriate matched filter (e.g., in test equipment).