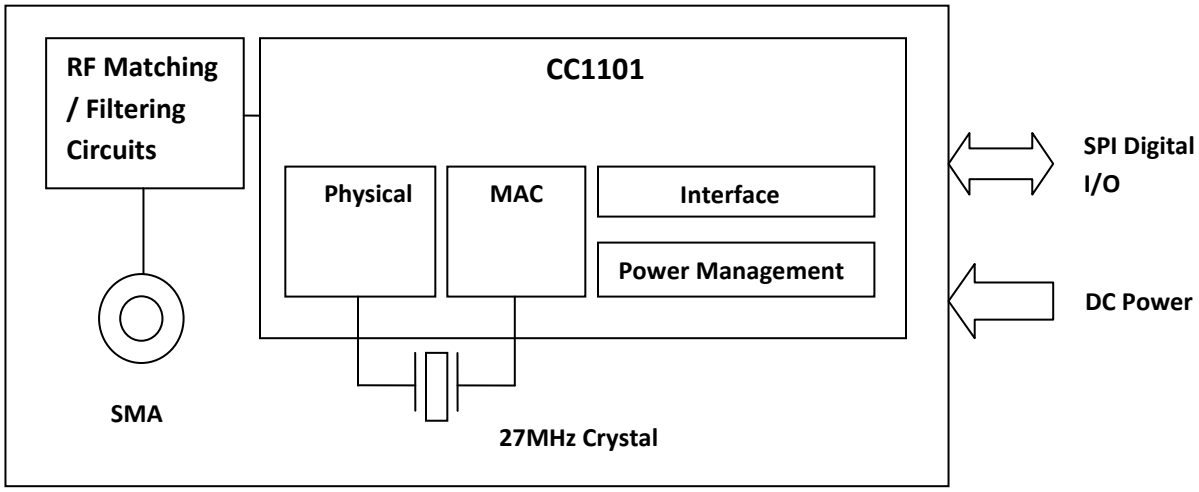
PN17TR 915Mhz Transceiver Module

1 Block Diagram



PN17TR 915MHz Transceiver block diagram

2 General Description

The PN17TR module is a low power single-chip CC1101 radio transceiver for the 915MHz ISM band. The transceiver consists of a fully integrated frequency synthesizer, a power amplifier, receiver chain with demodulator, a crystal oscillator and a modulator. It provides extensive hardware support for packet handling, data buffering, burst transmissions, clear channel assessment, link quality indication, and wake-on-radio. The main operating parameters and 64-byte transmit/receive FIFOs of the module can be controlled via an SPI interface.

Current consumption is very low in receive mode 15.7mA, 1.2kBaud and 200nA sleep mode. Fast start time, 240 µs from sleep to Rx or Tx mode.

The PN17TR module is designed and made for WiLAS series products not for sale on public or other manufacture host products.

3 Transceiver State Diagram

After initial setup of registers for desired behavior, the normal operation flow diagram is shown as follows. In applications of infrequent data transmissions the transceiver would be in "sleep" mode to save power (400nA). From there it would be woken up and enter "idle" mode. As part of the wake up process the crystal oscillator is started (~240µS) and the digital microcontroller interface is powered up. Before transmit or receive the frequency synthesizer needs to be started ("FS Wakeup") and having been powered off (or idle for a while) the control loop of the VCO/PLL needs to be calibrated ("calibrate").

A data frame is loaded into the transmit FIFO and the "TX" mode is entered. The transceiver will transmit the data and enter "idle" mode after completion. When transmit is complete "RX" mode is entered to wait for the acknowledge frame. Once a frame is received the transceiver will again enter "idle" mode. If no acknowledge frame is received within a given timeout the data frame would be transmitted. After the last data has successfully been transmitted the transceiver would again be put in "sleep" mode.

4 Hardware specification

General conditions (Vin = 3.3 V and 25°C

Absolute Maximum Ratings

Rating	Min.	Typ.	Max.	Unit
Storage temperature range	-50		150	°C
Supply voltage, Vin	-0.3		3.9	V
I/O pin voltage	-0.3		3.9	V
RF saturation input power			+10	+dBm

Recommended Operating conditions

Parameter	Min.	Max.	Unit	Condition
Operating temperature	-40	85	°C	
Operating supply voltage	1.8	3.6	V	All supply pins must have the same voltage
Centre Frequency range	915	915	MHz	Single channel certified, must not modify
Data rate	1	500	kBaud	2-FSK

PN17TR 915 module current consumption

Ta = 25°C, VDD = 3.0V if nothing else stated.

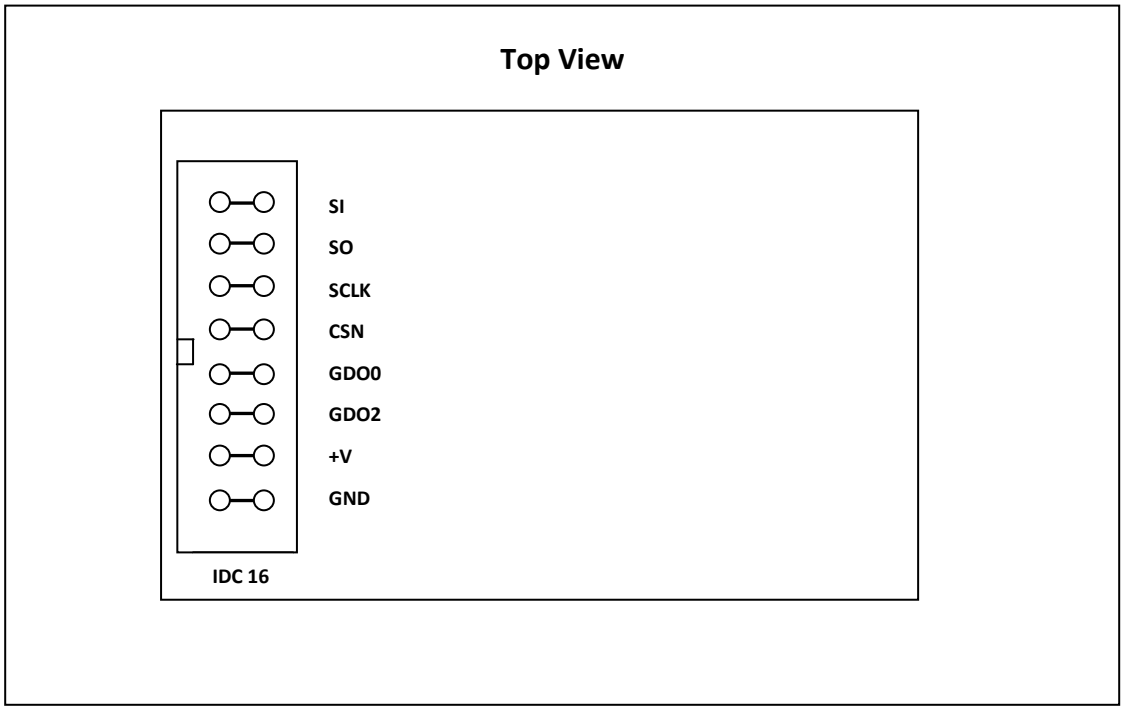
Parameter	Typ	Max	Unit	Condition
Current consumption in power down modes	0.2	1	µA	Voltage regulator to digital part off, register values retained (SLEEP state). All GDO pins programmed to 0x2F (HW to 0)
	0.5		µA	Voltage regulator to digital part off, register values retained, lowpowerRC oscillator running (SLEEP state with WOR enabled)
	100		µA	Voltage regulator to digital part off, register values retained, XOSC running (SLEEP state with MCSM0.OSC_FORCE_ON set)
	165		µA	Voltage regulator to digital part on, all other modules in power down (XOFF state)
Current consumption 915MHz	15.7		mA	Receive mode, 1.2 kBaud
	15.6		mA	Receive mode, 38.4 kBaud
	16.9		mA	Receive mode, 250 kBaud
	33.4		mA	Transmit mode, +11 dBm output power
	17.2		mA	Transmit mode, 0 dBm output power
	17.0		mA	Transmit mode, –6 dBm output power

4.1 Module RF compliance limits

The RF compliance limits are those tested for FCC certification are not allowed to exceed.

Modulation	Standards	Parameter	Max	Unit
2-FSK	FCC Part 15.207 FCC Part 15.247	Data rate	500	Kpbs
		Output power	+11.6	dBm

4.2 Pin connections

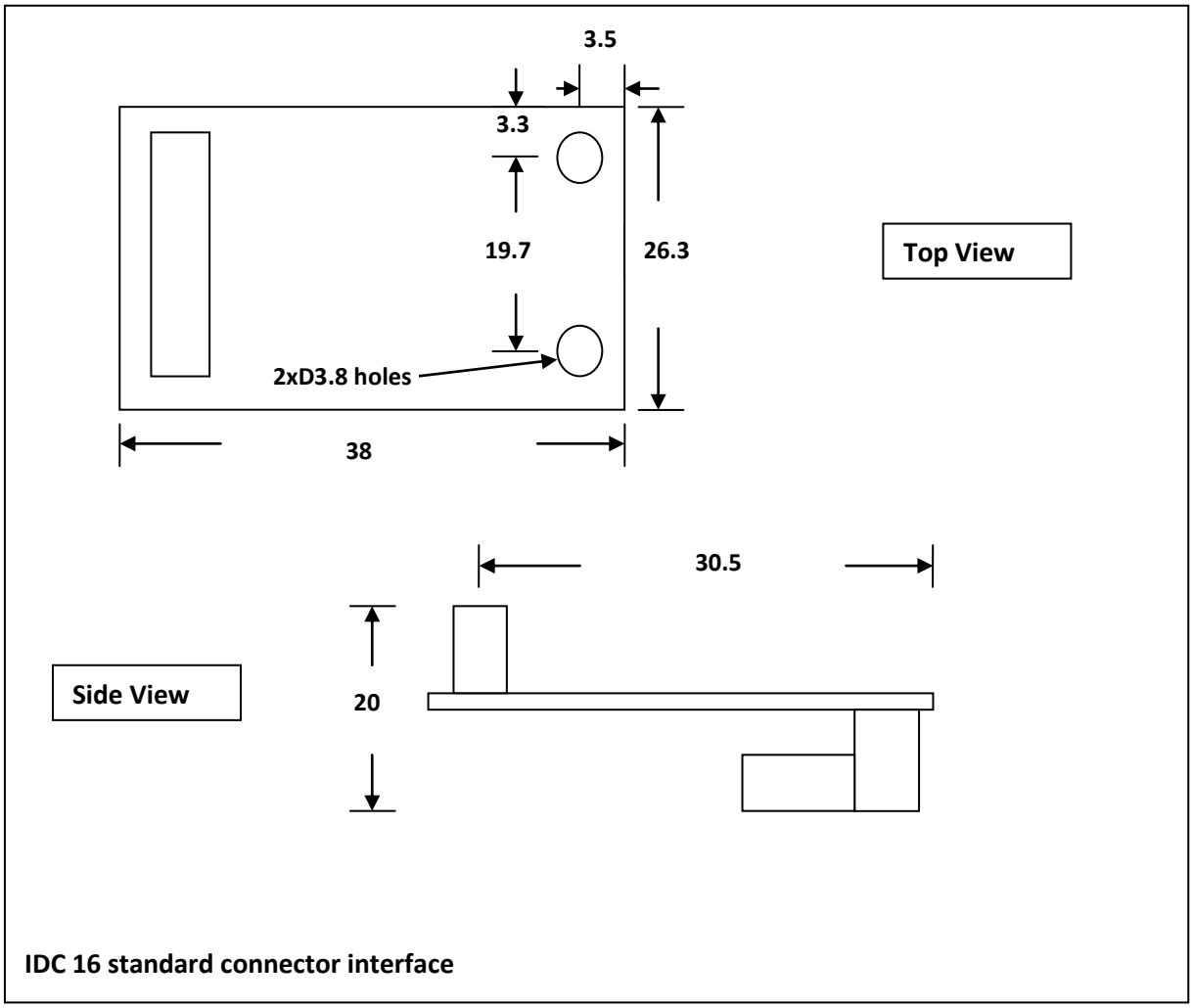


Pin numbering

Pin #	Pin name	Pin type	Description
1,2	SI	Digital input	Serial configuration interface, data input
3,4	SO	Digital output	Serial configuration interface, data output
5,6	SCLK	Digital input	Serial configuration interface, clock input
7,8	CSN	Digital input	Serial configuration interface, chip select

9,10	GDO0	Digital I/O	Digital output pin for general use
11,12	GDO2	Digital output	Digital output pin for general use
13,14	VDD	Power (Digital)	+3.6V DC input
15,16	GND	Ground (Digital)	Ground connection

5 Mechanical dimensions



IDC 16 standard connector interface

6 Module user firmware

6.1 CC1101 configuration:

Warning: Configuration settings of CC1101 chip are restricted to settings which have passed certification testing. Deviation from mandatory setting ranges violates module compliance.

Restricted settings detailed below.

Note: Other register values are essential to valid RX and basic operation, but are not listed in document due to IP confidentiality. Full list of recommended values is available in LibPN17TR software library with licensed use of the module. Other values do not impact Transmit behavior as certified and can be adjusted to suit application.

Restricted Settings

Registers	Address	Description
SMARTRF_SETTING_CHANNR	0x00	Mandatory value
SMARTRF_SETTING_FSCTRL1	0x06	Mandatory value
SMARTRF_SETTING_FSCTRL0	0x00	Mandatory value
SMARTRF_SETTING_FREQ2	0x21	Mandatory value
SMARTRF_SETTING_FREQ1	0xE3	Mandatory value
SMARTRF_SETTING_FREQ0	0x8E	Mandatory value
SMARTRF_SETTING_MDMCFG4	0x2A	Mandatory value
SMARTRF_SETTING_MDMCFG3	0x75	Mandatory value
SMARTRF_SETTING_MDMCFG2	0x03	Bits 6,5,4 mandatory
SMARTRF_SETTING_MDMCFG0	0xE4	Mandatory value
SMARTRF_SETTING_FREND0	0x10	Bits 5,4 mandatory
PA Power	0xC5	Restricted setting, lower power settings ok

LibPN17TR software library:

LibPN17TR is a C software code library facilitating usage of the PN17TR module. Usage is not mandatory for compliant operation, but usage is recommended for simplified interface. Reference to config table header file is essential to tune module to optimal settings.

Software package is available under license from Inventis Technology and is included with authorized development with the module.

6.2 Library functions brief:

cc1101_setup_38_4k_915_wide3.h - Configuration table values

void cc1101_coms_open(void) – Establish link with CC1101

void cc1101_coms_close(void) – Terminate link with CC1101

void cc1101_read(Uint8* buffer, Uint8 size) – Read RX data from CC1101

void cc1101_write(Uint8* buffer, Uint8 size) – Write to config or TX buffer

Uint8 cc1101_strobe(Uint8 data) – Send strobe command to CC1101

void cc1101_mode(Uint8 mode) – Select mode (powerdown, sleep, tx, rx etc)

void cc1101_configure(void) – Load configuration table

Uint8 cc1101ConfigTest(Uint8 option) – Readback verification of configuration

Uint8 cc1101_read_reg(Uint8 addr) – Read single value

void cc1101_cca(Uint8 mode) – Toggle Clear Channel Assessment

void cc1101_close_in(Uint8 level) – Configure for reduced power TX

void cc1101_desensitised_rx(void) – Configure for reduced RX sensitivity

void cc1101_pa_power(Uint8 level) – Configure PA Power. Restriction on max power allowed!

Uint8 rf_transmit(Uint8* buffer, Uint8 bytes, Uint8 options) – Perform TX operation

Uint8 rf_recieve_loop(Uint8* buffer, Uint8 bytes, Uint8 options, Uint8 timeout) – Perform RX operation

6.3 CC1101 Configuration Register descriptions:

For more firmware information, please refer to CC1101 datasheet.

Command strobe

Address	Strobe Name	Description
0x30	SRES	0x30 SRES Reset chip.
0x31	SFSTXON	Enable and calibrate frequency synthesizer (if MCSM0.FS_AUTOCAL=1). If in RX (with CCA):Go to a wait state where only the synthesizer is running (for quick RX / TX turnaround).
0x32	SXOFF	Turn off crystal oscillator.
0x33	SCAL	Calibrate frequency synthesizer and turn it off. SCAL can be strobed from IDLE mode without setting manual calibration mode (MCSM0.FS_AUTOCAL=0)
0x34	SRX	Enable RX. Perform calibration first if coming from IDLE and MCSM0.FS_AUTOCAL=1.
0x35	STX	In IDLE state: Enable TX. Perform calibration first if MCSM0.FS_AUTOCAL=1. If in RX state and CCA is enabled: Only go to TX if channel is clear.
0x36	SIDLE	Exit RX / TX, turn off frequency synthesizer and exit Wake-On-Radio mode if applicable.
0x38	SWOR	Start automatic RX polling sequence (Wake-on-Radio) as described in Section 19.5 if WORCTRL.RC_PD=0.
0x39	SPWD	Enter power down mode when CSn goes high.
0x3A	SFRX	Flush the RX FIFO buffer. Only issue SFRX in IDLE or RXFIFO_OVERFLOW states.
0x3B	SFTX	Flush the TX FIFO buffer. Only issue SFTX in IDLE or TXFIFO_UNDERFLOW states.
0x3C	SWORRST	Reset real time clock to Event1 value.
0x3D	SNOP	No operation. May be used to get access to the chip status byte.

Configuration Registers overview

Address	Register	Description	Preserved in SLEEP state
0x00	IOCFG2	GDO2 output pin configuration	YES
0x01	IOCFG1	GDO1 output pin configuration	YES
0x02	IOCFG0	GDO0 output pin configuration	YES
0x03	FIFOTHR	RX FIFO and TX FIFO thresholds	YES
0x04	SYNC1	Sync word, high byte	YES
0x05	SYNC0	Sync word, low byte	YES
0x06	PKTLEN	Packet length	YES
0x07	PKTCTRL1	Packet automation control	YES
0x08	PKTCTRL0	Packet automation control	YES
0x09	ADDR	Device address	YES
0x0A	CHANNR	Channel number	YES
0x0B	FSCCTRL1	Frequency synthesizer control	YES
0x0C	FSCCTRL0	Frequency synthesizer control	YES
0x0D	FREQ2	Frequency control word, high byte	YES
0x0E	FREQ1	Frequency control word, middle byte	YES

0x0F	FREQ0	Frequency control word, low byte	YES
0x10	MDMCFG4	Modem configuration	YES
0X11	MDMCFG3	Modem configuration	YES
0X12	MDMCFG2	Modem configuration	YES
0X13	MDMCFG1	Modem configuration	YES
0X14	MDMCFG0	Modem configuration	YES
0X15	DEVIATN	Modem deviation setting	YES
0X16	MCSM2	Main Radio Control State Machine configuration	YES
0X17	MCSM1	Main Radio Control State Machine configuration	YES
0X18	MCSM0	Main Radio Control State Machine configuration	YES
0X19	FOCCFG	Frequency Offset Compensation configuration	YES
0X1A	BSCFG	Bit Synchronization configuration	YES
0X1B	AGCTRL2	AGC control	YES
0X1C	AGCTRL1	AGC control	YES
0X1D	AGCTRL0	AGC control	YES
0X1E	WOREVT1	High byte Event 0 timeout	YES
0X1F	WOREVT0	Low byte Event 0 timeout	YES
0X20	WORCTRL	Wake On Radio control	YES
0X21	FREND1	Front end RX configuration	YES
0X22	FREND0	Front end TX configuration	YES
0X23	FSCAL3	Frequency synthesizer calibration	YES
0X24	FSCAL2	Frequency synthesizer calibration	YES
0X25	FSCAL1	Frequency synthesizer calibration	YES
0X26	FSCAL0	Frequency synthesizer calibration	YES
0X27	RCCTRL1	RC oscillator configuration	YES
0X28	RCCTRL0	RC oscillator configuration	YES
0X29	FSTEST	Frequency synthesizer calibration control	No
0X2A	PTEST	Production test	No
0X2B	AGCTEST	AGC test	No
0X2C	TEST2	Various test settings	No
0X2D	TEST1	Various test settings	No
0X2E	TEST0	Various test settings	No

Status Registers Overview

Address	Register	Description
0x30(0xF0)	PARTNUM	Part number for CC1101
0x31(0xF1)	VERSION	Current version number
0X32(0xF2)	FREQEST	Frequency Offset Estimate
0X33(0xF3)	LQI	Demodulator estimate for Link Quality
0X34(0xF4)	RSSI	Received signal strength indication
0X35(0xF5)	MARCSTATE	Control state machine state
0X36(0xF6)	WORTIME1	High byte of WOR timer
0X37(0xF7)	WORTIME0	Low byte of WOR timer
0X38(0xF8)	PKTSTATUS	Current GDOx status and packet status
0X39(0xF9)	VCO_VC_DAC	Current setting from PLL calibration module
0X3A(0xFA)	TXBYTES	Underflow and number of bytes in the TX FIFO
0X3B(0xFB)	RXBYTES	Overflow and number of bytes in the RX

		FIFO
0X3C(0xFC)	RCCTRL1_STATUS	Last RC oscillator calibration result
0X3D(0xFD)	RCCTRL0_STATUS	Last RC oscillator calibration result

0x00: IOCFG2 – GDO2 Output Pin Configuration

Bit	Field Name	Reset	R/W	Description
7			R0	Not used
6	GDO2_INV	0	R/W	Invert output, i.e. select active low (1) / high (0)
5:0	GDO2_CFG[5:0]	41 (0x29)	R/W	Default is CHP_RDYn

0x02: IOCFG0 – GDO0 Output Pin Configuration

Bit	Field Name	Reset	R/W	Description
7	TEMP_SENSOR_ENABLE	0	R/W	Enable analog temperature sensor. Write 0 in all other register bits when using temperature sensor.
6	GDO0_INV	0	R/W	Invert output, i.e. select active low (1) / high (0)
5:0	GDO0_CFG[5:0]	63 (0x3F)	R/W	Default is CLK_XOSC/192 (See Table 41 on page 62). It is recommended to disable the clock output in initialization, in order to optimize RF performance.

0x03: FIFOTHR – RX FIFO and TX FIFO Thresholds

Bit	Field Name	Reset	R/W	Description
7		0		Reserved , write 0 for compatibility with possible future extensions
6	ADC_RETENTION	0		0: TEST1 = 0x31 and TEST2= 0x88 when waking up from SLEEP 1: TEST1 = 0x35 and TEST2 = 0x81 when waking up from SLEEP Note that the changes in the TEST registers due to the ADC_RETENTION bit setting are only seen INTERNALLY in the analog part. The values read from the TEST registers when waking up from SLEEP mode will always be the reset value. The ADC_RETENTION bit should be set to 1before going into SLEEP mode if settings with an RX filter bandwidth below 325 kHz are wanted at time of wake-up.
5:4	CLOSE_IN_RX [1:0]	0 (00)		For more details, please see DN010 [8] Setting / RX Attention, Typical Values 0 (00) – 0 dB 1 (01) – 6 dB 2 (10) – 12 dB 3 (11) – 18 dB
3:0	FIFO_THR[3:0]	7 (0111)		Set the threshold for the TX FIFO and RX FIFO. The threshold is exceeded when the number of bytes in the FIFO is equal to or higher than the threshold value. Setting / Bytes in TX FIFO / Bytes in RX FIFO

				0 (0000)	61	4
				1 (0001)	57	8
				2 (0010)	53	12
				3 (0011)	49	16
				4 (0100)	45	20
				5 (0101)	41	24
				6 (0110)	37	28
				7 (0111)	33	32
				8 (1000)	29	36
				9 (1001)	25	40
				10 (1010)	21	44
				11 (1011)	17	48
				12 (1100)	13	52
				13 (1101)	9	56
				14 (1110)	5	60
				15 (1111)	1	64

0x04: SYNC1 – Sync Word, High Byte

Bit	Field Name	Reset	R/W	Description
7:0	SYNC[15:8]	211 (0xD3)	R/W	8 MSB of 16-bit sync word

0x05: SYNC0 – Sync Word, Low Byte

Bit	Field Name	Reset	R/W	Description
7:0	SYNC[7:0]	145 (0x91)	R/W	8 LSB of 16-bit sync word

0x06: PKTLEN – Packet Length

Bit	Field Name	Reset	R/W	Description
7:0	PACKET_LENGTH	255 (0xFF)	R/W	Indicates the packet length when fixed packet length mode is enabled. If variable packet length mode is used, this value indicates the maximum packet length allowed. This value must be different from 0.

0x07: PKTCTRL1 – Packet Automation Control

Bit	Field Name	Reset	R/W	Description
7:5	PQT[2:0]	0 (0x00)	R/W	Preamble quality estimator threshold. The preamble quality estimator increases an internal counter by one each time a bit is received that is different from the previous bit, and decreases the counter by 8 each time a bit is received that is the same as the last bit. A threshold of 4·PQT for this counter is used to gate sync word detection.When PQT=0 a sync word is always accepted.

4		0	R0	Not Used.
3	CRC_AUTOFLUSH	0	R/W	Enable automatic flush of RX FIFO when CRC is not OK. This requires that only one packet is in the RXIFIFO and that packet length is limited to theRX FIFO size.
2	APPEND_STATUS	1	R/W	When enabled, two status bytes will be appended to the payload of the packet. The status bytes contain RSSI and LQI values, as well as CRC OK.
1:0	ADR_CHK[1:0]	0 (00)	R/W	Controls address check configuration of received packages. Setting: 0 (00) — No address check 1 (01) — Address check, no broadcast 2 (10) — Address check and 0 (0x00) broadcast 3 (11) — Address check and 0 (0x00) and 255 (0xFF) broadcast

0x08: PKTCTRL0 – Packet Automation Control

Bit	Field Name	Reset	R/W	Description
7			R0	Not used
6	WHITE_DATA	1	R/W	Turn data whitening on / off 0: Whitening off 1: Whitening on
5:4	PKT_FORMAT[1:0]	0 (00)	R/W	Format of RX and TX data Setting: 0 (00) — Normal mode, use FIFOs for RX and TX 1 (01) — Synchronous serial mode, Data in on GDO0 and data out on either of the GDOx pins 2 (10) — Random TX mode; sends random data using PN9 generator. Used for test. Works as normal mode, setting 0 (00), in RX 3 (11) — Asynchronous serial mode, Data in on GDO0 and data out on either of the GDOx pins
3		0	R0	Not used
2	CRC_EN	1	R/W	1: CRC calculation in TX and CRC check in RX enabled 0: CRC disabled for TX and RX

1:0	LENGTH_CONFIG[1:0]	1 (01)	R/W	Configure the packet length Setting: Packet length configuration 0 (00): Fixed packet length mode. Length configured in PKTLEN register 1 (01): Variable packet length mode. Packet length configured by the first byte after sync word 2 (10): Infinite packet length mode 3 (11): Reserved

0x09: ADDR – Device Address

Bit	Field Name	Reset	R/W	Description
7:0	DEVICE_ADDR[7:0]	0 (0x00)	R/W	Address used for packet filtration. Optional broadcast addresses are 0 (0x00) and 255 (0xFF).

0x0A: CHANNR – Channel Number

Bit	Field Name	Reset	R/W	Description
7:0	CHAN[7:0]	0 (0x00)	R/W	The 8-bit unsigned channel number, which is multiplied by the channel spacing setting and added to the base frequency.

0x0B: FSCTRL1 – Frequency Synthesizer Control

Bit	Field Name	Reset	R/W	Description
7:6			R/0	Not used
5		0	R/W	Reserved
4:0	FREQ_IF[4:0]	15 (0x0F)	R/W	The desired IF frequency to employ in RX. Subtracted from FS base frequency in RX and controls the digital complex mixer in the demodulator. $f = f_{xdsc}/2^{10} - FREQ\_IF$ The default value gives an IF frequency of 381kHz, assuming a 26.0 MHz crystal.

0x0C: FSCTRL0 – Frequency Synthesizer Control

Bit	Field Name	Reset	R/W	Description
7:0	FREQOFF[7:0]	0 (0x00)	R/W	Frequency offset added to the base frequency before being used by the frequency synthesizer. (2s-complement). Resolution is $F_{XTAL}/2^{14}$ (1.59kHz-1.65kHz); range is ±202 kHz to ±210 kHz, dependent of XTAL frequency.

0x0D: FREQ2 – Frequency Control Word, High Byte

Bit	Field Name	Reset	R/W	Description
7:6	FREQ[23:22]	0 (00)	R	FREQ[23:22] is always 0 (the FREQ2 register is less than 36 with 26-27 MHz crystal)
5:0	FREQ[21:16]	30 (0x1E)	R/W	FREQ[23:0] is the base frequency for the frequency synthesiser in increments of $f_{XOSC}/2^{16}$. $f_{carrier} = f_{xosc}/2^{16}$ - FREQ[23:0]

0x0E: FREQ1 – Frequency Control Word, Middle Byte

Bit	Field Name	Reset	R/W	Description
7:0	FREQ[15:8]	196 (0xC4)	R/W	Ref. FREQ2 register

0x0F: FREQ0 – Frequency Control Word, Low Byte

Bit	Field Name	Reset	R/W	Description
7:0	FREQ[7:0]	236 (0xEC)	R/W	Ref. FREQ2 register

7 Regulatory compliance

7.1 RF Compliance

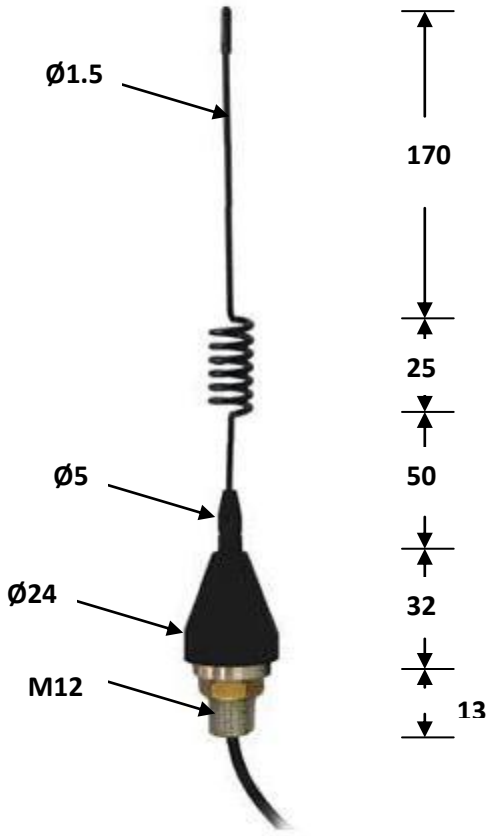
The RF certification obtained is described in the table below.

ID	Part	Comment
FCC ID	2ACT2-PN17TR	With External "ANT-915-06-03" antenna and RPSMA connector RF cable With External "W1063" antenna and RPSMA With Coil antenna "SW915-TH12"

7.2 Module approved antenna

External wireless Antenna part number "ANT-915-06-03" from Elecom Electronics Supply specification is below.

Items	Description
Frequency (MHz)	902 - 928
Bandwidth (MHz)	26
Gain (dBi)	5
Max. input power (W)	60
Input Impedance (Ω)	50
Polarization	Vertical
Size (mm)	Ø(Base) x 290 (Height)
Cable Length (m)	5m
Cable type	RG58
Connector	RPSMA
Mount	Screw
Housing	Black
Storage temperature (°C)	-45°C to +75°C
Operating temperature (°C)	-45°C to +75°C


Ø1.5
Ø5
Ø24
M12
170
25
50
32
13

External wireless antenna part number "W1063" from Pulse Electronics specification is below.

Features

- **Ideal for lower frequency wireless applications in the ISM 900 MHz band**
- **Omni-directional radiation pattern provides broad 360° coverage**
- **One-eighth wavelength dipole configuration**
- **Connection and color options easily integrate with OEM designs**
- **Black**

Connector

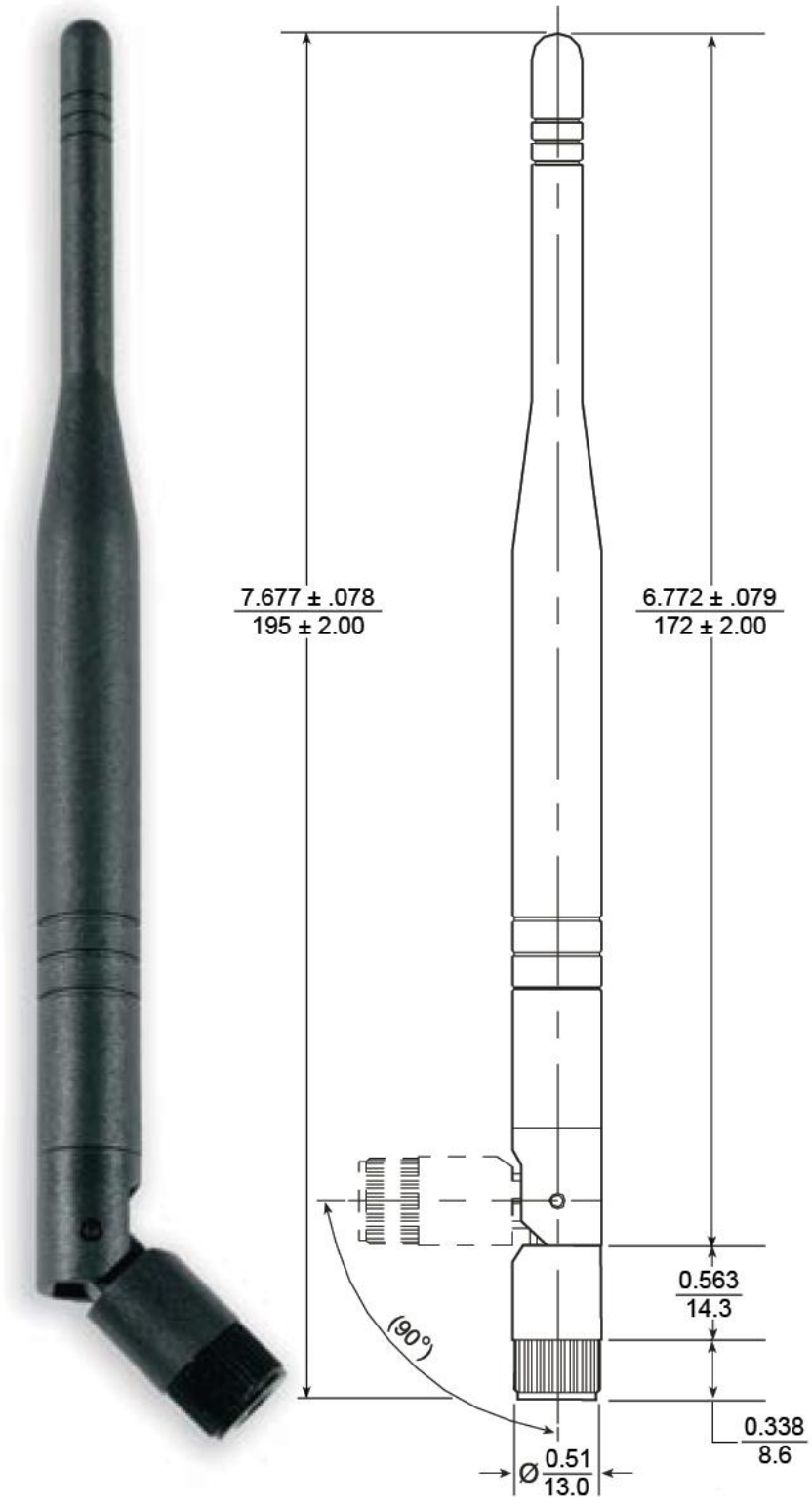
- **Reverse SMA Male**

Weight ---------- 25.6 grams
Carton ---------- 20/bag, 500/carton

Dimensions [in / mm]
Unless otherwise specified, all tolerances are ± .010 / 0.25

Electrical Specifications @ 25 ºC

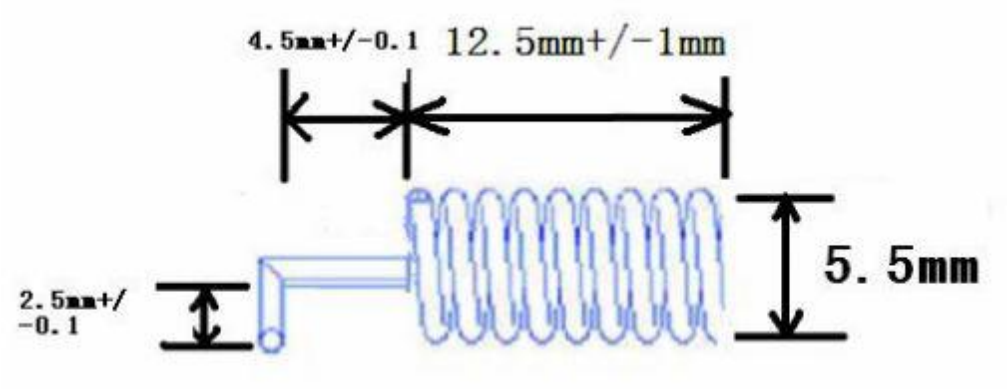
Part Number	Frequency [MHz]	Gain dBi	Impedance [Nom]	VSWR	Polarization	Radiation	colour
W1063	868 - 928	3.0	50	<2.5	Vertical	Omni	Black

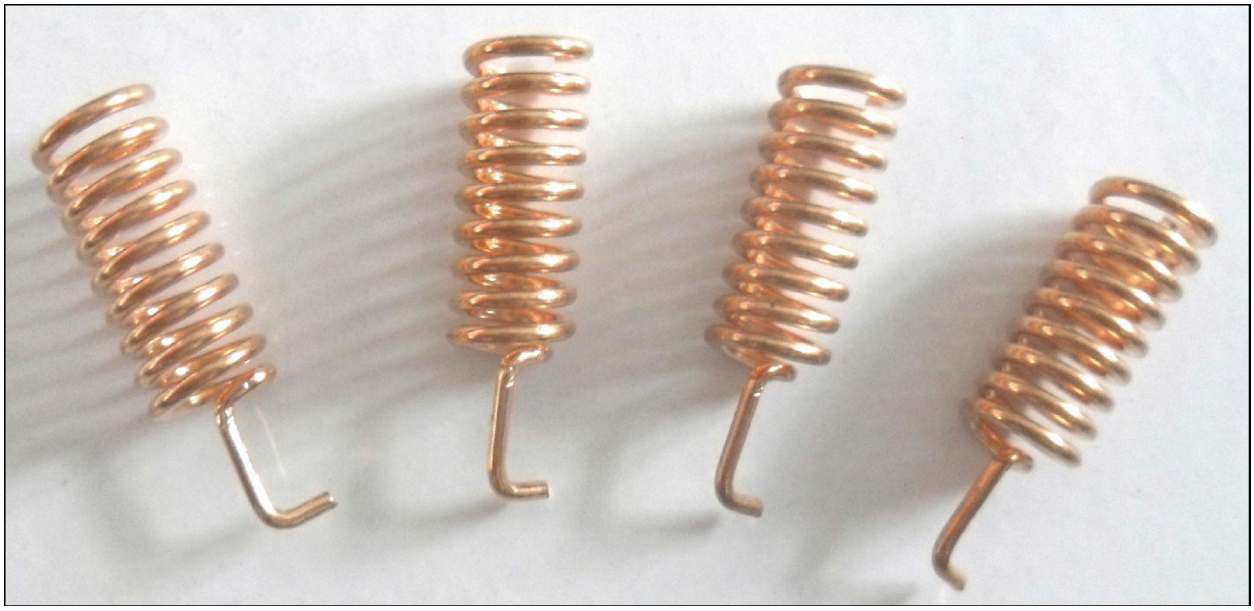

7.677 ± .078
195 ± 2.00
6.772 ± .079
172 ± 2.00
0.563
14.3
(90°)
0.338
8.6
Ø 0.51
13.0

Internal wireless Antenna part number "SW915-TH12" from NiceRF specification is below.

SW915–TH12 is a copper spring antenna. It is a dedicated antenna which designed for a wireless communication system (915MHz).It has good VSWR, small size, ingenious structure, easy installation, stable performance, with good anti-vibration and aging ability.

Features
Frequency range: 915 MHz (+ / -5)
VSWR: <= 1.5
Input impedance: 50 Ω
Maximum power: 5 W
Gain: 2.15 dBi
Weight: 1g
Height: 12.5 + / -1 mm (9T)
Antenna Color: Copper color
Interface Type: welded directly





8 FCC

8.1 Federal Communication Commission Interference Statement

PN17TR Transceiver Module has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This device generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this device does cause harmful interference to radio or television reception, which can be determined by turning the device off and on, the user is encouraged to try to correct the interference by one of the following measures:

. Reorient or relocate the receiving antenna.

. Increase the separation between the device and receiver.

. Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

. Consult the dealer or an experienced radio/TV technician for help.

WARNING: To assure continued compliance, any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

Limited single Modular approval, FCC

FCC ID: 2ACT2-PN17TR

IMPORTANT NOTE:

To comply with FCC RF exposure compliance requirements, the antenna used for this transmitter must be installed to provide a separation distance of at least 20cm from all persons and must not be collocated or operating in conjunction with any other antenna or transmitter." This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions (1) This device may not cause harmful interference and (2) This device must accept any interference received, including interference that may cause undesired operation.

In the event that these conditions can not be met (for example certain laptop configurations or collocation with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for reevaluating the end product (including the transmitter) and obtaining a separate FCC authorization. This device is intended only for OEM integrators under the following conditions:

The antenna must be installed such that 20 cm is maintained between the antenna and users. As long as a condition above is met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.). "

8.2 Labeling instructions

When integrating the PN17TR 915MHz Transceiver Module into the final product, ensure that the FCC and IC labeling requirements specified below are satisfied. Based on the Public Notice from FCC, the product into which the ST transmitter module is installed must display a label referring to the enclosed module. The label should use wording like the following:

Contains FCC ID: 2ACT2-PN17TR

Any similar wording that expresses the same meaning may also be used.