User Manual

EH-MA41

Brand Name:Ehong

FCC ID:2ACCRMA41

Description:

EH-MA41 is a class 2 Bluetooth® 3.0 module. It is a highly integrated and sophisticated module which contains all the necessary elements from radio to antenna and a fully implemented protocol stack. It is an ideal solution for integrating Bluetooth® into various products with limited knowledge of Bluetooth® and RF technologies.

With AT command stack firmware, designers can easily customize their applications to support different Bluetooth profiles, such as SPP, HID, HFP and etc.

And the module can also interface with Apple's Authentication Coprocessor and build an iAP over Bluetooth application.
Typical Bluetooth applications:

- Cable replacement
- Bar code and RFID scanners
- Measurement and monitoring systems
- Industrial sensors and controls
- Medical devices
- Industrial PCs and laptops

Features:

- Bluetooth V3.0
- TX power +5.18dbm, / -84dBm RX sensitivity
- Onboard Meander line PCB antenna support 10 meters
- Support sniff and deep sleep mode
- Supports master and slave
- Supports Bluetooth profiles SPP, iAP, HID
- UART and USB and data interfaces
- I^2C Master interface
- Support Apple iAP protocol
- PCM digital audio interfaces
- RoHS compliant

1. EH-MA41 Product numbering

EH-MA41-X-V1.0

A. EH ---------- Company Name(EHong)
B. MA41 ---------- Module Name
C. X ---------- N (no)
D. V ---------- Hardware revision

2. Pinout and Terminal Description

2.1.Pin Configuration

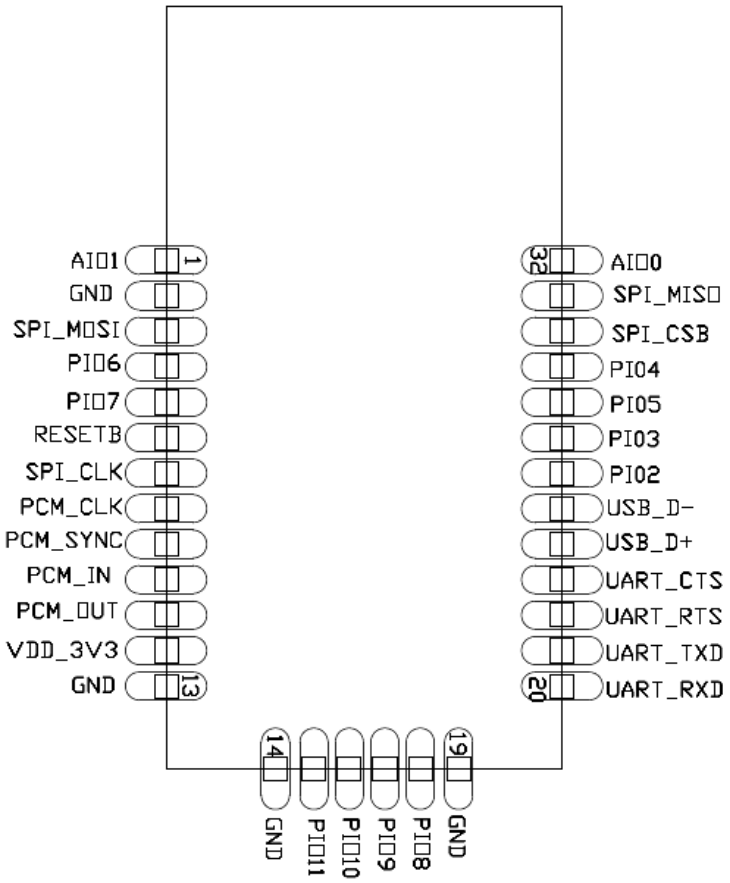

Figure 1： Pinout of EH-MA41

Pin	Symbol	I/O Type	Description
1	AIO1	Bi-directional	Programmable input/output line
2	GND	Ground	Ground

3	SPI_MOSI	CMOS input, with weak internal pull-down	Serial Peripheral Interface data input
4	PIO6	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
5	PIO7	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
6	RESETB	CMOS input with weak internal pull-up	Reset if low. Input denounced so must be low for >5ms to cause a reset
7	SPI_CLK	input with weak internal pull-down	Serial Peripheral Interface clock
8	PCM_CLK	Bi-directional with weak internal pull-down	Synchronous Data Clock
9	PCM_SYNC	Bi-directional with weak internal pull-down	Synchronous Data Sync
10	PCM_IN	CMOS Input, with weak internal pull-down	Synchronous Data Input
11	PCM_OUT	CMOS output, tristate, with weak internal pull-down	Synchronous Data Output
12	VDD_3V3	3V3 power input	3V3 power input
13	GND	Ground	Ground
14	GND	Ground	Ground
15	PIO11	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
16	PIO10	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
17	PIO9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
18	PIO8	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
19	GND	Ground	Ground
20	UART_RXD	CMOS input with weak internal pull-down	UART data input
21	UART_TXD	CMOS output, tristate, with weak internal pull-up	UART data output
22	UART_RTS	CMOS output, tri-state, with weak internal pull-up	UART request to send active low
23	UART_CTS	CMOS input with weak internal pull-down	UART clear to send active low

24	USB_D+	Bi-directional	USB data plus with selectable internal 1.5K pull-up resistor
25	USB_D-	Bi-directional	USB data minus
26	PIO2	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
27	PIO3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
28	PIO5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
29	PIO4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
30	SPI_CSB	CMOS input with weak internal pull-up	Chip select for Synchronous Serial Interface active low
31	SPI_MISO	CMOS output, tri-state, with weak internal pull-down	Serial Peripheral Interface data output
32	AIO0	Bi-directional	Programmable input/output line

Table 1：PIN Terminal Description

3. Power Supply

The module accepts a 3.3V DC power input. Power supply should guarantee good ripple suppression and enough current.

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4. Reset

The module may be reset from several sources: RESETB pin, power-on reset, a UART break character or via software configured watchdog timer.

The RESETB pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESETB being active. It is recommended that RESETB be applied for a period greater than 5ms.

Pin Name / Group	Pin Status on Reset
PIOs	Input with weak pull-down
AIOs	Output, driving low
PCM_OUT	Tristated with weak pull-down
PCM_IN	Input with weak pull-down
PCM_SYNC	Input with weak pull-down
PCM_CLK	PD
UART_TX	Output tristated with weak pull-up
UART_RX	Input with weak pull-down
UART_RTS	Output tristaed with weak pull-up
UART_CTS	Input with weak pull-down
USB_DP	Input with weak pull-down
USB_DN	Input with weak pull-down
SPI_CSB	Input with weak pull-up
SPI_CLK	Input with weak pull-down
SPI_MOSI	Input with weak pull-down
SPI_MISO	Tristated with weak pull-down
RESETB	Input with weak pull-up

Table 7: Pin Status on Reset

5. Antenna

The module integrates a Meander line PCB chip antenna so there's no need to use antenna on customer's PCB.

6. PIO

EH-MA41 has a total of 10 digital programmable I/O terminals. They are powered from VDD (3.3V). Their functions depend on firmware running on the device. PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs.

Note:

All PIO lines are configured as inputs with weak pull-downs at reset.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes.

7. AIO

EH-MA41 has 2 analogue I/O terminals. Their functions depend on software. Typically ADC functions can be configured to battery voltage measurement. They can also be used as a digital PIO.

8. UART

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

The UART CTS and RTS signals can be used to implement RS232 hardware flow control where both are active low indicators.

Table 8: Possible UART Settings

Parameter		Possible Values
Baud Rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	3M baud (≤1%Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per Byte		8

9. I2C Master

PIO6, PIO7 and PIO8 can be used to form a master I^2C interface. The interface is formed using software to drive these lines. It is suited only to relatively slow functions such as driving a LCD, keyboard scanner. In the case, PIO lines need to be pulled up through 2.2KΩ resistors.

10. SPI interface

The synchronous serial port interface (SPI) is used for flash/debug the module only. It can not be used for any user functionality. Please always design test points for this interface on the PCB in case that the module is needed to re-flash or flash-in-field in manufacture.

11. PCM interface

PCM is a standard method used to digitize audio (particularly voice) for transmission over digital communication channels. Through its PCM interface, the module has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for applications. The module offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on the module allows the data to be sent to and received from a SCO connection. Up to three SCO connections can be supported by the PCM interface at any one time.

The module can operate as the PCM interface master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave, it can operate with an input clock up to 2048kHz. The module is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13-bit or 16-bit linear, 8-bit μ-law or A-law companied sample formats at 8k samples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC.

The module interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channels A-law and μ-law CODEC
- Motorola MC145481 8-bit A-law and μ-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs
- The module is also compatible with the Motorola SSI™ interface.

12. PCM Interface Master

When PCM is configured as a master, the module generates PCM_CLK and PCM_SYNC.

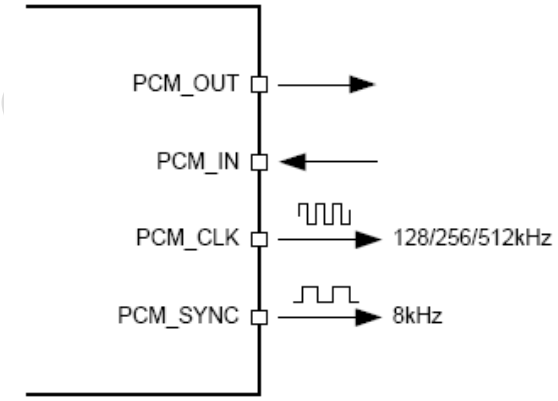

Figure 3: Configured PCM as a Master

When PCM is configured as the slave, the module accepts PCM_CLK rates up to 2048kHz.

13. USB

This is a full speed (12M bits/s) USB interface for communicating with other compatible digital devices. The module acts as a USB peripheral, responding to request from a master host controller, such as a PC.

The USB interface is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth specification V3.0 or alternatively can appear as a set of endpoints appropriate to USB audio devices such as speakers.

The module has an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when module is ready to enumerate. It signals to the USB master that it is a full speed (12Mbit/s) USB device.

"Attention - Limited Modular Approval
This RF Module is strictly limited to integration into battery-poerated host devices. Integration into devices that are directly or indirectly connected to AC lines may be added via Class II Permissive Change."

(OEM) Integrator has to assure compliance of the entire end-product incl. the integrated RF Module. Additional measurements (15B) and/or equipment authorizations(e.g Verification) may need to be addressed depending on co-location or simultaenous transmission issues if applicable.

Integrator is reminded to assure that these installation instructionswill not be made available to the end-user of the final host device.

With the documented max output power this RF Module meets the FCC SAR Exemption - so it comply with any applicable RF exposure requirements in its final configuration.

The RF Module is powered by DC ,the antenna is PCB antenna and the antenna gain is 0 dBi

The final host device, into which this RF Module is integrated" has to be labelledwith an auxilliary lable stating the FCC ID of the RF Module, such as"Contains FCC ID: 2ACCRMA41"

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:
(1) this device may not cause harmful interference, and
(2) this device must accept any interference received, including interference that may cause undesired operation.

"Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user’s authority to operate the equipment."