Circuit Description

Input Power and Charger

The battery charger of A6 is MAX8677. MAX8677 is with double Power supply (DC and USB) input integrated single day Li + battery charger and Smart Power Selector Selector.A6 equipment using DC external power supply.
MAX8677 with Smart Power Selecto, the most effective use of communication adapter Power supply.Can choose charging circuit, through the external resistors A6 equipment set up in 1.5 A charging current.MAX8677 recharging the battery can be set is divided into three stages: pre charge, constant current and constant voltage.In all stages of the internal control circuit monitoring charging current junction temperature, reduce the internal temperature exceeds the threshold.
MAX8677 include overvoltage protection (OVP) and indications for charging status.

MAX8660 power management IC
A6 equipment using power management chip for MAX8660,.Type MAX8660 chip integrates four-way step-down DC - DC output, three linear voltage regulator, a regular power management circuits.Two way for dynamic adjusting DC - DC processor core, memory, power supply;The other two lines of DC - DC converter for the I/O, memory and other peripherals.
All type step-down DC - DC converter adopts high speed 2 MHZ PWM switch, can automatically switch from PWM mode to funny light load work mode, in order to reduce the working current, extend battery life.

CPU

The PXA303 processors are integrated system-on-a-chip microprocessors for high-performance, low-power portable handheld and handset devices. They incorporate the XScale® microarchitecture with on-the-fly voltage and frequency scaling and sophisticated power management to provide industry leading MIPS/mW performance across its wide range of operating frequencies. The processors comply with the ARM* Architecture V5TE instruction set (excluding floating point instructions) and follow the ARM* programmers model. The multimedia coprocessor provides enhanced Intel® Wireless MMX™ 2 instructions to accelerate audio and video processing. The processors are available in a discrete package configuration. They provide a high degree of backward compatibility with the Marvell PXA27x Processor Family, but they offer significant performance and feature set enhancements.

The processor memory architecture offers greater flexibility and higher performance than previous core products. This architecture supports two dedicated memory interfaces for high-speed DDR SDRAM, VLIO devices, and NAND flash devices. This flexibility enables high-performance “store- and-download” as well as “execute-in-place” system architectures. The processor memory architecture features a memory switch that allows multiple simultaneous memory transactions among different sources and targets. For example, the processor architecture allows memory traffic between the core and DDR SDRAM to move in parallel with DMA-generated traffic between the LCD controller and internal SRAM. In an architecture with a single shared system bus, these transactions block each other. The PXA32x processor also provides a 256-Kbyte, unified L2 cache to maintain high memory system performance, lower power with a full feature OS, and several complex multimedia applications running simultaneously.The processor incorporates an internal boot ROM and a Marvell® Wireless Trusted Transaction Technology module to provide flexible boot-loading options while maintaining platform security. They have up to six 128 Kbyte banks of internal SRAM for a combination of display frame buffer, program code, or multimedia data. Each bank can be configured to retain its contents when the processor enters a low-power mode.The processor provides OS timer channels and synchronous serial ports (SSPs) that accept an external network clock input so that they can be synchronized to the cellular network.An integrated LCD panel controller supports active and passive displays. It permits color depths of up to 18-bits per pixels (24-bits per pixel for smart panels). The LCD controller also supports hardware cursor and two display overlays. The processor incorporates a comprehensive set of system and peripheral functions that make it useful in a variety of low-power applications.

Barcode(1D)

The SE955 is a scan engine combined with a microprocessor to control the functionality of the engine, perform software decoding of the bar code information and provide a communication link to the host computer.
The scan engine provides the following functions: laser drive circuit controlling a 650 nm laser diode; scan element drive circuit controlling a resonant single line scan element;analog receiver with circuitry to identify the bar and space locations in the received waveform; temperature sensor;power on reset functionality.
The microprocessor section provides the following functions:non-volatile memory for storing user preferences for decoder capability parameters;runs the bar code decoder software; watchdog timer.
A host Simple Serial Interface (SSI) provides the following functions: low current beeper line (BPR*) to provide beep signals;decode LED output line (DLED*) to indicate a successful decode; signal to indicate that the unit can be powered down (PWRDWN); two serial I/O lines (RXD and TXD); two hardware handshaking lines

(CTS* and RTS*); hardware trigger line (TRIG*) and a hardware Aim/wake-up line (AIM/WKUP*) line (FLASH_DWLD*) to support re-flashing the product software through the SSI interface.

Wifi and Bluetooth

The GB86321G is a low-power consumption module which has all of the Wi-Fi, Bluetooth functionalities. The highly integrated GB86321G module makes the possibilities of web browsing, VoIP, Bluetooth headsets and other applications. With seamless roaming capabilities and advanced security, GB86321G can also interact with different vendors!fl 802.11b/g/n ccess Points in the wireless LAN.
The wireless module complies with IEEE 802.11 b/g/n standard and it can achieve up to a speed of 72.2Mbps with single stream in 802.11n draft, 54Mbps as specified in IEEE 802.11g, or 11Mbps for IEEE 802.11b to connect to the wireless LAN. The integrated module provides SDIO interface for Wi-Fi and UART / audio PCM interface for Bluetooth. This compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

RFID(UHF)

The SARU200 is a fully functional UHF Gen 2 RFID reader based on the Impinj Indy R2000. The Impinj Indy R2000 UHF Gen 2 RFID reader chip is a highly integrated, high-performance, low power, SiGe BiCMOS device for EPC Gen2 / ISO18000-6C applications.
The Indy R2000 reader chip supports a zero intermediate frequency (ZIF) architecture in the worldwide UHF industrial, science, and medical (ISM) band. The Indy R2000 reader chip comprises all of the RF and baseband blocks to interrogate and receive data from compatible RFID tags, specifically: High compression point quadrature downconverting mixer Fully integrated voltage controlled oscillator (VCO) Variable receiver (RX) gain control Integrated Power Amplifier (PA) Self-jammer cancellation circuitry Integrated RF envelope detectors for forward and reverse power sense Integrated multipurpose Analog-to-Digital Converts (ADCs) and Digital-to-Analog Converters (DACs) Configurable digital baseband High speed synchronous serial bus or 4-bit parallel bus control .

Audio + Touchpanel CODEC
The Audio + Touchpanel CODEC of A6 is WM9713L. The WM9713L is a highly integrated input/output device designed for mobile computing and communications.
The chip is architected for dual CODEC operation, supporting Hi-Fi stereo Codec

functions via the AC linkinterface. A third Aux DAC is provided which may be used to support generation of supervisory tones, or ring-tones etc. at different sample rates to the main codec.

The device can connect directly to a 4-wire touchpanel, mono or stereo microphones, stereo headphones.and a stereo speaker, reducing total component count in the system.

All device functions are accessed and controlled through a single AC-Link interface compliant with the AC’97 standard.

The WM9713L operates at supply voltages from 1.8 to 3.6 Volts. Each section of the chip can be powered down under software control to save power.