MT7601U
802.11 b/g/n single chip
Preliminary datasheet

Version: 0.06
Release date: 2012-12-10

Document Revision History

Revision	Date	Author	Description
0.01	2012/03/30	Alex Lin	First formal release
0.02	2012/08/13	Ben Lin	1. Change the thickness of the package to 0.8mm. 2. Update power consumption information
0.03	2012/08/21	Alex Lin	Update bootstrap infomation
0.04	2012/8/26	Ben Lin	Update thermal information
0.05	2012/9/27	Alex Lin	1. Fix pin order 2. Update POD
0.06	2012/12/10	Alex Lin	1. Correct pin description typo 2. Correct strapping option typo

Table of Contents

1 System Overview

1.1 General Descriptions

The MT7601U is a highly integrated Wi-Fi single chip which supports 150 Mbps PHY rate. It fully complies with IEEE 802.11n and IEEE 802.11 b/g standards, offering feature-rich wireless connectivity at high standards, and delivering reliable, cost-effective throughput from an extended distance.

Optimized RF architecture and baseband algorithms provide superb performance and low power consumption. Intelligent MAC design deploys a high efficient DMA engine and hardware data processing accelerators which offloads the host processor.

The MT7601U is designed to support standard based features in the areas of security, quality of service and international regulations, giving end users the greatest performance any time and in any circumstance.

1.2 Features

- IEEE 802.11 b/g/n client
- Embedded high-performance 32-bit RISC microprocessor
- Highly integrated RF with 55nm CMOS technology
- 1T1R mode with support of 150Mbps PHY rate
- Integrate high efficiency switching regulator
- Best-in-class power consumption performance
- Compact 5mm x 5mm QFN40L package
- 1/2/3/4-wire PTA Wi-Fi / Bluetooth coexistence support
- 802.11 d/h/k compliant
- Security support for WFA WPA/WPA2 personal, WPS2.0, WAPI
- Supports 802.11w protected managed frames
- QoS support of WFA WMM, WMM PS
- Supports Wi-Fi Direct
- Fully compliance with USB v2.0 High-speed mode
- Per packet transmit power control
- Antenna diversity
- Auto-calibration

1.3 Applications

- Desk-Top PC
- Note-book
- TV
- Blue-ray Disk
- Tablet PC
- Set-top box

1.4 Block Diagram

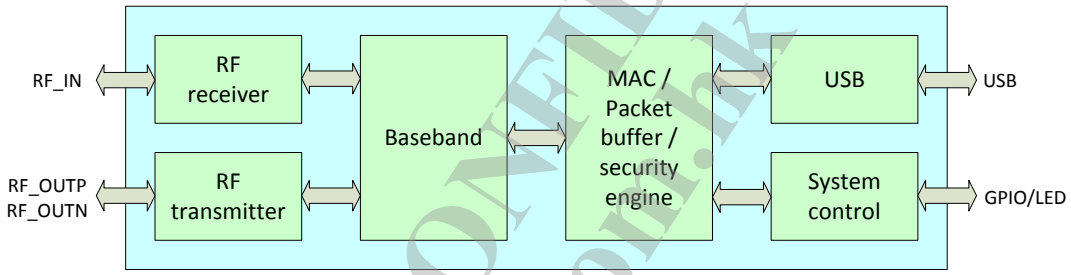


Figure 1 MT7601U block diagram

2 Product Descriptions

2.1 Pin Layout

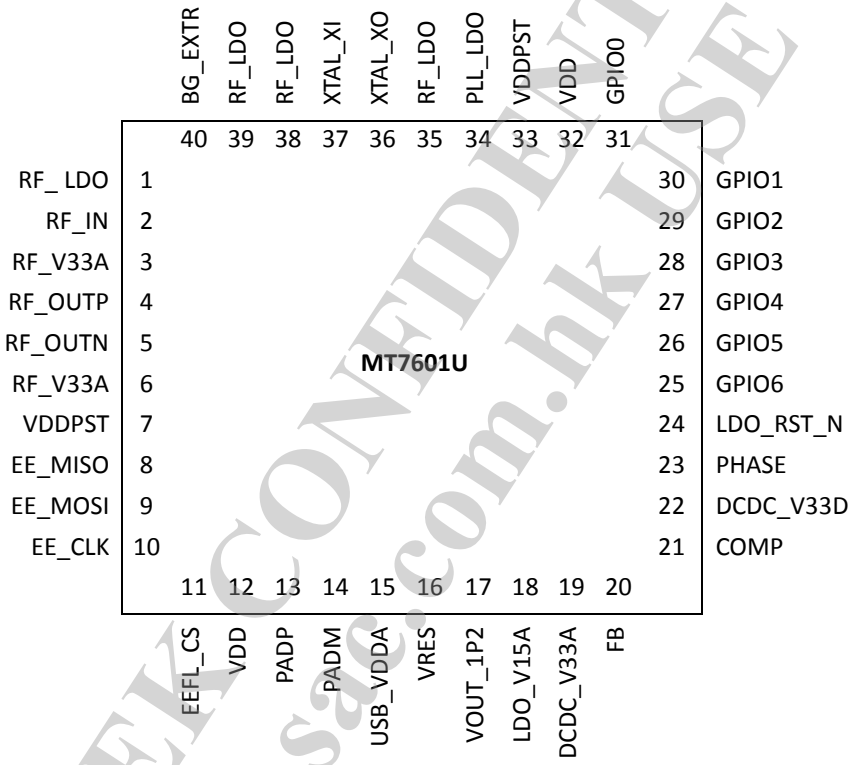


Figure 2 Top view of MT7601U QFN pin-out.

2.2 PIN Description

QFN40	Pin Name	Pin description	Default PU/PD	I/O	Supply domain
Reset and clocks					
24	LDO_RST_N	External system reset active low	N/A	Input	VDDPST
37	XTAL_XI	Crystal input or external clock input	N/A	Input	
36	XTAL_XO	Crystal output	N/A	Input	
USB interface					
15	USB_VDDA	USB 3.3V power supply	N/A		
16	VRES	USB BG reference	N/A		
13	PADP	USB D+ signal	N/A	In/out	USB_VDDA
14	PADM	USB D- signal	N/A	In/out	USB_VDDA
EEPROM/flash interface					
8	EE_MISO	External memory data input / Antenna select	PD	Input	VDDPST
9	EE_MOSI	External memory data output / Antenna select	PD	Output	VDDPST
10	EE_CLK	External clock	PU	Output	VDDPST
11	EEFL_CS	External chip select	PU	Output	VDDPST
Programmable I/O					
31	GPIO0	Programmable input/output / Bluetooth coexistence	PD	In/out	
30	GPIO1	Programmable input/output / Bluetooth coexistence	PD	In/out	VDDPST
29	GPIO2	Programmable input/output	PD	In/out	VDDPST
28	GPIO3	Programmable input/output / Bluetooth coexistence	PD	In/out	VDDPST
27	GPIO4	Programmable input/output / Bluetooth coexistence	PD	In/out	VDDPST
26	GPIO5	Programmable input/output	PD	In/out	VDDPST
25	GPIO6	Programmable input/output	PD	In/out	VDDPST
WIFI radio interface					
40	BG_EXTR	RF BG reference	N/A		
2	RF_IN	RF auxiliary RX input	N/A		
4	RF_OUTP	RF port	N/A		
5	RF_OUTN	RF port	N/A		
PMU/SMPS					
17	VOUT_1P2	LDO 1.2V output	N/A	Output	
18	LDO_V15A	SMPS 1.5V input	N/A	Iutput	
19,22	DCDC_V33	SMPS 3.3V power supply	N/A	Input	
20	FB	SMPS control	N/A		

21	COMP	SMPS control	N/A		
23	PHASE	SMPS control	N/A		
Power supplies					
7,33	VDDPST	Digital I/O power supply	N/A	Input	
12,32	VDD	Digital core power supply	N/A	Input	
3,6	RF_V33A	RF 3.3V power supply	N/A	Input	
1,35, 38,39	RF _LDO	RF power supply	N/A	Input	
34	PLL_LDO	RF power supply	N/A	Input	
E-PAD	DVSS	Digital ground	N/A		

Table 1 Pin descriptions

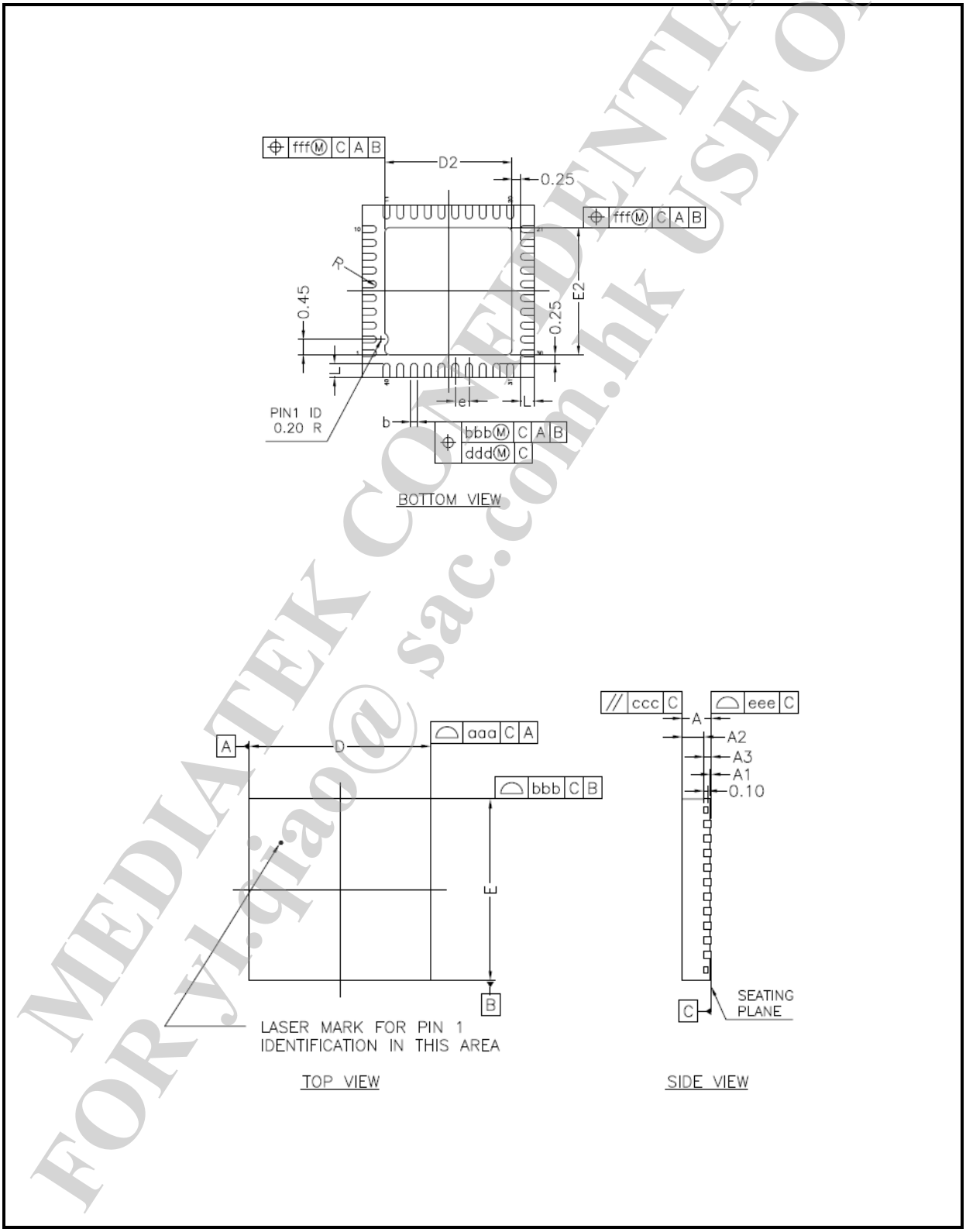
2.3 Strapping option

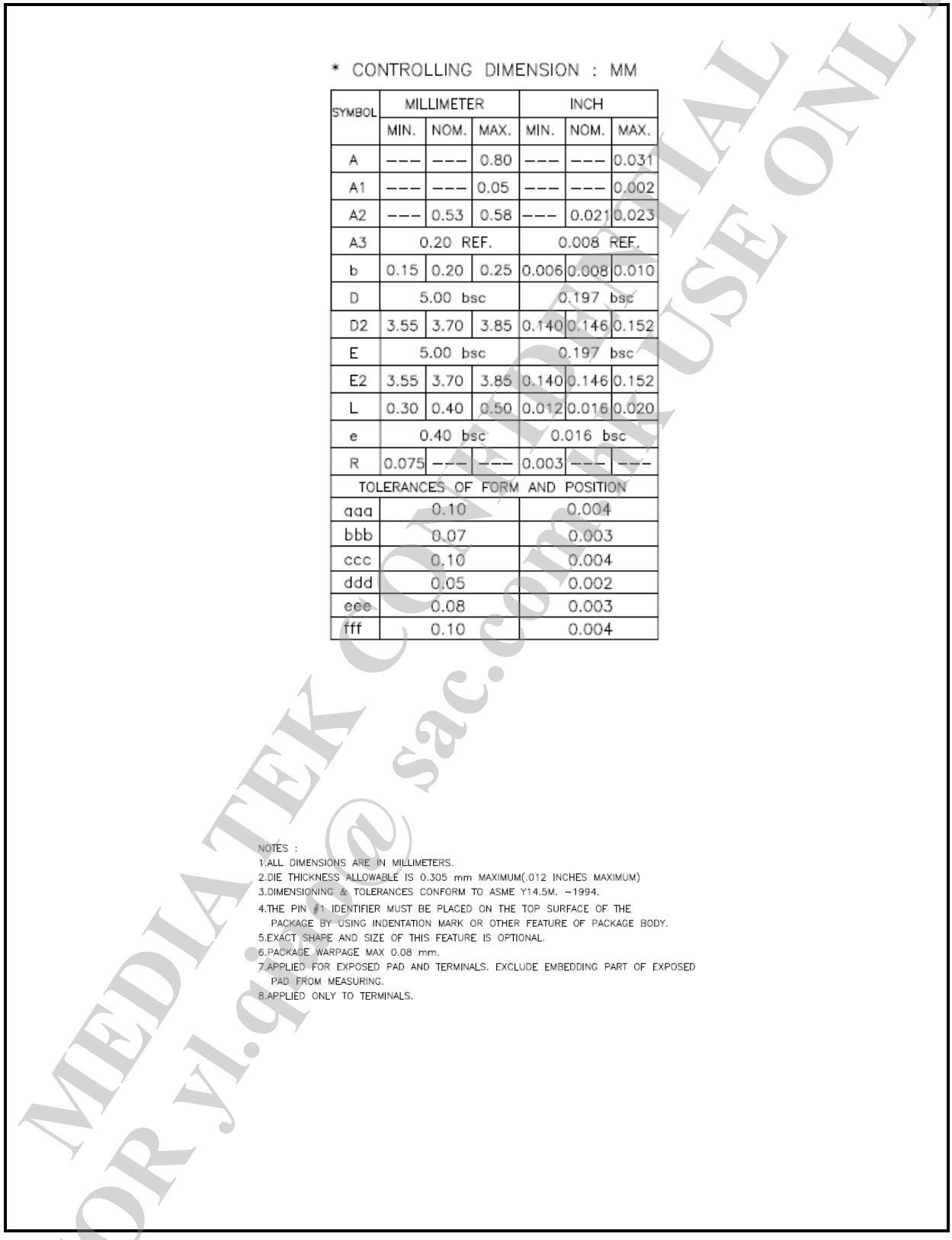
QFN40	Pin Name	Pin description	Default PU/PD
8	EE_MISO	XTAL_20_SEL XTAL is 20MHz: Pull up XTAL is 40MHz: Pull down	PD
27	GPIO4	EXT_EE_SEL: Pull down	PD
25	GPIO6	CHIP_MODE[2]: Pull down	PD
10	EE_CLK	CHIP_MODE[1]: Pull down	PD
9	EE_MOSI	CHIP_MODE[0]: Pull up	PU

Table 2 Strapping option

2.4 Package Information

2.4.1 QFN Packaging





* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.80	---	---	0.031
A1	---	---	0.05	---	---	0.002
A2	---	0.53	0.58	---	0.021	0.023
A3	0.20 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	5.00 bsc			0.197 bsc		
D2	3.55	3.70	3.85	0.140	0.146	0.152
E	5.00 bsc			0.197 bsc		
E2	3.55	3.70	3.85	0.140	0.146	0.152
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.40 bsc			0.016 bsc		
R	0.075	---	---	0.003	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6.PACKAGE WARPAGE MAX 0.08 mm.
7.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8.APPLIED ONLY TO TERMINALS.

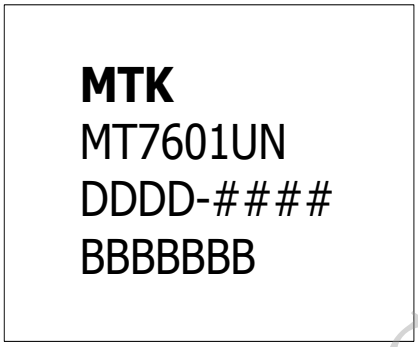
Figure 3 Package outline drawing

2.5 Ordering Information

Part number	Package	Operational temperature range
MT7601UN/A-L	5x5x0.8 mm 40-QFN	-10~70°C

Table 3 Ordering information

2.6 TOP Marking Information



MT7601UN : Part number
DDDD : Date code
: Internal control code
BBBBBBB : Lot number

Figure 4 Top marking

3 Electrical characteristics

3.1 Absolute maximum rating

Symbol	Parameters	Maximum rating	Unit
VDD33	3.3V Supply Voltage	-0.3 to 3.6	V
VDD12	1.2V Supply Voltage	-0.3 to 1.5	V
VDD15	1.5V Supply Voltage	-0.3 to 1.8	V
T_{STG}	Storage Temperature	-40 to +125	°C
VESD	ESD protection (HBM)	2000	V

Table 4 Absolute maximum ratings

3.2 Recommended operating range

Symbol	Rating	MIN	TYP	MAX	Unit
VDD33	3.3V Supply Voltage	2.97	3.3	3.63	V
VDD12	1.2V Supply Voltage	1.14	1.2	1.26	V
VDD15	1.5V Supply Voltage	1.425	1.5	1.575	V
$T_{AMBIENT}$	Ambient Temperature	-10	-	70	°C

Table 5 Recommended operating range

3.3 DC characteristics

Symbol	Parameter	Conditions	MIN	MAX	Unit
V_{IL}	Input Low Voltage	LVTTL	-0.28	0.6	V
V_{IH}	Input High Voltage		2.0	3.63	V
V_{T-}	Schmitt Trigger Negative Going Threshold Voltage	LVTTL	0.68	1.36	V
V_{T+}	Schmitt Trigger Positive Going Threshold Voltage		1.36	1.7	V
V_{OL}	Output Low Voltage	$\|I_{OL}\|$ = 1.6~14 mA	-0.28	0.4	V
V_{OH}	Output High Voltage	$\|I_{OH}\|$ = 1.6~14 mA	2.4	VDD33+0.33	V
R_{PU}	Input Pull-Up Resistance	PU=high, PD=low	40	190	KΩ
R_{PD}	Input Pull-Down Resistance	PU=low, PD=high	40	190	KΩ

Table 6 DC description

3.4 Thermal characteristics

Symbol	Description	Performance	
		TYP	Unit
T_J	Maximum Junction Temperature (Plastic Package)	125	°C
Θ_{JA}	Junction to ambient temperature thermal resistance[1][2]	48.11	°C/W
Θ_{JC}	Junction to case temperature thermal resistance	TBD	°C/W

Ψ_{Jt}	Junction to the package thermal resistance[3]	3.23	°C/W

Note:
[1] Air flow condition: Natural convection. 0.5m/s.
[2] PCB dimension 21mm x 11mm. 4-layer.
[3] 5mm x 5mm QFN40L package

Table 7 Thermal information

3.5 Current consumption

Description	Performance	
	TYP	Unit
Sleep mode	1.1	mA
RX Active, HT40, MCS7	151	mA
RX Power saving, DTIM=1	15	mA
RX Listen	6	mA
TX HT40, MCS7 @15dBm	210	mA
TX CCK, 11Mbps @19dBm	242	mA

Note: All result is measured at the antenna port and VDD33 is 3.3V

Table 8 WLAN 2.4GHz Current Consumption

ESD CAUTION

MT7601 is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although MT5931 is with built-in ESD protection circuitry, please handle with care to avoid the permanent malfunction or the performance degradation.