Golden Technology Corporation


# GBS 535-MD-01A
# Wi-Fi PCB Module Datasheet

**V 1.00**





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## REVISION HISTORY

| Version No. | Revised Date | Description |
|---|---|---|
| 0.80 | 2013-07-16 | Preliminary version released |
| 0.83 | 2013-10-23 | Pin assignment changed |
| 0.90 | 2014-02-01 | V 0.9 released |
| 0.92 | 2014-04-30 | Update alternate function of pin 17 and pin 18. |
| 0.95 | 2014-07-01 | Part number updated. |
| 1.00 | 2014-08-13 | V1.00 released. |




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## 1. High integration of 2.4GHz IEEE 802.11 PCB Module

The GBS 535-MD-01A series PCB modules provide the highest degree integration design for the embedded application. It incorporates a GBS 535 SiP module, a printed antenna, a iPEX connector, a crystal, a minimum number of resistors and capacitors. The high integration GBS 535 SiP module on the PCB module integrates a high performance, low power 802.11 b/g/n Wi-Fi IC , the Broadcom BCM43362 and an ARM Cortex M3 MCU, the STM32F207. The cost, easy production and low power consumption advantages allow the user to build a competitive, reliable and wireless embedded product.

## 2. Application

The GBS 535-MD-01A series including GBS 535-MD-01A, GBS 535-MD-01AP, GBS 535-MD-01B, GBS 535-MD-01BP, is designed for the embedded wireless application such as industrial control, vehicle system, automation control, medical instrument system, health care system and other embedded wireless applications.

## 3. Feature

- Single band : 2.4GHz.
- IEEE 802.11 b/g/n compliant.
- Integrate an ARM Cortex M3 MCU with on chip memory.
- Support USART/UART and SPI buses.
- Support SPI buses.
- Support ADC and CAN bus functions.
- Firmware down load through JTAG.
- External 3.3V operation voltage.
- Low power consumption.
- Hardware WAPI acceleration engine.
- Support WEP, WPA/WPA2.
- 32 pin, 28x20 mm compact board size.
- On board printed antenna.
- An optional U.FL. connector for the external antenna.
- Minimum external components to reduce design effort.
- CE/FCC certified.
- The easy to use, Smart Command is available upon request.




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## 4. System Block Diagram

The system block diagram of the GBS 535-MD-01A is shown in figure 4.1 and the system block diagram of GBS 535 SiP module is shown in figure 4.2. The Internal PMOS in figure 4.1 is to enable Wi-Fi power which is controlled by the GBS 535-MD-01A.

Figure 4.1 System block diagram of GBS 535-MD-01A

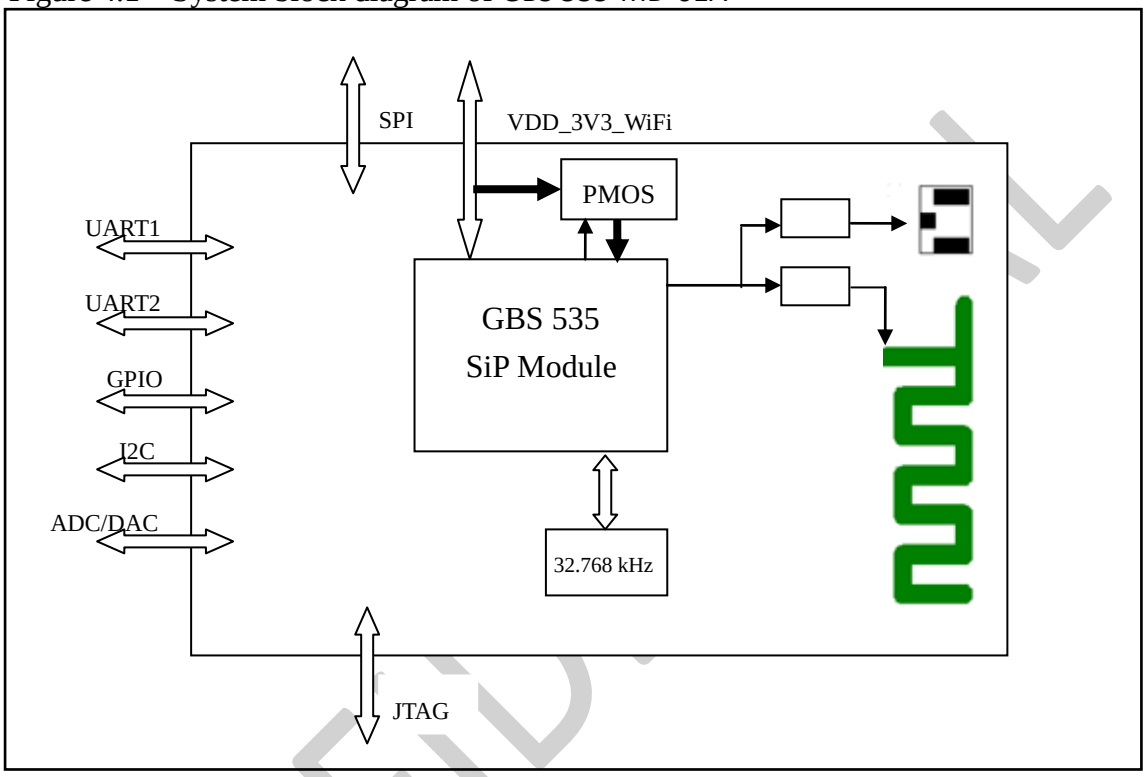
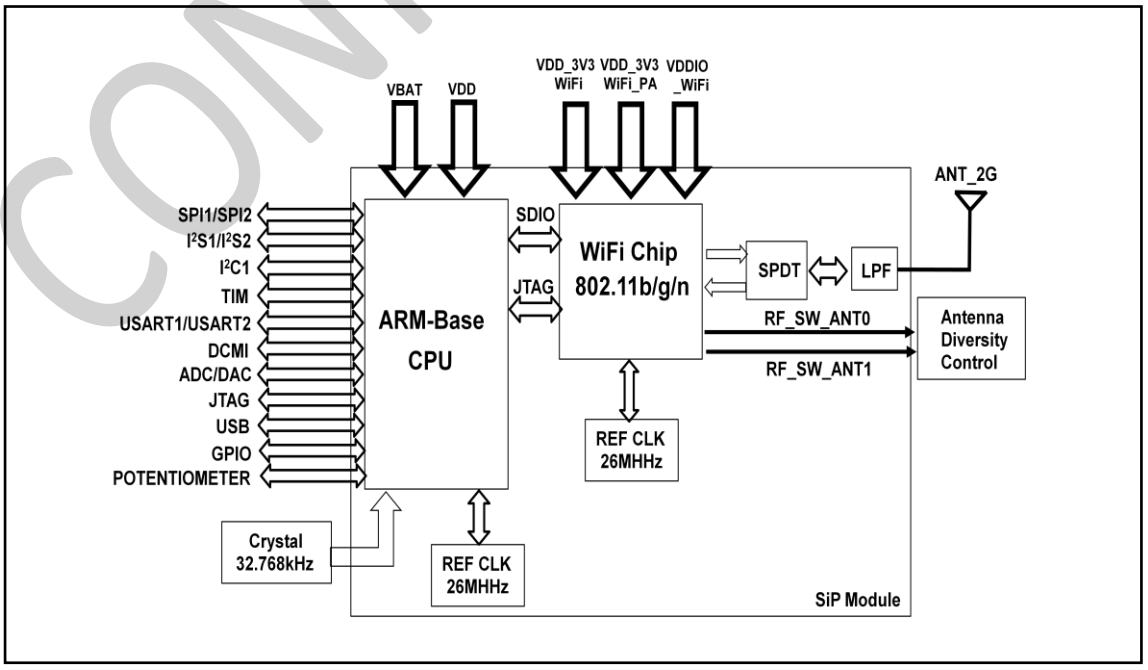



Figure 4.2 System block diagram of GBS 535 SiP module







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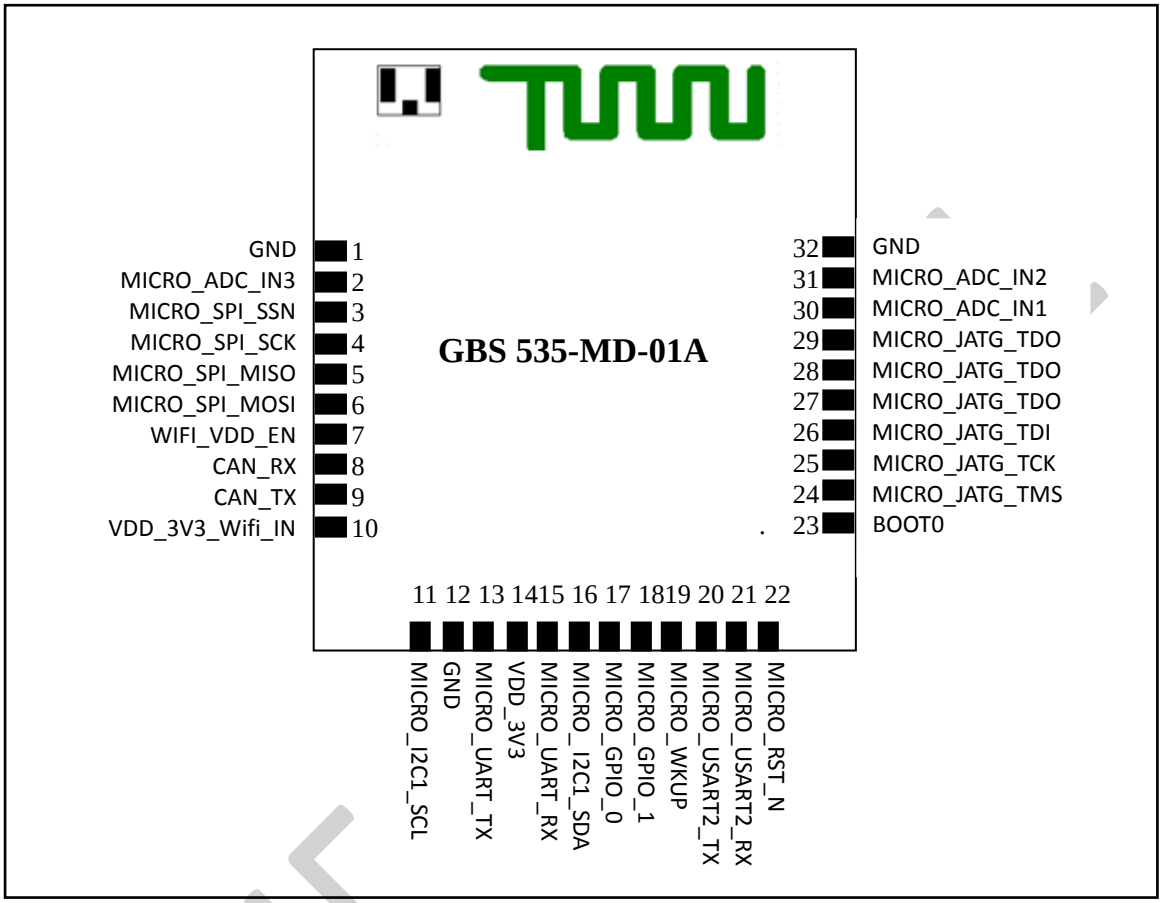
## 5. Pin Diagram

The pin diagram of the GBS 535-MD-01A is shown in figure 5.1.

Figure 5.1 The pin diagram of the GBS 535-MD-01A




## 6. Pin Description

The pin description of the GBS 535-MD-01A is listed in the Table 6.1.

Table 6.1 The pin description of the GBS 535-MD-01A

| Pin No. | Pin Name | Type | Description | Alternate Function |
|---|---|---|---|---|
| 1 | GND | I/O | Ground | |
| 2 | MICRO_ADC_IN3 | I/O | MCU_ADC_IN_3 | EVENTOUT / TIMER/GP IO |
| 3 | MICRO_SPI_SSN | I/O | MCU_SPI_SSN | ADC_IN_4/GPIO/ DAC1_OUT / EVENTOUT |
| 4 | MICRO_SPI_SCK | I/O | MCU_SPI_SCK | ADC_IN_5 /GPIO/ TIMER/DAC2_OUT / EVENTOUT |
| 5 | MICRO_SPI_MISO | I/O | MCU_SPI_MISO | ADC_IN_6 /GPIO/ TIMER/EVENTOUT |
| 6 | MICRO_SPI_MOSI | I/O | MCU_SPI_MOSI | ADC_IN_7/GPIO /TIMER/EVENTOUT |


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Table 6.1 The pin description of the GBS 535-MD-01A (cont.)

| Pin No. | Pin Name | Type | Description | Alternate Function |
|---|---|---|---|---|
| 7 | WIFI_VDD_EN | I/O | Enable Wi-Fi VDD | |
| 8 | CAN_RX | I/O | MCU_CAN_RX | EVENTOUT/ GPIO |
| 9 | CAN_TX | I/O | MCU_CAN_TX | EVENTOUT /GPIO |
| 10 | VDD_3V3_Wifi_IN | PI | Wi-Fi power supply | |
| 11 | MICRO_ I2C1_SCL | I/O | MCU_I2C1_SCL | EVENTOUT/GPIO |
| 12 | GND | I/O | Ground | |
| 13 | MICRO_UART_TX | I/O | MCU_UART_TX | EVENTOUT/TIMER/ GPIO |
| 14 | VDD_3V3 | PI | DC supply for MCU and I/O | |
| 15 | MICRO_UART_RX | I/O | MCU_UART_TX | EVENTOUT/ TIMER/ GPIO |
| 16 | MICRO_ I2C1_SDA | I/O | MCU_I2C1_SDA | EVENTOUT/GPIO |
| 17 | MICRO_GPIO_0 | I/O | MCU_GPIO | EVENTOUT/ I2C2_SDA/ ACK for Smart Command SPI/UART mode. |
| 18 | MICRO_GPIO_1 | I/O | MCU_GPIO | EVENTOUT / I2C2_SCL |
| 19 | MICRO_WKUP | I/O | MCU_WKUP | Smart Command<br>1 : UART<br>0 : SPI (default) |
| 20 | MICRO_USART2_TX | I/O | MCU_USART2_TX | EVENTOUT / GPIO |
| 21 | MICRO_USART2_RX | I/O | MCU_USART2_RX | EVENTOUT / GPIO |
| 22 | MICRO_RST_N | I/O | MCU_RST_N | |
| 23 | BOOT0 | O | Normal operation if connected to GND at power up. | |
| 24 | MICRO_JATG_TMS | I/O | MCU_JATG_TMS | EVENTOUT / GPIO |
| 25 | MICRO_JATG_TCK | I/O | MCU_JATG_TCK | EVENTOUT / GPIO |
| 26 | MICRO_JATG_TDI | I/O | MCU_JATG_TDI | EVENTOUT/TIMER/ GPIO |
| 27 | MICRO_JATG_TDO | I/O | MCU_JATG_TDO | EVENTOUT / GPIO |
| 28 | MICRO_JATG_TRSTN | I/O | MCU_JATG_RSTN | EVENTOUT /GPIO |
| 29 | VBAT | PI | Power supply for backup circuitry if VDD isn't present. | |
| 30 | MICRO_ADC_IN1 | I/O | MCU_ADC_IN_1 | EVENTOUT / TIMER/GPIO |
| 31 | MICRO_ADC_IN2 | I/O | MCU_ADC_IN_2 | EVENTOUT / TIMER/GPIO |
| 32 | GND | I/O | Ground | |

Note 1 : I/O = Input/Output. PI = Power Input.
Note 2 : Refer to the GBS 535 SiP module data sheet for more information about pin definition.
Note 3 : Contact GTC sales for more information about "Alternate Function".





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Table 6. 2 Alternate function mapping table

| Pin No | Mapping STM32F20x _LQFP176 | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4 /5 | TIM8/9 /10/11 | 2C1/I2C2/ I2C3 | SPI1/SPI 2/I2S2 | SPI3/ I2S3 | UASRT 1/2/3 | UART4/5 /USART6 | CAN1/CAN 2/TIM12/1 3/14 | OTG_FS/ OTG_HS | FSMC/SDI O/OTG_HS | DCMI | ADC DAC | EVENTOUT GPIO |
| 2 | PA3 | | TIM2_ CH4 | TIM5_ CH4 | TIM9_CH2 | | | | USART2_ RX | | | OTG_HS_ ULPI_D0 | | | ADC123_IN3 | EVENTOUT GPIO |
| 3 | PA4 | | | | | | SPI1_NSS | SPI3_NSS I2S3_WS | USART2_ CK | | | | OTG_HS_ SOF | DCMI_ HSYNC | ADC12_ IN4 DAC1_OUT | EVENTOUT GPIO |
| 4 | PA5 | | TIM2_CH1 TIM2_ETR | | TIM8_ CH1N | | SPI1_SCK | | | | | OTG_HS_ ULPI_CK | | | ADC12_ IN5 DAC2_OUT | EVENTOUT GPIO |
| 5 | PA6 | | TIM1_ BKIN | TIM3_CH1 | TIM8_ BKIN | | SPI1_MISO | | | | TIM13_ CH1 | | | DCMI_ PIXCK | ADC12 _IN6 | EVENTOUT GPIO |
| 6 | PA7 | | TIM1_ CH1N | TIM3_CH2 | TIM8_ CH1N | | SPI1_MOSI | | | | TIM14_ CH1 | | | | ADC12_IN7 | EVENTOUT GPIO |
| 8 | PD0 | | | | | | | | | | CAN1_RX | | FSMC_D2 | | | EVENTOUT GPIO |
| 9 | PD1 | | | | | | | | | | CAN1_TX | | FSMC_D3 | | | EVENTOUT GPIO |
| 11 | PB6 | | | TIM4_CH1 | | I2C1_SCL | | | USART1_ TX | | CAN2_TX | | | DCMI_ D5 | | EVENTOUT GPIO |
| 13 | PA9 | | TIM1_CH2 | | | I2C3_ SMBA | | | USART1_ TX | | | | | DCMI_D0 | | EVENTOUT GPIO |
| 15 | PA10 | | TIM1_CH3 | | | | | | USART1_ RX | | | OTG_FS_ID | | DCMI_D1 | | EVENTOUT GPIO |
| 16 | PB7 | | | TIM4_ CH2 | | I2C1_SDA | | | USART1_ RX | | | | FSMC_NL | DCMI_ VSYNC | | EVENTOUT GPIO |
| 17 | PF0 | | | | | I2C2_SDA | | | | | | | FSMC_A0 | | | EVENTOUT GPIO |




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Table 6. 2 Alternate function mapping table (cont.)

| Pin NO | Mapping STM32F20x_LQFP176 | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/I2C2/I2C3 | SPI1/SPI2/I2S2 | SPI3/I2S3 | UASRT1/2/3 | UART4/5/USART6 | CAN1/CAN2/TIM12/13/14 | OTG_FS/OTG_HS | FSMC/SDIO/OTG_HS | DCMI | ADC/DAC | EVENTOUT/GPIO |
| **18** | **PF1** | | | | | I2C2_SCL | | | | | | | FSMC_A1 | | | EVENTOUT/GPIO |
| **19** | **PA0-WKUP** | | TIM2_CH1 TIM2_ETR | TIM5_CH1 | TIM8_ETR | | | | USART2_CTS | UART4_TX | | | | | ADC123_IN0 | EVENTOUT/GPIO |
| **20** | **PD5** | | | | | | | | USART2_TX | | | | FSMC_NWE | | | EVENTOUT/GPIO |
| **21** | **PD6** | | | | | | | | USART2_RX | | | | FSMC_NWAIT | | | EVENTOUT/GPIO |
| **24** | **PA13** | JTMS-SWDIO | | | | | | | | | | | | | | EVENTOUT/GPIO |
| **25** | **PA14** | JTCK-SWCLK | | | | | | | | | | | | | | EVENTOUT/GPIO |
| **26** | **PA15** | JTDI | TIM2_CH1 TIM2_ETR | | | | SPI1_NSS | SPI3_NSS, I2S3_WS | | | | | | | | EVENTOUT/GPIO |
| 27 | PB3 | JTDO/TRACESWO | TIM2_CH2 | | | | SPI1_SCK | SPI3_SCK , I2S3_SCK | | | | | | | | EVENTOUT/GPIO |
| **28** | **PB4** | JTRST | | TIM3_CH1 | | | SPI1_MISO | SPI3_MISO | | | | | | | | EVENTOUT/GPIO |
| **30** | **PA1** | | TIM2_CH2 | TIM5_CH2 | | | | | USART2_RTS | UART4_RX | | | | | ADC123_IN1 | EVENTOUT/GPIO |
| **31** | **PA2** | | TIM2_CH3 | TIM5_CH3 | TIM9_CH1 | | | | USART2_TX | | | | | | ADC123_IN2 | EVENTOUT/GPIO |




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## 7. Part number, Physical Dimension and the Footprint

Description of the part number of the GBS 535-MD-01A series is listed in the Table 7.1.

Table 7.1 The part number of the GBS 535-MD-01A series

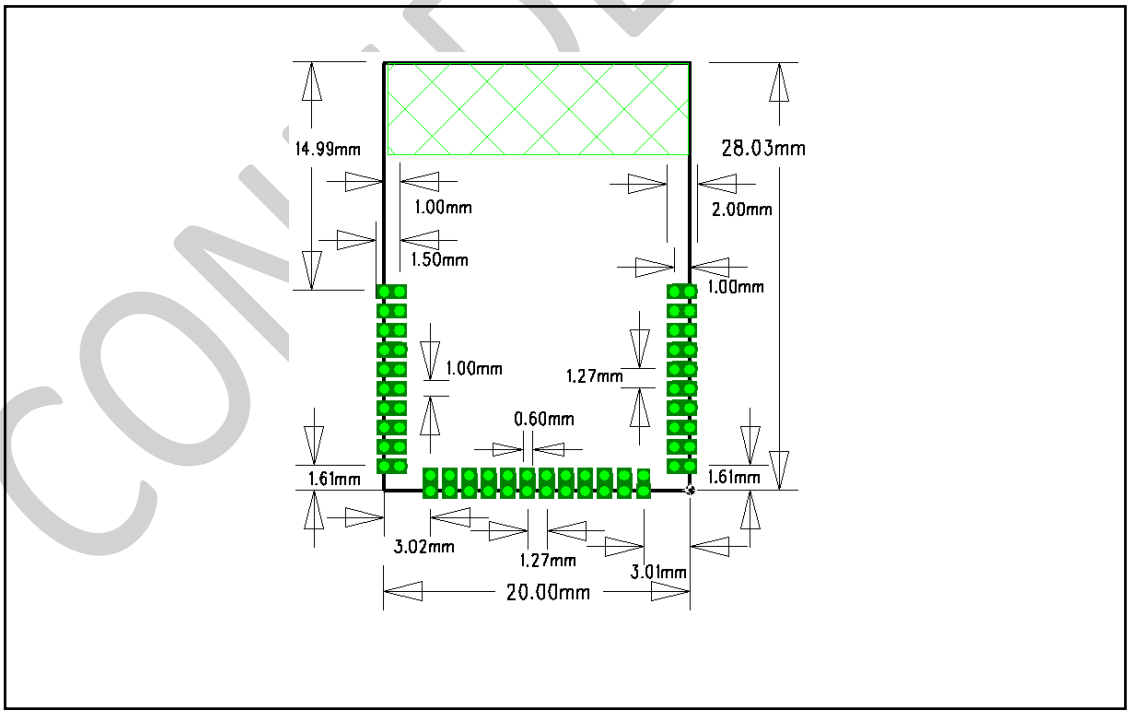
| Part Number | Printed antenna | U. FL connector | Pin header |
|---|---|---|---|
| GBS 535-MD-01A | Yes | --- | --- |
| GBS 535-MD-01AP | Yes | --- | Yes |
| GBS 535-MD-01B | --- | Yes | --- |
| GBS 535-MD-01BP | --- | Yes | Yes |

The physical dimension of the GBS 535-MD-01A is shown in the Table 7.2. and the footprint is shown in figure 7.1.

Table 7.2 The physical dimension of the GBS 535-MD-01A

| Board | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|
| GBS 535-MD-01A | 28.03mm | 20mm | 3.5mm |

Fig 7.1 Footprint of the GBS 535-MD-01A







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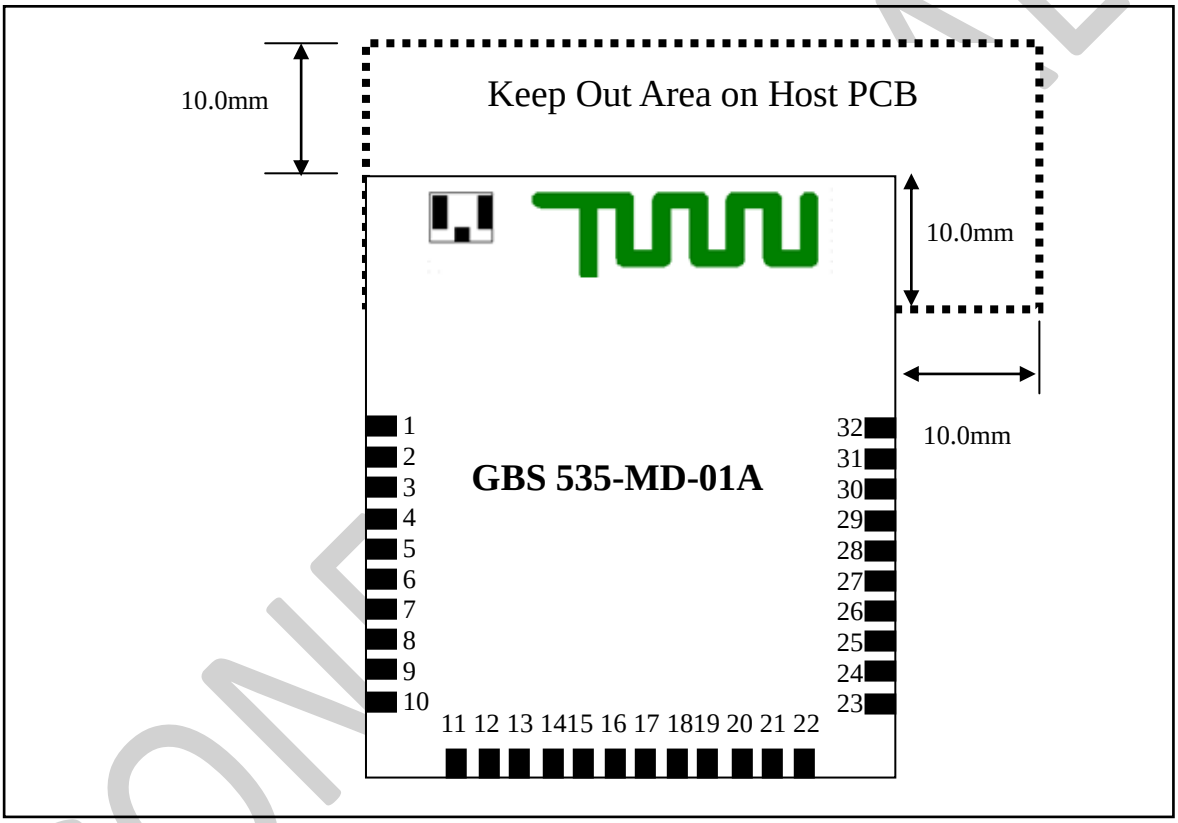
## 8. Recommended HOST PCB Keep Out Area

It is required to have a keep out area on the customer's HOST PCB underneath of the GBS 535-MD-01A if the printed antenna is used. Metal components, traces, ground fill or the presence of any other components within the keep out area will affect the performance and the radiation pattern of the printed antenna. Ensure that there is no exposed copper in the keep out area on mounting. The recommended HOST PCB keep out area is shown in figure 8.1.

Fig 8.1 The Recommended Keep Out Area of Host PCB







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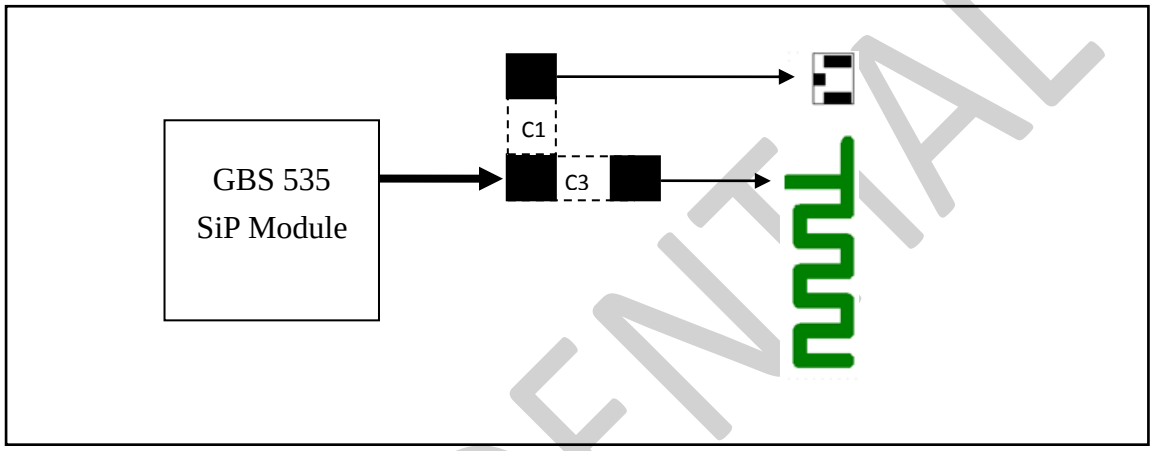
## 9. External Antenna

The GBS 535-MD-01A/GBS 535-MD-01AP implements the on board printed antenna and the GBS 535-MD-01B/GBS 535-MD-01BP uses the U.FL connector for the external antenna. The co-layout capacitors, C1, C3 as shown in figure 9.1, are designed to satisfy the antenna option. Mount the C1, a 10 PF capacitor if the external antenna is used.

Figure 9.1 Co-layout diagram of C1 and C3




The antenna optional and the corresponding capacitor is listed in Table 9.1.

Table 9.1 Part number of the GBS 535-MD-01A series

| Type of Antenna | Type of Antenna | Capacitor |
|---|---|---|
| GBS 535-MD-01A<br>GBS 535-MD-01AP | Printed antenna | C3 |
| GBS 535-MD-01B<br>GBS 535-MD-01BP | U. FL. connector | C1, 10PF, 0402 type |

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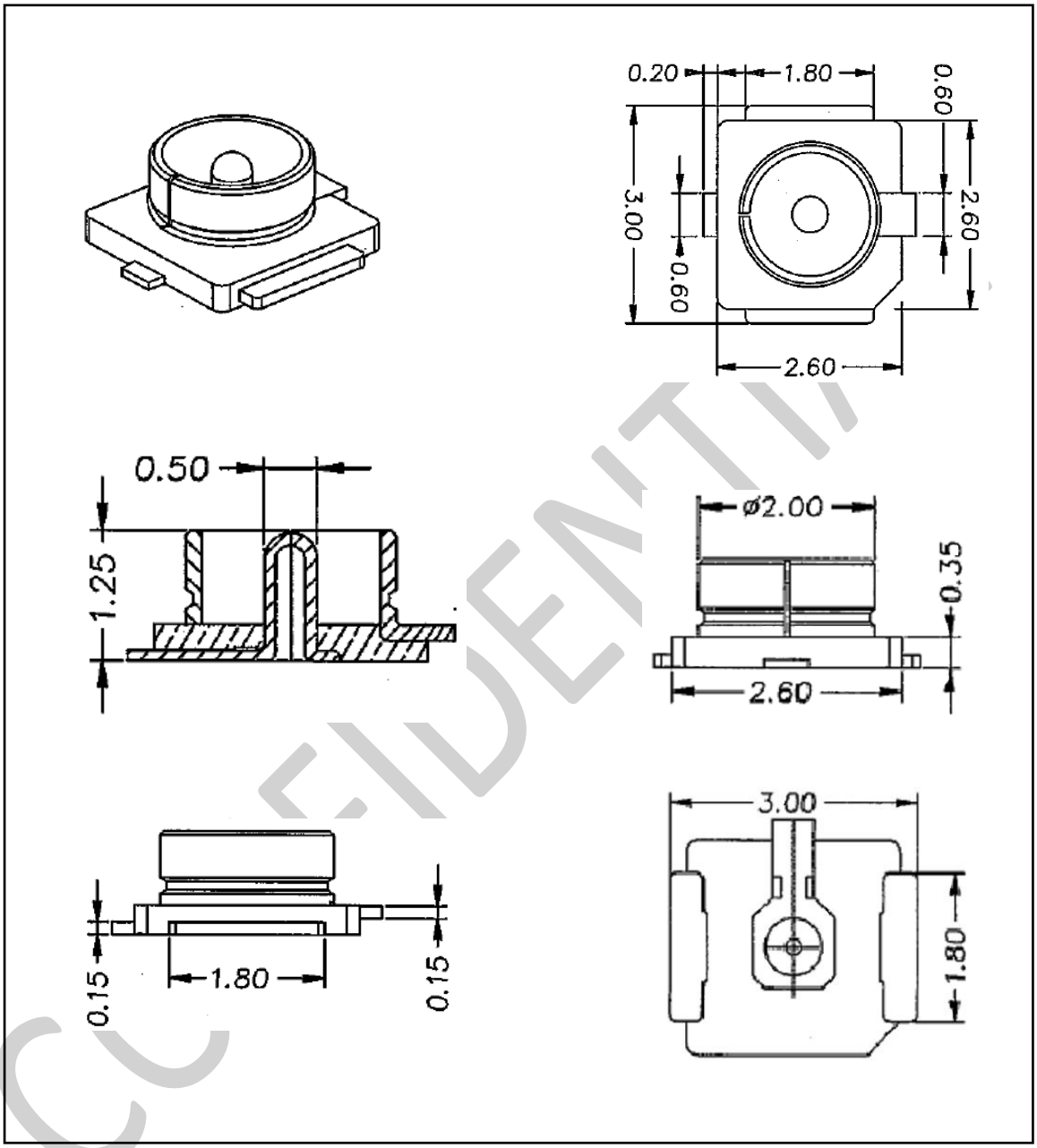
The dimension of the U.FL connector is shown in figure 9.3.

Figure 9.3 The dimension of the U.FL connector Unit : mm







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# 10. Wi-Fi Specification

## 10. 1 IEEE 802.11 Feature and Standard

The GBS 535-MD-01A complies with the following 802.11 features and standards.

Table 10.1.1 The WLAN feature and standard

| Features | Description |
|---|---|
| **WLAN Standards** | IEEE 802 Part 11b/g/n (802.11b/g/n single stream) |
| **Antenna Port** | Support single antenna for Wi-Fi |
| **Frequency Band** | 2.400 – 2.4835 GHz |

The RF performance is given as follows. The default voltage is 3.3V.

Table 10.1.2 The RF performance of the GBS 535-MD-01A

| Features | Description |
|---|---|
| Frequency Band | 2.4000 – 2.4835 GHz (2.4 GHz ISM Band) |
| Number of selectable Sub channels | 11 channels |
| Modulation | OFDM, DSSS, DBPSK, DQPSK, CCK , 16QAM, 64QAM |
| Supported Rate | 1, 2, 5.5, 11, 6, 9, 12, 24, 36, 48, 54 Mbps &<br>HT20 MCS 0~7 |
| Maximum Receive Input | - 10dBm (with PER < 8%@11 Mbps)<br>- 20dBm (with PER < 10%@54 Mbps)<br>- 20dBm (with PER < 10%@MCS7) |
| Output Power | 17dBm @ 802.11b<br>13dBm @ 802.11g<br>11dBm @ 802.11n |
| Carrier Frequency Accuracy | +/- 20ppm (crystal: 26MHz +/-10ppm in $25^0$C) |




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## 10.2 802.11b Specification

Table 10.2.1 The RF Specifications of 802.11b

| Features | Description |
|---|---|
| Frequency Band | 2.4000 – 2.4835 GHz (2.4 GHz ISM Band) |
| Number of Selectable Sub Channel | 11 channels |
| Modulation | OFDM |
| Data Rate | 1, 2, 5.5, 11 Mbps |
| Carrier Frequency Accuracy | +/- 20ppm (crystal: 26MHz +/-10ppm in $25^0$C) |

Table 10.2.2 The RF transmitter performance of 802.11b

| RF Transmitter, 802.11b | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Output Power (1, 2, 5.5, 11Mbps) | 15.5 | 17 | 18.5 | dBm |
| Center frequency tolerance | -20 | 0 | 20 | ppm |
| **Spectrum Mask** | | | | |
| Fc-22MHz < F < Fc-11MHz & Fc+11MHz < F < Fc+22MHz | | | -30* | dBr |
| F< Fc-22MHz & F > Fc+22MHz | | | -50* | dBr |
| Power-on (10% ~ 90 %) | | 0.3 | 2* | us |
| Power-down (90% ~ 10 %) | | 1.5 | 2* | us |
| Modulation Accuracy | | -17 | -10 | dB |

"*" indicates IEEE802.11 specification.

Table 10.2.3 The RF receiver performance of GBS 535-MD-01A

| RF Receiver, 802.11b | Data Rate | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Minimum Input Sensitivity (PER< 8 % )** | 1Mbps | | -90 | -80* | dBm |
| | 2Mbps | | -90 | -80* | dBm |
| | 5.5Mbps | | -90 | -76* | dBm |
| | 11Mbps | | -87 | -76* | dBm |
| **Maximum Input Sensitivity (PER< 8 % )** | 1/2/5.5/11 Mbps | | | -10* | dBm |

"*" indicates IEEE802.11 specification.


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## 10.3 802.11g Specification

Table 10.3.1 The RF transmitter specification, 802.11g

| 802.11g Transmit | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Output Power** | 6M/9M/12M/18M/ 24M/36M/48M/54 M | 11.5 | 13 | 14.5 | dBm |
| | | | | | dBm |
| | | | | | dBm |
| **Center Frequency Tolerance** | | -20 | 0 | 20 | ppm |
| **Modulation Accuracy** | 6Mbps | | -30 | -5* | dB |
| | 9Mbps | | -30 | -8* | dB |
| | 12Mbps | | -30 | -10* | dB |
| | 18Mbps | | -30 | -13* | dB |
| | 24Mbps | | -30 | -16* | dB |
| | 36Mbps | | -30 | -19* | dB |
| | 48Mbps | | -30 | -22* | dB |
| | 54Mbps | | -30 | -25* | dB |
| **Spectrum Mask** | @ 11MHz | | | -20* | dBr |
| | @ 20MHz | | | -28* | dBr |
| | @ 30MHz | | | -40* | dBr |

"*" indicates IEEE802.11 specification.

Table 10.3.2 The RF receiver specification, 802.11g

| 802.11g Transmit | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Minimum Input Sensitivity (PER<10 % )** | 6Mbps | | -85 | -82* | dBm |
| | 9Mbps | | -85 | -81* | dBm |
| | 12Mbps | | -85 | -79* | dBm |
| | 18Mbps | | -84.5 | -77* | dBm |
| | 24Mbps | | -82 | -74* | dBm |
| | 36Mbps | | -78.5 | -70* | dBm |
| | 48Mbps | | -74 | -66* | dBm |
| | 54Mbps | | -70 | -65* | dBm |
| **Maximum Input Sensitivity (PER<10%)** | 6/9/12/18/24/36/48 /54Mbps | | | -20* | dBm |

"*" indicates IEEE802.11 specification.


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## 10.4 802.11n Specification

Table 10.4.1 The RF transmitter specification, 802.11n

| 802.11n Transmit | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Output Power (**HT20 MCS 0~7) | | 9.5 | 11 | 12.5 | dBm |
| **Center Frequency Tolerance** | | -20 | 0 | 20 | ppm |
| **Modulation Accuracy (**HT20, MCS0~7) | | | -30 | -28* | dB |
| **Spectrum Mask** | @ 11MHz | | | -20* | dBr |
| | @ 20MHz | | | -28* | dBr |
| | @ 30MHz | | | -40* | dBr |

"*" indicates IEEE802.11 specification.

Table 10.4.2 The RF receiver specification, 802.11n

| 802.11n Receiver | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Minimum Input Sensitivity (PER<10 % )** | HT20, MCS0 | | -84 | -82* | dBm |
| | HT20, MCS1 | | -84 | -79* | dBm |
| | HT20, MCS2 | | -82.5 | -77* | dBm |
| | HT20, MCS3 | | -80.5 | -74* | dBm |
| | HT20, MCS4 | | -77 | -70* | dBm |
| | HT20, MCS5 | | -73 | -66* | dBm |
| | HT20, MCS6 | | -71 | -65* | dBm |
| | HT20, MCS7 | | -70 | -64* | dBm |
| **Maximum Input Sensitivity (PER<10%)** | MSC0~MSC7 | | | -20* | dBm |

"*" indicates IEEE802.11 specification.


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# 11. Communications Interface

## 11.1 I2C Interface Characteristics

Table 11.1.1 I2C interface Characteristics

| Symbol | Parameter | Standard mode $I^2C$(1) | | Fast mode $I^2C$(1)(2) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | - | 1.3 | - | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | - | 0.6 | - | |
| $t_{su(SDA)}$ | SDA setup time | 250 | - | 100 | - | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0(3) | - | 0(4) | 900(3) | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | - | 1000 | $20 + 0.1C_b$ | 300 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | - | 300 | - | 300 | |
| $t_{h(STA)}$ | Start condition hold time | 4.0 | - | 0.6 | - | µs |
| $t_{su(STA)}$ | Repeated Start condition setup time | 4.7 | - | 0.6 | - | |
| $t_{su(STO)}$ | Stop condition setup time | 4.0 | - | 0.6 | - | µs |
| $t_{w(STO:STA)}$ | Stop to Start condition time (bus free) | 4.7 | - | 1.3 | - | µs |
| $C_b$ | Capacitive load for each bus line | - | 400 | - | 400 | pF |

1. Guaranteed by design, not tested in production.
2. $f_{PCLK1}$ must be at least 2 MHz to achieve standard mode I2C frequencies. It must be at least 4MHz to achieve fast mode I2C frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum I2C fast mode clock.
3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.




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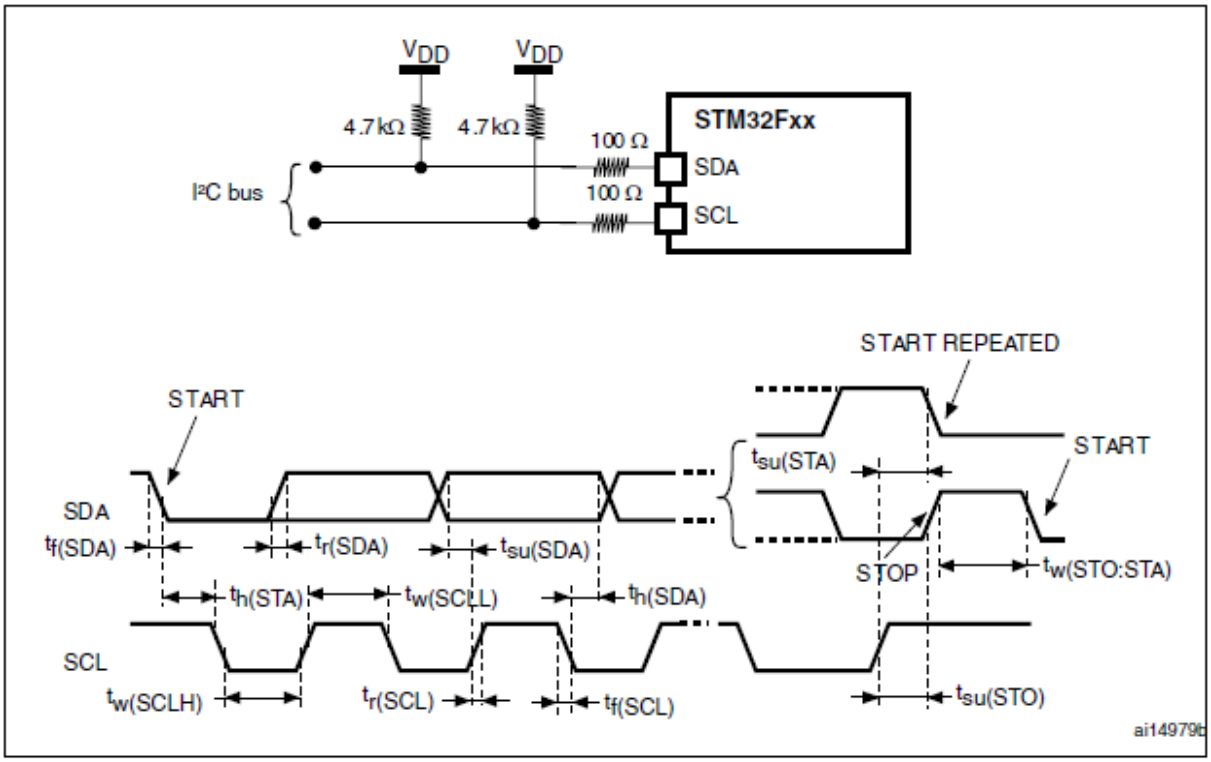
Figure 11.1 I2C timing diagram




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

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## 11.2 SPI Interface Characteristics

Table 11.2.1 SPI interface Characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI clock frequency | Master mode | - | 30 | MHz |
| | | Slave mode | - | 30 | |
| $t_{r(SCL)}$<br>$t_{f(SCL)}$ | SPI clock rise and fall time | Capacitive load: C = 30 pF | - | 8 | ns |
| DuCy(SCK) | SPI slave input clock duty cycle | Slave mode | 30 | 70 | % |
| $t_{su(NSS)}$ (2) | NSS setup time | Slave mode | $4t_{PCLK}$ | - | ns |
| $t_{h(NSS)}$ (2) | NSS hold time | Slave mode | $2t_{PCLK}$ | - | |
| $t_{w(SCLH)}$ (2)<br>$t_{w(SCLL)}$ (2) | SCK high and low time | Master mode, $f_{PCLK}$ = 30 MHz, presc = 2 | $t_{PCLK}$-3 | $t_{PCLK}$+3 | |
| $t_{su(MI)}$ (2)<br>$t_{su(SI)}$ (2) | Data input setup time | Master mode | 5 | - | |
| | | Slave mode | 5 | - | |
| $t_{h(MI)}$ (2)<br>$t_{h(SI)}$ (2) | Data input hold time | Master mode | 5 | - | |
| | | Slave mode | 4 | - | |
| $t_{a(SO)}$ (2)(3) | Data output access time | Slave mode, $f_{PCLK}$ = 20 MHz | 0 | $3t_{PCLK}$ | |
| $t_{dis(SO)}$ (2)(4) | Data output disable time | Slave mode | 2 | 10 | |
| $t_{v(SO)}$ (2)(1) | Data output valid time | Slave mode (after enable edge) | - | 25 | |
| $t_{v(MO)}$ (2)(1) | Data output valid time | Master mode (after enable edge) | - | 5 | |
| $t_{h(SO)}$ (2) | Data output hold time | Slave mode (after enable edge) | 15 | - | |
| $t_{h(MO)}$ (2) | | Master mode (after enable edge) | 2 | - | |

1. Remapped SPI1 characteristics to be determined.
2. Based on characterization, not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z


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# 12. Power Consumption

## 12.1 WLAN Sub-System

Voltage reference : VBAT @ 3.6V, 20°C, VDDIO = 1.8V, CBUCK out = 1.5V

Table 12.1.1 WLAN sub-system power consumption

| Operational Modes | Condition | Typical | Unit |
|---|---|---|---|
| **OFF** | 1 | 11 | uA |
| **OFF** | 2 | 40 | uA |
| **IDLE** | | 185 | uA |
| **SLEEP** | 5 | 200 | uA |
| **Rx** (Listen) | 3 | 52 | mA |
| **Rx** (Active) | 4 | 59 | mA |
| **Power Save** | 6, 9 | 1.9 | mA |
| **Tx CCK** (11 Mbps at 18.5 dBm) | 7, 11 | 320 | mA |
| **Tx OFDM** (54 Mbps at 15.5 dBm) | 8,11 | 270 | mA |
| **Tx OFDM** (65 Mbps at 14.5 dBm) | 10, 11 | 260 | mA |

Note 1: WL_RST_N = Low, VDDIO is not present

Note 2: WL_RST_N = Low, VDDIO is present

Note 3: Carrier Sense (CCA) when no carrier present

Note 4: Carrier Sense (CS) detect/Packet Rx

Note 5: Intra-beacon Sleep

Note 6: Beacon Interval = 102.4 ms, DTIM = 1, Beacon duration = 1 ms @1 Mbps Integrated Sleep + wakeup + Beacon Rx current over 1 DTIM interval

Note 7: CCK power at chip port. Duty cycle is 100%. Includes PA contribution at 3.6V

Note 8: OFDM power at chip port. Duty cycle is 100%. Includes PA contribution at 3.6V

Note 9: In WLAN power-saving mode, the following blocks are powered down: Crystal oscillator, Baseband PLL, AFE, RF PLL, Radio

Note 10: OFDM power at chip port is 16 dBm, duty cycle is 100%, includes PA contribution at 3.6V

The above blocks are turned ON in the required order with sufficient time for them to settle.

This sequencing is done by the PMU controller that controls the settling





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## 12.2 MCU Sub-System

Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled) is listed in the Table 12.2.1.

Table 12.2.1 Typical and maximum current consumption in Run mode code with data processing running from Flash memory (ART accelerator disabled)

| Operational Mode | Conditions | $f_{HCLK}$ | Typical | Maximum(1) | | Unit |
|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| Supply Current in Run mode | External clock(2), all peripherals enabled(3) | 120 MHz | 61 | 81 | 93 | mA |
| | | 90 MHz | 48 | 68 | 80 | |
| | | 60 MHz | 33 | 53 | 65 | |
| | | 30 MHz | 18 | 38 | 50 | |
| | | 25 MHz | 14 | 34 | 46 | |
| | | 16 MHz(4) | 10 | 30 | 42 | |
| | | 8 MHz | 6 | 26 | 38 | |
| | | 4 MHz | 4 | 24 | 36 | |
| | | 2 MHz | 3 | 23 | 35 | |
| | External clock(3), all peripherals disabled | 120 MHz | 33 | 54 | 66 | |
| | | 90 MHz | 27 | 47 | 59 | |
| | | 60 MHz | 19 | 39 | 51 | |
| | | 30 MHz | 11 | 31 | 43 | |
| | | 25 MHz | 8 | 28 | 41 | |
| | | 16 MHz(4) | 6 | 26 | 38 | |
| | | 8 MHz | 4 | 24 | 36 | |
| | | 4 MHz | 3 | 23 | 35 | |
| | | 2 MHz | 2 | 23 | 34 | |

1. Based on characterization, tested in production at VDD max and $f_{HCLK}$ max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when $f_{HCLK}$ > 25 MHz.
3. When the ADC is on (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
4. In this case HCLK = system clock/2.
5. The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry standard ARM® Cortex™-M3 processors.




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Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM [1] is listed in the Table 12.2.2.

Table 12.2.2 Typical and maximum current consumption (ART accelerator enabled)

| Operational Mode | Conditions | $f_{HCLK}$ | Typ | Max[2] | | Unit |
|---|---|---|---|---|---|---|
| | | $f_{HCLK}$ | $T_A$ =25 °C | $T_A$ =85°C | $T_A$ =105 °C | |
| Supply Current in Run mode | External clock[3], all peripherals enabled[4] | 120 MHz | 49 | 63 | 72 | mA |
| | | 90 MHz | 38 | 51 | 61 | |
| | | 60 MHz | 26 | 39 | 49 | |
| | | 30 MHz | 14 | 27 | 37 | |
| | | 25 MHz | 11 | 24 | 34 | |
| | | 16 MHz[5] | 8 | 21 | 30 | |
| | | 8 MHz | 5 | 17 | 27 | |
| | | 4 MHz | 3 | 16 | 26 | |
| | | 2 MHz | 2 | 15 | 25 | |
| | External clock[3], all peripherals disabled | 120 MHz | 21 | 34 | 44 | |
| | | 90 MHz | 17 | 30 | 40 | |
| | | 60 MHz | 12 | 25 | 35 | |
| | | 30 MHz | 7 | 20 | 30 | |
| | | 25 MHz | 5 | 18 | 28 | |
| | | 16 MHz[5] | 4.0 | 17.0 | 27.0 | |
| | | 8 MHz | 2.5 | 15.5 | 25.5 | |
| | | 4 MHz | 2.0 | 14.7 | 24.8 | |
| | | 2 MHz | 1.6 | 14.5 | 24.6 | |

1. Code and data processing running from SRAM1 using boot pins.
2. Based on characterization, tested in production at VDD max and $f_{HCLK}$ max with peripherals enabled.
3. External clock is 4 MHz and PLL is on when $f_{HCLK}$ > 25 MHz.
4. When the ADC is on (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part
5. In this case HCLK = system clock/2.




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# 13. Electrical Specification

## 13.1 Absolute Maximum Rating

Table 13.1.1 Absolute maximum rating

| **Supply Power** | Maximum +4 Volt | | |
|---|---|---|---|
| **Voltage ripple** | +/- 2% | Maximum values not exceeding operating voltage. | |
| | Power | Minimum | Maximum |
| **Power Supply Absolute Maximum Ratings** | VBAT | 0 | 4 |
| | VDD_3V3 | 0 | 4 |
| | VDD_3V3_WIFI | 0 | 6 |

## 13.2 Power Supply

Power supply of the GBS 535-MD-01A is provided by the host system via the power pins of the GBS 535-MD-01A.

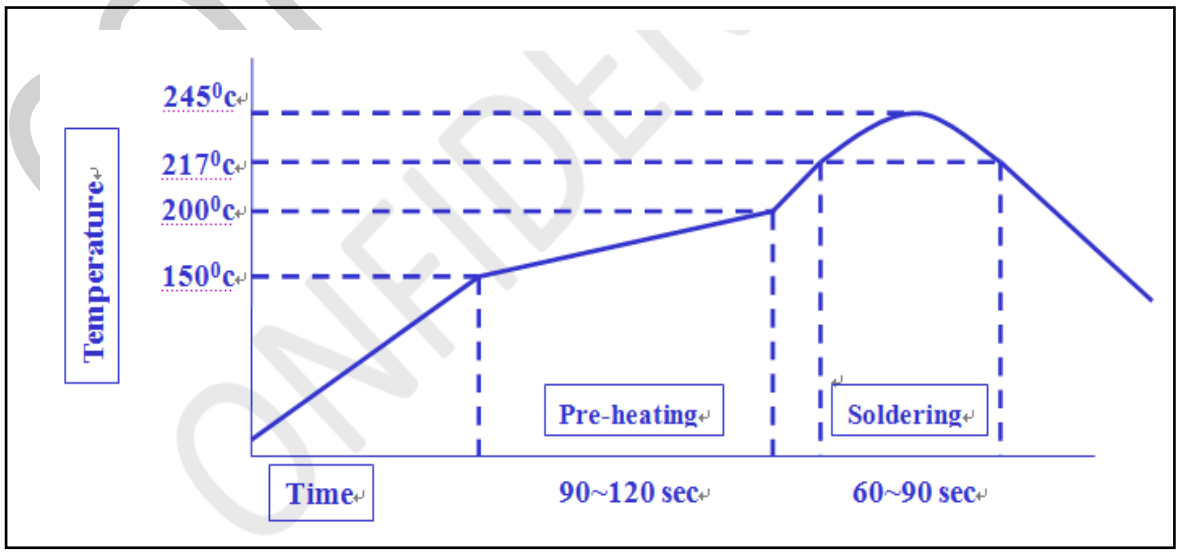
Table 13.2.1 Power supply

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **VBAT** | MCU VBAT Voltage | 2.0 | 3.3 | 3.6 | V |
| **VDD_3V3** | GPIO I/O Supply | 2.4 | 3.3 | 3.6 | V |
| **VDD_3V3_WIFI** | Wi-Fi Voltage/ Wi-Fi PA Voltage | 3.0 | 3.3 | 3.6 | V |

# 14. Recommended Reflow Profile

The recommended solder reflow temperature profile is shown in figure 15.1.

Figure 14.1 Solder reflow temperature profile





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## 15. Storage Condition

The recommended storage temperature and humidity condition of the GBS 535-MD-01A is listed in the Table 14.1.

Table 15.1 Storage condition

| Item | Condition | Remark |
|---|---|---|
| Operating Temperature | -40° to 85° Celsius | |
| Humidity range | Maximum 95% | Non condensing, relative humidity. |




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## 16. Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

. Reorient or relocate the receiving antenna.
. Increase the separation between the equipment and receiver.
. Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
. Consult the dealer or an experienced radio/TV technician for help.

***FCC Caution***: To assure continued compliance, any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. (Example - use only shielded interface cables when connecting to computer or peripheral devices).

### End Product Labeling

This transmitter module is authorized only for use in devices where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in visible area with the following: “Contains FCC ID: 2ABVG-001”

”

### End Product Manual Information

The user manual for end users must include the following information in a prominent location “IMPORTANT NOTE: To comply with FCC RF exposure compliance requirements, the antenna used for this transmitter must be installed to provide a separation distance of at least 20cm from all persons and must not be colocated or operating in conjunction with any other antenna or transmitter.” This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions (1) This device may not cause harmful interference and (2) This device must accept any interference received, including interference that may cause undesired operation.




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IMPORTANT NOTE: In the event that these conditions can not be met (for example certain laptop configurations or colocation with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for reevaluating the end product (including the transmitter) and obtaining a separate FCC authorization. This device is intended only for OEM integrators under the following conditions: The antenna must be installed such that 20 cm is maintained between the antenna and users. As long as a condition above is met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).




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## 17. Sales and Service

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