W-LAN+Bluetooth Combo Module Data Sheet

Texas Instruments Chipset for 802.11b/g/n + Bluetooth 4.0

Tentative P/N : LBEH59XUHC-TEMP

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Revision History

Revision Code	Date	Description	Comments
-	2011/3/2	First Issue	
A	2011/8/4	P2; Add RoHS Compliance P33; Delete the Amount of Solder Paste	

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1. Scope

This specification is applied to the IEEE802.11 b/g/n + Bluetooth 4.0 module.

Interface
- W-LAN : SDIO, SPI
- Bluetooth : UART, PCM

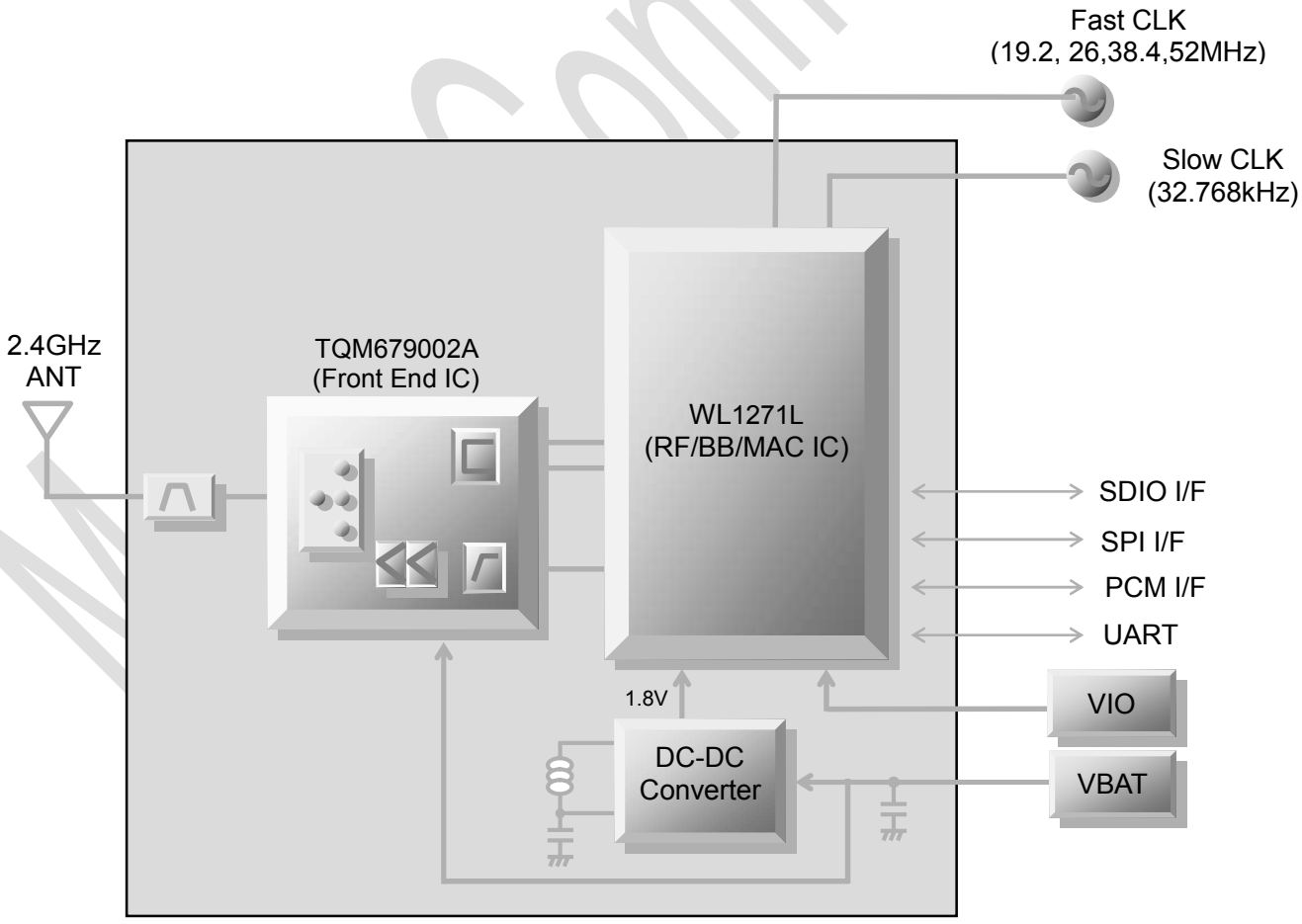
IC/Firmware
- W-LAN/BT/FM(Tx/Rx) BB/MAC : WL1271L (PG3.1)
- FEM for WL1271L : TriQuint TQM679002A (E2.6)

Reference Clock : External Reference Clock is required.
Sleep Clock : External 32.768kHz oscillator is required.
Weight : 234(mg)
MSL : Level3
RoHS Compliance

2. Part Number

Sample Part Number	LBEH59XUHC–TEMP

3. Block Diagram



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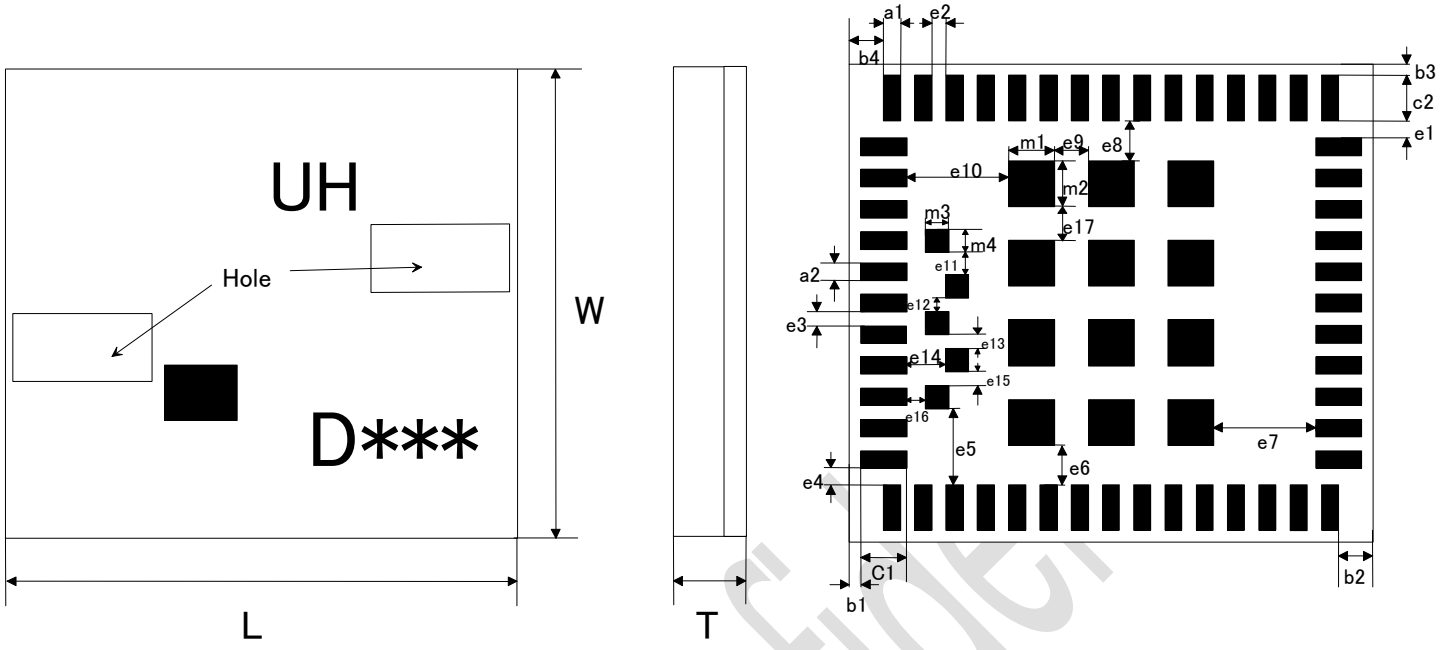
4. Dimensions and Terminal Configurations

<Top View> <Side View> <Bottom View>



Dimensions

Mark	Dimensions	Mark	Dimensions	Mark	Dimensions
L	9.2 +/- 0.2	W	8.4 +/- 0.2	T	1.35 max.
a1	0.3 +/- 0.1	a2	0.3 +/- 0.1	b1	0.2 +/- 0.2
b2	0.6 +/- 0.2	b3	0.2 +/- 0.2	b4	0.6 +/- 0.2
c1	0.8 +/- 0.1	c2	0.8 +/- 0.1	e1	0.3 +/- 0.1
e2	0.25 +/- 0.1	e3	0.25 +/- 0.1	e4	0.3 +/- 0.1
e5	1.35 +/- 0.1	e6	0.7+/- 0.1	e7	1.8 +/- 0.1
e8	0.7+/- 0.1	e9	0.6 +/- 0.1	e10	1.8+/- 0.1
e11	0.4 +/- 0.1	e12	0.25 +/- 0.1	e13	0.25 +/- 0.1
e14	0.7 +/- 0.1	e15	0.25+/- 0.1	e16	0.35 +/- 0.1
e17	0.6 +/- 0.1	m1	0.8 +/- 0.1	m2	0.8 +/- 0.1
m3	0.4 +/- 0.1	m4	0.4 +/- 0.1	-	-

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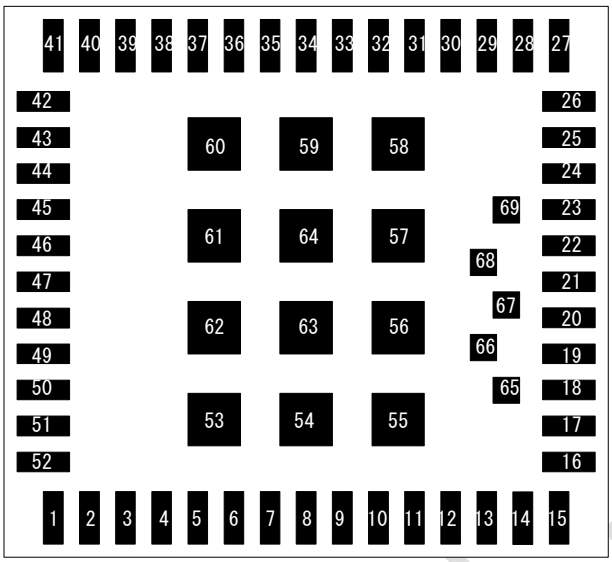
Terminal configuration



<Top View>

No.	Terminal Name	Type	Power	System	Connection to IC Terminal		Description
1	FM_I2S_DO/PCM_OUT	I/O		BT	1271L	AUD_OUT	PCM I/F
2	FM_I2S_DI/PCM_IN	I/O		BT	1271L	AUD_IN	PCM I/F
3	HOST_WAKE	I/O	-	BT	1271L	BT_FUNC5	HOST Wake Up
4	CLK_REQ	I/O	-	-	1271L	CLK_REQ_OUT	CLK_REQ_positive polarity
5	BT_RESETX	I	-	BT	1271L	BT_EN	BT_RST
6	WLAN_IRQ	O	-	WLAN	1271L	WLAN_IRQ	WLAN interrupt request
7	GND	-	-	-	1271L	FM_EN	Ground
8	NC	-	-	-	1271L	FM_I2S_DI	NC
9	NC	-	-	-	1271L	FM_I2S_FSYNC	NC
10	NC	-	-	-	1271L	FM_I2S_CLK	NC
11	NC	-	-	-	1271L	FM_I2S_DO	NC
12	WL_RS232_TX	I/O	-	WLAN	1271L	WL_RS232_Tx	RS232_Tx or I2C_M_SDA
13	WL_RS232_RX	I/O	-	WLAN	1271L	WL_RS232_Rx	RS232_Rx or I2C_M_SCL
14	WLAN_EN	I	-	WLAN	1271L	WL_EN	WL_RST
15	GND	-	-	-	-	-	Ground
16	SDIO_D2	I/O	-	WLAN	1271L	SDIO_D2	SDIO mode: DATA 2
17	SDIO_D1	I/O	-	WLAN	1271L	SDIO_D1	SDIO mode: DATA 1
18	SDIO_CMD/SPI_DIN	I/O	-	WLAN	1271L	SPI_DIN	SDIO mode: CMD SPI mode: SPI_MOSI
19	SDIO_CLK/SPI_CLK	I	-	WLAN	1271L	SPI_CLK	SDIO mode: CLK SPI mode: SPI_CLK
20	SDIO_D0/SPI_DOUT	I/O	-	WLAN	1271L	SPI_DOUT	SDIO mode: DATA 0 SPI mode: SPI_MISO
21	SDIO_D3/SPI_CSX	I/O	-	WLAN	1271L	SPI_CSX	SDIO mode :DATA 3 SPI mode: SPI_CSX
22	GND	-	-	-	-	-	Ground
23	SLEEP_CLK	I	-	-	1271L	SLOWCLK	SLEEP_CLK input
24	GND	-	-	-	-	-	Ground
25	NC	-	-	-	1271L	FMRFOUTP	NC
26	GND	-	-	-	-	-	Ground
27	GND	-	-	-	1271L	FMRFINP	Ground
28	GND	-	-	-	-	-	Ground
29	GND	-	-	-	1271L	FMAUDRIN	Ground

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30	GND	-	-	-	1271L	FMAUDLIN	Ground
31	NC	-	-	-	1271L	FMAUDLOUT	NC
32	NC	-	-	-	1271L	FMAUDROUT	NC
33	BT_WAKEUP	IO	-	BT	1271L	BT_FUNC2	BT_WU/BT DC2DC or BT_IRQ
34	GND	-	-	-	-	-	Ground
35	XTALP	-	-	-	1271L	XTALP	FREF input
36	XTALM	-	-	-	1271L	XTALM	FREF input
37	GND	-	-	-	-	-	Ground
38	VIO	P	-	-	1271L	VDDS1 VDDS2 VDDS3 VDDS4	Power supply input
39	1V8_PRE_REG	P	-	-	1271L/ LDO	DCDC, VIN_DIG_LDO VDD1P8VFM LDO_INW VDD_LDO_INBT LDO_IN_DCOW	Monitor pin for feed back voltage from DCDC converter
40	VDD_LDO_IN_CLASS1P5	P	-	-	1271L	VDD_LDO_IN_CLASS1P5	For choosing BT operation mode. Details are described on reference schematic.
41	VBAT	P	-	-	1271L/ LDO	PMS VBAT, DCDC Converter	Power supply input
42	GND	-	-	-	-	-	Ground
43	UART_CTS	I/O	-	BT	1271L	HCI_CTS	BT UART I/F or BT SPI_CS
44	UART_RTS	I/O	-	BT	1271L	HCI_RTS	BT UART I/F or BT SPI_IRQ
45	UART_TX	I/O	-	BT	1271L	HCI_TX	BT UART I/F or BT SPI_DOUT
46	UART_RX	I/O	-	BT	1271L	HCI_RX	BT UART I/F or BT SPI_DIN
47	GND	-	-	-	-	-	Ground
48	GND	-	-	-	-	-	Ground
49	2.4G_ANT	I/O	-	BT/ WLAN	-	-	RF transmitter output and RF receiver input
50	GND	-	-	-	-	-	Ground
51	FM_I2S_FSYNC/PCM_FSYNC	I/O	-	BT	1271L	AUD_FSYNC	PCM I/F
52	FM_I2S_CLK/PCM_CLK	I/O	-	BT	1271L	AUD_CLK	PCM I/F
53	GND	-	-	-	-	-	Ground
54	GND	-	-	-	-	-	Ground
55	GND	-	-	-	-	-	Ground
56	GND	-	-	-	-	-	Ground
57	GND	-	-	-	-	-	Ground
58	GND	-	-	-	-	-	Ground
59	GND	-	-	-	-	-	Ground
60	GND	-	-	-	-	-	Ground
61	GND	-	-	-	-	-	Ground
62	GND	-	-	-	-	-	Ground
63	GND	-	-	-	-	-	Ground
64	GND	-	-	-	-	-	Ground
65	NC	-	-	-	1271L	FM_SCL	NC
66	WL_UART_DBG	I/O	-	WLAN	1271L	WL_UART_DBG	WL_UART_DBG Should be connected to TP on board for software debug.
67	NC	-	-	-	1271L	FM_IRQ	NC
68	NC	-	-	-	1271L	FM_SDA	NC
69	BT_UART_DBG	I/O	-	BT	1271L	BT_FUNC4	BT_UART_DBG

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							Should be connected to TP for software debug.

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5. Rating

Parameter		min.	max	unit
Storage Temperature		-40	85	deg.C
Supply Voltage	VBAT	-0.5	4.8	V
	VIO	-0.5	2.1	V

6. Operating Condition

Parameter		min.	max	unit
Operating Temperature		-20	70	deg.C
Supply Voltage	VBAT	2.7	4.8	V
	VIO	1.65	1.92	V

7. Input/Output Terminal Characteristic

	Condition	min.	max	unit
V_{IH} : High-level input voltage(VDD_IO = IO supply for ring)	Default	0.7 x VIO	VIO	V
V_{IL} : Low-level input voltage	Default	0	0.35 x VIO	V
V_{OH} : High-level output voltage	4mA	VIO - 0.45	VIO	V
	1mA	VIO - 0.112	VIO	V
	0.3mA	VIO-0.033	VIO	V
V_{OL} : Low-level output voltage	4mA	0	0.45	V
	1mA	0	0.112	V
	0.09mA	0	0.01	V

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8. External Fast Clock specification

8.1 External Fast Clock Source Requirements (-40℃ to +85℃)

Characteristics(1)(2)	Condition	Sym	min.	Typ.	max	unit
Supported frequencies		Fref		19.2,26, 38.4,52		MHz
Reference frequency acuuracy	Initial + temp + aging				±20	ppm
Clock input voltage limits	AC coupled(sine wave)		500(1)(3)		1200	mVp-p
	Digital		0		VIO	V
Duty Cycle			35	50	65	%
Sine wave clock harmonics	2nd harmonic				-30	dBc
	3rd harmonic				-14	dBc
	4th harmonic				-30	dBc
Rise/Fall times	Square-wave clock	Tr/Tf			10	% of clock period

Setting time	Time from asserting CLK_REQ/CLKREQ_n until Clock is available at device input					20	20	20	20	ms
Phase noise	FM,BT,WLAN b/g modes(200mVp-p min amplitude)	Off set				**19.2MHz**	**26MHz**	**38.4MHz**	**52MHz**	dBc/Hz
		1kHz				-126	-123.4	-120	-117.3	
		10kHz				-136	-133.4	-130	-127.3	
		100kHz				-141	-138.4	-135	-132.3	

(1) The slope of the clock at zero-crossings should not be less than that of a 200 mVpp sine-wave.
(2) System clock is a fail safe input.
(3) If operated at 200mVpp, TX EVM may degrade by approximately 1dB.

8.2 External Fast Clock Port Characteristics

Rating	Condition	Sym	Min	Typ	Max	Unit
Fref input impedance(1)	Does not change in different operating modes	Rp	30			kohm
	Does not change in different operating modes	Cp		2.4	3.3	pF

(1) For 52MHz Fref clock Rp can be up to 10kohm less.

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8.3 External Fast Clock Crystal Requirements and Operation

Characteristics[(1)(2)]	Condition	Sym	min.	Typ.	max	unit
Supported frequencies		Fin		26,38.4		MHz
Frequency acuuracy	Initial + temp + aging				±20	ppm
Crystal oscillator negative resistance	38.4MHz external capacitor=8pF, Iosc=500uA		228	284		ohm
	38.4MHz external capacitor=20pF, Iosc=2.2mA		192	285		ohm

9.External Slow Clock specification

Characteristics(*)	Condition	min.	Typ.	max	unit
Input slow clock frequency			32.768		kHz
Input slow clock accuracy	WLAN, BT,			±150	ppm
Input transition time Tr/Tf -10% to 90%	Tr/Tf			100	ns
Frequency input duty cycle		30	50	70	%
Input voltage limits	Square wave, DC-coupled	0.65 × VIO		VIO	V
		0		0.35 × VIO	V
Input impedance		1			MΩ
Input capacitance				5	pF
Rise and fall time				100	ns
Phase noise				-125	dBc/Hz

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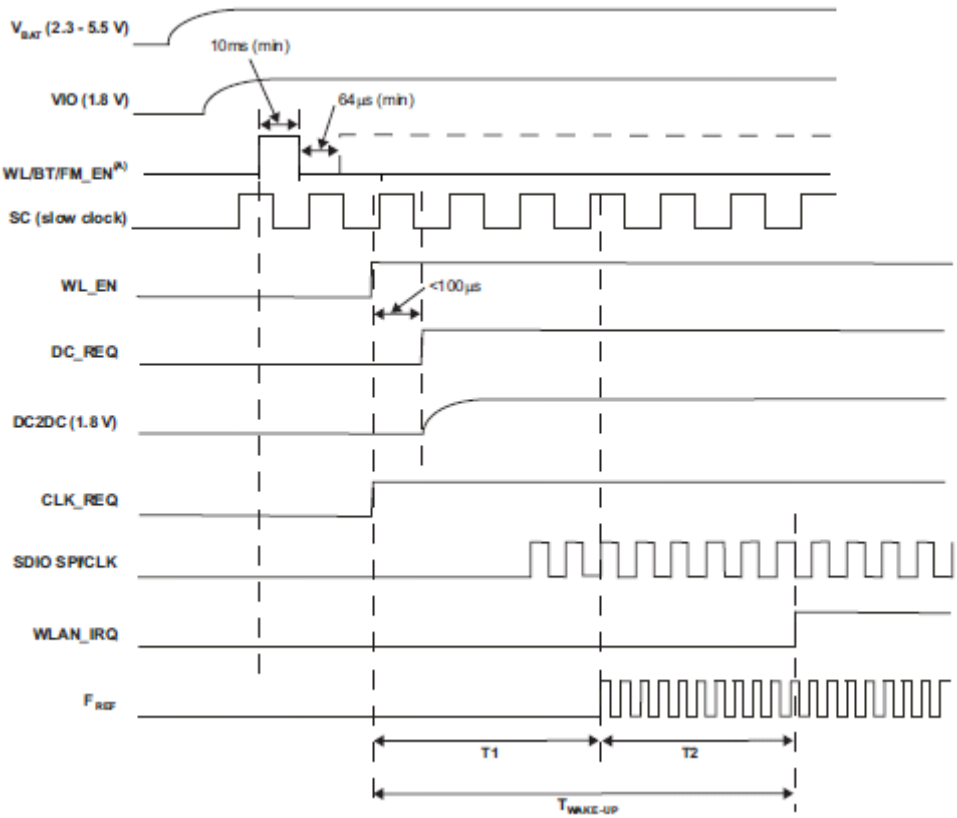
10. WLAN Power Up/Down Sequence

10.1 Power Up Sequence



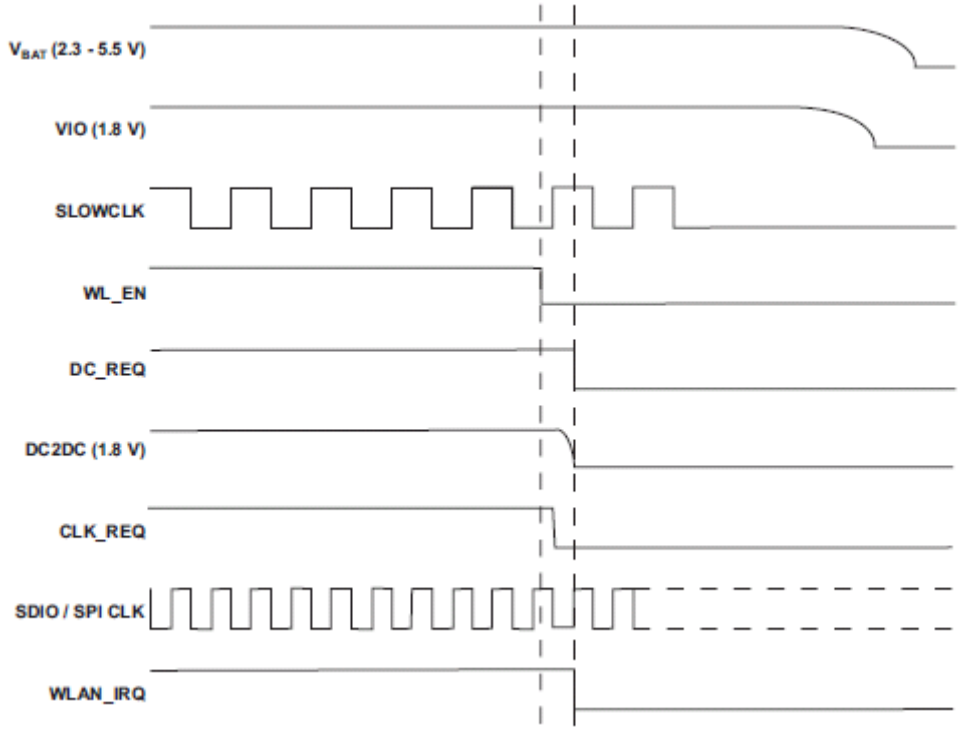
The following sequence describes device powerup from shutdown. Only the WLAN Core is enabled; the BT and FM cores are disabled.

1. No signals are allowed on the IO pins if no IO power supplied, because the IOs are not 'fail safe'. Exceptions are CLK_REQ, SLEEP_CLK, XTALP and AUD_xxx, which are failsafe and can tolerate external voltages with no VIO and DC2DC.

2. VBAT,VIO and SLEEP_CLK must be available before WLAN_EN.

3. Twakeup = T1 + T2
The duration of T1 is defined as the time from WLAN_EN=high until Fref is valid for the WL1271L
T1 ~55ms
The duration of T2 depends on:
– Operating system
– Host enumeration for the SDIO/WSPI
– PLL configuration
– Firmware download
– Releasing the core from reset
– Firmware initialization

10.2 Power Down Sequence



1. DC_REQ of WL1271L will go low only if WLAN is the only core working. otherwise if another core is working (e.g BT) it will stay high.

2. CLK_REQ will go low only if WLAN is the only core working. otherwise if another core is working and using the Fref (e.g BT) it will stay high.

3. If WLAN is the only core that is operating, WLAN_EN must remain de-asserted for at least 64msec before it is re-asserted.

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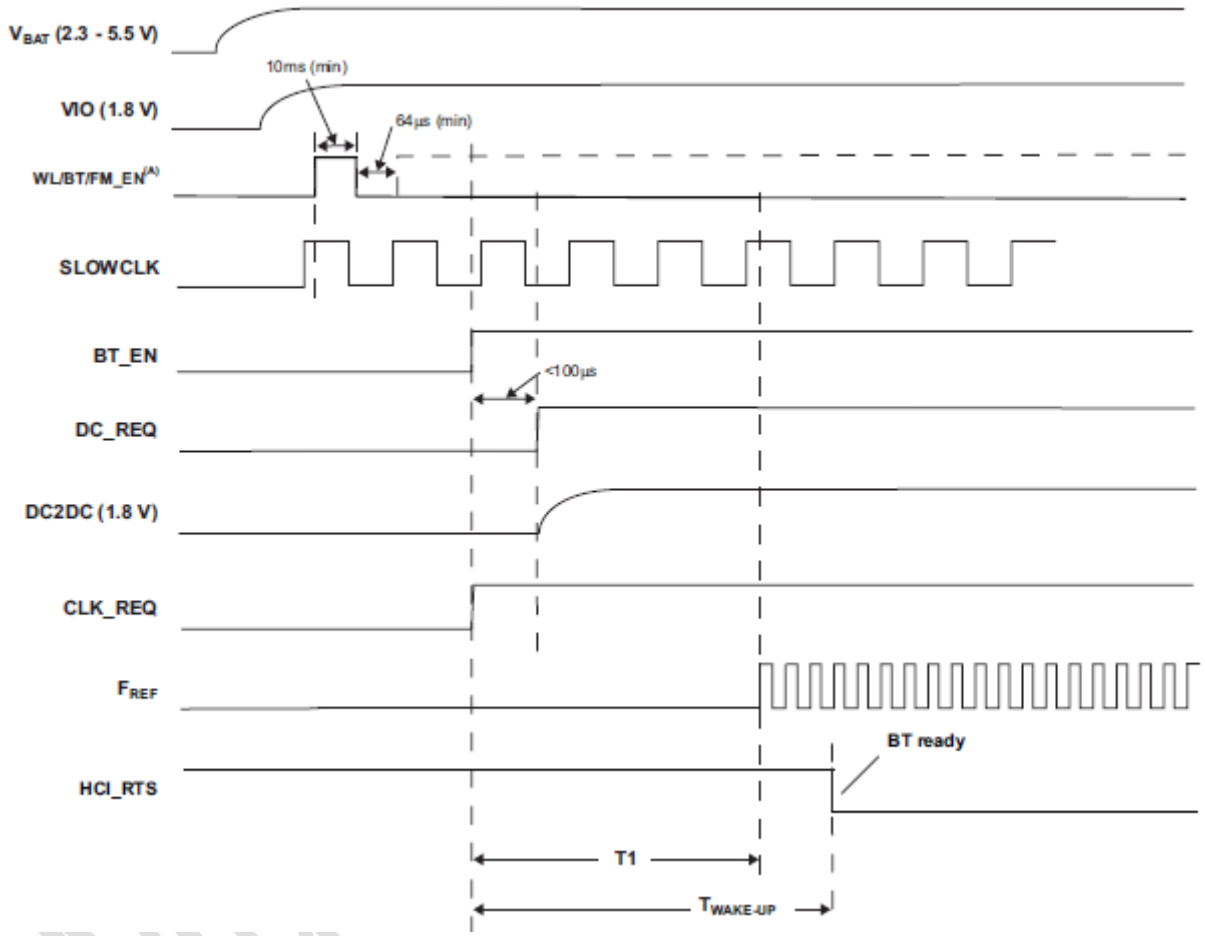
11. BT Power Up/Down Sequence

11.1 Power Up Sequence

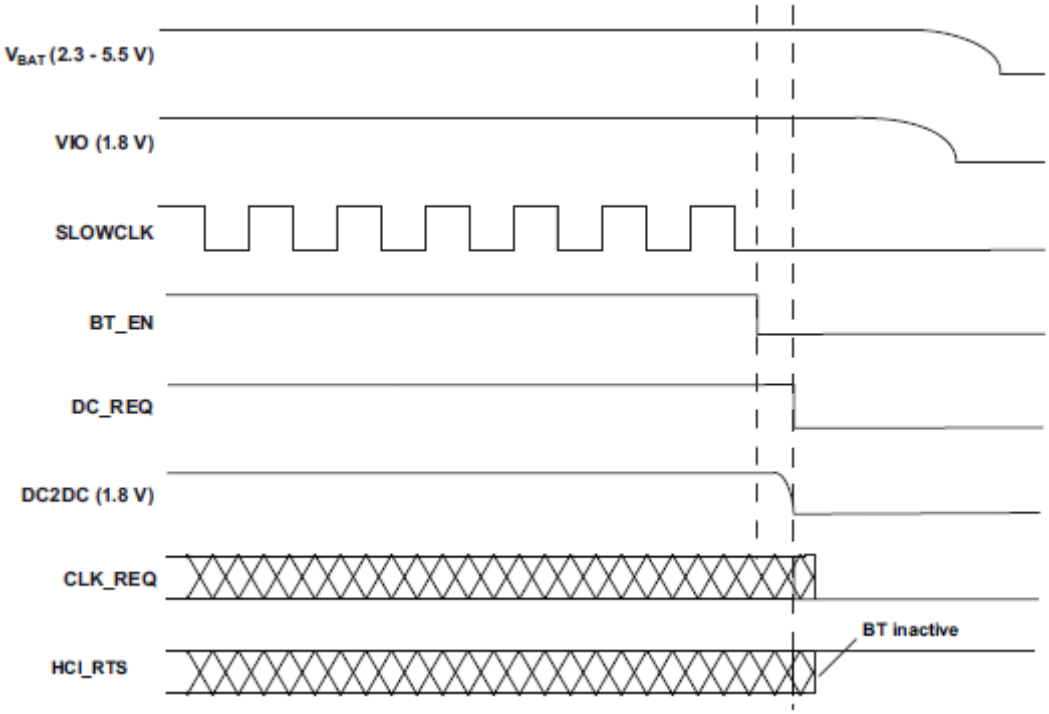
The following sequence describes device powerup from shutdown. Only the BT core is enabled; the WLAN and FM cores are disabled.

Power up requirements:
1. No signals are allowed on the IO pins if no IO power supplied, because the IOs are not 'failsafe'. Exceptions are CLK_REQ, SLEEP_CLK, XTALP and AUD_xxx, which are failsafe and can tolerate external voltages with no VIO and DC2DC.
2. VIO and SLEEP_CLK must be stable before releasing BT_EN.
3. Fast clock must be stable maximum 55ms after BT_EN goes HIGH.



1. The duration of T1 is defined as the time from BT_EN=high until Fref is valid for the WL1271L.
2. T1≒55ms
3. The duration of $T_{WAKE-UP}$ is defined as the time from BT_EN rising edge to HCI_RTS falling edge, <70ms.

11.2 Power Down Sequence



The WL1271L indicates completion of BT power up sequence by asserting RTS low. This occurs up to 100ms after BT_EN goes high.

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12. HOST Interface

12.1 Host interface Combination

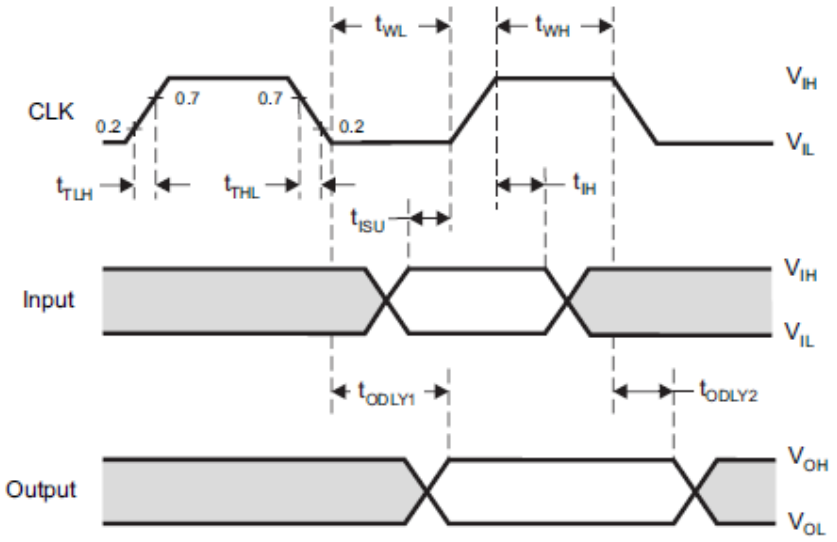
Use case	WLAN	BT	Remarks
1	WSPI	UART	
2	SDIO	UART	

12.2 SDIO Interface

12.2.1 SDIO Clock Switching Characteristics

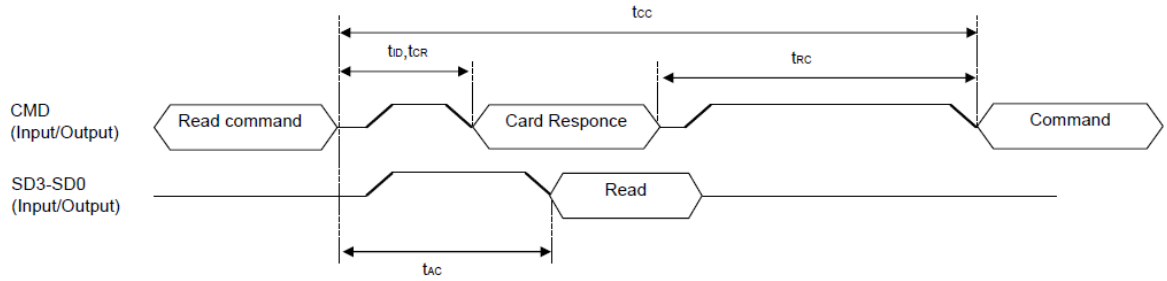
Note: all timing parameter are indicated for the maximum Host interface clock frequency.

PARAMETER			MIN	MAX	UNIT
Fclock	Clock frequency,CLK	CL ≦ 25pF	0	25	MHz
DC	Low/High duty cycle	CL ≦ 25pF	40	60	%
tWL	Pulse duration, CLK low	CL ≦ 25pF	10		ns
tWH	Pulse duration, CLK high	CL ≦ 25pF	10		ns
tTLH	Rise time, CLK	CL ≦ 25pF		4.3	ns
tTHL	Fall time, CLK	CL ≦ 25pF		3.5	ns
tISU	Setup time, input calid before CLK↑	CL ≦ 25pF	5		ns
tIH	Hold time, input valid after CLK↑	CL ≦ 25pF	5		ns
tODLY1	Delay time, CLK↓ to output valid	CL ≦ 25pF	0	14	ns
tODLY2	Delay time, CLK↓ to output invalid	CL ≦ 25pF	0	14	ns



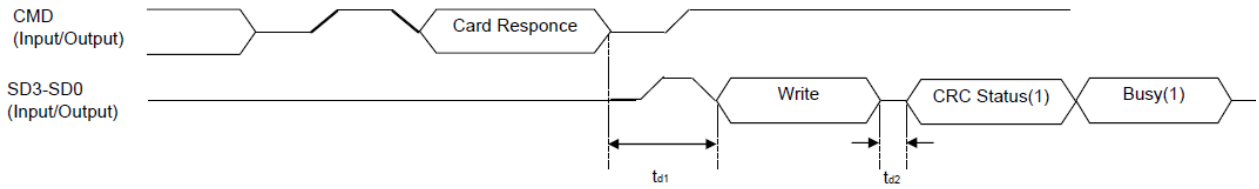
12.2.2 SDIO Data Switching Characteristics

SDIO Interface Read



Parameter			MIN	MAX	Unit
tCR	Delay time,assign relative address or data transfer mode	Read-command CMD invalid to card-response CMD valid	2	64	Clock Cycle
tCC	Delay time,CMD command invalid to CMD command valid		8		Clock Cycle
tRC	Delay time,CMD response invalid to CMD command valid		8		Clock Cycle
tAC	Access time,CMD command invalid to SD3-SD0 read data valid		8		Clock Cycle

SDIO Interface Write

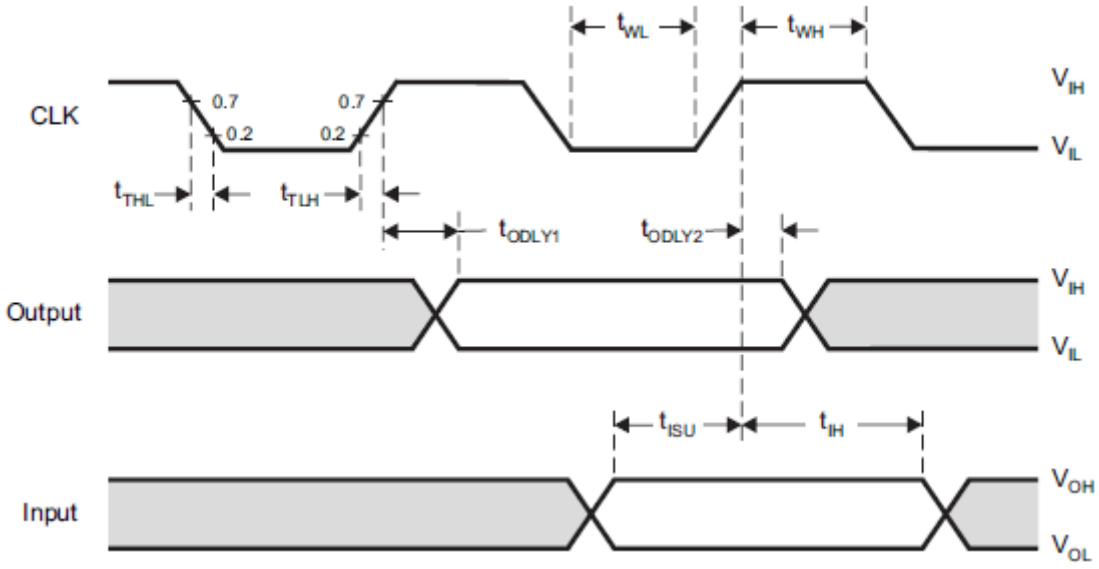


Parameter		MIN	MAX	Unit
T_{d1}	Delay time,CMD card response invalid to SD3-SD0 write data valid	2		Clock Cycle
T_{d2}	Delay time,SD3-SD0 wirte data invalid end to CRC status valid	2	2	Clock Cycle

12.3 WSPI Interface timing
12.3.1 WSPI Clock Switching Characteristic

PARAMETER			MIN	MAX	UNIT
f_{clock}	Clock frequency,CLK	CL ≦10pF	0	48	MHz
DC	Low/High duty cycle	CL ≦10pF	40	60	%
t_{WL}	Pulse duration, CLK low	CL ≦10pF	5		ns
t_{WH}	Pulse duration, CLK high	CL ≦10pF	5		ns
t_{TLH}	Rise time, CLK	CL ≦10pF		4.3	ns
t_{THL}	Fall time, CLK	CL ≦10pF		3.5	ns
t_{ISU}	Setup time, input valid before CLK↑	CL ≦10pF	5		ns
t_{IH}	Hold time, input valid after CLK↑	CL ≦10pF	5		ns
t_{ODLY1}	Delay time, CLK↓ to output valid	CL ≦10pF	4	15	ns
t_{ODLY2}	Delay time, CLK↓ to output invalid	CL ≦10pF	5	15	ns

SPI/WSPI Timing



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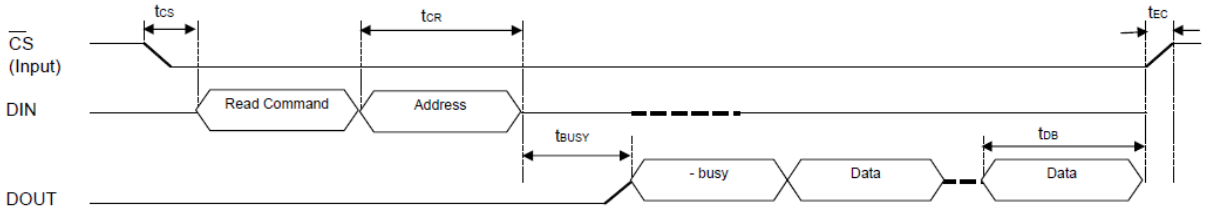
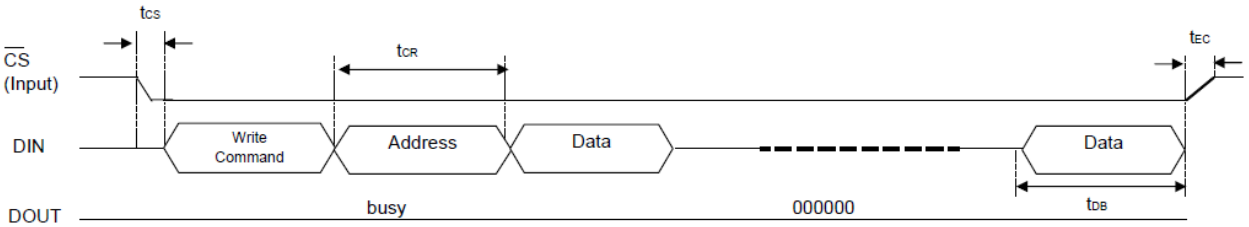
12.3.2 WSPI Data Switching Characteristic

WSPI Inter face read



WSPI Inter face write



Parameter		MIN	MAX	Unit
t_{CS}	Delay time, $\overline{CS}$ ↓ to DIN read/write command valid	0		16 Clock Cycle
t_{CR}	Delay time, DIN read command invalid to DOUT/DIN card reponse valid		1	16 Clock Cycle
t_{busy}	Fixed busy delay till DOUT data valid	1	7	32 Clock Cycle
t_{EC}	Delay time, DOUT data invalid to $\overline{CS}$ ↑	0		16 Clock Cycle
t_{DB}	Data Block Size		1	32 Clock Cycle

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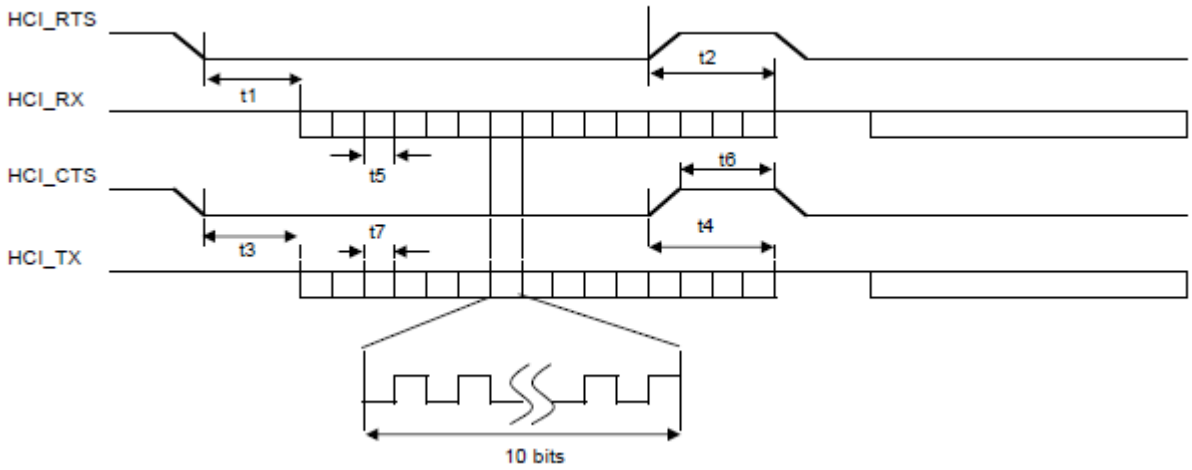
12.4 UART Interface timing



Symbol	Characteristics	Condition	MIN	Typ	MAX	Unit
	Baud rate	Most rates	37.5		4000	kbps
t5,t7	Baud rate accuract	Receive/Transmit			-2.5 to 1.5	%
t3	CTS low to TX_DATA		0	2		us
t4	CTS high to TX_DATA	Hardware flow control			1	byte
t6	CTS-high pulse width		1			bit
t1	RTS low to RX_DATA on		0	2		us
t2	RTS high to RX_DATA off	Interrupt set to 1/4 FIFO			16	byte

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13. Fast Clock Using External Clock Source

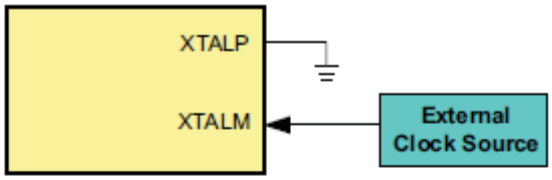
13.1 Reference Clock

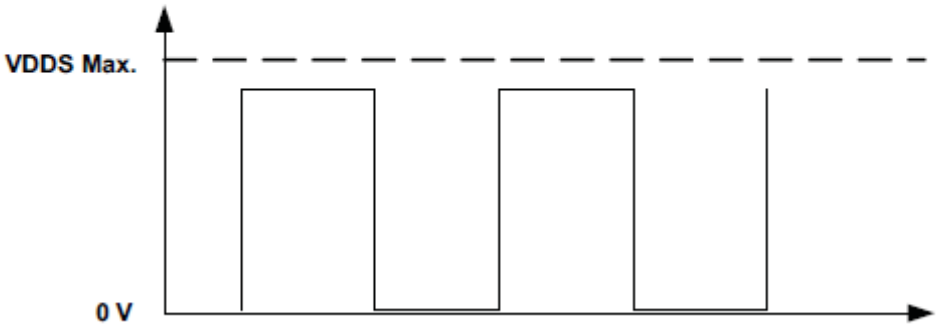
This module supports the following reference clock: 19.2, 26, 38.4, and 52MHz. All three core functions share a single reference-clock input. The supported sources for the reference clock are;

-Digital clock, VDDS level
-Analog sine wave (AC coupled)
-XTAL (26MHz and 38.4MHz)

13.2 External Digital Fast Clock Source

Below illustrates the configuration when using a digital external source for the fast-clock input.



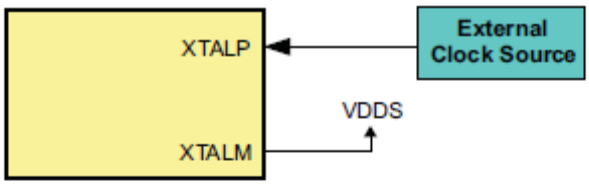


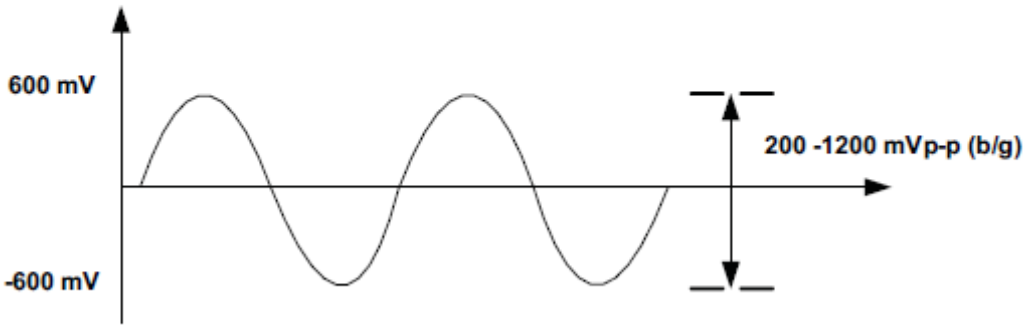
Clock input level = 1.8 V typical CMOS level

Note: Clock signal must not float

13.3 External Analog AC-Coupled Fast Clock (recommended)

Below figure illustrates the configuration when using an AC-coupled external source for the fast-clock input.



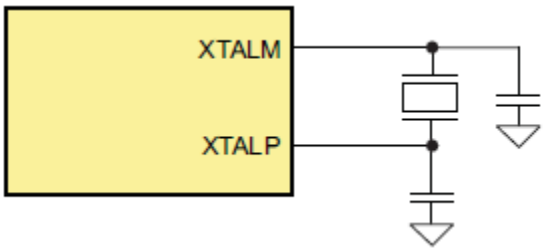


Clock input level = 500 mVp-p typical (Sinusoidal)

In cases where the input amplitude is greater than 1.2V, the amplitude should be lowered by reducing the value of the coupling capacitor, or by using a resistor to ground. This forms a voltage divider capacitance to provide the required amplitude at this module input.

14.4 Fast Clock Using External Crystal

If an external crystal is used, it must be connected as shown below.



14. Electrical Characteristics

14.1 DC/RF Characteristics for IEEE802.11b

11Mbps mode unless otherwise specified. 25deg.C, VBAT=3.6V, VDDIO=1.8V

Fast Clock source : TCXO

Items	Contents			
Specification	IEEE802.11b			
Mode	DSSS / CCK			
Frequency	2412 – 2472MHz (5MHz)			
Data rate	1, 2, 5.5, 11Mbps			
- DC Characteristics -	min.	typ.	max.	unit
1. DC current				
1) Tx mode	-	250	320	mA
2) Rx mode	-	100	150	mA
3) Sleep mode	-	100	200	uA
- Tx Characteristics -	min.	typ.	max.	unit
2. Power Levels	14	16	18	dBm
3. Spectrum Mask				
1) 1st side lobes	-	-40	-30	dBr
2) 2nd side lobes	-	-55	-50	dBr
4. Power-on and Power-down ramp	-	0.1	2	µsec
5. RF Carrier Suppression	15	37	-	dB
6. Modulation Accuracy (EVM)	-	10	35	%
7. Spurious Emissions				
1) 30MHz to 1GHz	-	-80	-36	dBm
2) 1GHz to 12.75GHz	-	-60	-30	dBm
3) 1.8GHz to 1.9GHz	-	-80	-47	dBm
4) 5.15GHz to 5.3GHz		-80	-47	dBm
- Rx Characteristics -	min.	typ.	max.	unit
8. Minimum Input Level Sensitivity				
1) 11Mbps (FER ≤ 8%)	-	-87	-76	dBm
9. Maximum Input Level (FER ≤ 8%)	-10	0	-	dBm

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14.2 DC/RF Characteristics for IEEE802.11g

54Mbps mode unless otherwise specified. 25deg.C, VBAT=3.6V, VDDIO=1.8V

Fast Clock source : TCXO

Items	Contents			
Specification	IEEE802.11g			
Mode	OFDM			
Frequency	2412 - 2472MHz (5MHz)			
Data rate	6, 9, 12, 18, 24, 36, 48, 54Mbps			
- DC Characteristics -	min.	typ.	max.	unit
1. DC current				
1) Tx mode	-	180	245	mA
2) Rx mode	-	100	150	mA
3) Sleep mode	-	100	200	uA
- Tx Characteristics -	min.	typ.	max.	unit
2. Power Levels	11	13	15	dBm
3. Spectrum Mask				
1) at fc +/- 11MHz	-	-30	-20	dBr
1) at fc +/- 20MHz	-	-33	-28	dBr
1) at fc +/- 30MHz	-	-45	-40	dBr
4. Spurious Emissions				
1) 30MHz to 1GHz	-	-80	-36	dBm
2) 1GHz to 12.75GHz	-	-65	-30	dBm
3) 1.8GHz to 1.9GHz	-	-80	-47	dBm
4) 5.15GHz to 5.3GHz		-80	-47	dBm
5. Constellation Error (EVM)	-	-30	-25	dB
- Rx Characteristics -	min.	typ.	max.	unit
6. Minimum Input Level Sensitivity				
1) 54Mbps (PER $\leq$ 10%)	-	-73	-65	dBm
7. Maximum Input Level (PER $\leq$ 10%)	-20	-4	-	dBm

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14.3 DC/RF Characteristics for IEEE802.11n-2.4G

65Mbps (MCS7) mode unless otherwise specified. 25deg.C, VBAT=3.6V, VDDIO=1.8V
Fast Clock source : TCXO

Items	Contents			
Specification	IEEE802.11n-2.4G			
Mode	OFDM			
Frequency	2412 - 2472MHz (5MHz)			
Data rate	6.5, 13,19.5, 26, 39, 52, 58.5, 65Mbps			
- DC Characteristics -	min.	typ.	max.	unit
1. DC current				
1) Tx mode	-	180	245	mA
2) Rx mode	-	100	150	mA
3) Sleep mode	-	100	200	uA
- Tx Characteristics -	min.	typ.	max.	unit
2. Power Levels	10	12	14	dBm
3. Spectrum Mask				
1) at fc +/- 11MHz	-	-30	-20	dBr
1) at fc +/- 20MHz	-	-35	-28	dBr
1) at fc +/- 30MHz	-	-50	-45	dBr
4. Spurious Emissions				
1) 30MHz to 1GHz	-	-80	-36	dBm
2) 1GHz to 12.75GHz	-	-65	-30	dBm
3) 1.8GHz to 1.9GHz	-	-80	-47	dBm
4) 5.15GHz to 5.3GHz		-80	-47	dBm
5. Constellation Error (EVM)	-	-80	-28	dB
- Rx Characteristics -	min.	typ.	max.	unit
6. Minimum Input Level Sensitivity				
1) 65Mbps (PER ≤ 10%)	-	-67	-64	dBm
7. Maximum Input Level (PER ≤ 10%)	-20	-5	-	dBm

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14.4 DC/RF Characteristics for Bluetooth

25deg.C, VBAT=3.6V, VDDIO=VDDHOST=1.8V, Fast Clock source : TCXO

Items	Contents			
Bluetooth specification	Ver 4.0			
Channel spacing	1MHz			
Number of RF channel	79			
Power class	1			
Operation mode (Rx/Tx)	Time division multiplex either transmit or receive Frequency hopping after one Rx/Tx cycle			
Items	min.	typ.	max.	unit
1. DC Current				
1) DH1 Packet 50% Rx/Tx slot duty cycle	-	37	60	mA
2) DH3 Packet 50% Rx/Tx slot duty cycle	-	46	60	mA
3) DH5 Packet 50% Rx/Tx slot duty cycle	-	48	60	mA
- TX characteristics -	min.	typ.	max.	unit
2. Output Power	4.5	8.0		dBm
3. Frequency range (Rx/Tx)	2400 - 2483.5			MHz
4. -20dB bandwidth	-	0.8	1	MHz
5. Adjacent Channel Power *1				
5.1 [M-N] = 2	-	-45	-20	dBm
5.2 [M-N] ≧ 3	-	-46	-40	dBm
6. Modulation characteristics				
6.1 Modulation δf1avg	140	158	175	kHz
6.2 Modulation δf2max	115	132	-	kHz
6.3 Modulation δf2avg/δf1avg	0.8	0.9	-	-
7. Carrier Frequency Drift				
7.1 1slot	-25	-	+25	kHz
7.2 3slot	-40	-	+40	kHz
7.3 5slot	-40	-	+40	kHz
7.4 Maximum drift rate	-20	-	+20	kHz/50μs
8. Out-of-Band Spurious Emissions				
8.1 30-1000MHz (Operation Mode)	-	-58	-36	dBm
8.2 1000-12750MHz (Operation Mode)	-	-40	-30	dBm
8.3 1800-1900MHz(Operation Mode)		-80	-47	dBm
8.4 5150-5300MHz (Operation Mode)	-	-80	-47	dBm
9. EDR Relative Power (Pi/4-DQPSK and 8DPSK)	-4	-0.2	1	
10. EDR Carrier Frequency Stability and Modulation Accuracy				
10.1 ωi (Pi/4-DQPSK and 8DPSK)	-75	0	75	kHz
10.2 ω0 (Pi/4-DQPSK and 8DPSK)	-10	0	10	kHz
10.3 ωi+ω0 (Pi/4-DQPSK and 8DPSK)	-75	0	75	kHz
10.4 RMS DEVM (Pi/4-DQPSK)	-	6	20	%
10.5 99% DEVM (Pi/4-DQPSK)	-	10	30	%
10.6 Peak DEVM (Pi/4-DQPSK)	-	14	35	%
10.7 RMS DEVM (8DPSK)	-	6	13	%
10.8 99% DEVM (8DPSK)	-	10	20	%
10.9 Peak DEVM (8DPSK)	-	15	25	%
- RX characteristics -	min	typ	max	unit
11. Sensitivity (BER ≦ 0.1%)				
11.1 2402MHz	-	-90	-70	dBm
11.2 2441MHz	-	-90	-70	dBm
11.3 2480MHz	-	-90	-70	dBm

12. C/I Performance (BER ≤ 0.1%) [*2]				
12.1 co-channel ratio (-60dBm input)	-	7	11	dB
12.2 1MHz ratio (-60dBm input)	-	-9	0	dB
12.3 2MHz ratio (-60dBm input)	-	-46	-30	dB
12.4 3MHz ratio (-67dBm input)	-	-48	-40	dB
12.5 image +/- 1MHz ratio (-67dBm input)	-	-30	-20	dB
13. Blocking performance (BER ≤ 0.1%) [*3]				
13.1 30MHz-2000MHz	-10	-8		dBm
13.2 2000MHz-2400MHz	-27	0	-	dBm
13.3 2500MHz-3000MHz	-27	0	-	dBm
13.4 3000MHz-12750MHz	-10	-5	-	dBm
14. Intermodulation performance (BER ≤ 0.1%, -64dBm input)	-39	-30	-	dBm
15. Maximum Input Level	-20	10	-	dBm
16. EDR Sensitivity (at 0.01% BER)				
16.1 Pi/4-DQPSK	-	-90	-70	dBm
16.2 8DPSK	-	-84	-70	dBm

[*1] Up to three spurious responses within Bluetooth limits are allowed.
[*2] Up to five spurious responses within Bluetooth limits are allowed.
[*3] Up to twenty-four spurious responses within Bluetooth limits are allowed.

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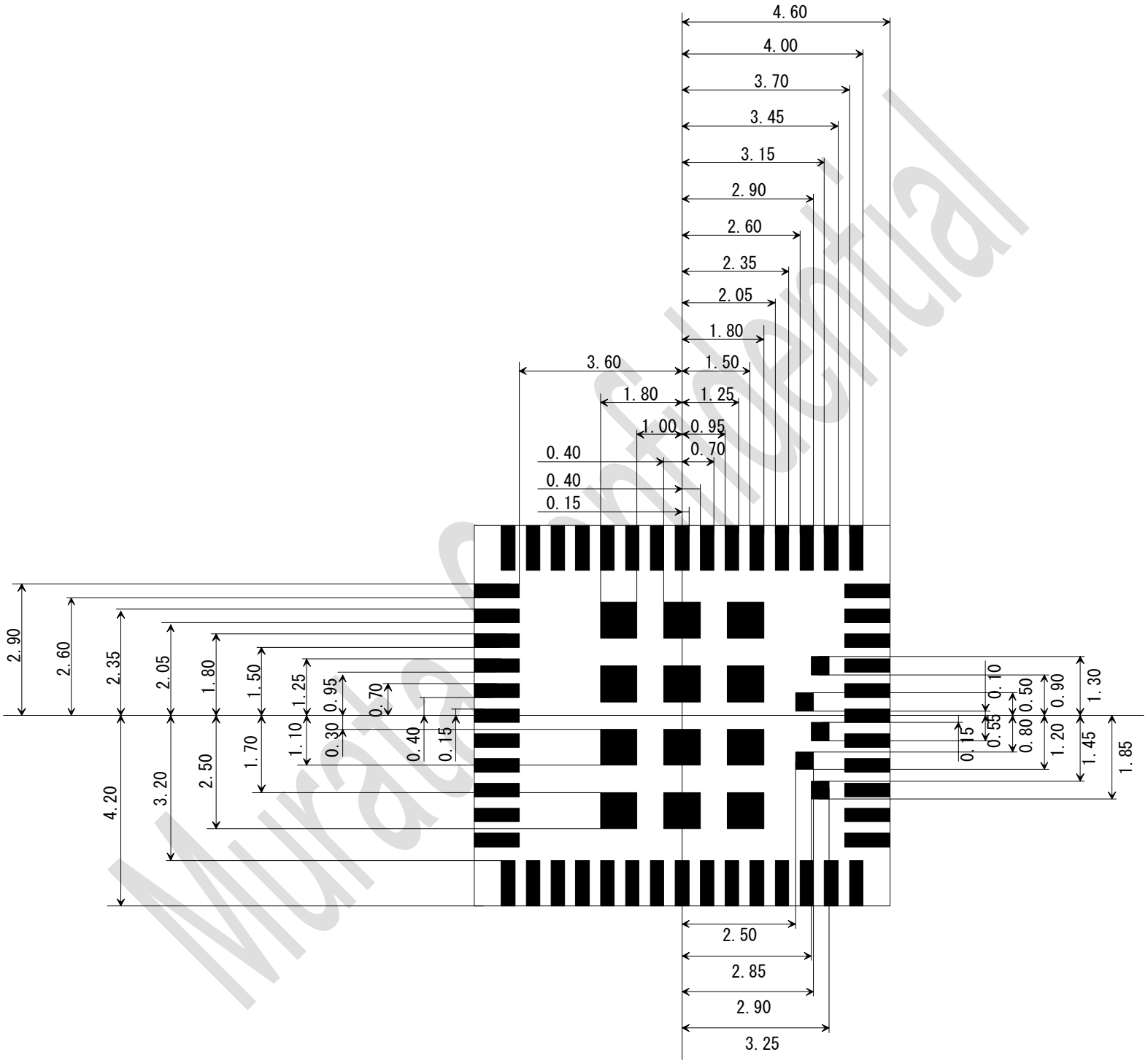
15. Land pattern



(unit : mm)

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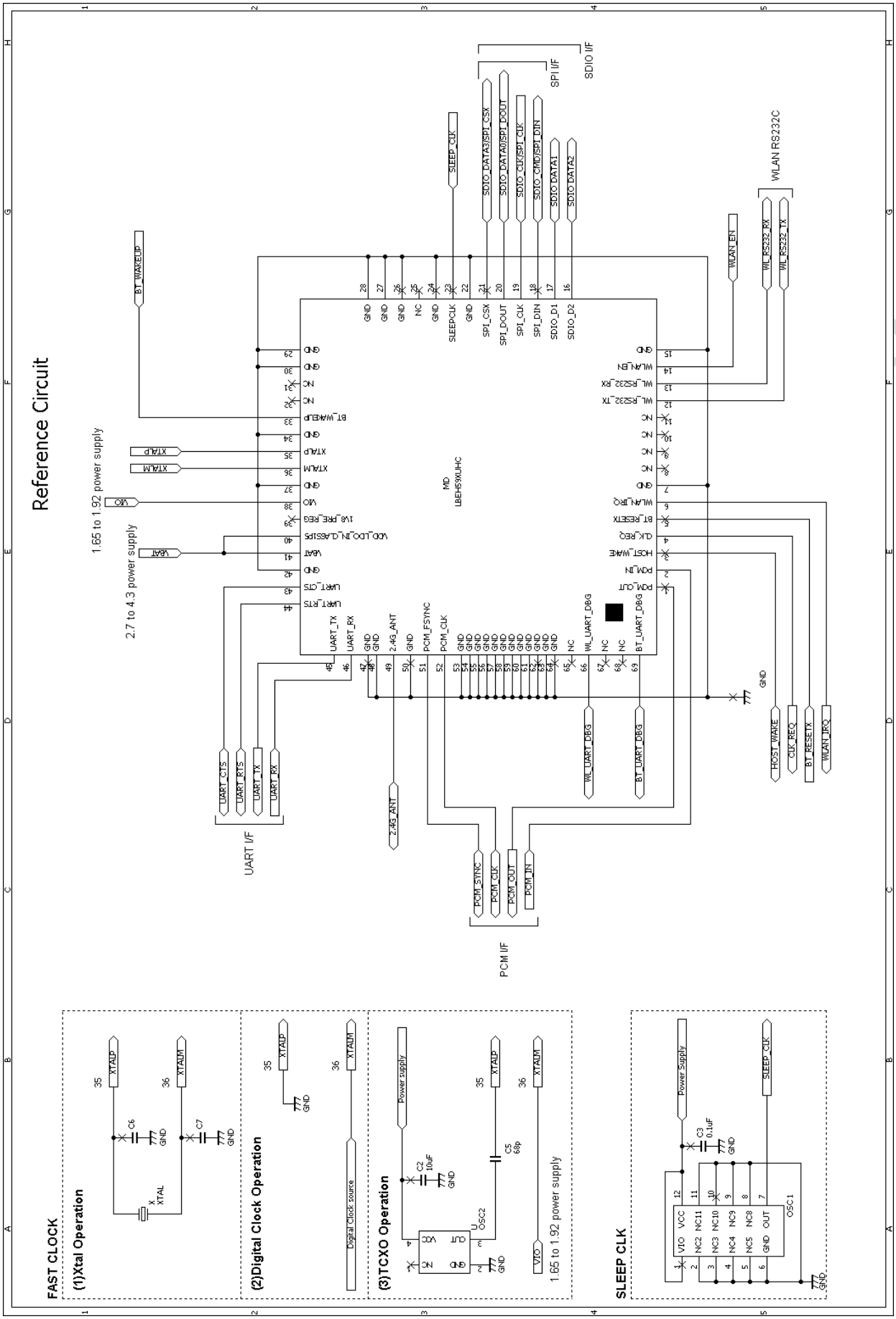
16. Reference Circuit



17. Evaluation board of LBEH59XUHC -TEMP

Murata has operation manual of Murata's evaluation board. If you want to get more detail of it, please refer "operation Manual_ LBEH59XUHC".

Evaluation board Part Number	LBEH59XUHC -TEMP-D

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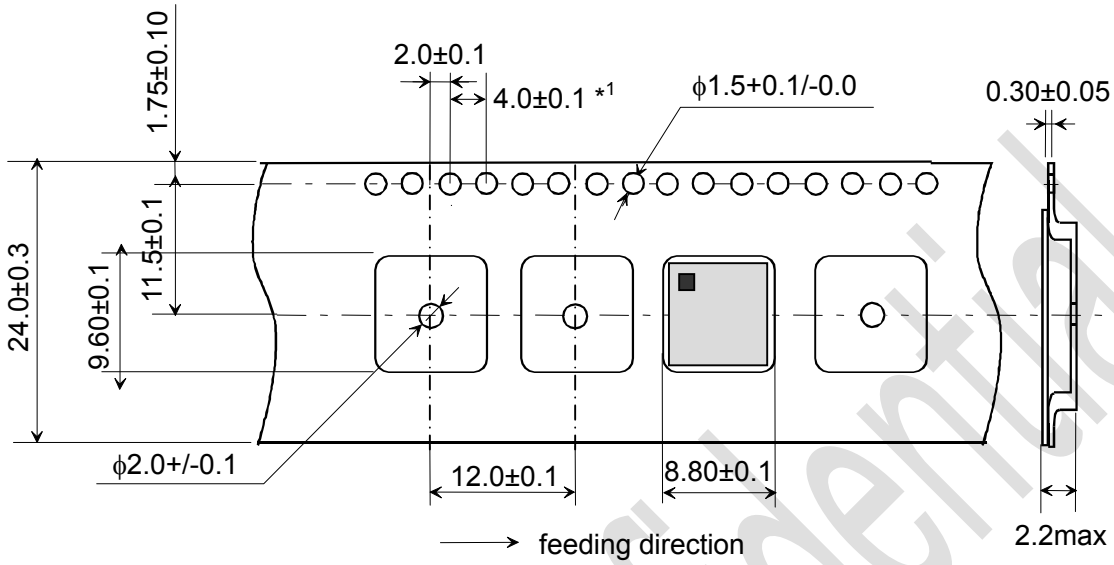
18.Tape and Reel Packing

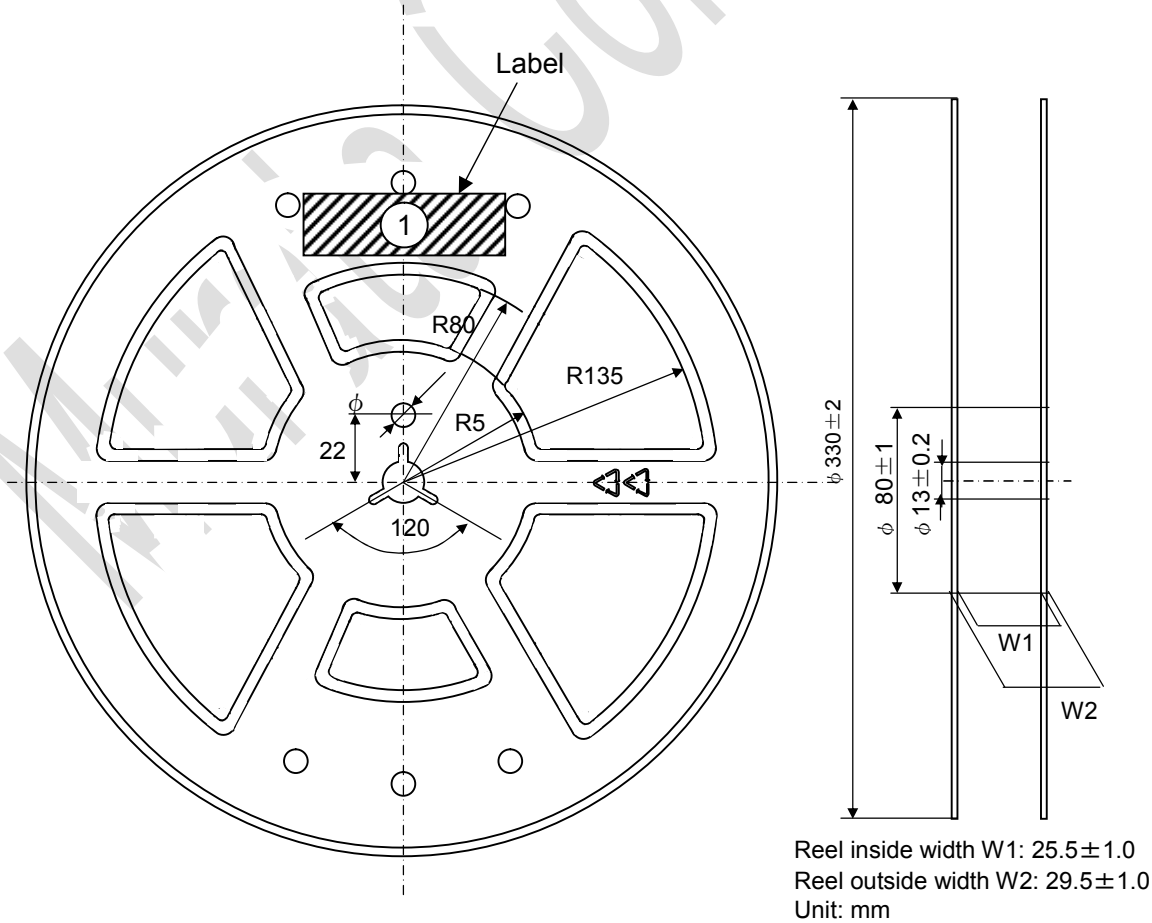
(1) Dimensions of Tape (Plastic tape)



*1 Cumulative tolerance of max. ± 0.3 every 10 pitches

(unit : mm)

(2) Dimensions of Reel



Reel inside width W1: 25.5±1.0
Reel outside width W2: 29.5±1.0
Unit: mm

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< Specification may be changed by Murata without notice >
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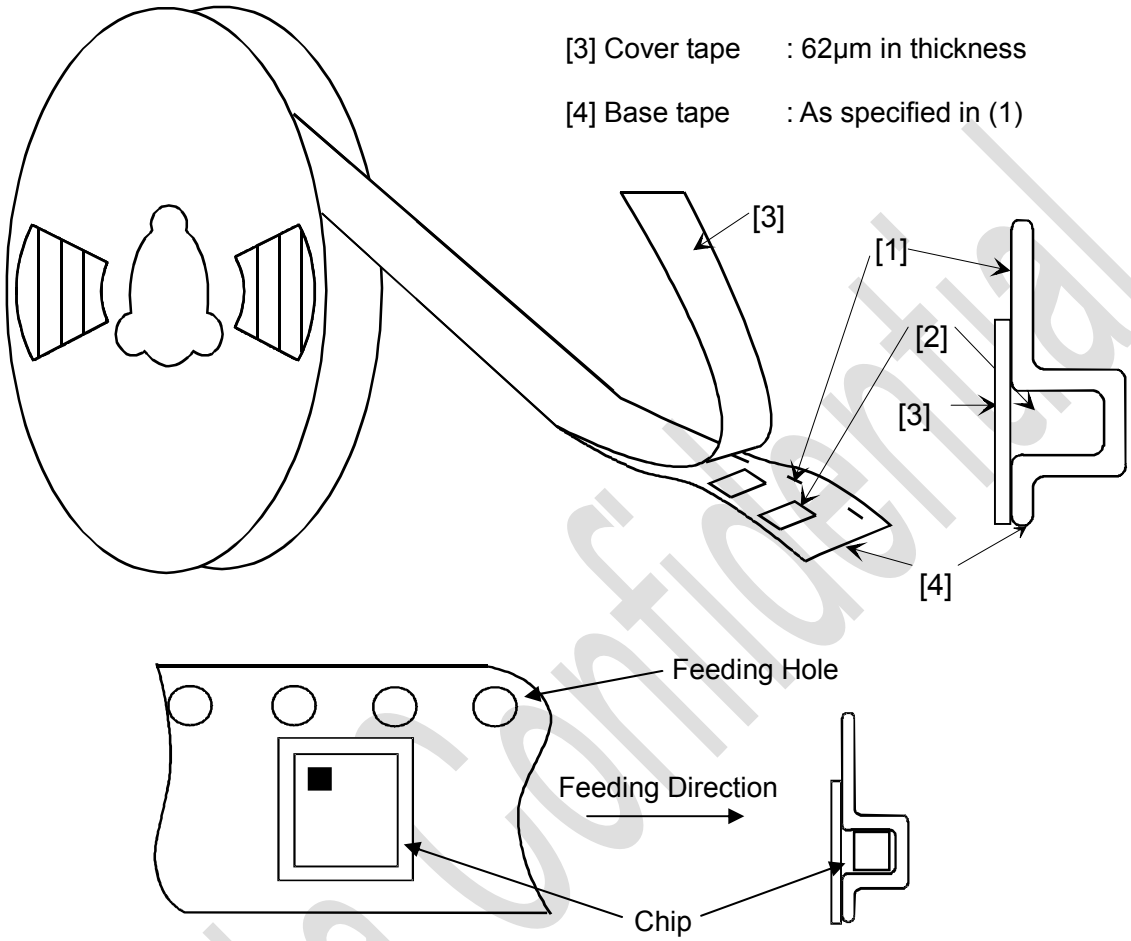
(3) Taping Diagrams

[1] Feeding Hole : As specified in (1)

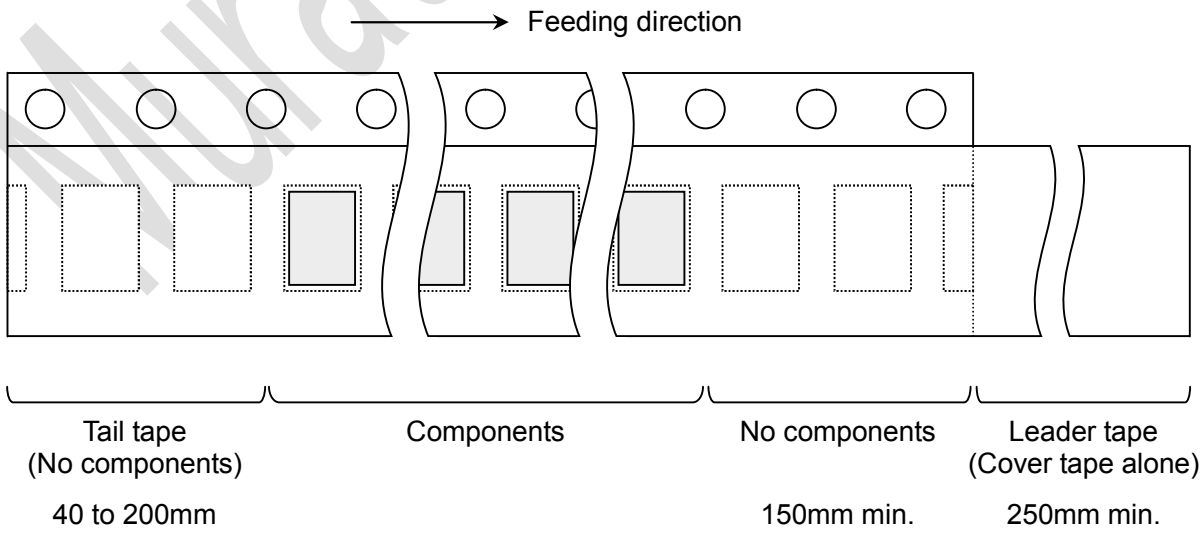
[2] Hole for chip : As specified in (1)

[3] Cover tape : 62μm in thickness

[4] Base tape : As specified in (1)



(4) Leader and Tail tape



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(5) The tape for chips are wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.

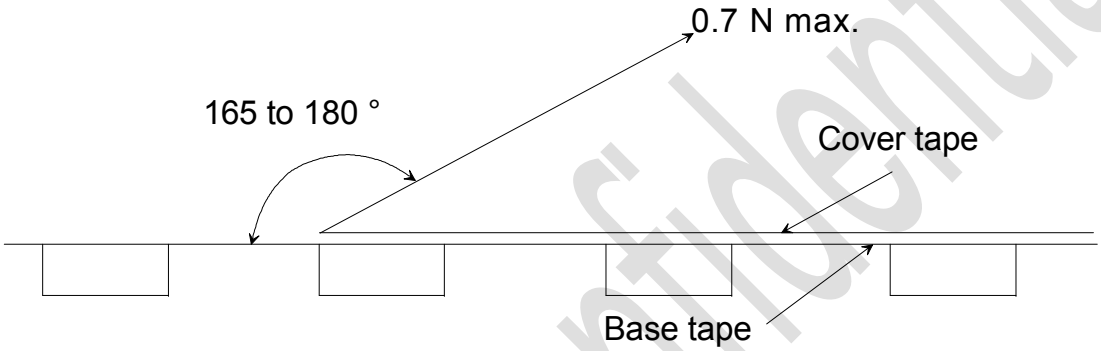
(6) The cover tape and base tape are not adhered at no components area for 250mm min.

(7) Tear off strength against pulling of cover tape : 5N min.

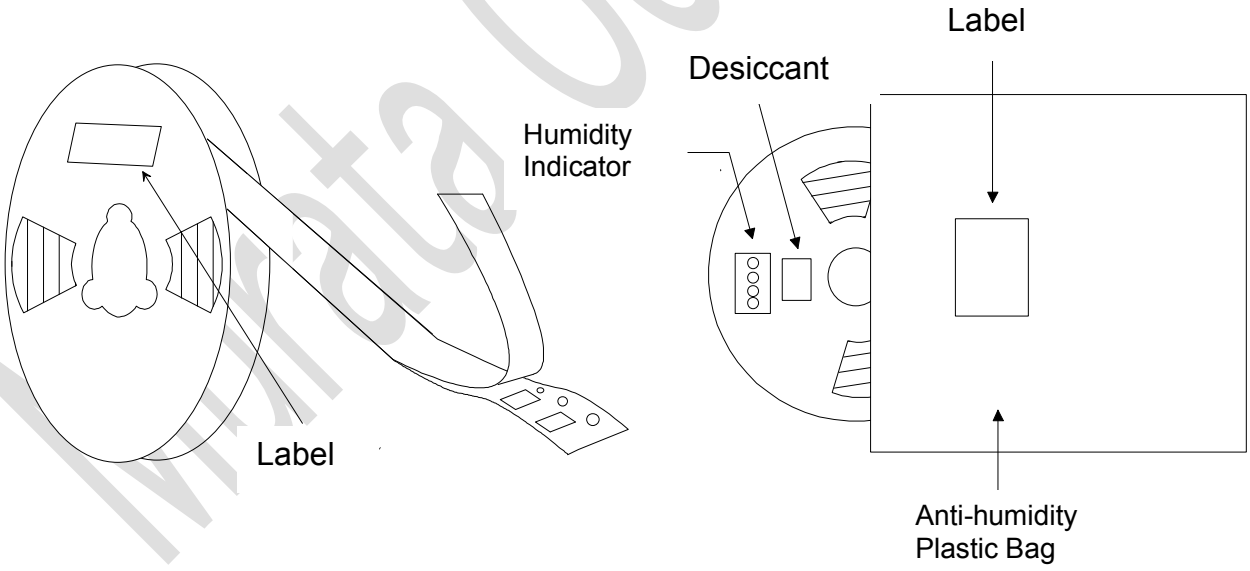
(8) Packaging unit : 1000pcs./ reel

(9) material : Base tape : Plastic
Real : Plastic
Cover tape, cavity tape and reel are made the anti-static processing.

(10) Peeling of force : 0.7N max. in the direction of peeling as shown below.



(11) Packaging (Humidity proof Packing)



Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.

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NOTICE

1. Storage Conditions :

Please use this product within 6month after receipt.
- The product shall be stored without opening the packing under the ambient temperature from 5 to 35deg.C and humidity from 20 to 70%RH.
(Packing materials, in particular, may be deformed at the temperature over 40deg.C.)
- The product left more than 6months after reception, it needs to be confirmed the solderbility before used.
- The product shall be stored in non corrosive gas (Cl_2, NH_3, SO_2, No_x, etc.).
- Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object and dropping the product, shall not be applied in order not to damage the packing materials.

This product is applicable to MSL3 (Based on JEDEC Standard J-STD-020)
- After the packing opened, the product shall be stored at ≦30deg.C / ≦60%RH and the product shall be used within 168hours.
- When the color of the indicator in the packing changed, the product shall be baked before soldering.

Baking condition : 125+5/-0deg.C, 24hours, 1time

The products shall be baked on the heat-resistant tray because the material (Base Tape, Reel Tape and Cover Tape) are not heat-resistant.

2. Handling Conditions :

Be careful in handling or transporting products because excessive stress or mechanical shock may break products.

Handle with care if products may have cracks or damages on their terminals, the characteristics of products may change. Do not touch products with bear hands that may result in poor solderability.

3. Standard PCB Design (Land Pattern and Dimensions) :

All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.

The recommended land pattern and dimensions is as Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set. When using non-standard lands, contact Murata beforehand.

4. Notice for Chip Placer :

When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

5. Soldering Conditions:

Carefully perform preheating so that the temperature difference (□T) between the solder and products surface should be in the following range. After mounting, pay special attention to maintain the temperature difference within 100deg.C. Soldering must be carried out by the above mentioned conditions to prevent products from damage. Contact Murata before use if concerning other soldering conditions.

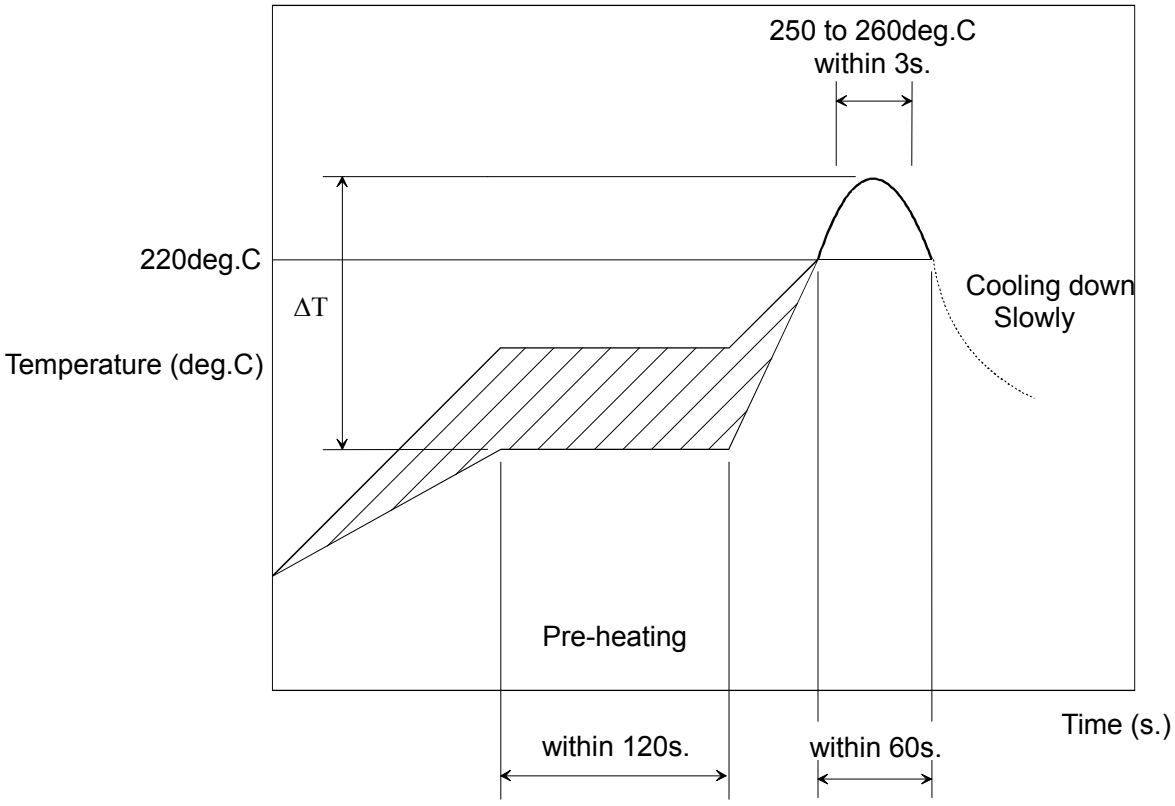
Soldering method	Temperature
Soldering iron method	□T≦130deg.C
Reflow method	

- Soldering iron method conditions are indicated below.

Kind of iron / Item	Ceramics heater
Soldering iron wattage	≦18W
Temperature of iron-tip	≦350deg.C
Iron contact time	within 3s.

- Diameter of iron-tip : Φ3.0mm max.

Reflow soldering standard conditions(Example)



Use rosin type flux or weakly active flux with a chlorine content of 0.2wt% or less.

6. Cleaning :

Since this Product is Moisture Sensitive, any cleaning is not permitted.

7. Operational Environment Conditions :

Products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity and pressure). Therefore, products have no problems to be used under the similar conditions to the above-mentioned. However, if products are used under the following circumstances, it may damage products and leakage of electricity and abnormal temperature may occur.

- In an atmosphere containing corrosive gas (Cl_2, NH_3, SO_x, NO_x etc.).
- In an atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.

If there are possibilities for products to be used under the preceding clause, consult with Murata before actual use.

As it might be a cause of degradation or destruction to apply static electricity to products, do not apply static electricity or excessive voltage while assembling and measuring.

8. Input Power Capacity :

Products shall be used in the input power capacity as specified in this specifications.
Inform Murata beforehand, in case that the components are used beyond such input power capacity range.

9. Limitation of Applications:

The product is designed and manufactured for consumer application only and is not available for any application listed below which requires especially high reliability for the prevention of such defect as may directly cause damage to the third party's life, body or property.

- Aircraft equipment.
- Aerospace equipment
- Undersea equipment.
- Power plant control equipment
- Medical equipment.
- Transportation equipment (vehicles, trains, ships, etc.).
- Traffic signal equipment.
- Disaster prevention / crime prevention equipment.
- Application of similar complexity and/ or reliability requirements to the applications listed in the above.

10. Underfill Condition:

Halfway underfill on components in the module can make unexpected stress on the components and the module has a possibility not to meet the specification.
In order to avoid this, any underfill shall not be into module inside in case of applying underfill on your PCB.

⚠ Note:

Please make sure that your product has been evaluated and confirmed against your specifications when our product is mounted to your product.

All the items and parameters in this product specification have been prescribed on the premise that our product is used for the purpose, under the condition and in the environment agreed upon between you and us. You are requested not to use our product deviating from such agreement.

We consider it not appropriate to include other terms and conditions for transaction warranty in product specifications, drawings or other technical documents. Therefore, even if your original part of this product specification includes such terms and conditions as warranty clause, product liability clause, or intellectual property infringement liability clause, we are not able to accept such terms and conditions in this product specification unless they are based on the governmental regulation or what we have agreed otherwise in a separate contact. We would like to suggest that you propose to discuss them under negotiation of contract.