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AR6302 Single Chip 802.11n MAC/BB/Radio for Embedded Applications

General Description

The Atheros AR6302 is a single chip, small form factor IEEE 802.11 g/n MAC/baseband/radio optimized for low-power mobile applications. It is the 3rd generation WLAN design in the ROCm® family, employing the world's lowest power consumption WLAN architecture in the smallest possible form factor. The AR6302 is a single stream 1x1 802.11n implementation providing improved link robustness, extended range, increased throughput and better performance for an unparalleled user experience.

The AR6302 is part of the Align™ product family.

The AR6302 implements sophisticated design techniques to deliver a solution which will greatly extend the battery life of mobile and embedded systems. It leverages its near-zero power in idle and stand-by modes to enable users to leave WLAN "always-on" without impacting battery life.

The AR6302 implements Atheros' proprietary Internal Efficient Power Amplifier™ (EPA) technology in CMOS with advanced linearization algorithms and an internal LNA, thereby reducing the BOM costs in the system design. It provides the option for an additional external PA for larger output power if needed.

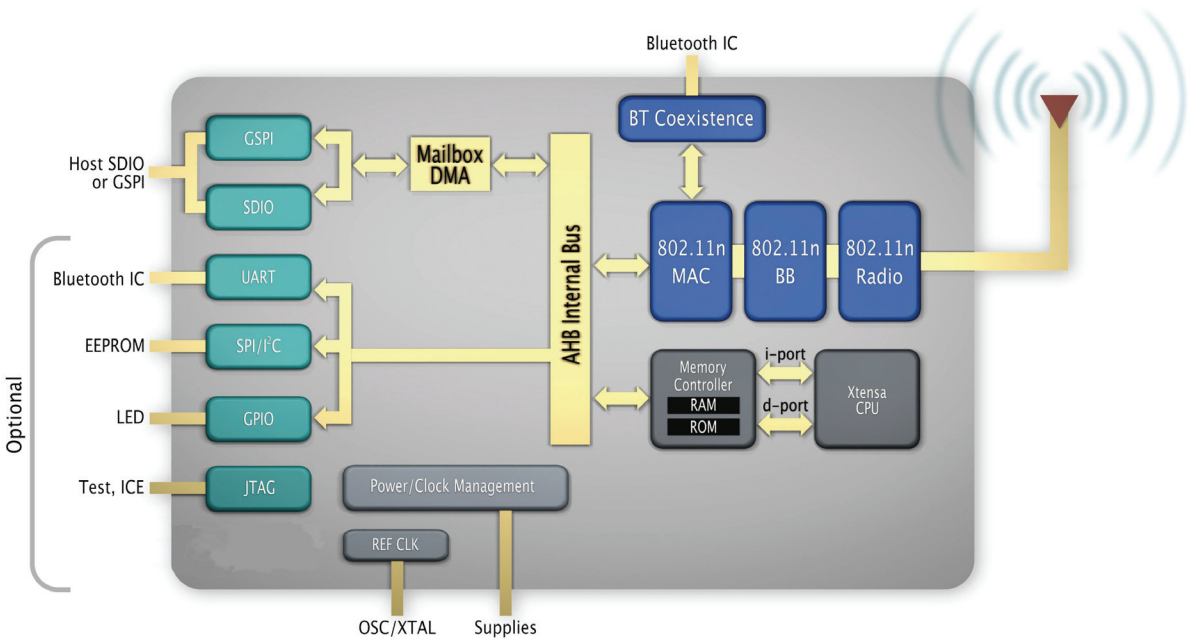
The AR6302 has additional LDOs to provide noise isolation for digital and analog supplies.

The AR6302 supports 2 and 3-wire Bluetooth coexistence protocols with advanced algorithms for predicting channel usage by a co-located Bluetooth transceiver.

The AR6302 provides multiple peripheral interfaces including UART, SPI, I^2C, etc., via 22 GPIO pins. The only external clock source needed for AR6302-based designs is a high-speed crystal or oscillator. A variety of reference clocks are supported which include 19.2, 24, 26, 38.4, 40 and 52 MHz. AR6302 is available in a small 7 x 7 QFN package.

AR6302 Features

- All-CMOS IEEE 802.11 g/n or 802.11b/g/n single-chip client
- Single stream 802.11n provides highest throughput and superior RF performance for handhelds.
- Advanced 1x1 802.11n features:
  - Full/Half Guard Interval
  - Frame Aggregation
  - Space Time Block Coding (STBC)
  - Low Density Parity Check (LDPC) Encoding
- Integrated high-output Atheros Efficient Power Amplifier™ and LNA for lowest BOM.
- Supports popular interfaces used in embedded designs: SDIO v2.0 (50MHz, 4-bit and 1-bit) and GSPI.
- Lowest power consumption in the industry with near zero in idle/standby modes, extending battery life.
- Integrated on-chip processor to minimize the loading on host processor.
- Supports 2/3-wire enhanced PTA scheme for use with any BT solution for optimal coexistence implementation.
- Supports several reference clocks from 19.2MHz to 52MHz.



AR6302 System Block Diagram

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1. Functional Description

1.1 Overview

The AR6302 is a single chip 802.11b/g/n device based on cutting edge technology, optimized for low power embedded applications. The typical data path consists of the host interface, mailbox DMA, AHB, memory controller, MAC, BB, and radio. The CPU drives the control path via register and memory accesses. External interfaces include SDIO or GSPI, reference clock, and front-end components as well as optional connections such as UART, SPI/I2C, GPIO, JTAG, 32 kHz source. See the AR6302 block diagram.

1.2 XTENSA CPU

At the heart of the chip is the XTENSA CPU. This CPU has four interfaces:

- The Code RAM/ROM interface (iBus), going to the Memory Controller (MC).
- The Data RAM Interface (dBus), going to the MC
- The AHB interface, used mainly for register accesses.
- JTAG interface for debugging

1.3 Memory Controller (MC)

The MC contains 256 kBytes of ROM and 256 kBytes of RAM. It has three interfaces:

- iBus,
- dBus, and
- AHB interface.

Any one of these interfaces can request access to the ROM or RAM modules within the MC. The MC contains arbiters to serve these three interfaces on a first-come-first-serve basis.

1.4 AHB and APB Blocks

The AHB block acts as an arbiter. It has AHB interfaces from three Masters:

- MAC,
- MBOX (from the Host), and
- CPU.

See below for more on the MBOX and MAC. Depending upon the address, the AHB data request can go into one of the two slaves: APB block or the MC. Data requests to the MC are generally high-speed memory requests, while requests to the APB block are primarily meant for register access.

The APB block acts as a decoder. It is meant only for access to programmable registers within the AR6302's main blocks. Depending on the address, the APB request can go to one of the places listed below:

- Radio
- MC
- SI/SPI
- MBOX
- GPIO
- UART
- Real Time Clock (RTC), or
- MAC/BB

1.5 Master SI/SPI Control

The AR6302 has a master serial interface (SI) that can operate in two, three, or four-wire bus configurations to control EEPROMs or other I2C/SPI devices. Multiple I2C devices with different device addresses are supported by sharing the two-wire bus. Multiple SPI devices are supported by sharing the clock and data signals and using separate software-controlled GPIO pins as chip selects.

An SI transaction consists of two phases: a data transmit phase of 0-8 bytes followed by a data receive phase of 0-8 bytes. The flexible SI programming interface allows software to support various address and command configurations in I2C/SPI devices. In addition, software may operate the SI in either polling or interrupt mode.

1.6 GPIO

The AR6302 has 22 GPIO pins with direct software access. Many are multiplexed with other functions such as the host interface, UART, SI, Bluetooth coexistence, etc. (see Chapter 6 for details). Each GPIO supports the following configurations via software programming:

- Internal pull-up/down options
- Input available for sampling by a software register
- Input triggering an edge or level CPU interrupt

- Input triggering a level chip wakeup interrupt
- Open-drain or push-pull output driver
- Output source from a software register or the Sigma Delta Pulse-width Modulation (PWM) DAC

The AR6302 has one Sigma Delta PWM DAC that is shared by all of the GPIO pins. It allows the GPIO pins to approximate intermediate output voltage levels. The DAC has a period of 256 samples with a software controllable duty cycle. In applications where the AR6302 is driving LEDs using GPIO pins, the Sigma Delta PWM DAC can provide a continuous dimmer function.

1.7 MBOX

The MBOX is a service module to handle one of two possible external hosts: SDIO or GSPI. The AR6302 can handle only one of these hosts at any given time. The type of host the AR6302 uses depends upon the polarity of some package pins upon system power-up. The MBOX has two interfaces: an APB interface for access to the MBOX registers and an AHB interface which is used by the external host to access the MC memory or other registers within the AR6302.

1.8 Debug UART

The AR6302 includes a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface that is fully compatible with the 16550 UART industry standard. This UART is a general purpose UART although it is primarily used for debug.

1.9 Reset Control

The AR6302 CHIP_PWD_L pin can be used to completely reset the entire chip. After this signal has been de-asserted, the AR6302 waits for host communication. Until then, the MAC, BB, and SOC blocks are powered off and all modules except the host interface are held in reset.

Once the host has initiated communication, the AR6302 turns on its crystal and later on its PLL. After all clocks are stable and running, the resets to all blocks are automatically de-asserted.

1.10 Reset Sequence

After a COLD_RESET event (e.g., the host toggles CHIP_PWD_L) the AR6302 will enter the HOST_OFF state and await communication from the host. From that point, the typical AR6302 COLD_RESET sequence is shown below:

1. When the host is ready to use the AR6302, it initiates communication via SDIO or GSPI.
2. The AR6302 enters the WAKEUP state then the ON state and enables the XTENSA CPU to begin executing ROM code. Software configures the AR6302 functions and interfaces. When the AR6302 is ready to receive commands from the host, it will set an internal function ready bit.
3. The host reads the ready bit and can now send function commands to the AR6302.
4. The CPU may continue to be held in reset under some circumstances until its reset is cleared by an external pin or when the host clears a register.
5. The MAC cold reset and the MAC/BB warm reset will continue to stay asserted until their respective reset registers are cleared by software.

1.11 Power Management Unit

The AR6302 has an integrated Power Management Unit (PMU) which generates all the power supplies required by its internal circuitry from external 3.3V and 1.8V supplies.

The main components of the PMU are as follows:

- A linear regulator (SREG) which converts the host IO supply to a 1.2V supply for some small control blocks which are turned on when CHIP_PWD_L is de-asserted.
- A linear regulator (AREG) which converts the 1.8V input to 1.2V for the AR6302 core circuitry.

1.12 Power Transition Diagram

The AR6302 provides integrated power management and control functions and extremely low power operation for maximum battery life across all operational states by:

- Gating clocks for logic when not needed
- Shutting down unneeded high speed clock sources
- Reducing voltage levels to specific blocks in some states

1.12.1 Hardware Power States

AR6302 hardware has five top level hardware power states managed by the RTC block. Table 1-1 describes the input from the MAC, CPU, SDIO/MBOX, interrupt logic, and timers that affect the power states.

1.12.2 Sleep State Management

Sleep state minimizes power consumption while saving system states. In SLEEP state, all high speed clocks are gated off and the external reference clock source is powered off. For the AR6302 to enter SLEEP state, the MAC, MBOX, and CPU systems must not be active.

The system remains in sleep state until a WAKEUP event causes the system to enter WAKEUP state, wait for the reference clock source to stabilize, and then ungate all enabled clock trees. The CPU wakes up only when an interrupt arrives, which may have also generated the system WAKEUP event.

Figure 1-1 depicts the state transition diagram.

Table 1-1. **Power Management States**

State	Description
OFF	CHIP_PWD_L pin assertion immediately brings the chip to this state.
	Sleep clock is disabled.
	No state is preserved.
HOST_OFF	WLAN is turned off.
	Only the host interface is powered on - the rest of the chip is power gated (off).
	The host instructs the AR6302 to transition to WAKEUP by writing a register in the host interface domain.
	Embedded CPU and WLAN do not retain state (separate entry).
	This state can be bypassed by asserting FORCE_HOST_ON_L during CHIP_PWD_L deassertion.
SLEEP	Only the sleep clock is operating.
	The crystal or oscillator is disabled.
	Any wakeup events (MAC, host, LF-Timer, GPIO-interrupt) will force a transition from this state to the WAKEUP state.
	All internal states are maintained.
WAKEUP	The system transitions from sleep states to ON.
	The high frequency clock is gated off as the crystal or oscillator is brought up and the PLL is enabled.
	WAKEUP duration is programmable.
ON	The high speed clock is operational and sent to each block enabled by the clock control register.
	Lower level clock gating is implemented at the block level, including the CPU, which can be gated off using the WAITI instruction while the system is on. No CPU, host and WLAN activities will transition to sleep states.

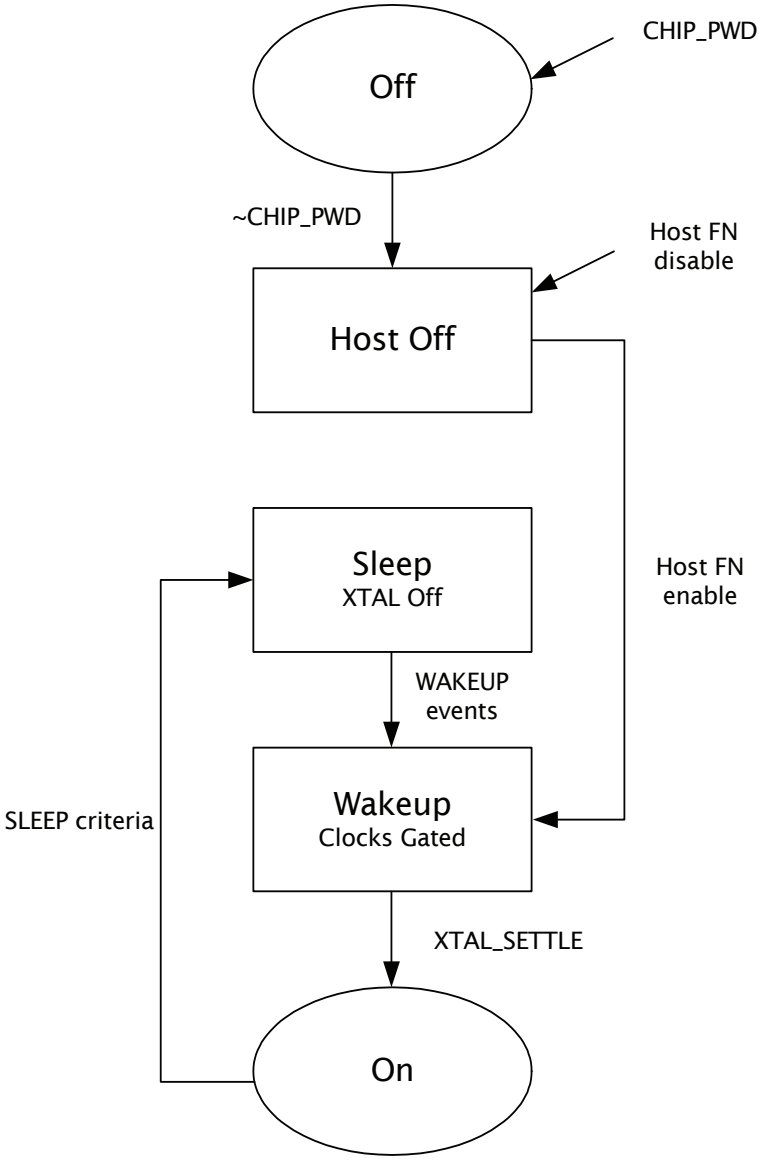

Figure 1-1. **AR6302 Power State**

1.13 System Clocking (RTC Block)

The AR6302 has an RTC block which controls the clocks and power going to other internal modules. Its inputs consist of sleep requests from these modules and its outputs consists of clock enable and power signals which are used to gate the clocks going to these modules. The RTC block also manages resets going to other modules with the device. The AR6302's clocking is grouped into two types: high-speed and low-speed.

1.13.1 High Speed Clocking

The reference clock source drives the PLL and RF synthesizer within the AR6302. It can be either an external crystal or oscillator. To minimize power consumption, the reference clock source is powered off in SLEEP, HOST_OFF, and OFF states. For an external crystal, the AR6302 disables the on-chip oscillator driver. For an external oscillator, the AR6302 de-asserts its CLK_REQ signal to indicate that a reference clock is not needed.

When exiting SLEEP state, the AR6302 waits in WAKEUP state for a programmable duration. During this time, the CLK_REQ signal is asserted to allow for the reference clock source to settle. The CLK_REQ signal remains asserted in ON state.

The AR6302 supports reference clock sharing in all power states. For an external crystal, the on-chip oscillator driver drives a reference clock output whenever an external clock request signal is asserted. For an external oscillator, the external clock request signal is forwarded on the CLK_REQ signal, and the input clock is passed along to the reference clock output.

1.13.2 Low-Speed Clocking

The AR6302 has eliminated the need for an external sleep clock source thereby reducing system cost. Instead, an internal ring oscillator is used to generate a low frequency sleep clock. It is also used to run the state machines and counters related to low power states.

The AR6302 has an internal calibration module which produces a 32.768 KHz output with minimal variation. For this, it uses the reference clock source as the golden clock. As a result, the calibration module adjusts for process and temperature variations in the ring oscillator when the system is in ON state.

The AR6302 also supports using an external low frequency sleep clock source in applications where one is already available.

1.13.3 Interface Clock

The host interface clock represents another clock domain for the AR6302. This clock comes from the SDIO or GSPI host and is completely independent from the other internal clocks. It drives the host interface logic as well as certain registers which can be accessed by the host in HOST_OFF and SLEEP states.

1.14 Front End Control

For applications that use external front-end components, the AR6302 provides the ability to control them with five antenna switch control outputs named as follows:

- ANTA
- ANTB
- ANTC
- ANTD
- ANTE

A programmable switch table indexed by transceiver state offers flexibility for various front-end configurations. The AR6302 supports antenna sharing with another wireless chip in all power states by using ANTE to control the shared antenna switch.

1.15 MAC/BB/RF Block

The AR6302 Wireless MAC consists of five major blocks:

- Host interface unit (HIU) for bridging to the AHB for MC data accesses and APB for register accesses
- Ten queue control units (QCU) for transferring TX data
- Ten DCF control units (DCU) for managing channel access
- Protocol control unit (PCU) for interfacing to baseband
- DMA receive unit (DRU) for transferring RX data

1.16 Baseband Block

The AR6302 baseband module (BB) is the physical layer controller for the 802.11b/g/n air interface. It is responsible for modulating data packets in the transmit direction, and detecting and demodulating data packets in the receive direction. It has a direct control interface to the radio to enable hardware to adjust analog gains and modes dynamically.

1.17 Design for Test

The AR6302 has a built in JTAG boundary scan of its pins. It also has features which enable testing of digital blocks via ATPG scan, memories via MBIST, analog components, and the radio.

2. Radio

The AR6302 transceiver consists of five major functional blocks (see Figure 2-1):

- Receiver (Rx)
- Transmitter (Tx)
- Frequency synthesizer (SYNTH)
- Associated bias/control (BIAS)
- Power Management Unit (PMU)

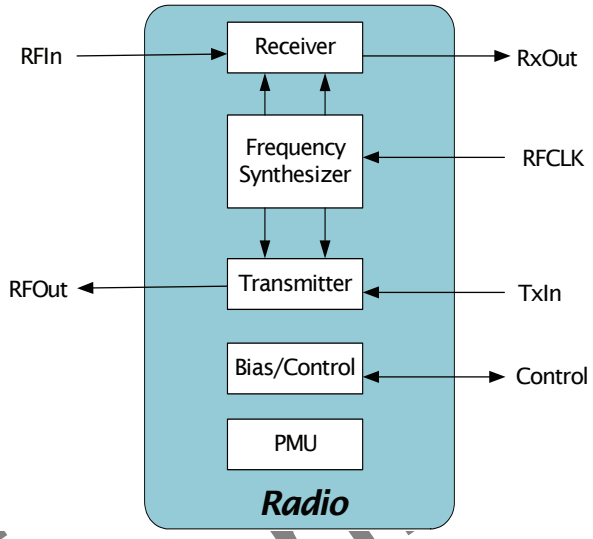

Figure 2-1. **Radio Functional Block Diagram**

2.1 Receiver (Rx) Block

The receiver converts an RF signal (with 40 MHz bandwidth) to baseband I and Q outputs. The receiver is tuned to 2.4 GHz for IEEE 802.11b/g/n signals. Figure 2-2 shows the Radio Tx/Rx block diagram.

For 2 GHz operation, the receiver is comprised of an LNA, a direct conversion mixer, and a baseband programmable gain filter. This receiver is implemented using the direct conversion topology.

For 2 GHz paths, mixers down convert the signal to baseband in-phase (I) and quadrature-phase (Q) signals. The I and Q signals are low-pass filtered and amplified by the baseband programmable gain filter controlled by digital logic. The baseband I and Q signals are sent to the ADC.

The DC offset of the receive chain is reduced using multiple digital to analog converters (DACs) controlled by the MAC/baseband block. Additionally, the receive chain can be digitally powered down to conserve power.

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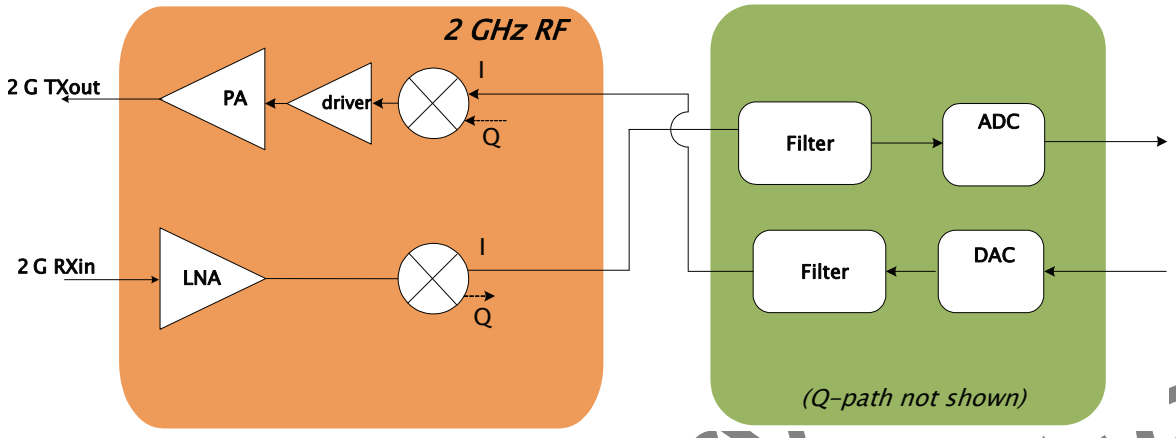

Figure 2-2. **Radio Tx/Rx Block Diagram**

2.2 Transmitter (Tx) Block

The transmitter converts baseband I and Q inputs to bands centered around 2.4 GHz for IEEE 802.11 b/g/n operations. A block diagram is shown in Figure 2-2.

The outputs of the DAC are low pass filtered through an on-chip reconstruction filter to remove spectral images and out-of-band quantization noise.

For 2 GHz operation, the transmitter is comprised of a programmable reconstruction filter, a direct conversion mixer, a preamplifier and a PA. This transmitter is implemented using the direct conversion topology.

The transmit chain can be digitally powered down to conserve power. To ensure that FCC limits are observed and that output power stays close to the maximum allowed, the transmit output power is adjusted by a digitally programmable control loop at the start of each packet. The power control can also compensate for temperature variation.

2.3 Synthesizer (SYNTH) Block

The radio supports an on-chip synthesizer to generate local oscillator (LO) frequencies for the receiver and transmitter mixers. Figure 2-3 shows the synthesizer topology.

The synthesizer can use several crystals such as 19.2, 24, 26, 38.4, 40, and 52 MHz. For AR6302, the default crystal frequency is 26 MHz.

A reference circuitry generates a signal used as the synthesizer reference input. An on-chip voltage controlled oscillator (VCO) provides the desired LO signal based on a phase/frequency locked loop. The loop filter components are all integrated on-chip and can be digitally controlled.

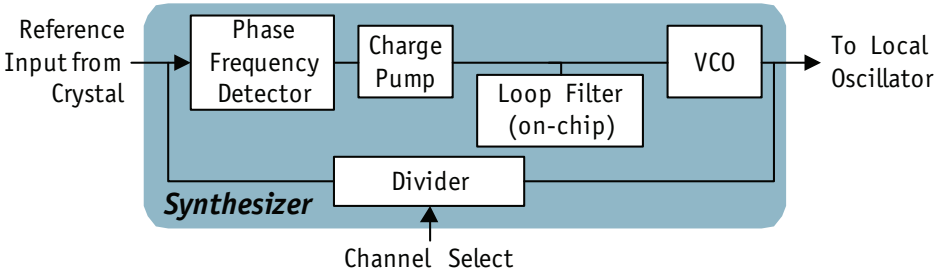

Figure 2-3. **Radio Synthesizer Block Diagram**

2.4 Bias/Control (BIAS) Block

The bias/control block provides reference voltages and currents for all other circuit blocks (see Figure 2-4). An on-chip bandgap reference circuit provides the needed voltage and current references based on an external 6.19 KΩ ± 1% shunted to GND resistor.

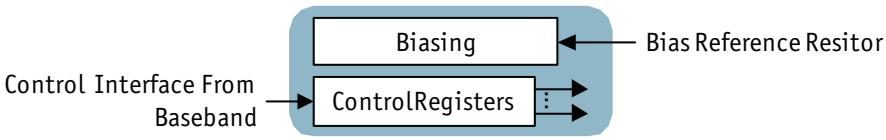

Figure 2-4. **Bias/Control Block Diagram**

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 summarizes the absolute maximum ratings and Table 3-2 lists the recommended operating conditions for the AR6302. Absolute maximum ratings are those values beyond which damage to the device can occur.

Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

NOTE: Maximum rating for signals follows the supply domain of the signals.

Table 3-1. **Absolute Maximum Ratings**

Symbol (Domain)	Parameter	Max Rating	Unit
VREG	Digital 1.8V supply	-0.3 to 2.5	V
AVDD18	Analog 1.8V supply	-0.3 to 2.5	V
DVDD_SOC1	SOC1 GPIO I/O supply	-0.3 to 4.0	V
VDD18_XTAL	Clock sharing interface I/O supply (same as DVDD_SOC1)	-0.3 to 4.0	V
DVDD_SOC2	SOC2 GPIO I/O supply	-0.3 to 4.0	V
DVDD_SDIO	Host interface I/O supply	-0.3 to 4.0	V
VDD33_ANT	Antenna control I/O supply	-0.3 to 4.0	V
VDD33_PA	EPA supply	-0.3 to 4.0	V
VBATTERY_42	External 3.3V supply	-0.3 to 4.0	V
RF_{in}	Maximum RF input (reference to 50-ohm input)	+10	dBm
T_{store}	Storage temperature	-45 to 135	°C
ESD	Electrostatic discharge tolerance	2000	V
1.8V I/O VIH MAX	Maximum digital I/O input voltage for 1.8V I/O supply.	V_{DD} +0.2	V
3.3V I/O VIH MAX	Maximum digital I/O input voltage for 3.3V I/O supply.	V_{DD} +0.3	V
VIH MIN	Minimum digital I/O input voltage for 1.8V or 3.3V I/O supply.	-0.3	V

3.2 Recommended Operating Conditions

Table 3-2. **Recommended Operating Conditions**

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
VREG	Digital 1.8V supply	1.71	1.8	1.89	V
AVDD18	Analog 1.8V supply	1.71	1.8	1.89	V
DVDD_SDIO	Host interface I/O supply	1.71		3.46	V
DVDD_SOC1	SOC1 GPIO I/O supply	1.71		3.46	V
VDD18_XTAL	Clock sharing interface I/O supply (same as DVDD_SOC1)	1.71		3.46	V
DVDD_SOC2	SOC2 GPIO I/O supply	1.71		3.46	V
VBATTERY_42	External 3.3V supply	3.14	3.3	3.46	V
VDD33_ANT	Antenna control I/O supply	1.71		3.46	V
VDD33_PA	EPA supply	3.14	3.3	3.46	V
$T_{ambient}$	Ambient temperature	-40		85	°C

3.3 DC Electrical Characteristics

Table 3-3 and Table 3-4 list the general DC electrical characteristics over recommended operating conditions (unless otherwise specified).

Table 3-3. **General DC Electrical Characteristics (For 3.3 V I/O Operation)**

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage			0.7 x V_{DD}			V
V_{IL}	Low Level Input Voltage					0.3 x V_{DD}	V
I_{IL}	Input Leakage Current	Without Pull-up or Pull-down	0 V < V_{IN} < V_{DD} 0 V < V_{OUT} < V_{DD}	0		-3	nA
		With Pull-up	0 V < V_{IN} < V_{DD} 0 V < V_{OUT} < V_{DD}	16		48	µA
		With Pull-down	0 V < V_{IN} < V_{DD} 0 V < V_{OUT} < V_{DD}	-14		-47	µA
V_{OH}	High Level Output Voltage		I_{OH} = -4mA	0.9 x V_{DD}			V
			I_{OH} = -12mA	0.9 x V_{DD}			V
V_{OL}	Low Level Output Voltage		I_{OH} = 4mA			0.1 x V_{DD}	V
			I_{OH} = 12mA			0.1 x V_{DD}	V

Table 3-4. **General DC Electrical Characteristics (For 1.8 V I/O Operation)**

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage			0.7 x V_{DD}			V
V_{IL}	Low Level Input Voltage					0.3 x V_{DD}	V
I_{IL}	Input Leakage Current	Without Pull-up or Pull-down	0 V < V_{IN} < V_{DD} 0 V < V_{OUT} < V_{DD}	0		-3	nA
		With Pull-up	0 V < V_{IN} < V_{DD} 0 V < V_{OUT} < V_{DD}	3.5		13	µA
		With Pull-down	0 V < V_{IN} < V_{DD} 0 V < V_{OUT} < V_{DD}	-6.2		-23	µA
V_{OH}	High Level Output Voltage		I_{OH} = -4mA	0.9 x V_{DD}			V
			I_{OH} = -12mA	0.9 x V_{DD}			V
V_{OL}	Low Level Output Voltage		I_{OH} = 4mA			0.1 x V_{DD}	V
			I_{OH} = 12mA			0.1 x V_{DD}	V

The following two figures show the recommended power up/down and reset sequences for the AR6302 using external 3.3V and 1.8V supplies.

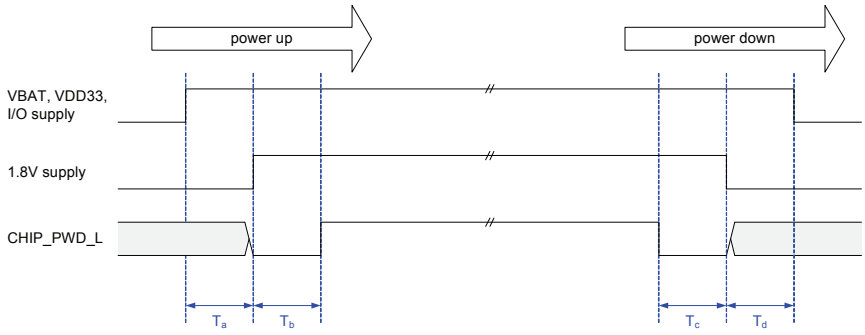

Figure 3-1. **Power Up/Power Down Timing**

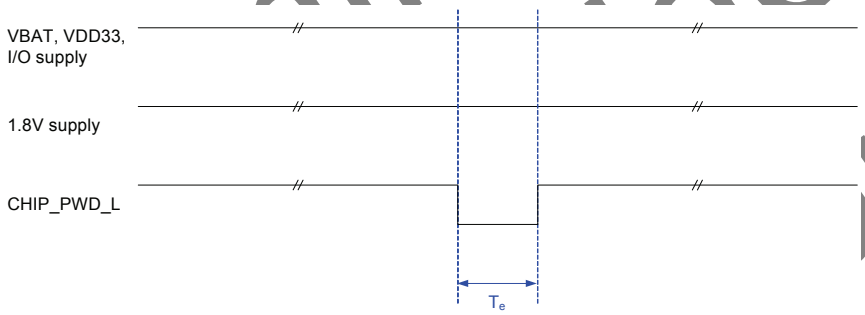

Figure 3-2. **Reset and Power Cycle Timing**

VBAT = VBATTERY_42

VDD33 = VDD33_ANT, VDD33_PA

I/O = DVDD_SDIO, DVDD_SOC1, DVDD_SOC2, VDD18_XTAL

1.8V supply = VREG, AVDD18

Table 3-5. **Timing Diagram Definitions**

	Description	**Min (**μsec)
T_a	Time between VBAT, VDD33, and I/O supplies valid and 1.8V supply valid[1]	0
T_b	Time between 1.8V supply valid and CHIP_PWD_L deassertion	5
T_c	Time between CHIP_PWD_L assertion and 1.8V supply invalid	0
T_d	Time between 1.8V supply invalid and VBAT, VDD33, and I/O supplies invalid	N/A[2]
T_e	Length of CHIP_PWDP_L pulse	5

[1]Supply valid represents the voltage level has reached 90% level.
[2]No strict requirements. This parameter can also be negative.

3.4 Radio Receiver Characteristics

Table 3-6 summarizes the AR6302 receiver characteristics.

Table 3-6. **Receiver Characteristics for 2.4 GHz Operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	Receive input frequency range		2.412		2.484	GHz
S_{rf}	Sensitivity					
	CCK, 1 Mbps	[1]	-93	-97	-99	dBm
	CCK, 2 Mbps		-89	-93	-95	
	CCK, 5.5 Mbps		-87	-91	-94	
	CCK, 11 Mbps		-85	-89	-91	
	OFDM, 6 Mbps		-89	-93	-95	
	OFDM, 9 Mbps		-88	-92	-94	
	OFDM, 12 Mbps		-87	-91	-93	
	OFDM, 18 Mbps		-84	-88	-91	
	OFDM, 24 Mbps		-81	-85	-87	
	OFDM, 36 Mbps		-78	-82	-84	
	OFDM, 48 Mbps		-73	-77	-79	
	OFDM, 54 Mbps		-72	-76	-78	
	HT20, MCS0		-89	-93	-95	
	HT20, MCS1		-86	-90	-93	
	HT20, MCS2		-84	-88	-90	
	HT20, MCS3		-79	-83	-85	
	HT20, MCS4		-77	-81	-82	
	HT20, MCS5		-72	-76	-78	
	HT20, MCS6		-70	-74	-76	
	HT20, MCS7		-69	-73	-75	
R_{adj}	Adjacent channel rejection					
	OFDM, 6 Mbps	[1]	31	37	39	dB
	OFDM, 54 Mbps		17	21	24	
	HT20, MCS0		31	37	39	
	HT20, MCS7		16	20	22	

[1]Performance based on the AR5BSD-00031A with balun, Tx/Rx switch (~1dB loss). Excludes cellular coexistence filter.

3.5 Radio Transmitter Characteristics

Table 3-7 summarizes the transmitter characteristics for AR6302.

Table 3-7. **Transmitter Characteristics for 2.4 GHz operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range		2.412		2.484	GHz
P_{out}	Output power[1]	[2]				
	11b mask compliant	1Mbps	17	18	19	dBm
	11g mask compliant	6Mbps	17.5	19	21	
	11n HT20 mask compliant	MCS0	17	18.5	20	
	11g EVM compliant	54Mbps	15	16	17	
	11n HT20 EVM compliant	MCS7	11	13	16	
A_{pl}	Accuracy of power leveling loop	[3]		±1.5		dB

[1]Refer to IEEE 802.11 specification for transmit spectrum limits:
- 802.11b mask (18.4.7.3)
- 802.11g mask (19.5.4)
- 802.11g EVM (17.3.9.6.3)
- 802.11n HT20 mask (20.3.21.1)
- 802.11n HT20 EVM (20.3.21.7.3)

[2]Performance based on the AR5BSD-00031A with balun, Tx/Rx switch (~1dB loss). Excludes cellular coexistence filter.
[3]Performance based on the AR5BSD-00031A after calibration.

3.6 AR6302 Synthesizer Characteristics

Table 3-8 summarizes the synthesizer characteristics for the AR6302.

Table 3-8. **Synthesizer Composite Characteristics for 2.4 GHz Operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_c	Center channel frequency	Center frequency at 5MHz spacing[1]	2.412		2.484	GHz
F_{ref}	Reference oscillator frequency	±20ppm		26[2]		MHz
F_{step}	Frequency step size (at RF)			1		MHz
TS_{powup}	Time for power up (from sleep)			0.2		ms

[1]Frequency is measured at the Tx output.
[2]Other supported frequencies are: 19.2, 24, 26, 38.4, 40, and 52MHz.

3.7 Typical Power Consumption Performance

Table 3-9. **AR6302 Typical Current Consumption – Low Power States (Individual Voltage Rails)**

Mode		Typical Current Consumption [mA]	
		1.8V[1]	3.3V[2]
Standby	OFF	0.000	0.004
	HOST_OFF	0.043	0.005
	SLEEP	0.210	0.005
IEEE PS[3] (2.4GHz)	DTIM=1	2.011	0.005
	DTIM=3	0.868	0.005
	DTIM=10	0.467	0.005

[1]VREG, VDD18_XTAL, DVDD_SOC1, DVDD_SDIO, DVDD_SOC2, VDD18_BB_SYNTH, VDD18_RF
[2]PAREG_BASE, VBATTERY_42, VDD33_ANT, VDD33_PA
[3]Calculated assuming Rx time of 2ms + 0.1* DTIM

3.7.1 Measurement Conditions for Low Power States

- T_ambient = 25C
- All I/O pins except CHIP_PWD_L are maintained at their default polarities (I/Os without default internal pulls are pulled low).

Table 3-10. **AR6302 Typical Current Consumption [2.4 GHz operation] – Continuous Receive (Individual Voltage Rails)**

Mode/Rate [Mbps]	Typical Current Consumption [mA]		
	1.8V[1]	3.3V[2]	I/O[3]
CCK, 1 Mbps	81	0	5
CCK, 11 Mbps	82	0	5
OFDM, 6 Mbps	83	0	5
OFDM, 54 Mbps	85	0	5
HT20, MCS0	84	0	5
HT20, MCS7	86	0	5

[1]VREG, VDD18_BB, VDD18_SYNTH, VDD18_RF
[2]PAREG_BASE, VBATTERY_42, VDD33_ANT, VDD33_PA
[3]VDD18_XTAL, DVDD_SOC1, DVDD_SDIO, DVDD_SOC2

3.7.2 Measurement Conditions for Continuous Receive [2.4 GHz Operation]

- T_ambient = 25C

- Measured using AR5BSD-00031A with AR6302 Atheros Radio Test software running in broadcast throughput receive mode

Table 3-11. **AR6302 Typical Current Consumption [2.4 GHz operation] – Continuous Transmit (Individual Voltage Rails)**

Mode/Rate [Mbps]	Target Output Power [dBm]	Typical Current Consumption [mA]		
		1.8V[1]	3.3V[2]	I/O[3]
CCK, 1 Mbps	18.5	58	177	5
CCK, 11 Mbps	18.5	58	175	5
OFDM, 6 Mbps	19.0	64	168	5
OFDM, 54 Mbps	16.5	65	123	5
HT20, MCS0	18.5	64	163	5
HT20, MCS7	13.0	65	99	5

[1]VREG, VDD18_BB, VDD18_SYNTH, VDD18_RF
[2]PAREG_BASE, VBATTERY_42, VDD33_ANT, VDD33_PA
[3]VDD18_XTAL, DVDD_SOC1, DVDD_SDIO, DVDD_SOC2

3.7.3 Measurement Conditions for Continuous Transmit [2.4 GHz Operation]

- T_ambient = 25C
- Measured using AR5BSD-00039A with AR6302 Atheros Radio Test software running in continuous transmit mode.
- Output power is targeted on AR5BSD-00039A with balun, Tx/Rx switch (~1dB loss). Excludes cellular coexistence filter.

4. AC Specifications

4.1 External 19.2/24/26/38.4/40/52 MHz Reference Input Clock Timing

Figure 4-1 and Table 4-1 show the external 19.2/24/26/38.4/40/52 MHz reference input clock timing requirements.

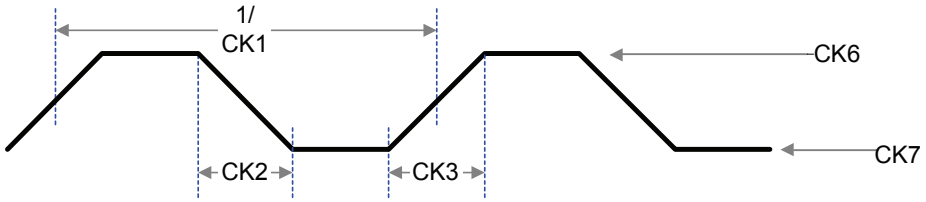

Figure 4-1. **External 19.2/24/26/38.4/40/52 MHz**

Table 4-1. **External 19.2/24/26/38.4/40/52 MHz Reference Input Clock Timing**

Symbol	Description	Min	Typ	Max	Unit
CK2	Fall time	-	-	0.1 x period	ns
CK3	Rise time	-	-	0.1 x period	ns
CK4	Duty cycle (high-to-low ratio)	40	-	60	%
CK5	Frequency stability	-20	-	20	ppm
CK6	Input high voltage	0.75		3.46	V
CK7	Input low voltage	-0.55		0.3	V

4.2 SDIO/GSPI Interface Timing

Figure 4-2 shows the SDIO timing. Figure 4-3 shows the write timing for GSPI style transactions.

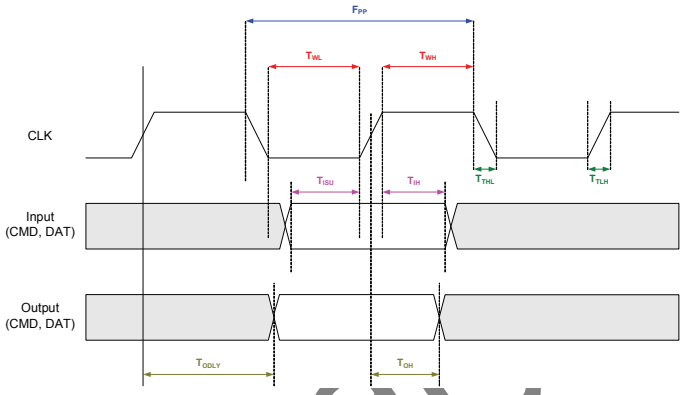

Figure 4-2. **SDIO 2.0 Timing**

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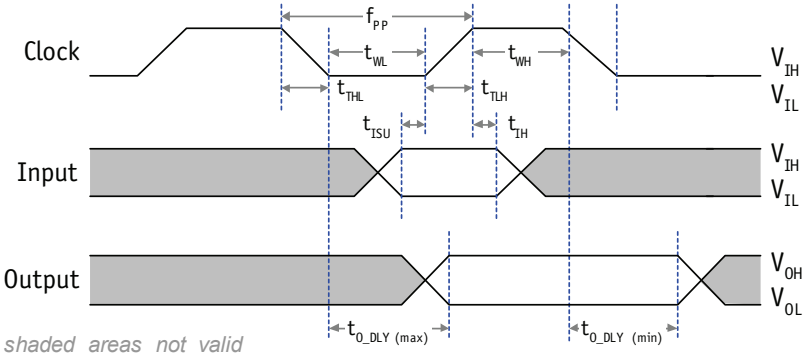

Figure 4-3. **GSPI Timing**

Table 4-2 shows the values for timing constraints for SDIO.

Table 4-2. **SDIO Timing Constraints**

Parameter	Description	Min	Max	Unit	Note
f_{PP}	Clock frequency data transfer mode	0	50	MHz	40 pF ≥ C_L
t_{WL}	Clock low time	7	-	ns	40 pF ≥ C_L
t_{WH}	Clock high time	7	-	ns	40 pF ≥ C_L
t_{TLH}	Clock rise time	-	10	ns	40 pF ≥ C_L
t_{THL}	Clock fall time	-	10	ns	40 pF ≥ C_L
t_{ISU}	Input setup time	6	-	ns	40 pF ≥ C_L
t_{IH}	Input hold time	2	-	ns	40 pF ≥ C_L
t_{OH}	Output hold time	2.5	-	ns	40 pF ≥ C_L
$t_{O\_DLY\ (min)}$	Output delay time during data transfer mode	0	14	ns	40 pF ≥ C_L

Table 4-3 shows the values for timing constraints for GSPI.

Table 4-3. **GSPI Timing Constraints**

Parameter	Description	Min	Max	Unit
f_{PP}	Clock frequency	0	48	MHz
t_{WL}	Clock low time	8.3	-	ns
t_{WH}	Clock high time	8.3	-	ns
t_{TLH}	Clock rise time	-	2	ns
t_{THL}	Clock fall time	-	2	ns
t_{ISU}	Input setup time	5	-	ns
t_{IH}	Input hold time	5	-	ns
t_{O_DLY}	Output delay	0	5	ns

5. Pin Descriptions

This section contains a listing of the signal descriptions (see Figure 5-1 for the AR6302 QFN package pin-out).

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types described in Table 5-1:

IA	Analog input signal
I	Digital input signal
IO	Digital bidirectional signal
OA	An analog output signal
O	A digital output signal
P	A power or ground signal

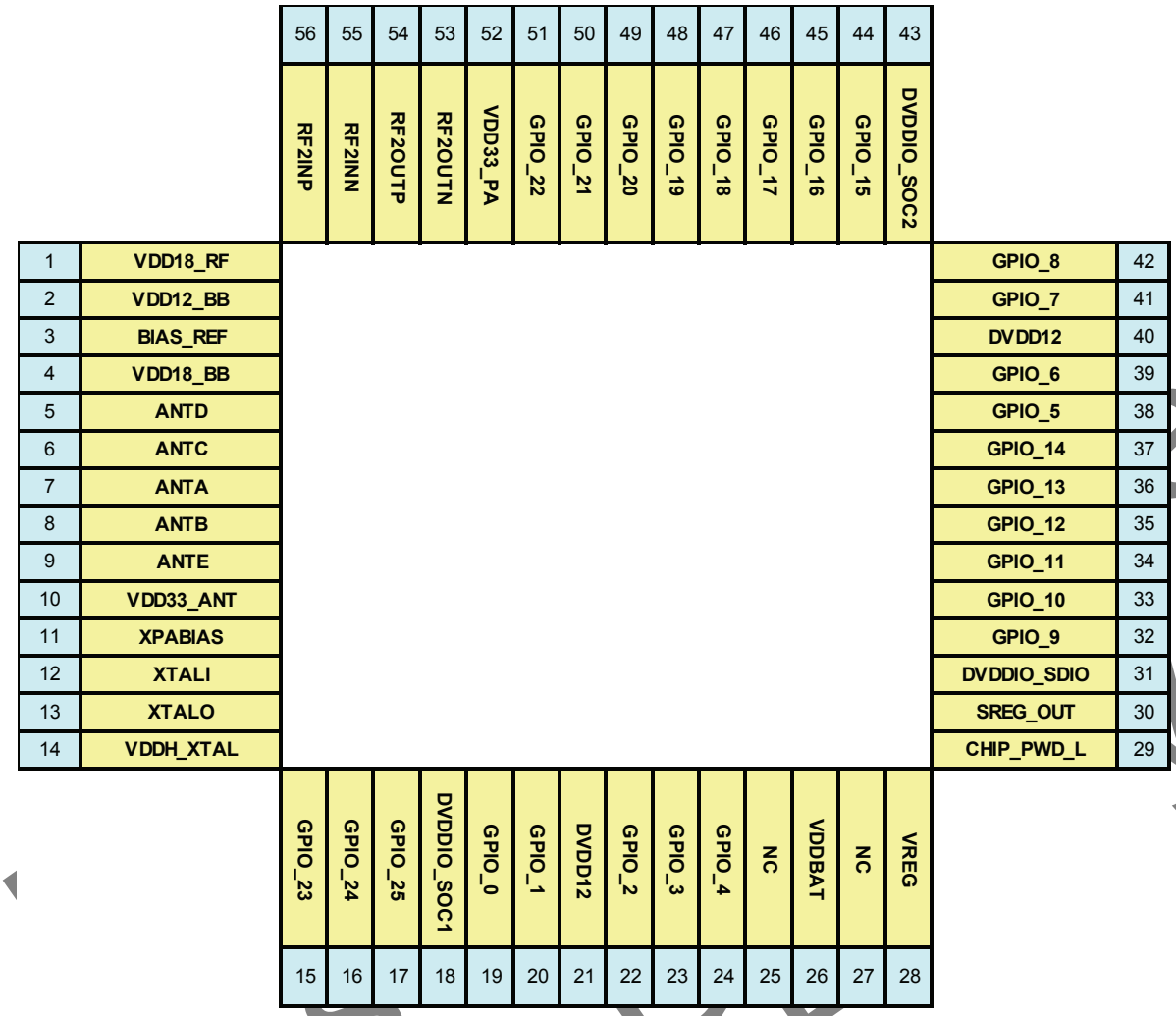

Figure 5-1. **AR6302 QFN Pinout**

Table 5-1. **AR6302 Package Pinout**

Pin	Name	Description	Signal Name/ Type
1	VDD18_RF	Analog 1.8V supply	P
2	VDD12_BB	Analog 1.2V output	P
3	BIAS_REF	Reference for internal analog biasing	IA
4	VDD18_BB	Analog 1.8V supply	P
5	ANTD	Control signal for RF front end components	O
6	ANTC	Control signal for RF front end components	O
7	ANTA	Control signal for RF front end components	O
8	ANTB	Control signal for RF front end components	O
9	ANTE	Control signal for RF front end components	O
10	VDD33_ANT	Antenna control I/O supply	P
11	XPABIAS	Bias Voltage for 2.4 GHz external PA	
12	XTALI	Reference crystal interface signal	
13	XTALO	Reference crystal interface signal or external reference clock input	
14	VDDH_XTAL	Clock sharing interface I/O supply	P
15	GPIO_23	Reference clock output to BT chip	O
16	GPIO_24	Clock request signal from BT chip	I
17	GPIO_25	CLK_REQ signal indicating when a reference clock is needed	O
18	DVDDIO_SOC1	SOC1 GPIO I/O supply	P
19	GPIO_0	BT FREQUENCY signal from BT chip	I
20	GPIO_1	WLAN ACTIVE signal to BT chip	O
21	DVDD12	Digital 1.2V core supply	P
22	GPIO_2	BT ACTIVE signal from BT chip	I
23	GPIO_3	BT_PRIORITY signal from BT chip	I
24	GPIO_4	Optional software GPIO	I
25	NC	No connection should be made to this pin	
26	VDDBAT	External 3.3V supply	P
27	NC	No connection should be made to this pin	P
28	VREG	Digital 1.8V supply	P
29	CHIP_PWD_L	Reset signal to power down the AR6302	I
30	SREG_OUT	SREG output	P
31	DVDDIO_SDIO	Host interface I/O supply	P
32	GPIO_9	SDIO command (also GSPI MOSI)	IO
33	GPIO_10	SDIO data pin bit 3 (also GSPI CS)	IO
34	GPIO_11	SDIO data pin bit 2	IO

Table 5-1. **AR6302 Package Pinout**

35	GPIO_12	SDIO data pin bit 1 (also GSPI host interrupt)	IO
36	GPIO_13	SDIO data pin bit 0 (also GSPI MISO)	IO
37	GPIO_14	SDIO clock (also GSPI clock)	I
38	GPIO_5	JTAG TMS Input	I
39	GPIO_6	JTAG TCK Input	I
40	DVDD12	Digital 1.2V core supply	P
41	GPIO_7	JTAG TDI Input	I
42	GPIO_8	JTAG TDO Output	O
43	DVDDIO_SOC2	SOC2 GPIO I/O supply	P
44	GPIO_15	HCI UART TXD	O
45	GPIO_16	HCI UART RTS	O
46	GPIO_17	HCI UART RXD	I
47	GPIO_18	HCI UART CTS	I
48	GPIO_19	GPIO_19 and GPIO_20 are used to select the host interface (SDIO or GSPI)	I
49	GPIO_20	GPIO_19 and GPIO_20 are used to select the host interface (SDIO or GSPI)	I
50	GPIO_21	Optional external input sleep clock	I
51	GPIO_22	Optional Wake On Wireless output	O
52	VDD33_PA	EPA supply	P
53	RF2OUTN	2.4 GHz RF output	OA
54	RF2OUTP	2.4 GHz RF output	OA
55	RF2INN	2.4 GHz RF input	IA
56	RF2INP	2.4 GHz RF input	IA

6. Package Dimensions

- 7 x 7 mm (body size), 0.4 mm pitch QFN-56

Dimensions

The AR6302 package drawing and measurements are provided in Figure 6-1 . Also see Table 6-1 for dimensions.

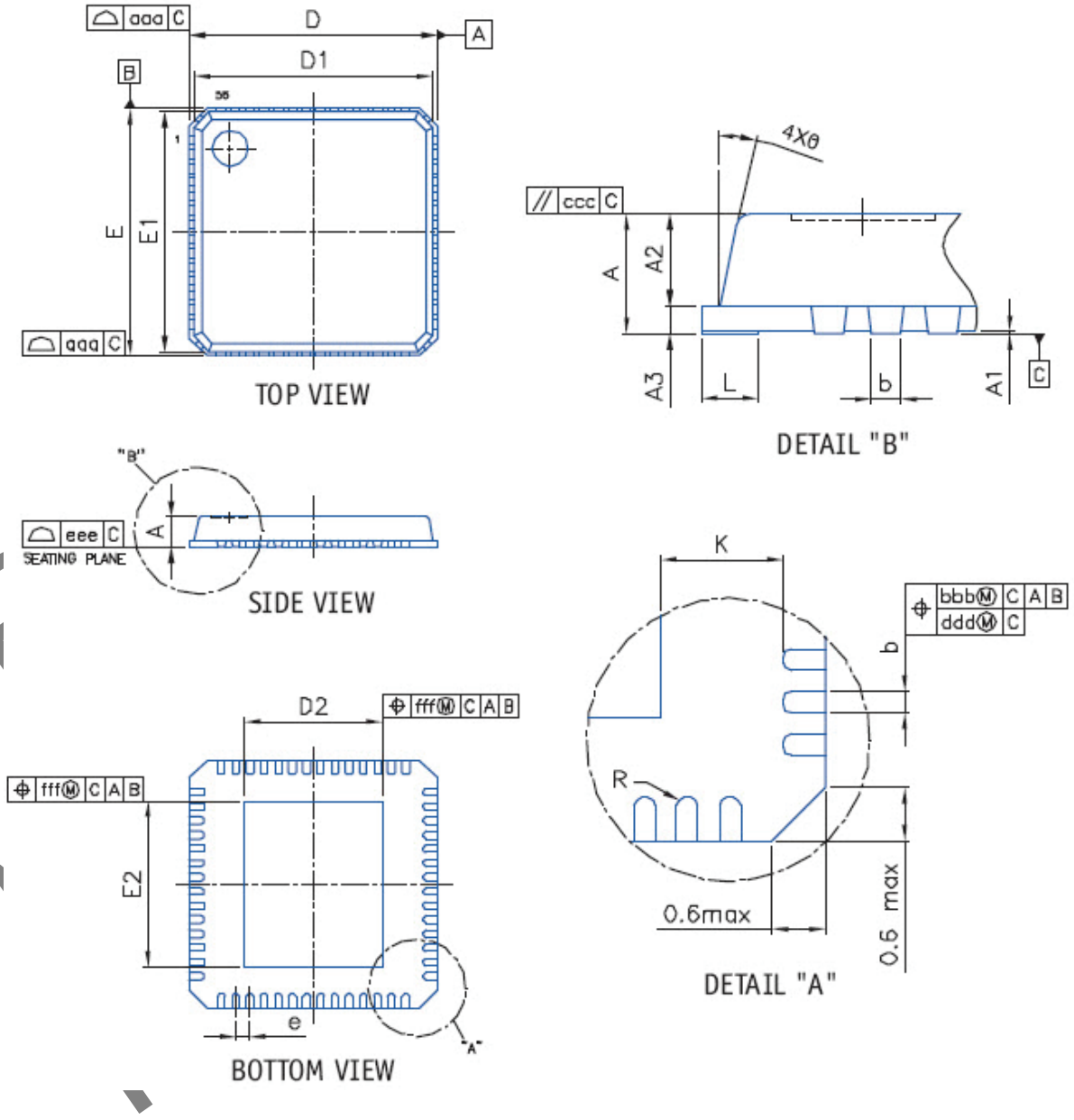

Figure 6-1. **7 x 7mm QFN Package Dimensions**

Table 6-1. **Package Dimensions**

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	0.80	0.85	0.90	mm	0.031	0.033	0.035	inches
A1	0.00	0.02	0.05	mm	0.000	0.001	0.002	inches
A2	0.60	0.65	0.70	mm	0.024	0.026	0.028	inches
A3		0.20 REF		mm		0.008 REF		inches
b	0.15	0.20	0.25	mm	0.006	0.008	0.010	inches
D/E	6.90	7.00	7.10	mm	0.272	0.276	0.280	inches
D1/E1		6.75 BSC		mm		0.266 BSC		inches
D2/E2	4.45	4.60	4.75	mm	0.175	0.181	0.187	inches
e		0.40 BSC		mm		0.016 BSC		inches
L	0.30	0.40	0.50	mm	0.012	0.016	0.020	inches
θ	0°	—	14°	°	0°	—	14°	°
R	0.075	—	—	mm	0.003	—	—	inches
K	0.20	—	—	mm	0.008	—	—	inches
aaa	—	—	0.10	mm	—	—	0.014	inches
bbb	—	—	0.07	mm	—	—	0.003	inches
ccc	—	—	0.10	mm	—	—	0.004	inches
ddd	—	—	0.05	mm	—	—	0.002	inches
eee	—	—	0.08	mm	—	—	0.003	inches
fff	—	—	0.10	mm	—	—	0.004	inches

Notes:
1. Controlling dimension: Millimeters.
2. Reference document: JEDEC MO–220.

7. Ordering Information

The AR6302 may be ordered as follows:

- AR6302G-AL1B (2.4 GHz, QFN)

MKG-14831 Rev. 1

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