Monarch Platform - VZM20Q Module

Datasheet

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Preface

Legal Notices

Document Revision History

Revision	Date	Product Application
01	July 2016	First edition.
02	January 2017	Second edition of VZM20Q Datasheet.
03	July 2018	Third edition of VZM20Q Datasheet. See detail on changes in Section Changes in this Document on page iii.

About this Datasheet

Purpose and Scope

The VZM20Q is a complete Verizon Wireless certified LTE Category M1 module including base-band, RF and memory, for the design of connected machine-to-machine devices, and other Internet-of-Things devices with embedded LTE connectivity. This document provides technical information about VZM20Q LGA module. VZM20Q is based on Sequans' Monarch platform.

Who Should Read this Datasheet

This document is intended for engineers who are developing User Equipment (UE) for LTE systems.

Changes in this Document

The changes since the previous edition of the document are as follows:

- Updated ECCN in Section 3.1 ECCN and Part Number on page 6.
- Added a note related to default configuration at boot time for GPIO and RFDATA pads in Section 3.5 I/O Characteristics on page 11.
- Added ADC specification in Section 3.6 Auxiliary ADC on page 14.
- Added an important note on UART0 configuration on host side in Section 4.2 UART Interfaces on page 21.
- Added detail on WAKE pins characteristics in Section 4.4.1 General Information on page 24.
- Added Sections Detailed Behavior of IO Pads of BIDIR Type and Detailed Behavior of IO Pads of BIDIR_WAKE Type in Section 4.4 LTE Low Power Mode on page 24.
- Added details in Section 3.10 Packing Information on page 17.

- Updated FCC id.
- Change of layout of xls pinlist companion file. Some edits, including in signal descripions for `CTS0`, `GPIO25/RING0`, `WAKE0`, `WAKE1`, `GPIO2/PS_STATUS`, `GPIO24`.
- Various edits

References

[1]
- Verizon Wireless Unified Module Process for Compliance Testing and Approval, Version 12.0; Feb 2015
- Verizon Wireless Device Requirements LTE 3GPP Band 13 Network Access, Version 29.00; June 2016
- Verizon Wireless Device Requirements LTE 3GPP Multi-Band Network Access, Version 3.00; June 2016

[2] Core technology specifications:
- 3GPP E-UTRA 21 series Release 13 (EPS)
- 3GPP E-UTRA 22 series Release 13 (IMEI)
- 3GPP E-UTRA 23 series Release 13 (NAS, SMS)
- 3GPP E-UTRA 24 series Release 13 (NAS)
- 3GPP E-UTRA 31 series Release 13 (UICC)
- 3GPP E-UTRA 33 series Release 13 (security)
- 3GPP E-UTRA 36 series Release 13 (RAN)
- 3GPP2 C.S0015-A v1.0 (SMS)
- IETF, RFC 3261, 4861, 4862, 6434

For more information, see
- ftp://ftp.3gpp.org/Specs/archive/
- http://www.3gpp2.org/public_html/specs/CS0015-0.pdf
- https://tools.ietf.org/html/

[3] Test specifications:
3GPP E-UTRA 36 series Release 13 (RAN)
ftp://ftp.3gpp.org/Specs/archive/

[4] Vocabulary reference:
- 3GPP TR 21.905: "Vocabulary for 3GPP Specifications"

For more information, see http://www.3gpp.org/ftp/specs/archive/21_series/21.905/

Documentation Conventions

This section illustrates the conventions that are used in this document.

General Conventions	
Note	Important information requiring the user's attention.
Caution 	A condition or circumstance that may cause damage to the equipment or loss of data.
Warning 	A condition or circumstance that may cause personal injury.
Italics	Italic font style denotes • emphasis of an important word; • first use of a new term; • title of a document.
Screen Name	Sans serif, bold font denotes • on-screen name of a window, dialog box or field; • keys on a keyboard; • labels printed on the equipment.

Software Conventions	
`Code`	Regular Courier font denotes code or text displayed on-screen.
Code	Bold Courier font denotes commands and parameters that you enter exactly as shown. Multiple parameters are grouped in brackets [ ]. If you are to choose only one among grouped parameters, the choices are separated with a pipe: [parm1 | parm2 | parm3] If there is no pipe separator, you must enter each parameter: [parm1 parm2 parm3]
`Code`	Italic Courier font denotes parameters that require you to enter a value or variable. Multiple parameters are grouped in brackets [ ]. If you are to choose only one among grouped parameters, the choices are separated with a pipe: [parm1 | parm2 | parm3] If there is no pipe separator, you must enter a value for each parameter: [parm1 parm2 parm3]

Table of Contents

1 Product Features

1.1 Features Description

Sequans VZM20Q module includes Monarch SQN3330 Cat-M1 baseband, a complete dual band RF front end, memory and required circuitry to meet 3GPP E-UTRA (Long Term Evolution - LTE, Release 13 set of specifications) and Verizon Wireless LTE Cat-M1 UE specifications.

For more information on the core technology specifications see the section References on page iv. The term VZM20Q module refers to the hardware and the associated embedded software.

The architecture block diagram of the VZM20Q is presented on Figure 1-1.

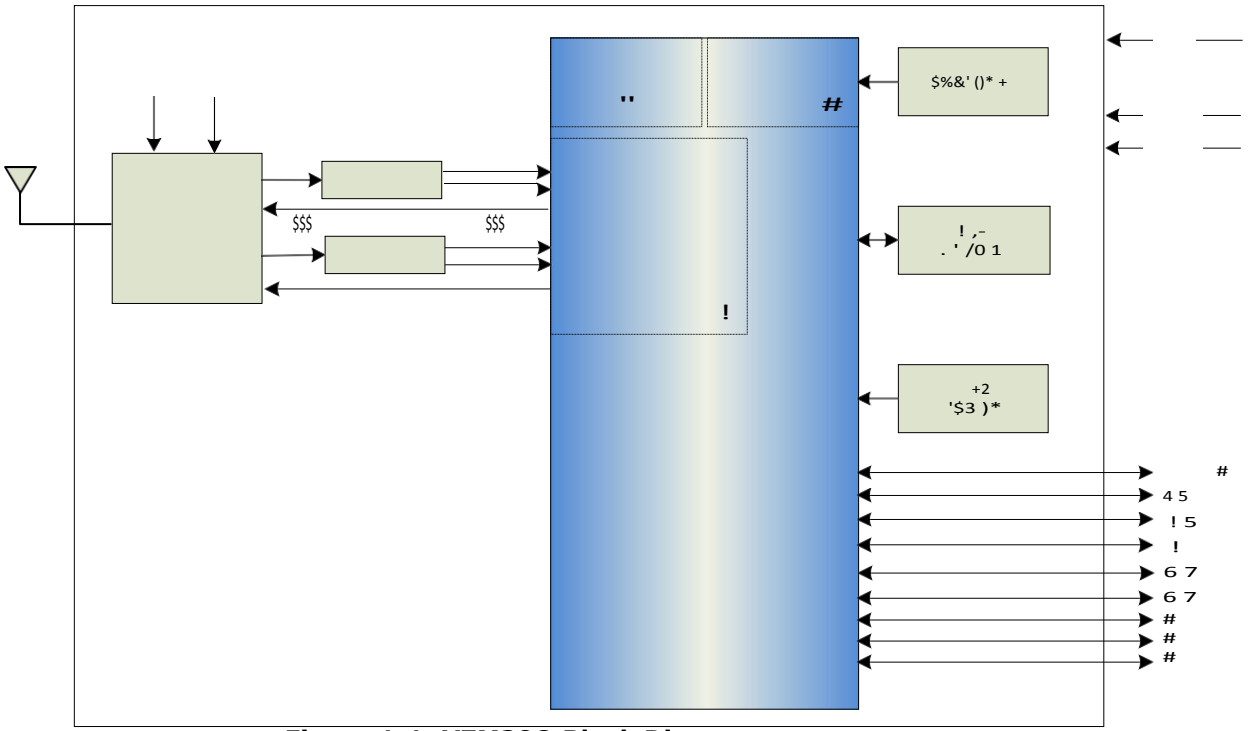

Figure 1-1: VZM20Q Block Diagram

Table 1-1 on page 2 provides detail on general features of the VZM20Q.

Table 1-2 on page 2 provides detail for the LTE-related features of the VZM20Q.

VZM20Q's ECCN and part number are detailed in the Section 3.1 ECCN and Part Number on page 6.

Table 1-1: General Features

General interfaces	• JTAG • I2C (reserved) • USIM • SPI (reserved) • GPIO • UART (x3, including one reserved)
Supported Frequency Bands	• LTE Band 4 • LTE Band 13
Operation voltages	• V_{bat1} (range from 3.1 V to 4.5 V)
Packaging	• LGA module • 108 pads (21.35 x 20.25 x 1.79 mm) • RoHS compliant, halogen-free
Operating temperature	• RF compliant -30°C to +60°C (ambient) • Operational: -40°C to +85°C (board) See also Section 3.3 Environmental Operating Conditions on page 9.
Humidity	• 10% to 85% See also Section 3.3 Environmental Operating Conditions on page 9.

Table 1-2: LTE Features

Standard compliance	• 3GPP E-UTRA Release 13 compliant

Table 1-2: LTE Features (Continued)

PHY	• One UL and one DL transceiver • Support of HD-FDD Duplexing • Category M1 UE • Channel 1.4 MHz bandwidth • Normal and extended cyclic prefix • Support of MPDCCH • Modulation - DL: QPSK, 16QAM - UL: QPSK, 16QAM • All coding schemes corresponding to modulations • All channel coding (turbo-coding with interleaver, tail biting convolutional coding, block and repetition coding) and CRC lengths • Sounding (including in special subframes) • Control and data in special subframes • All power control schemes and DL power allocation schemes • HARQ Incremental Redundancy and Chase Combining, with bundling or multi-plexing • Measurements and computations related to CQI (Channel Quality Indicator), PMI (Pre-coding Matrix Indicator) and RI (Rank Indicator), RSRP, and RSRQ • UEPCOP (from 3GPP Release 12) Power Saving Mode
MAC	• Random Access procedure in normal and special subframes • Scheduling Request, Buffer Status Reporting, and Power Headroom Reporting • Discontinuous reception (DRX, eDRX) with long and short cycles • Fast scanning • Hosted configuration • IPv4, IPv6 • RoHC • Location based services • Advanced QoS features
RLC	• ARQ modes: UM, AM, and TM
PDCP	• Ciphering and deciphering: NULL, AES, SNOW 3G • Integrity and protection: AES, SNOW 3G
RRC	• MIB and new SIB1bis • Intra and inter-frequency measurements and handover • Up to 8 Data Radio Bearers supported • Support of CE (Coverage Extension) Mode
NAS and above	• NAS • SMS over SG • LWM2M Client

2 FCC Regulation Warning

Attention: FCC-ID: 2AAGMVZM20Q (limited modular approval)
This above identified LTE radio module is not intended to be provided to end-users but is for installation by OEM integrators only.

Installation/Integration

OEM integrators must follow Sequans installation instructions to provide for and benefit from FCC compliant module integrations and must abide especially by the following:

The maximum antenna gain values (accounting for cable attenuation) to comply with the FCC maximum ERP/EIRP limits and with RF Exposure rules:

– LTE band 13 (700 MHz): 3 dBi

– LTE band 4 (1700 MHz): 3 dBi

The Sequans' module integration guidelines must be closely followed.

Compliance of host integrations of the module is limited to hosts adaptation designs which are identical to Sequans' reference design.

Host integrations with adaption designs deviating from Sequans' reference design require either class 2 permissive change to this modular approval or a separate host approval with different FCC-ID;

Host integrations with co-located (simultaneously operating) radio transmitters must be evaluated in accordance with FCC multi-transmitter rules and may require either class 2 permissive change to this modular approval or a separate host approval with different FCC-ID, dependent on the result of the evaluation; Inquiry at FCC or a TCB is urgently recommended.

Integrations of the module into host products which are intended for portable use, i.e. less than 20cm distance between its radiating structures (antenna) and the body of nearby persons, or which otherwise put additional technical requirements like Hearing Aid compatibility require either class 2 permissive change to this modular approval or a separate host approval with different FCC-ID;

Compliance with Unwanted Emission Limits for Digital Device

If the OEM host integration fully complies with the above described reference design and can completely inherit and rest on compliance of the existing modular approval the OEM remains still responsible to show compliance of the overall end-product with the FCC limits for unwanted conducted and radiated emissions from the digital device (unintentional radio) portion of such end-product (commonly addressed as part 15B compliance or similar).

End-product Labelling

– FCC-ID

The module's FCC-ID must either be visible from the exterior of the host product (e.g. per window) or per electronic display, or shall be displayed on an additional exterior label per the following or similar string:

```
contains FCC-ID: 2AAGMVZM2OQ
```

– Digital Device - Unwanted Emissions Notice

If the end-product falls under part 15 of the FCC rules (it shall display the following user notice on its exterior acc. to part 15.19 (the notice may be printed in the manual in case the host is too small):

```
This device complies with Part 15 of the FCC Rules.
Operation is subject to the following two conditions:
(1) This device may not cause harmful interference,
and
(2) This device must accept any interference received, including interference that may
cause undesired operation.
```

– Further Labelling Requirements may apply dependent on the FCC rule parts relevant to the host product.

– End-product User Instructions / Notices in the Manual

At a minimum, end-product users must be provided with the following notices at a prominent location of the product literature furnished with the product:

```
* Product Modifications
Modifications not expressly approved by the party responsible for compliance could void
the user's authority to operate this equipment.
* RF Exposure Compliance
This equipment complies with FCC radio frequency radiation exposure rules and limits set
forth for an uncontrolled environment, when installed and operated with minimum distance
of 20cm between its radiating structures (antenna) and the body of nearby persons and
when not operated simultaneously with other nearby radio-transmitters.
```

– Maximum Antenna Gain

The user instructions of end-products equipped with standard external antenna connectors for the modular radio transmitter providing the option to connect other antennae than those which may or may not be bundled with the end-product must list the maximum allowed antenna gain values as derived from those given above, accounting for the cable attenuations of the actual installation.

– Digital Device - Unwanted Emissions Notice

If the end-product is or contains a digital device (unintentional radio portions) and is not exempted by its use case (like vehicular use) the following part 15.105 (b) user notice shall be provided at prominent location of the product literature:

```
This equipment has been tested and found to comply with the limits for a Class B digital
device, pursuant to part 15 of the FCC rules. These limits are designed to provide
reasonable protection against harmful interference in a residential installation.
This equipment generates uses and can radiate radio frequency energy and, if not
installed and used in accordance with the instructions, may cause harmful interference to
radio communications. However, there is no guarantee that interference will not occur in
a particular installation. If this equipment does cause harmful interference to radio or
television reception, which can be determined by turning the equipment off and on, the
user is encouraged to try to correct the interference by one or more of the following
measures:
o Reorient or relocate the receiving antenna.
o Increase the separation between the equipment and receiver.
o Connect the equipment into an outlet on a circuit different from that to which the
receiver is
connected.
o Consult the dealer or an experienced radio/TV technician for help.
```

– Further User Notices

May be required dependent on the FCC rule parts relevant to the host product.

– Non-allowed User Instructions

The end-product user guidance may NOT include instructions about how to install or de-install the module.

3 Physical Characteristics

3.1 ECCN and Part Number

The orderable part number of the VZM20Q module is VM20R63QRZ.

The ECCN of the VZM20Q module is 5A992.c. CCATS number is G168006.

The following comment from licensing officer is reported on the license information:

- This encryption item is described in paragraph B to note 3 (mass market note) of category 5 part 2. It is authorized for export and reexport under section 740.17(B)(3) of the export administration regulations (EAR).

3.2 Electrical Operating Conditions

3.2.1 Detailed Information

Table 3-1 describes the electrical operating conditions for VZM20Q.

Table 3-1: Electrical Operating Conditions

	Direction	Minimum	Typical	Maximum
VBAT1	In	3.1 V		4.5 V
SIM_VCC (1.8 V or 3.0 V)	Out	1.62 V	1.8 V	1.98 V
		2.7 V	3.0 V	3.3 V
1V8 See notes below.	Out	1.71 V	1.8 V	1.89 V
3V0 See note 2 below.	Out	2.85 V	3.0 V	3.15 V
VCC1_PA	In	2.85 V	3.0 V	3.3 V
VCC2_PA	In	2.85 V	3.0 V	3.3 V

Note:

1. The maximum current consumption allowed from the 1V8 reference pin is 100 mA.
2. Each output reference voltage (1V8, 3V0) can be either running or powered off depending on the internal software configuration. They should not be used to power external IC or parts that require permanent supply.

3.2.2 VZM20Q Power Tree

Figure 3-1 provides a representation of the power tree of the VZM20Q. All current values are maximum RMS current.

Note:	SKY68000 is the Front-End module.

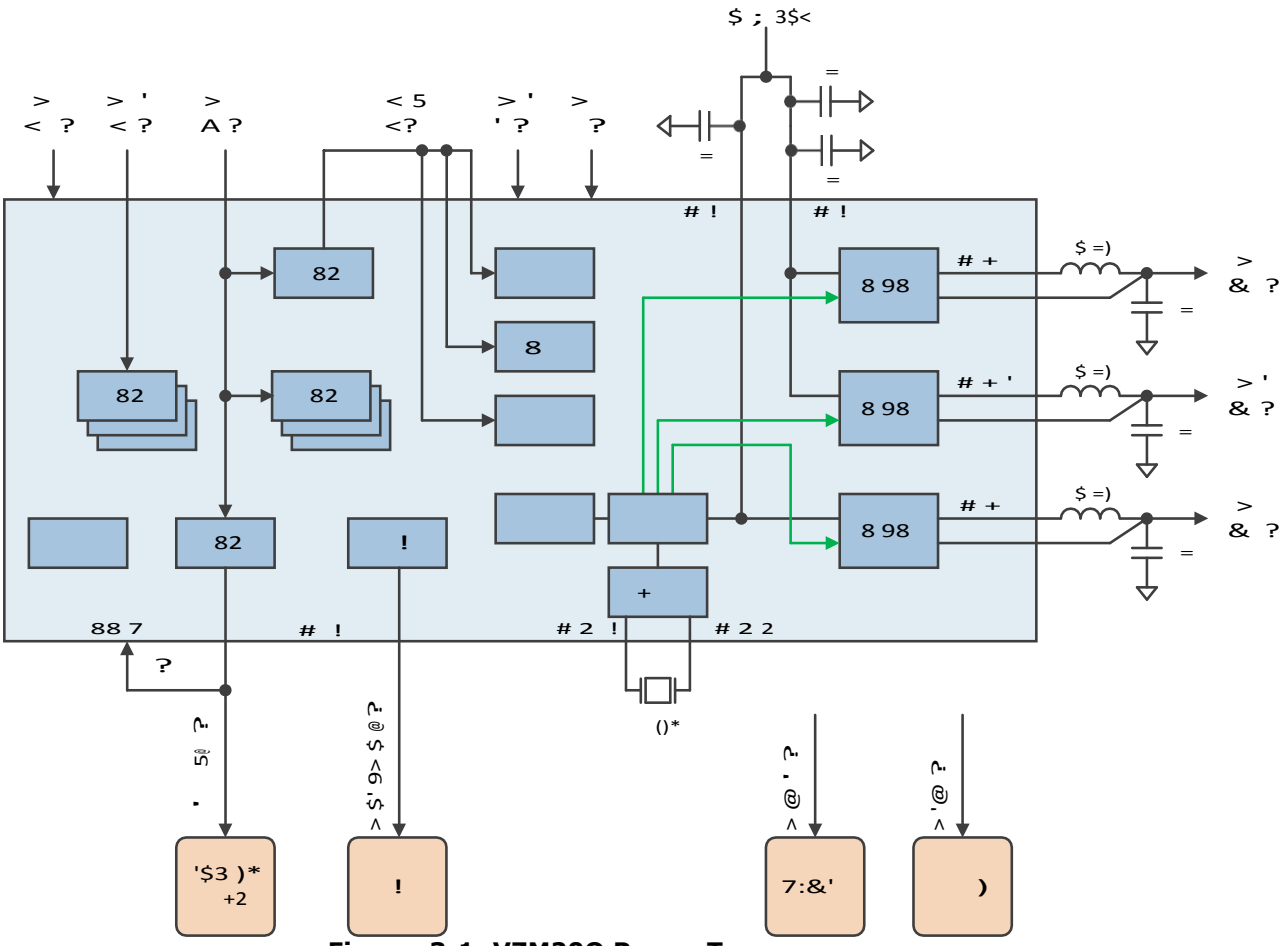

Figure 3-1: VZM20Q Power Tree

3.2.3 Power Supplies Environment

Figure 3-2 illustrates the connections between the RF front-end power supplies of the VZM20Q.

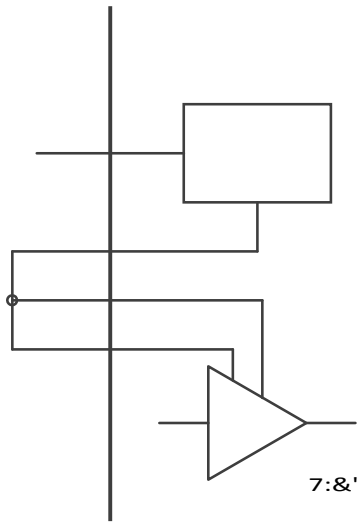

Figure 3-2: VZM20Q LTE RF Front-End Power Supplies Diagram

3.3 Environmental Operating Conditions

3.3.1 Temperature

- RF compliant: -30°C to +60°C (ambient)
- Operational, with additional software to limit TxPower: -40°C to +85°C (measured on board)
- Storage: -40°C to +85°C

3.3.2 Humidity

- Operating: 10% to 85% (non condensing)
- Storage: 5% to 85% (non condensing)

3.4 Power Supply Dimensioning

Important: - Information provided here is ***estimated peak current consumption*** for the VZM20Q Module in various LTE Tx/Rx configurations, with and without the DC/DC losses. It represents the maximum RMS current.

- The power consumption depends on LTE band of operation. The figures in Table 3-2 are provided for LTE Band 13 only. Please contact your Sequans' representative for LTE Band 4 figures.

- Average and detailed power consumption figures are provided in Sequans' Software Release Notes.

Table 3-2: Estimated Peak Current and Peak Power Consumption (LTE Band 13)

		Estimated Peak Power Consumption	Estimated Battery Peak Current (for V_{BAT1}=4.2 V)
TX	TX Power = 23 dBm	1.8 W	430 mA
	TX Power = 20 dBm	1.6 W	380 mA
	TX Power = 18 dBm	1.5 W	360 mA
	TX Power = 13 dBm	1.3 W	310 mA
RX		1.1 W	260 mA

3.5 I/O Characteristics

The voltage and current characteristics of the various IO pads of the VZM20Q versus IO bank supply voltage are illustrated in the tables below.

Caution: Note that the V_{oh} values in the tables below do not apply to GPIOs configured in open drain mode. GPIOs can be individually configured in open drain mode. When in open drain mode they either drive the line to V_{ol}, or leave it floating, to be pulled up by an external pullup resistance. The PCB designer must ensure that the voltage on these pads never exceeds V_{ih} of the IO group to which they belong.

Refer to VZM20Q Pin List to know the type of IO pad used on every termination.

- The Minimum values for I_{ol} and I_{oh} should not be exceeded to guarantee that the logical level are not spoiled for each pad type.
- The Nominal values for I_{ol} and I_{oh} represent the nominal values for the pad type. They are provided for information only.

- The Maximum values for I_{ol} and I_{oh} represent the maximal values for the pad type. They are provided for information only.

Table 3-3: DC Characteristics for Digital IOs, Voltage 1.8 V - BIDIR and IN Types

Parameter	Drive Strength	Min.	Nom.	Max.	Unit
V_{IL} Input Low Voltage		0		0.54	V
V_{IH} Input High Voltage		1.26		3.6	V
V_T Threshold Point		0.79	0.87	0.94	V
V_{T+} Schmitt Trigger Low to High Threshold Point		1	1.12	1.22	V
V_{T-} Schmitt Trigger High to Low Threshold Point		0.61	0.71	0.8	V
$V_{T\ PU}$ Threshold Point with Pull-up Resistor Enabled		0.79	0.86	0.93	V
$V_{T\ PD}$ Threshold Point with Pull-down Resistor Enabled		0.8	0.87	0.95	V
$V_{T+\ PU}$ Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled		1	1.12	1.21	V
$V_{T-\ PU}$ Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled		0.61	0.7	0.8	V
$V_{T+\ PD}$ Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled		1.01	1.13	1.23	V
$V_{T-\ PD}$ Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled		0.62	0.72	0.81	V
I_I Input Leakage Current @ VI=1.8V or 0V				±10	µA
I_{OZ} Tri-state Output Leakage Current @ VO=1.8V or 0V				±10	µA
Input Capacitance			3		pF
R_{PU} Pull-up Resistor		56	89	148	kOhm

Table 3-3: DC Characteristics for Digital IOs, Voltage 1.8 V - BIDIR and IN Types

Parameter	Drive Strength	Min.	Nom.	Max.	Unit
R_{PD} Pull-down Resistor		52	90	167	kOhm
V_{OL} Output Low Voltage				0.45	V
V_{OH} Output High Voltage		1.35			V
I_{OL} Low Level Output Current at V_{OL}(max)	2 mA	1.2	2.2	3.6	mA
	4 mA	2.3	4.3	7.1	mA
	8 mA	4.6	8.6	14.3	mA
I_{OH} High Level Output Current at V_{OH}(max)	2 mA	1.0	2.4	4.6	mA
	4 mA	2.0	4.7	9.2	mA
	8 mA	4.0	9.4	18.4	mA

Table 3-4: DC Characteristics - IN_PMU Type

Parameter	Drive Strength	Min.	Nom.	Max.	Unit
V_{IL} Input Low Voltage		-0.3		0.4	V
V_{IH} Input High Voltage		1.1		3.6	V

Table 3-5: DC Characteristics - BIDIR_WAKE Type

Parameter	Min.	Nom.	Max.	Unit
V_{IL} Input Low Voltage	0		0.2	V
V_{IH} Input High Voltage. See note below related to maximum value.	0.8		3.6	V
V_{OL} Output Low Voltage			0	V

Table 3-5: DC Characteristics - BIDIR_WAKE Type (Continued)

Parameter	Min.	Nom.	Max.	Unit
V_{OH} Output High Voltage	1.6		1.8	V

3.6 Auxiliary ADC

ADC specification is described in Table 3-6.

Table 3-6: ADC Specification

Performance Specification	Description	Value			Unit
		Min.	Typical	Max.	
ADC voltage range		0.1		1.8	V
ADC tolerance	After calibration. The tolerance considered is the highest value between the percentage and the absolute voltage mentioned.	Highest of -2% or -5 mV		Highest of +2% or +5 mV	% or mV
ADC resolution	Nominal resolution		10		bit
ADC input capacitance	ADC input capacitance. See the note below to prevent current leakage in low-power mode.			2	pF
ADC input resistance	ADC input resistance. See the note below to prevent current leakage in low-power mode.	1			MOhm

Important: If the ADC input is interfacing with an external device which doesn't drive 0V when the VZM20Q is in Sleeping Mode, then an external analog switch (such as FET) must be connected to ADC input pin to prevent any current leakage in PMU sleeping state.

3.7 Performance

Table 3-7 and Table 3-8 present the VZM20Q module's performance in LTE Band 4 and Band 13.

Table 3-7: Output Power

LTE Band	Frequency (kHz)	TCH	Conducted Power (dBm) Bandwidth 1.4 MHz, Full RB
Band 13	779500	23205	23 +1/-1.7
	782000	23230	23 +1/-1.7
	784500	23255	23 +1/-1.7
Band 4	1712500	19975	23 +1/-1.7
	1732500	20175	23 +1/-1.7
	1752500	20375	23 +1/-1.7

Table 3-8: RF Sensitivity

LTE Band	Frequency (kHz)	TCH	Typ. Sensitivity level (dBm) Bandwidth 1.4 MHz
Band 13	748500	5205	-104
	751000	5230	-104
	753500	5255	-104
Band 4	2112500	1975	-104
	2132500	2175	-104
	2152500	2375	-104

3.8 Component Reliability

Note: Information related to component reliability will be provided in a future edition of this document.

3.9 Package Description

3.9.1 Marking Information

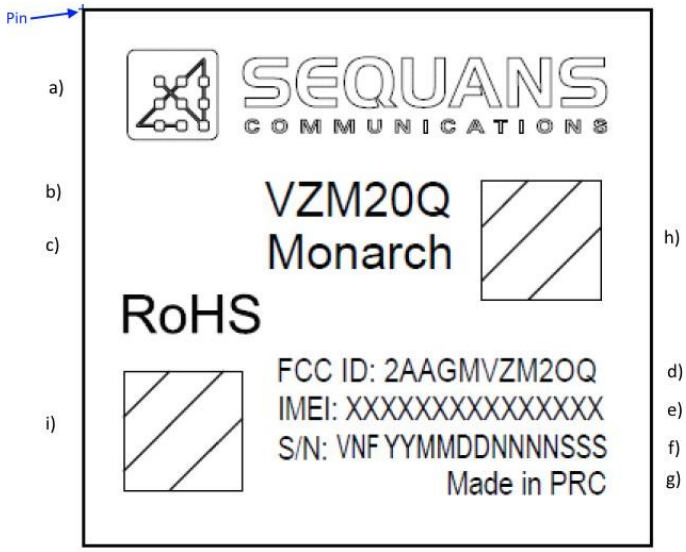

Figure 3-3: VZM20Q Marking Description

Table 3-9: Marking Details

Symbol	Description
a	Sequans' Logo
b	VZM20Q Product Name
c	Monarch / RoHS logo
d	FCC ID: 2AAGMVZM2OQ
e	IMEI: XXXXXXXXXXXXXXX (15 digits)

Table 3-9: Marking Details (Continued)

Symbol	Description
f	S/N: VZQYYMMDDNNNNSSS (16 digits) VZQ: is immovable (3digits) YYMMDD: Manufacturing Date(YY: Year, MM: Month, DD: Date) NNNN: Panel Counter(4 digits 0001~9999); SSS: Piece counter(001~020)
g	Made in PRC
h	IMEI Barcode
i	S/N Barcode

3.10 Packing Information

The module is delivered in Tape-and-Reel as described in Figure3-4.

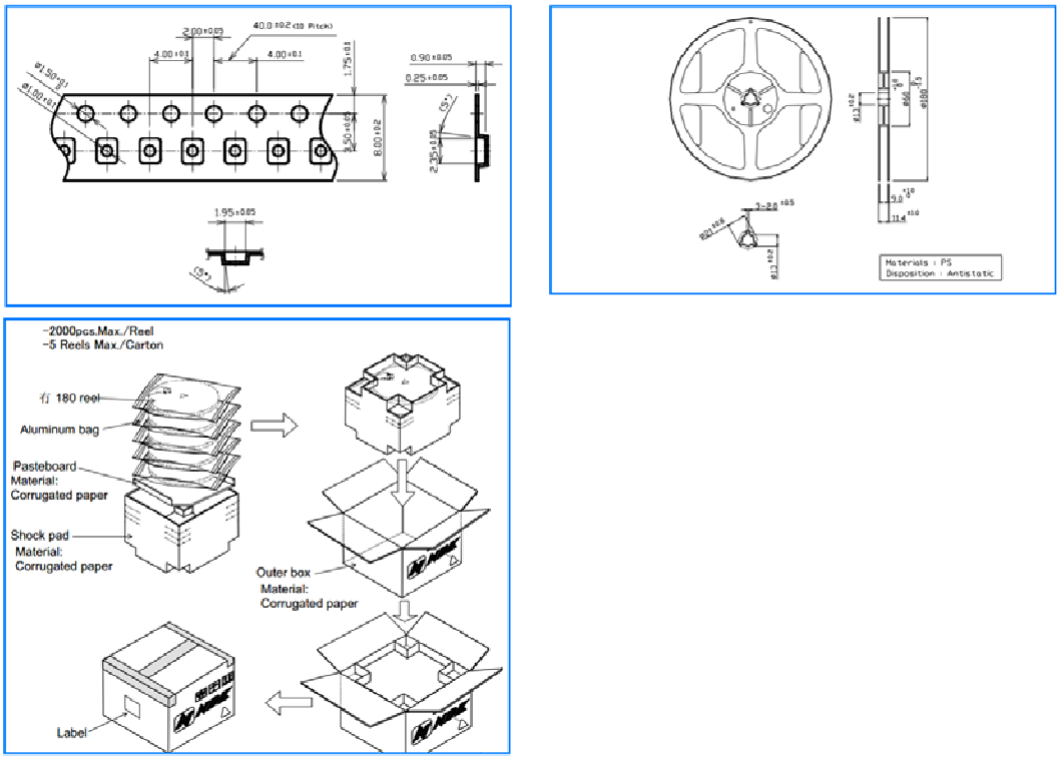

Figure 3-4: Packing Tape and Reel Description

3.11 Storage Conditions

Note: Additional storage conditions impacting the mounting process are provided in Section 3.12 Mounting Considerations on page 19.

1. Calculated shelf life in sealed bag : 12 months at < 40°C and < 90% RH
2. Peak package body temperature: 250°C
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be:
   a) mounted within 168 hours of factory conditions ≤ 30°C/60%RH, or
   b) Stored as per J-STD-033
4. Devices require bake, before mounting, if
   a) Humidity Indicator Card reads >10% for level 2a-5a devices or >60% for level 2 devices when read at 23±5°C
   b) 3a or 3b above are not met
5. If baking is required, refer to IPC/FEDEC J-STD-033 for bake procedure.

Note: Level and body temperature are defined by IPC/JEDEC J-STD-020.

3.12 Mounting Considerations

The VZM20Q can support up to 3 reflows with 250°C maximum.

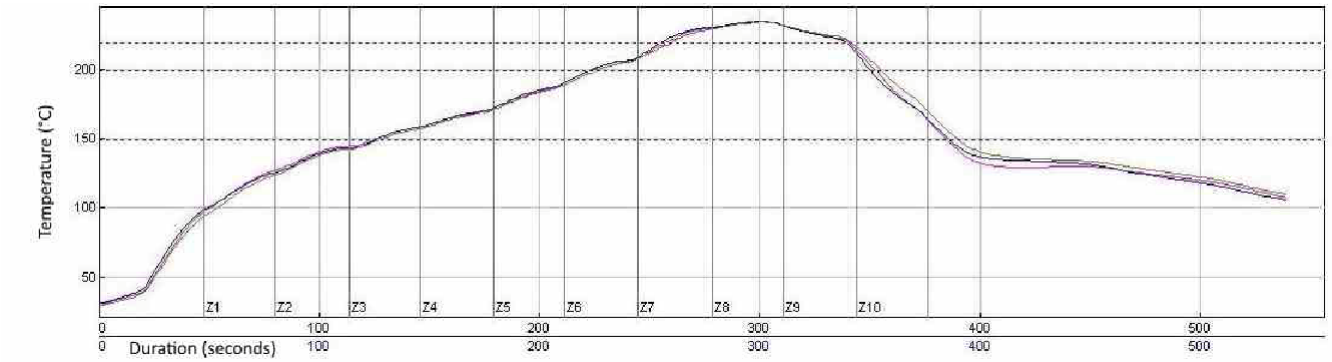

Figure 3-5: Reflow Profile

Table 3-10: Reflow Parameters

Parameter	Setting
Peak package body temperature	To be defined
Liquidous Time	To be defined
Preheat/Soak	To be defined
Ramp-up rate	To be defined
Ramp-down rate	To be defined

4 Signal and Pins

4.1 VZM20Q Pinout

The signals and all the related details are listed in the MS-Excel companion file delivered together with the present document in a PDF portfolio.

The pads listed in Table 4-1 are connected to ground.

Table 4-1: Ground and Thermal Pads

Pad #	Pad Name	Comment
1 20 22 24 26 28 30 31 32 33 34 42 43 45 46 53 55 62 63 64 65 66 68 69 70 71 72 73 74 86 87	GND	All GND pads shall be connected to the same copper.
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14 T15 T16 T17 T18 T19 T20 T21 T22 T23 T24 T25 T26 T27 T28 T29 T30	GND	T1 to T30 pads are used as both GND and thermal drops.

4.2 UART Interfaces

Figure 4-1 represents the typical implementation for the hardware flow control for UART0, UART1 and UART2. TXD and RXD signals are mandatory. RTS and CTS are strongly recommended. The other signals are optional.

VZM20Q is designed for use as DCE (Data Communication Equipment).

Based on the conventions for DCE-DTE connections, the DCE device will communicate with the customer application (DTE) using the following signals:

- Port TXD on Application sends data to the module's TXD signal line.
- Port RXD on Application receives data from the module's RXD signal line.

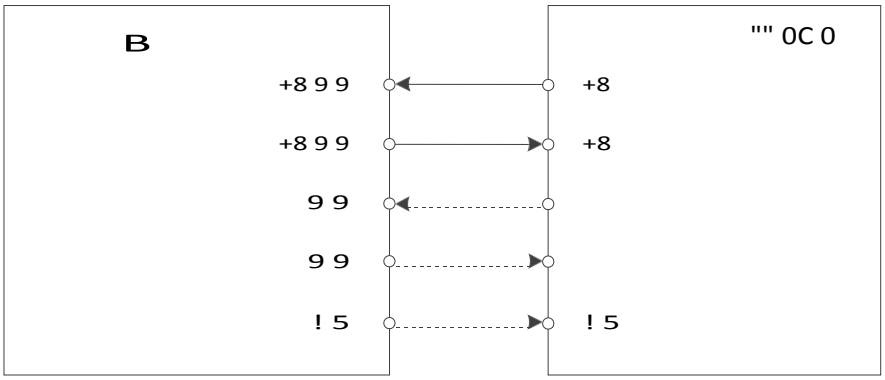

Figure 4-1: UART0, UART1 and UART2 Signals Convention and Flow Control

Note: CLK signals can be input or output.

The default configuration is:

- UART0

  4 wires (hardware flow control RTS0/CTS0), baud rate 921600 baud, 8 bit data, no parity, 1 stop bit, low power wake-up capability enabled with RTS0.

  UART0 is the main interface for the LTE modem, configured for AT commands.

Important: VZM20Q UART0 is configured with hardware flow control (RTS0, CTS0). During the boot cycle, it is mandatory that the Application Host connected to UART0 implements hardware flow control on its UART, because the VZM20Q will send SYSSTART URC. Not complying with this requirement can prevent the module to boot.

- UART1

  2 wires (no hardware flow control), baud rate 115200 baud, 8 bit data, no parity, 1 stop bit, low power wake-up capability is disabled on UART1. UART1 is console interface for debug.

Note: UART1 hardware is capable to support 4 wires, higher speed up to 921600 baud and low power wake-up capability with RTS1; this capability is enabled with a persistent AT command.

- UART2

  4 wires (hardware flow control RTS2/CTS2), baud rate 921600 baud, 8 bit data, no parity, 1 stop bit, no wake-up capability on UART2 RTS2.

  UART2 interface is configured for AT commands.

- VZM21Q UART0 is configured with hardware flow control (RTS0, CTS0). During the boot cycle, it is mandatory that the Application Host connected to UART0 implements hardware flow control on its UART, because the VZM21Q will send SYSSTART URC. Not complying with this requirement can prevent the module to boot.

4.3 Power-up Sequence

The following timing requirement applies to the signals VBAT1, POWER_EN and RESET_N. It must be respected for proper VZM20Q's behavior.

Note: The POWER_EN signal has no function for Monarch platform modules. It is mentioned here for compatibility reasons with Calliope platform modules.

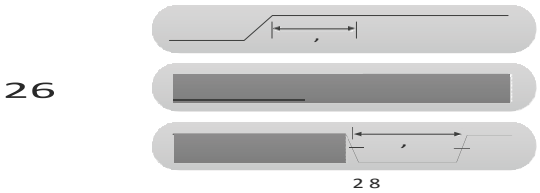

Figure 4-2: VBAT1, POWER_EN and RESET_N Signals Timing Requirement for Cold Start

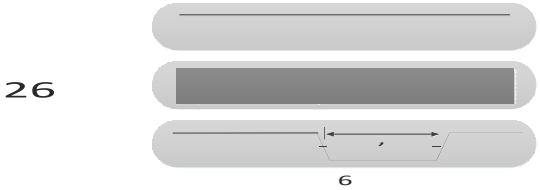

Figure 4-3: VBAT1, POWER_EN and RESET_N Signals Timing Requirement for Warm Start

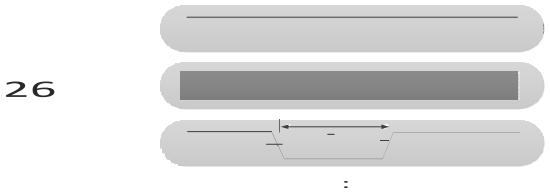

Figure 4-4: VBAT1, POWER_EN and RESET_N Signals Timing Requirement for Reset Cycle

The timing minimum values are listed in Table 4-2.

Note: For cold start: ts+ts1=10 s maximum.

Table 4-2: VBAT1 and RESET_N Signal Timing Values

Symbol	Description	Minimum Duration	Maximum Duration
th1	RESET_N hold time	1 µs	-
ts	VBAT1 setup time	1 ms	-
ts1	RESET_N setup time	1 ms	-

4.4 LTE Low Power Mode

4.4.1 General Information

Important: The VZM20Q module is provided with an internal RTC whose supply is VBAT1. As a consequence, VBAT1 should not be removed, in order to keep RTC active.

The VZM20Q will automatically enter in low-power mode. VZM20Q can be woken from low power mode by external sources through:

- SIM_DETECT input signal to cope with SIM card insertion or removal into a SIM card connector with built-in hardware detection.
- The RTS0 input signal whenever data traffic is initiated by the host connected to the module UART0 with hardware flow control; The default configuration to wake-up the module is low level.
- Two dedicated input signal WAKE0 and WAKE1; The default configuration to wake-up the module is on a high-to-low transition. This can be modified by software. As example, these signals can be used to detect an alarm from an external IC such as a sensor. Software can enable and disable the wake-up functionality on these signals.

Important: WAKE inputs are detected on level (configurable by software to 0 or 1) that must last at least 5 periods of the 32 kHz clock, that is 156.25 µs. Their polarity is configurable by software.

- A subset of GPIO input signals: GPIO2, GPIO3, GPIO25, GPIO27, GPIO42; they are not configured by default as wake-up source but software can configure them for future use.

To get the lowest possible power consumption during low-power mode, all IOs must be stable. At software configuration time, take care of the following, to prevent them from being in conflict or floating:

- Pads that are not driven by an external device shall be driven low by software if they have a GPIO or RFDATA mode that allows it.
- For pads that are known to be driven by an external device:

  Configure that external device to hold the signal stable during low-power mode, and configure VZM20Q to treat that pin as an input, without internal pull-up or pull-down.

- For pads where, at the time of low-power mode, the signal may or may not be driven by an external device:

  Configure VZM20Q to enable the internal pull-up/pull-down on the pad to guarantee that it will not be floating during low-power mode.

Note:	Each signal's pull (up or down) is determined by register. It can be modified by software. Please see the default configuration in the signal's list.

4.4.2 Detailed Behavior of IO Pads of BIDIR Type

- Behavior in PS-P or Active Mode

  Figure 4-5 shows a simplified diagram of the Digital bi-directional IOs in PS-P or active mode.

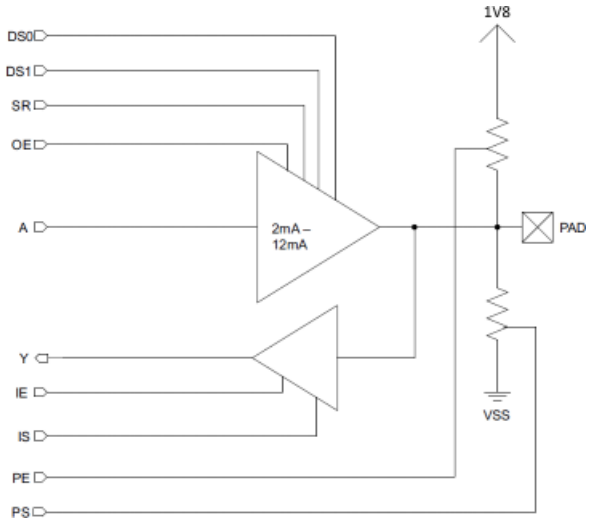

Figure 4-5: Digital Bi-Directional IOs in PS-P or Active Mode

- Behavior in PS-PM

  In PS-PM the Digital bi-directional IOs are completly powered Off.

  In PS-PM the Digital bi-directional IOs can be seen as high-impedance from the outside.

  Table 4-3 shows the Digital bi-directional IOs expected impedance value as seen from the ouside in PS-PM.

Table 4-3: Digital Bi-Directional IOs Expected Impedance Value (Seen from the Outside) in PS-PM

Typica
50 MOhm

4.4.3 Detailed Behavior of IO Pads of BIDIR_WAKE Type

- Behavior in PS-P or Active Mode

  PMU bi-directional wake IOs are used as general purposed IO buffers in PS-P or active mode. Figure 4-6 shows a simplified diagram of the PMU bi-directional wake IOs in PS-P or active mode.

Note:	The PMU bi-directional wake IOs output buffer requires the 3.0V power supply to be ON.

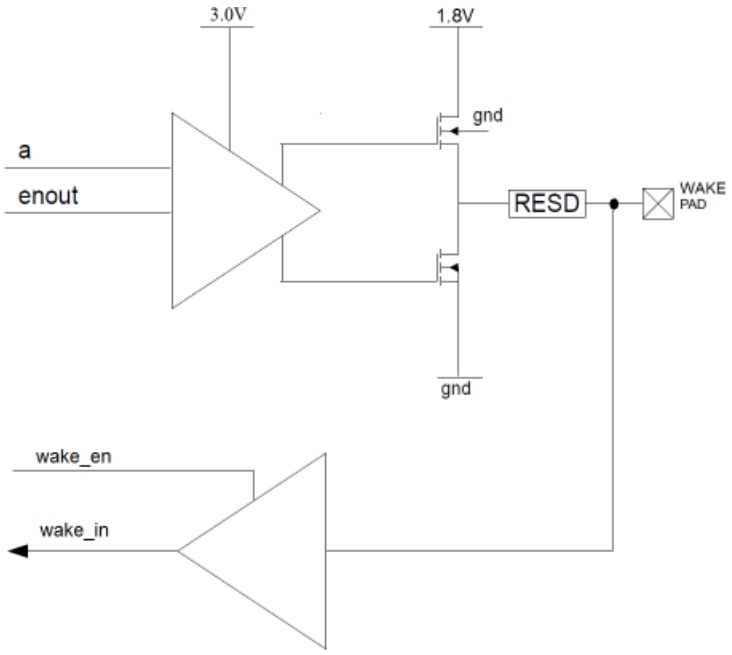

Figure 4-6: PMU Wake IOs in PS-P or Active Mode

- Behavior in PS-PM.

Note:	The PMU bi-directional wake IOs output buffer is disabled in PS-PM.

Figure 4-7 shows a simplified diagram of the PMU bi-directional wake IOs in PS-PM.

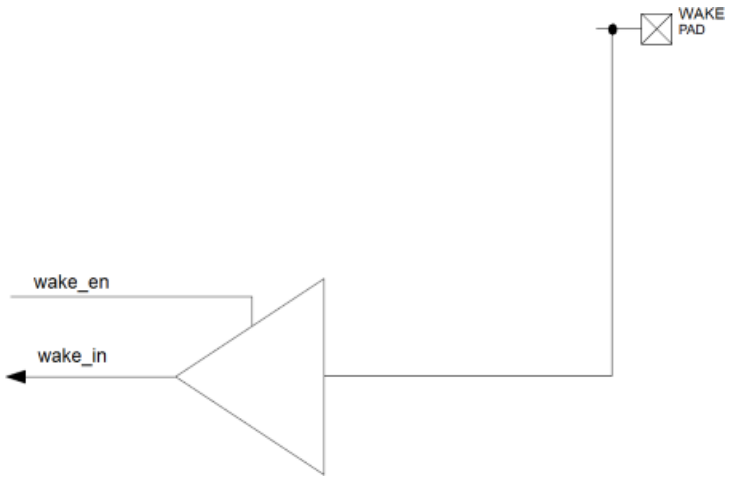

Figure 4-7: PMU Wake IOs in PS-PM Mode

In PS-PM, all PMU bi-directional wake IOs are high impedance with ultra low leakage current. This corresponds to a minimum impedance of 180 MOhm at the maximum input supply voltage of 3.6 V.

If an event is presented on the wake IO pad and this wake IO has been configured to be sensitive on that event, this will take the system back to Active mode.

Table 4-4 shows the values of the measured leakage current (measurements taken on silicon) for the PMU bi-directional wake IOs.

Table 4-4: Measured leakage current for the PMU bi-directional wake IOs.

Minimum	Typical	Maximum
3 nA	4 nA	12 nA

Table 4-5 shows values of the external pull-up/pull-down resistor to be used on the PMU bi-directional wake IOs pads.

Table 4-5: External pull-up/pull-down resistor to be used on the PMU bi-directional wake IOs Pads.

Minimum	Typical	Maximum
1 kOhm	10 kOhm	100 kOhm

Table 4-6 shows details about the PMU bi-directional wake IOs pulses detection mechanism timings.

Table 4-6: Details about the PMU bi-directional wake IOs pulses detection mechanism timings

Maximum pulse width that is guaranteed to be ignored	Minimum pulse width that is guaranteed to be seen
11.1 ns	100 µs

A Acronyms

Acronym	Definition
AFE	Analog Front-End
APC	Automatic Control Power
CE	Coverage Extension
COO	Country of origin
CPU	Central Processing Unit
DC/DC	Direct current converter
DDR	Double Data Rate (SDRAM)
DL	Downlink
DPLL	Digital Phase-Locked Loop
ECCN	Export Control Classification Number
EPS	Evolved Packet System
ESD	Electro-static discharge
ETSI	European Telecommunications Standard Institute
FCC	Federal Communications Commission (USA)
GND	Ground
GPIO	General Purpose Input Output
HBM	Human Body Model (ESD)
I/O	Input/Output
I2C	Inter-integrated circuit (bus)

Acronym	Definition
IETF	Internet Engineering Task Force. See https://www.ietf.org/
IMEI	International Mobile Equipment Identity
IMS	Instant Messaging Service
IP	Internet Protocol
JTAG	Joint Test Action Group. See IEEE 1149.7 specification
LDO	Low Drop-Out regulator
LGA	Large Grid Array
LNA	Low-Noise Amplifier
LTE	Long Term Evolution, or 4G. Standard is developed by the 3GPP www.3gpp.org.
MM	Machine Model (ESD)
NAS	Network Access Server
NVM	Non Volatile Memory
OEM	Original Equipment Manufacturer
OMADM	Open Mobile Alliance Device Management
PCB	Printed Circuit Board
PHY	Physical Layer
PLL	Phase-Locked Loop
PMIC	Power Management Integrated Circuit
pSRAM	Pseudo-Static Random Access Memory
QTY	Quantity
RAM	Random Access Memory
RAN	Radio Access Network
RB	Resource Block
RF	Radio Frequency
RFIC	RF Integrated Circuit

Acronym	Definition
RoHS	Restriction of Hazardous Substances
RTC	Real-Time Clock
Rx	Reception
S/N	or SN: Serial Number
SAW	Surface Acoustic Wave (filters)
SDM	Socketed Device Model (ESD)
SDRAM	Synchronous Dynamic Random Access Memory
SIM	Subscriber Identification Module
SMS	Short Message Service
SPI	Serial Peripheral Interface
TCXO	Temperature-controlled crystal oscillator
Tx	Transmission
UART	Universal asynchronous receiver transmitter.
UE	User Equipment
UICC	Universal integrated circuit card (SIM)
UL	Uplink
XTAL	Crystal