Cassiopeia Platform - Module CB410L

Datasheet

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Preface

Legal Notices

Document Revision History

Revision	Date	Product Application
01	February 2019	First edition.
02	July 2019	Second edition.
03	August 2019	Third edition.
04	December 2019	Fourth edition.
05	January 2020	Fifth edition.
06	February 2020	Sixth edition.
07	March 2020	Seventh edition. See details in Changes in this Document on page iii.

About this Datasheet

Purpose and Scope

The CB410L is a complete LTE module including base-band, RF and memory, for CAT-4 devices for CBRS market. It meets also almost all requirements for M2M application such as automotive, metering, tracking system, security solutions, routers, wireless POS, mobile computing devices, among others. This document provides technical information about CB410L LCC module. CB410L is based on Sequans' Cassiopeia platform.

Who Should Read this Datasheet

This document is intended for engineers who are developing User Equipment (UE) for LTE systems.

Changes in this Document

The following changes are done since the previous edition:

- Updated Section 1.2 FCC Interference Statement on page 6.
- Updated Section 2.1 ECCN and Part Number on page 9.

References

[1] Core technology specifications:

- 3GPP E-UTRA 21 series Release 9 (EPS)
- 3GPP E-UTRA 22 series Release 9 (IMEI)
- 3GPP E-UTRA 23 series Release 9 (NAS, SMS)
- 3GPP E-UTRA 24 series Release 9 (NAS)
- 3GPP E-UTRA 31 series Release 9 (UICC)
- 3GPP E-UTRA 33 series Release 9 (security)
- 3GPP E-UTRA 36 series Release 9 (RAN)
- 3GPP2 C.S0015-A v1.0 (SMS)
- IETF, RFC 3261, 4861, 4862, 6434

For more information, see

- ftp://ftp.3gpp.org/Specs/latest/Rel-9/21_series/
- ftp://ftp.3gpp.org/Specs/latest/Rel-9/22_series/
- ftp://ftp.3gpp.org/Specs/latest/Rel-9/23_series/
- ftp://ftp.3gpp.org/Specs/latest/Rel-9/24_series/
- ftp://ftp.3gpp.org/Specs/latest/Rel-9/31_series/
- ftp://ftp.3gpp.org/Specs/latest/Rel-9/33_series/
- ftp://ftp.3gpp.org/Specs/latest/Rel-9/36_series/
- http://www.3gpp2.org/public_html/specs/CS0015-0.pdf
- https://tools.ietf.org/html/

[2] Test specifications:
3GPP E-UTRA 36 series Release 9 (RAN)
ftp://ftp.3gpp.org/Specs/latest/Rel-9/36_series/

[3] Vocabulary reference:

- 3GPP TR 21.905: "Vocabulary for 3GPP Specifications"

For more information, see http://www.3gpp.org/ftp/specs/archive/21_series/21.905/

[4]

- "Universal Serial Bus Specification", Revision 2.0, April 27, 2000 (http://www.usb.org/developers/docs/). ECM (Ethernet Networking Control Model) is specified in “USB Class Definitions for Communication Devices”, Version 1.1, January 19,1999, section 3.8.2. EEM (CDC Ethernet Emulation Model) is specified in “Universal Serial Bus Communications Class Subclass Specification for Ethernet Emulation Model Devices”, Revision 1.0, February 2, 2005.
- SQN3220SC Application CPU runs OpenWrt, a Linux distribution for embedded devices. See https://openwrt.org/.

Documentation Conventions

This section illustrates the conventions that are used in this document.

General Conventions	
Note	Important information requiring the user's attention.
Caution 	A condition or circumstance that may cause damage to the equipment or loss of data.
Warning 	A condition or circumstance that may cause personal injury.
Italics	Italic font style denotes • emphasis of an important word; • first use of a new term; • title of a document.
Screen Name	Sans serif, bold font denotes • on-screen name of a window, dialog box or field; • keys on a keyboard; • labels printed on the equipment.

Software Conventions	
`Code`	Regular Courier font denotes code or text displayed on-screen.
Code	Bold Courier font denotes commands and parameters that you enter exactly as shown. Multiple parameters are grouped in brackets [ ]. If you are to choose only one among grouped parameters, the choices are separated with a pipe: [parm1 | parm2 | parm3] If there is no pipe separator, you must enter each parameter: [parm1 parm2 parm3]
`Code`	Italic Courier font denotes parameters that require you to enter a value or variable. Multiple parameters are grouped in brackets [ ]. If you are to choose only one among grouped parameters, the choices are separated with a pipe: [parm1 | parm2 | parm3] If there is no pipe separator, you must enter a value for each parameter: [parm1 parm2 parm3]

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1 Product Overview

1.1 Product Features

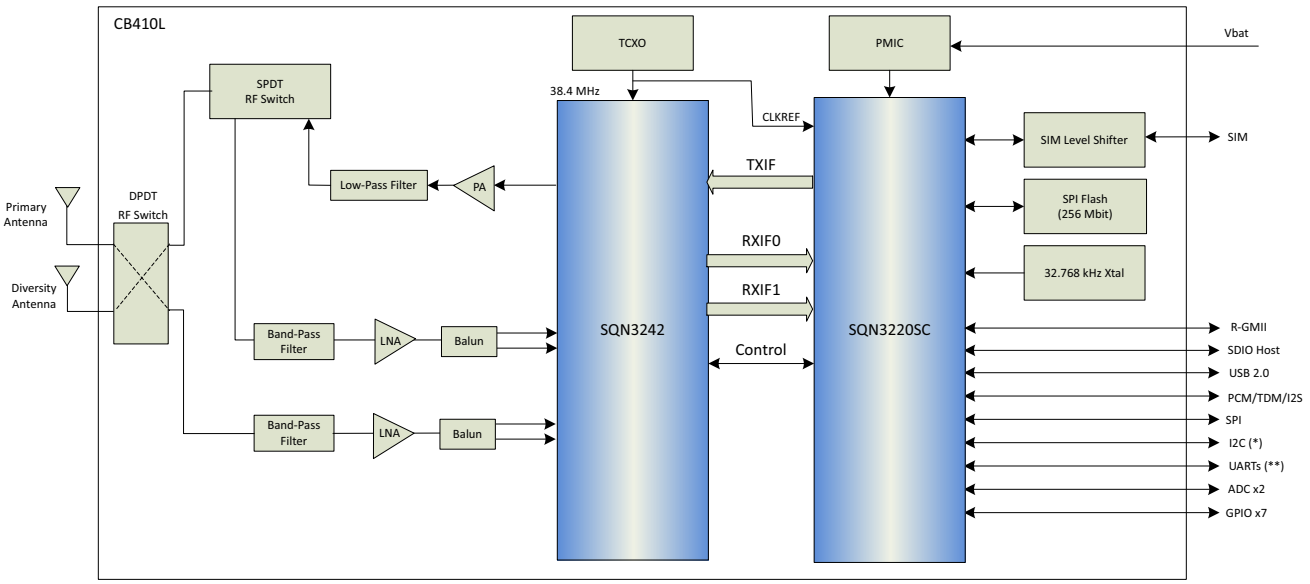
1.1.1 Features Description

Sequans CB410L module includes a baseband, a complete dual band RF front end, memory and required circuitry to meet 3GPP E-UTRA (Long Term Evolution - LTE, Release 9 set of specifications) and LTE UE specifications.

It is compliant with CBRS networks operating on LTE band 48 (3550 MHz - 3700 MHz) in the USA. It can also operate on other networks operating on LTE band 42 (3400 MHz - 3600 MHz) and on LTE band 43 (3600 MHz - 3800 MHz).

For more information on the core technology specifications see the section References. The term CB410L module refers to the hardware and the associated embedded software.

The architecture block diagram of the CB410L is presented on Figure 1-1.



(*) I2C interface over 2 GPIOs
(**) 2x HS-UART with hardware flow control and 2x UART without hardware flow control

Figure 1-1: CB410L Block Diagram

Note: Refer to Table 2-1 on page 9 and Table 3-1 on page 23 for details on interfaces availability for each part number.

Table 1-1 on page 2 provides detail on general features of the CB410L.

Table 1-2 on page 3 provides detail for the LTE-related features of the CB410L.

CB410L's ECCN and part number are detailed in the Section ECCN and Part Number.

Table 1-1: General Features

General interfaces	• JTAG • USIM • SPI • GPIO • USB 2.0 Device • UART (2 HS-UART with hardware flow control and 2 UART without hardware flow control) • SDIO Host • PCM/I2S • I2C (over GPIO) • ADCs Note that interfaces HS-UART3, RGMII, SDIO are multiplexed with GPIO signals. So more GPIOs are available if some of the other interfaces are not used.
Supported Frequency Bands	• LTE Bands 42 and 43, and CBRS Band 48

Table 1-1: General Features (Continued)

Operation voltages	• V_{bat} (range from 3.135 V to 5.5 V)
Packaging	• LCC module • 32 x 29 x 2.4 mm. 80 pads carrying useful signals on 134 pads in total. • RoHS compliant, halogen-free
Operating temperature	• -30°C to +60°C ambient See also Section Environmental Operating Conditions
Humidity	• 10% to 85% See also Section Environmental Operating Conditions

Table 1-2: LTE Features

Standard compliance	• 3GPP E-UTRA Release 9 compliant
PHY	• One UL and two DL transceivers • Category 4 UE • TDD • Normal and extended cyclic prefix • Modulation - DL: QPSK, 16QAM, 64QAM - UL: QPSK, 16QAM • All coding schemes corresponding to modulations • All channel coding (turbo-coding with interleaver, tail biting convolutional coding, block and repetition coding) and CRC lengths • Channels 5, 10, 15, and 20 MHz • Sounding (including in special subframes) • Control and data in special subframes • Antenna diversity on DL: MRC (Maximum Ratio Combining) • Tx diversity • All power control schemes and DL power allocation schemes • HARQ Incremental Redundancy and Chase Combining, with bundling or multi-plexing • Measurements and computations related to CQI (Channel Quality Indicator), PMI (Pre-coding Matrix Indicator) and RI (Rank Indicator), RSRP, and RSRQ

Table 1-2: LTE Features (Continued)

MAC	• Random Access procedure in normal and special subframes • Scheduling Request, Buffer Status Reporting, and Power Headroom Reporting • Discontinuous reception (DRX) with long and short cycles • Fast scanning • Hosted configuration • Semi-persistent scheduling • IPv4, IPv6 • RoHC • Location based services • Advanced QoS features
RLC	• ARQ modes: UM, AM, and TM
PDCP	• Ciphering and deciphering: NULL, AES, SNOW 3G • Integrity and protection: AES, SNOW 3G
RRC	• MIB and all SIBs • Intra and inter-frequency measurements and handover • Up to 8 Data Radio Bearers supported

1.1.2 TDM-PCM Interface Specification

The features of the CB410L's TDM-PCM controller include:

- Support of PCM slave mode with PCM_CLK input and PCM_FS input.
- Support of PCM master mode with with PCM_CLK input and PCM_FS output generated internally
- PCM_CLK input frequency from 128 kHz to 8192 kHz
- Variable number of time-slots within a frame depending on PCM_CLK frequency
- Support of PCM data format of 8-bits or 16-bits
- In master mode, SQN3220 can generate other Frame Sync periods than the standard Frame Sync period (125 µs).
- Support of short and long Frame Sync formats (active for 1 or 3 PCM_CLK periods)
- Separated programmable time-slot-offset value for Tx and Rx, for each voice channel.

Sequans PCM interface takes PCM_CLK as an input in both master and slave modes. It supports a set of different frequencies, in the range 128 kHz to 8192 kHz.

Caution: This clock signal is an input in both master and slave modes.

The signals implementing the PCM interface are detailed in I2S/PCM Interface Signals.

1.2 FCC Interference Statement

FCC ID for CB410L module is `2AAGMCB410L`.

This following statement applies to all products based on CB410L supporting Band 48 that would be deployed in CBRS network in USA.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution:

- Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.
- This transmitter is certified under the standalone operation condition and may not be installed to co-transmission with other transmitter without separate reassessment. It is OEM/Host manufacturers' s responsibility to conduct a separate compliance reevaluation for confirming that final system continuously complies with the applicable FCC rules under that circumstance.

Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This module is intended for OEM integrators only. Per FCC KDB 996369 D03 OEM Manual v01 guidance, the following conditions must be strictly followed when using this certified module:

KDB 996369 D03 OEM Manual v01 rule sections:

2.2 List of applicable FCC rules

This module has been tested for compliance to FCC Part 96 CBRS as an End User Device.

2.3 Summarize the specific operational use conditions

The module is tested for standalone mobile RF exposure use condition. Any other usage conditions such as co-location with other transmitter(s) or being used in a portable condition will need a separate reassessment through a class II permissive change application or new certification.

2.4 Limited module procedures

Not applicable.

2.5 PCB Trace design info

Please refer to Appendix PCB Layout Rules on page 34.

2.6 RF exposure considerations

This equipment complies with FCC mobile radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator & your body. If the module is installed in a portable host, a separate SAR evaluation is required to confirm compliance with relevant FCC portable RF exposure rules.

2.7 Antennas

Following antenna has been approved with this module, other antenna type or same type with higher gain will need separate approval.

- Antenna type: Dipole
- LTE band 48 : Max. 0.64 dBi, assuming 0.5 dB attenuation loss between LCC module pad and antenna SMA connector.

The dipole antenna must be installed such that 20cm can be maintained between the antenna and users to comply with the FCC maximum EIRP limits and RF Exposure rules.

2.8 Label and compliance information

The final end product must be labeled in a visible area with the following: "Contains FCC ID: 2AAGMCB410L". The grantee's FCC ID can be used only when all FCC compliance requirements are met.

2.9 Information on test modes and additional testing requirements

This transmitter is tested in a standalone mobile RF exposure condition and any co-located or simultaneous transmission with other transmitter(s) or portable use will require a separate class II permissive change re-evaluation or new certification.

2.10 Additional testing, Part 15 Subpart B disclaimer

This transmitter module is tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B (unintentional radiator) rule requirement applicable to the final host. The final host will still need to be reassessed for compliance to this portion of rule requirements if applicable.

As long as all conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

IMPORTANT NOTE:

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

OEM/Host manufacturer responsibilities

OEM/Host manufacturers are ultimately responsible for the compliance of the Host and Module. The final product must be reassessed against all the essential requirements of the FCC rule such as FCC Part 15 Subpart B before it can be placed on the US market. This includes reassessing the transmitter module for compliance with the Radio and EMF essential requirements of the FCC rules. This module must not be incorporated into any other device or system without retesting for compliance as multi-radio and combined equipment

2 Physical Characteristics

2.1 ECCN and Part Number

The ECCN of the CB410L is 5A992.c. CCATS number is G180697.

The following comment from licensing officer is reported on the license information:

- This encryption item is described in paragraph b to Note 3 (Mass Market Note) of Category 5 Part 2. It is authorized for export and reexport under section 740.17(b)(3) of the Export Administration Regulations.

Table 2-1: Orderable Part Numbers

Orderable Part Number	Hardware Version	Software Build	UE Version	PTCRB Model Name/Model	SVN	Orderable Status
CB41Q85QRB	Mass production FCC certified Reliability completed	N/A	N/A	N/A	N/A	Not yet orderable.
CB41Q85QRA	Mass production FCC certified Reliability started	LR4.2.2.0-48105	UE4.2.2.0-48105	N/A	N/A	Product is orderable.
CB41Q85QRZ	Engineering samples Reliability started	LR4.2.2.0-46614	UE4.2.2.0-46614	N/A	N/A	Product is orderable.

Note: IOs available with the part numbers are listed in table Table 3-1, in column “Rev Z, Rev A”.

2.2 Electrical Operating Conditions

2.2.1 Detailed Information

Table 2-2presents the electrical operating conditions for the CB410L module.

Table 2-2: Electrical Operating Conditions

	Direction	Minimum	Typical	Maximum
VBAT (recommended for performance)	In	3.3 V		4.42 V
VBAT (functional)	In	3.135 V		5.5 V
SIM_VCC (1.8 V or 3.0 V)	Out	1.62 V	1.8 V	1.98 V
		2.7 V	3.0 V	3.3 V
1V8 See note below.	Out	1.71 V	1.8 V	1.89 V

Note: The maximum current consumption allowed from the 1V8 reference pin is 50 mA.

2.3 Environmental Operating Conditions

2.3.1 Temperature

Note: The temperatures listed here are ambient.

- Operating: -30°C to +60°C
- Storage: -40°C to +85°C

2.3.2 Humidity

- Operating: 10% to 85% (non condensing)
- Storage: 5% to 85% (non condensing)

2.4 Power Supply Dimensioning

Table 2-3 presents peak power consumptions (in worst case conditions) in order to help designers with the power supply dimensioning of the system.

Table 2-3: CB410L Estimated Peak Power Consumption

Voltage (V)	Current (mA)	Power (W)
1.1 V	1000 mA	1.1 W
1.2 V	15 mA	0.018 W
1.8 V	775 mA	1.395 W
3.2 V	100 mA	0.320 W
3.3 V	500 mA	1.65 W
Total:		4.48 W

2.5 I/O Characteristics

The voltage and current characteristics of the various IO pads of the CB410L versus IO bank supply voltage are illustrated in the tables below.

Caution: Note that the V_{oh} values in the tables below do not apply to GPIOs configured in open drain mode. GPIOs can be individually configured in open drain mode. When in open drain mode they either drive the line to V_{ol}, or leave it floating, to be pulled up by an external pull-up resistance. The PCB designer must ensure that the voltage on these pads never exceeds V_{ih} of the IO group to which they belong.

Table 2-4 details the various pad types as listed in CB410L signals list.

Table 2-4: Pad Types Detail

Pad Type	Description	Maximum Input High Voltage
analog	analog (or power for powers and ground for grounds)	Not Applicable
BIDIR_DDR	1.8 V in/out. Refer to Table 2-6 for DC IO characteristics.	V_{IH} max = 1.9 V
BIDIR_PD	1.8 V in/out with software controlled internal pull-down. Refer to Table 2-5 for DC IO characteristics.	V_{IH} max = 3.6 V
BIDIR_PD_SLEW_SCHMITT	1.8 V slew-rate controlled in/out with Schmitt trigger and software controlled internal pull-down.Refer to Table 2-5 for DC IO characteristics.	V_{IH} max = 3.6 V
BIDIR_PU	1.8 V in/out with software controlled internal pull-up.Refer to Table 2-5 for DC IO characteristics.	V_{IH} max = 3.6 V
IN	1.8V input.	V_{IH} max = 3.6 V
IN_PD	1.8 V input with software controlled internal pull-down.Refer to Table 2-5 for DC IO characteristics.	V_{IH} max = 3.6 V
IN_PU	1.8V input with software controlled internal pull-up.	V_{IH} max = 3.6 V
OUT	1.8 V output.Refer to Table 2-5 for DC IO characteristics.	V_{IH} max = 3.6 V

Refer to CB410L Pin List to know the type of IO pad used on every termination.

- The Minimum values for I_{ol} and I_{oh} should not be exceeded to guarantee that the logical level are not spoiled for each pad type.
- The Nominal values for I_{ol} and I_{oh} represent the nominal values for the pad type. They are provided for information only.

- The Maximum values for I_{ol} and I_{oh} represent the maximal values for the pad type. They are provided for information only.

Table 2-5: DC Characteristics for Digital IOs, Voltage 1.8 V

Parameter	Drive Strength	Min.	Nom.	Max.	Unit
V_{IL} Input Low Voltage		-0.3		0.63	V
V_{IH} Input High Voltage		1.17		3.6	V
V_T Threshold Point		0.79	0.87	0.94	V
V_{T+} Schmitt Trigger Low to High Threshold Point		1	1.12	1.22	V
V_{T-} Schmitt Trigger High to Low Threshold Point		0.61	0.71	0.8	V
$V_{T\ PU}$ Threshold Point with Pull-up Resistor Enabled		0.79	0.86	0.93	V
$V_{T\ PD}$ Threshold Point with Pull-down Resistor Enabled		0.8	0.87	0.95	V
$V_{T+\ PU}$ Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled		1	1.12	1.21	V
$V_{T-\ PU}$ Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled		0.61	0.7	0.8	V
$V_{T+\ PD}$ Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled		1.01	1.13	1.23	V
$V_{T-\ PD}$ Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled		0.62	0.72	0.81	V
I_I Input Leakage Current @ VI=1.8V or 0V				±10	µA
I_{OZ} Tri-state Output Leakage Current @ VO=1.8V or 0V				±10	µA
Input Capacitance			3		pF
R_{PU} Pull-up Resistor		56	89	148	kOhm

Table 2-5: DC Characteristics for Digital IOs, Voltage 1.8 V (Continued)

Parameter	Drive Strength	Min.	Nom.	Max.	Unit
R_{PD} Pull-down Resistor		52	90	167	kOhm
V_{OL} Output Low Voltage				0.45	V
V_{OH} Output High Voltage		1.35			V
I_{OL} Low Level Output Current at V_{OL}(max)	2 mA	1.2	2.2	3.6	mA
	4 mA	2.3	4.3	7.1	mA
	8 mA	4.6	8.6	14.3	mA
I_{OH} High Level Output Current at V_{OH}(max)	2 mA	1.0	2.4	4.6	mA
	4 mA	2.0	4.7	9.2	mA
	8 mA	4.0	9.4	18.4	mA

Table 2-6: DC Characteristics for Digital IOs, Voltage 1.8 V - DDR IO Pins (BIDIR_DDR Type)

Parameter	Drive Strength	Min.	Nom.	Max.	Unit
VDDQ MOBILE DDR 1.8V I/O power		1.7	1.8	1.9	V
Input Capacitance			2.689		pF
V_{IL} Input Low Voltage		-0.3		0.3 * VDDQ	V
V_{IH} Input High Voltage		0.7 * VDDQ		VDDQ + 0.3	V
$V_{ILD(AC)}$ AC Input Low Voltage		-0.3		0.2 * VDDQ	V
$V_{IHD(AC)}$ AC Input High Voltage		0.8 * VDDQ		VDDQ + 0.3	V
V_{OL} Output Low Voltage (I_{OH}=-0.1mA)				0.1 * VDDQ	V

Table 2-6: DC Characteristics for Digital IOs, Voltage 1.8 V - DDR IO Pins (BIDIR_DDR Type) (Continued)

Parameter	Drive Strength	Min.	Nom.	Max.	Unit
V_{OH} Output High Voltage (I_{OH}=-0.1mA)		0.9 * VDDQ			V
I_{OL} Low Level Output Current at V_{OL}(max)	2 mA		2.00		mA
	4 mA		4.00		mA
	8 mA		8.00		mA
	10 mA		10.00		mA
I_{OH} High Level Output Current at V_{OH}(max)	2 mA		2.00		mA
	4 mA		4.00		mA
	8 mA		8.00		mA
	10 mA		10.00		mA

Table 2-7: DC Characteristics for MODULE_PWR_EN, Voltage VDD_PWR_EN

Parameter	Drive Strength	Min.	Nom.	Max.	Unit
V_{IL} Input Low Voltage		-0.3		0.4	V
V_{IH} Input High Voltage		1.1		VBAT1 + 0.3	V

2.6 Package Description

2.6.1 Module Weight

The module weight is 5.1 g.

2.6.2 Module Footprint

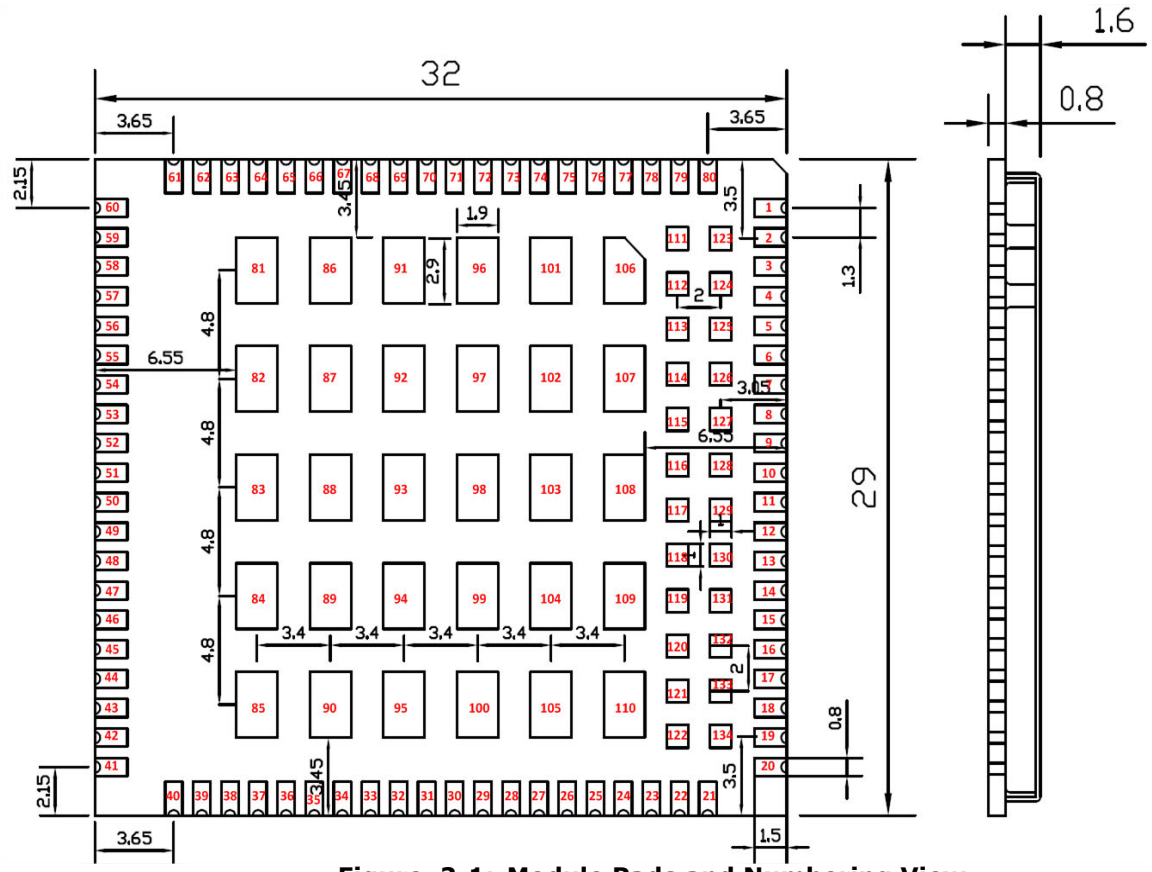


Figure 2-1: Module Pads and Numbering View

Dimensions on Figure 2-1 are indicated in mm.

Attention:	Pads 81 to 110 are used as both GND and thermal drops.

2.6.3 Marking Information

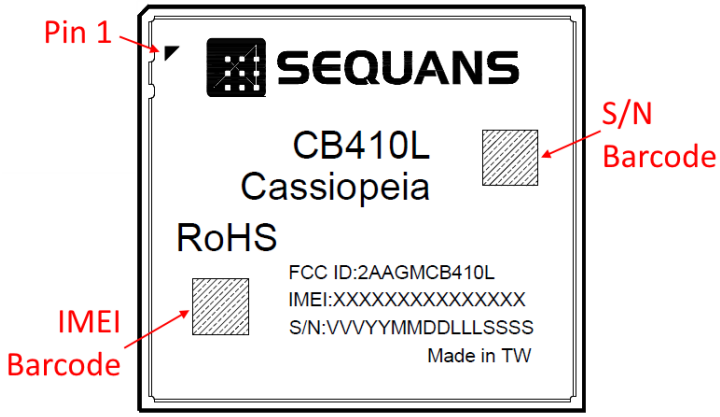


Figure 2-2: CB410L Marking Description

The elements marked on the package are:

- Sequans' Logo
- CB410L Product Name
- Cassiopeia Platform Name
- RoHS Logo
- FCC ID 2AAGMCB410L
- IMEI as digits and barcode
- Serial number as digits (`VVVYYMMDDLLLSSSS`) and barcode
  - `VVV`: Product hardware and software identification code
  - `YYMMDD`: Manufacturing date
  - `LLL`: tracking batch number
  - `SSSS`: four-digits serial number (HEX format 0000 to FFFF)
- Manufacturing country

2.7 Packing Information

The CB410L is delivered in Tape-and-Reel. One reel can hold up to 500 pieces. Each reel is included in a box, and a carton can contain five boxes, hence up to 2500 pieces. This is represented on Figure 2-3.

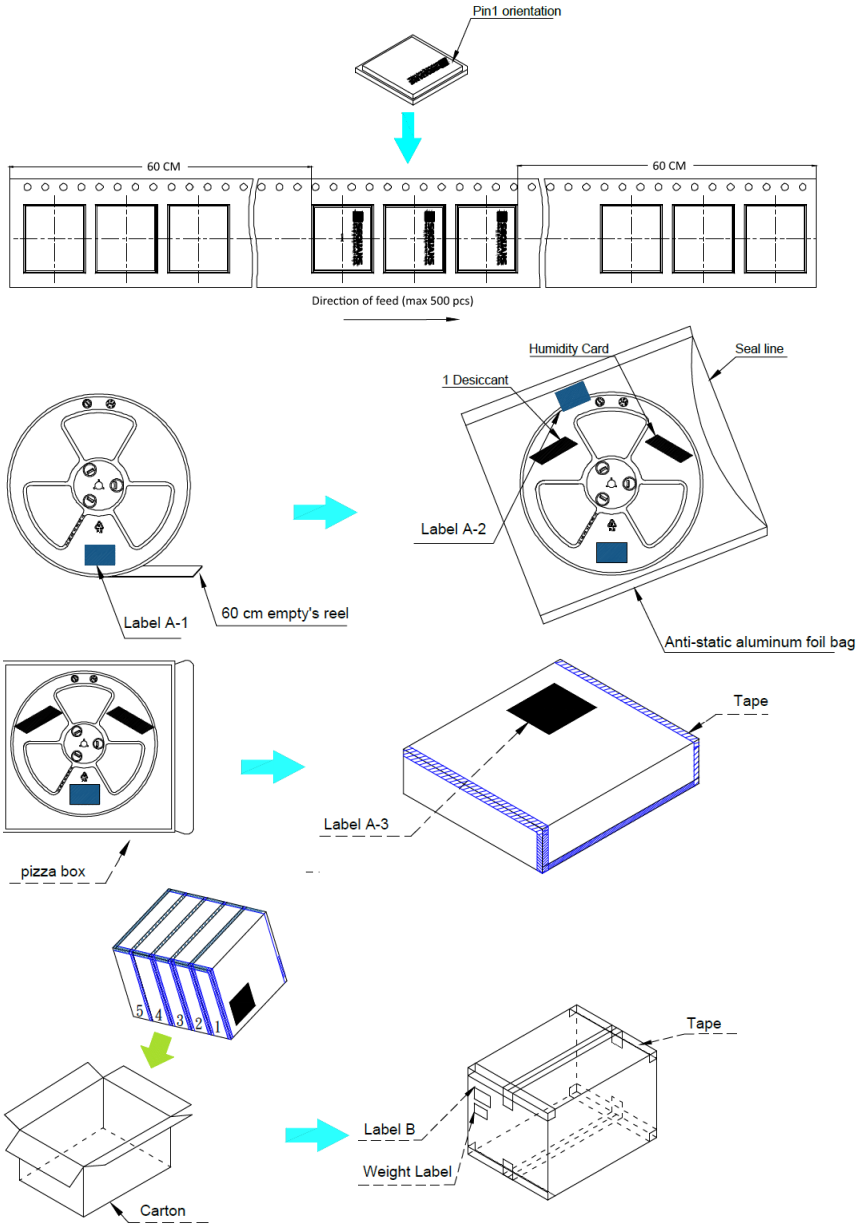


Figure 2-3: Packing Description

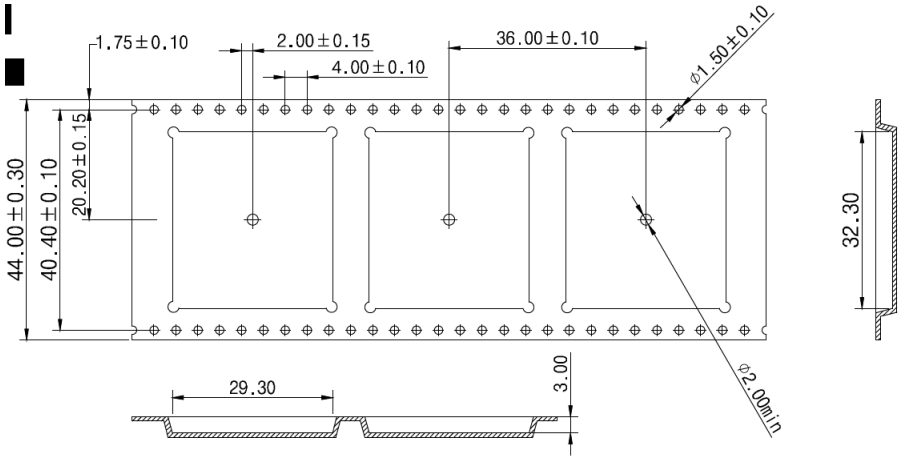


Figure 2-4: Tape Dimensions Details

2.8 Storage Conditions

1. Calculated shelf life in sealed bag: 6 months at <40 degree and <90% relative humidity (RH).
2. Peak package body temperature: 250 °C.
3. After bag was opened, devices that will be subjected to reflow solder or other high temperature process must:
   a) Mounted within: 168 hours of factory conditions <30 °C / 60% RH.
   b) Stored at ≤10% RH with N2 flow box.
4. Devices require baking, before mounting, if:
   a) Package bag does not keep in vacuumed while first time open.
   b) Humidity Indicator Card is >10% when read at 23°C ±5 °C.
   c) Expose at 3A condition over 8 hours or Expose at 3B condition over 24 hours.
5. If baking is required, devices may be baked for 12 hours at 125 °C ±5°C.

Note:	Level and body temperature are defined by IPC/JEDEC J-STD-020.

2.9 Mounting Considerations

This section provides reflow information.

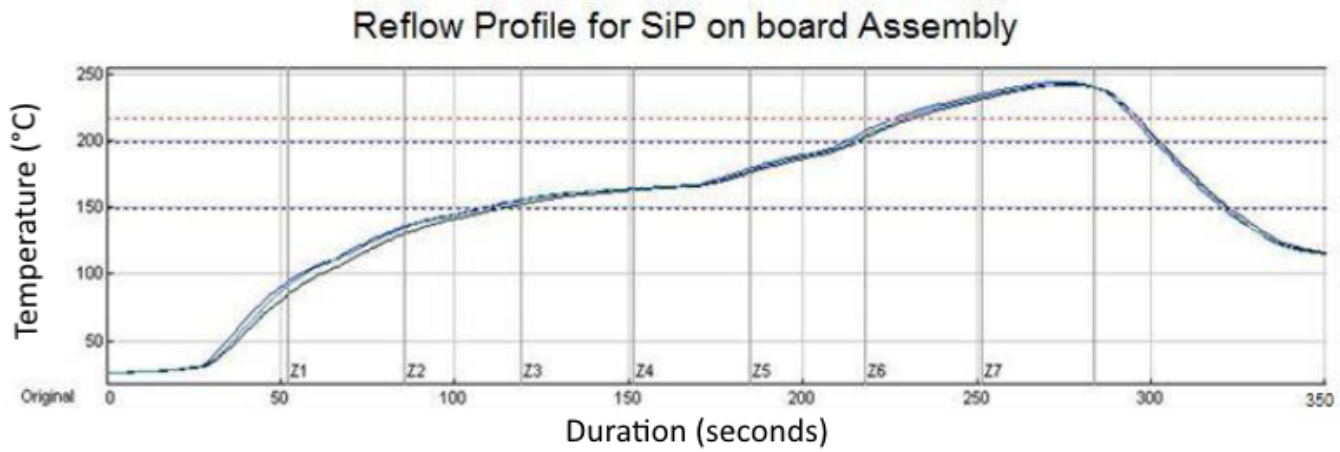


Figure 2-5: Reflow Profile

Table 2-8: Reflow Parameters

Parameter	Setting
Preheat Time	Temp: 150°C ~200 °C Time: 105±15 seconds
Dwell Time (Liquidous Time)	Temp: over 220 °C Time: 70 +5/-10 seconds
Peak Temperature	240 +10/-5 °C
Ramp-up rate	3 +0/-2 °C/second
Ramp-down rate	2 +0/-1 °C/second

2.10 Component Reliability

Notes:

1. This section does not apply to part number CB41Q85QRZ (engineering samples).
2. Relability test results will be provided in a future edition of this document.

Table 2-9: Reliability Test Plan

Item	Test conditions	Standard	Result
Preconditioning	(a) Bake: 125°C / 24 hours (b) MSL3: 30°C/60% RH, 192 hours (c) Reflow 3 cycles @ Tp: 250 ±2°C for modules	JESD22-A113	
TC	Temperature Shock Cycling (TC) -40°C to +85°C Air to air, 20 minutes, ramp rate 20°C /minute, 500 cycles	JESD22-A104	
THB	Temperature Humidity Bias Test +85°C, 85 % RH, Vcc Max, 168 hrs	JESD22-A101	
HTS	High Temperature Storage test (+125°C, 1000hrs)	JESD22-A103	
LTS	LowTemperature Storage test (-40°C, 1000hrs)	JESD22-A119	
Shock	Mechanical Shock (MS) (Half Sine, 500 m/s2, 11 ms, 6 shocks (1 shock for each ±axis)	DIN IEC 68-2-29	
Drop	Drop Test 1. Heigh t: 80cm, 2. concrete or steel 3. All surfaces and edges.	DIN IEC 68-2-31 ETS 300019-2-7	
Vibration	Vibration Test (Vib) Sweep-Sine Vibration & Random Vibration Sinusoidal, 10 ~ 500 Hz, 1.0 octave/min, 10 sweep cycles for 2h for each axis	DIN IEC 68-2-6 EIA/TIA 571 §4.1.1.2	
Bump	Bump (Half Sine, 250m/s2, 6ms, 2 bumps/sec, 1000 bumps per ±axis)	DIN IEC 68-2-29	

Table 2-9: Reliability Test Plan (Continued)

Item	Test conditions	Standard	Result
ESD	HBM Start: ±1000V, Stop:± 1000V Target: Classification 2 (±2000V to ±4000V)	ANSI/ESDA/JEDEC JS-001-2014	
	CDM Start: ±150V, Stop: ±150V Target: Classification C1 (±250V to <±500V)	ANSI/ESDA/JEDEC JS-002-2014	

2.11 RF Performance

This section presents the module's performance in LTE Band 42 and 43, and in CBRS Band 48.

Table 2-10: Output Power

LTE Band / CBRS Band	Conducted Power (dBm) Bandwidth 5 MHz, Full RB
Band 42	23 +1/-1.7
Band 43	23 +1/-1.7
Band 48	22 +1/-1.7

Rx sensitivity test is done using 2 receive paths, and with Tx power @ 23dBm.

Table 2-11: RF Sensitivity

LTE Band / CBRS Band	Typ. Sensitivity level (dBm) Bandwidth 5 MHz
Band 42	Less than -101
Band 43	Less than -101
Band 48	Less than -101

3 Signals and Pins

3.1 CB410L Pinout

Table 3-1 lists the function and main information for CB410L pads for part numbers CB41Q85QRZ and CB41Q85QRA defined in Table 2-1 on page 9.

The pads listed in Table 3-2 are connected to ground.

The pads listed in Table 3-3 are to be left unconnected.

Refer also to Section 3.2.1 High-Speed UARTs Flow Control Signals on page 28 that represents the typical implementation for UART hardware flow control.

Table 3-1: Pinout

Pad #	Pad Name	Alternate Function	Direction (HW)	Comments	RevZ RevA
2	ANT_DIV		In	Auxiliary antenna	X
4	ANT_MAIN		In / Out	Main antenna	X
6	HWID2	GPIO_28	In	This signal shall be pull-up.	X
7	HWID1	GPIO_27	In	This signal shall be pull-up.	X
8	AP_READY				
9	ACTIVITY_LED	GPO_2	Out	This signal is currently not managed by software.	
11	VBAT2		In		X
12	VBAT2		In		X
14	MODULE_ON_IND	GPIO_19	Out	See Section Notes on Signals	
15	SLEEP_IDLE_1				
16	WAKE_1	GPIO_3	In		

Table 3-1: Pinout (Continued)

Pad #	Pad Name	Alternate Function	Direction (HW)	Comments	RevZ RevA
17	WAKE_0		In		
18	NETWORK_LED	GPO_3, SPI_CS_N_2	Out	Light on the LED shows that DL packets are pushed on the network interface.	X
19	AUX_ADC1		In		
20	AUX_ADC0		In		
21	UART0_SIN	GPIO_34	In		X
22	UART0_SOUT	GPIO_35	Out		X
23	UART2_CTS	GPIO_6	In	See Section Notes on Signals	X
24	UART2_RTS	GPIO_7	Out		X
25	UART2_SIN	GPIO_4	In		X
26	UART2_SOUT	GPIO_5	Out		X
27	RFDATA_16		Out		
28	RFDATA_17		Out		
30	SPI _CS_N_1	GPIO_47	Out	Active low	
31	SPI _CS_N_2			Active low	
32	SPI SDO	GPIO_45	In	Data from SPI device to module.	
33	SPI SDI	GPIO_44	Out	Data from module to SPI device.	
34	SPI SCK	GPIO_43	Out		
35	SDIO_HOST_CMD	GPO_8	In/Out		
36	SDIO_HOST_D0	GPO_4	In / Out		
37	SDIO_HOST_D1	GPO_5, WAKE_3	In / Out		
38	SDIO_HOST_D2	GPO_6	In / Out		
39	SDIO_HOST_D3	GPO_7	In / Out		
40	SDIO_HOST_CLK	GPO_9	Out		

Table 3-1: Pinout (Continued)

Pad #	Pad Name	Alternate Function	Direction (HW)	Comments	RevZ RevA
41	RGMII_RX_DV				
42	RGMII_RXCLK				
43	RGMII_RXD0				
44	RGMII_RXD1				
45	RGMII_RXD2				
46	RGMII_RXD3				
47	RGMII_TX_EN				
48	RGMII_TXD0				
49	RGMII_TXD1				
50	RGMII_TXD2				
51	RGMII_TXD3				
52	RGMII_TXCLK				
53	RGMII_GTXCLK				
54	RGMII_MDC				
55	RGMII_MDIO				
56	USB_EXT_VBUS_VLD	WAKE_2	In		X
57	USB_D+		In/Out		X
58	USB_D-		In/Out		X
59	VBAT1		In		X
60	VBAT1		In		X
62	1V8_D		Out	Reference voltage for IOs. Note: it can be used to provide power small devices (50 mA max usage)	X
63	RESET_N		In		X
64	MODULE_PWR_EN		In	See IO Characteristics for VDD_PWR_EN	X

Table 3-1: Pinout (Continued)

Pad #	Pad Name	Alternate Function	Direction (HW)	Comments	RevZ RevA
65	SIM_VCC		Out		X
66	SIM_RST		Out		X
67	SIM_IO		In/Out		X
68	SIM_CLK		Out		X
69	SIM_DETECT		In		X
70	PCM_CLK	GPO_1	In	See Section Notes on Signals	
71	PCM_FS	GPIO_9	In/Out	See Section Notes on Signals	
72	PCM_RXD	GPIO_10	In	See Section Notes on Signals	
73	PCM_TXD	GPIO_8	Out	See Section Notes on Signals	
74	UART3_CTS	GPIO_16	In	See Section Notes on Signals	
75	UART3_RTS	GPIO_17	Out	See Section Notes on Signals	
76	UART3_SIN	GPIO_14	In		
77	UART3_SOUT	GPIO_15	Out		
78	GPIO20_I2C_SDA		In / Out		
79	GPIO20_I2C_SCK		In / Out		
80	FFF_FFH	GPIO_18	In	- Pull-up for a system boot in FFF mode.- Pull-down for a system boot in FFH mode.	X
119	UART1_SIN		In		X
120	TRST_N		In	JTAG	X
121	TMS		In	JTAG	X
122	TDI		In	JTAG	X
131	UART1_SOUT		Out		X
133	TCK		In	JTAG	X
134	TDO		Out	JTAG	X

Table 3-2: Ground Pads

Pad #	Pad Name	Comment
1 3 5 10 13 29 61	GND	All GND pads shall be connected to the same copper.
81 to 110	GND	All GND pads shall be connected to the same copper. Those pads have a thermal dissipation function also.

Table 3-3: DNC Pads

Pad #	Pad Name	Comment
111 to 118, 123 to 130, 132	DNC	Do not connect

3.2 Notes on CB410L Signals

3.2.1 High-Speed UARTs Flow Control Signals

- UART2_CTS: UART2 flow control, Clear-To-Send, active low, of the CB410L. To be connected to the RTS of the remote UART device. Provision a 1 kOhm pull-down on CTS pin when flowcontrol is not used. If it is connected to an external component (like a RS232 driver), the user should make sure that this component will present a low level to the CB410L. See Figure 3-1.
- UART2_RTS: UART2 flow control, Ready-To-Send, active low, of the CB410L. To be connected to the CTS of the remote UART device. See Figure 3-1.
- UART3_CTS: UART3 flow control, Clear-To-Send, active low, of the CB410L. To be connected to the RTS of the remote UART device. Provision a 1 kOhm pull-down on CTS pin when flowcontrol is not used. If it is connected to an external component (like a RS232 driver), the user should make sure that this component will present a low level to the CB410L. Figure 3-1.
- UART3_RTS: UART3 flow control, Ready-To-Send, active low, of the CB410L. To be connected to the CTS of the remote UART device. See Figure 3-1.

Figure 3-1 represents the typical implementation for the hardware flowcontrol.

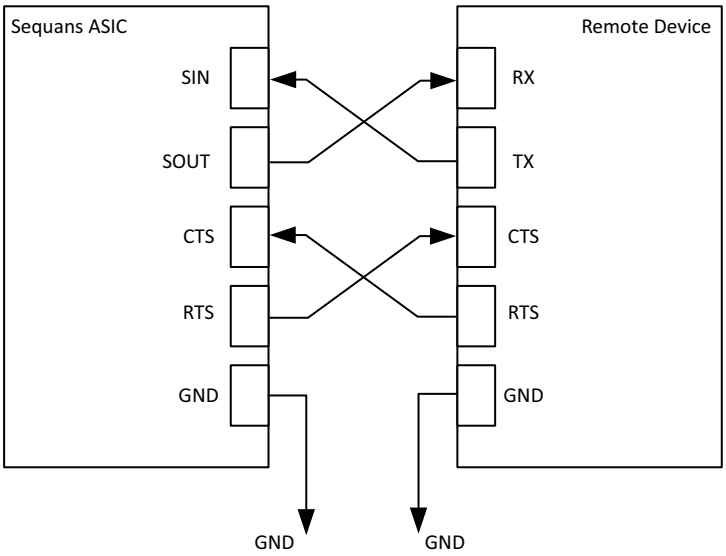


Figure 3-1: UART Flow Control

Note:	High-Speed UART can be used as low-speed UART, given a specific software registers configuration and the setting of the CTS signal to 0. Please contact Sequans customer support for details.

3.2.2 I2S/PCM Interface Signals

- PCM_RXD: PCM receive data. PCM data block is 8-bits or 16-bits. Only one data block is received per frame. Receive time-slot offset is programmable by using the RX_SLOT register. For instance, if RX_SLOT=5, then the 8-bit data block is received from time-slot #5 to #12. Bit-order is configurable.
- PCM_CLK: PCM clock input, from 128 kHz to 8192 kHz

  Sequans PCM interface takes PCM_CLK as an input in both master and slave modes.

Caution: This clock signal is an input in both master and slave modes.

When choosing a clock source for PCM_CLK, it is important to ensure that the selected frequency is supported by the IC connected to CB410L's PCM interface.

The choice of frequency depends on:

- Sampling frequency Fs
- Number of bits per sample Nbps
- Number of slots per PCM frame

It is given by the following formula:

```
PCM_CLK = Fs * Nbps * slots-per-PCM-frame
```

Where CB410L supports:

- All commonly used sampling frequencies (8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz, 192 kHz, 22.05 kHz, 44.1 kHz, 88.2 kHz, 176.4 kHz)
- 8 or 16 bits per sample (Nbps)
- 1 to (1024/Nbps) slots per PCM frame

- PCM_FS: Frame synchronization at 8 kHz. The number of time-slots within a frame varies, depending on PCM_CLK frequency. To be flexible in offset configuration, we define one PCM clock period per time-slot. Therefore, in 8-bit format, 8 time-slots are used to receive or transmit one 8-bit data block. If PCM_CLK=128 kHz, there are 16 time-slots per frame. If PCM_CLK=8192 kHz, there are 1024 time-slots per frame. In master mode, PCM_FS is an output generated internally. In slave mode, PCM_FS is an input. Both short and long Frame Sync standards are supported. Short Frame Sync is high for one and only one PCM clock period. Long Frame Sync is high for three consecutive PCM clock periods. In both cases, the positive edge of PCM_FS occurs every 125 µs.
- PCM_TXD: PCM transmit data. PCM data block is 8-bits or 16-bits. Only one data block is transmitted per frame. Transmit time-slot offset is programmable by using the TX_SLOT register. For instance, if TX_SLOT=8, then the 8-bit data block is transmitted from time-slot #8 to #15. Bit-order is configurable. PCM_TXD is in low-impedance during data transmission, otherwise it is in high impedance.

3.3 Power-Up Sequence

Important: The RESETN (pin 63) should be driven by the Host (active low). This signal should be kept high (100K pull up, 1V8).

The following timing requirement applies to the signals VBAT1, VBAT2, MODULE_PWR_EN and RESET_N. It must be respected for proper CB410L's behavior. The RESET_N signal is controlled automatically in case of cold start and warm start.

Caution: VBAT1 and VBAT2 should remain stable in the voltage range listed in 2.2 Electrical Operating Conditions on page 10; if this condition is not met, the internal OTP (One-Time Programmable) area of the baseband chip might be randomly corrupted and it can lead to a non-functional and unrecoverable state preventing the module to correctly boot.

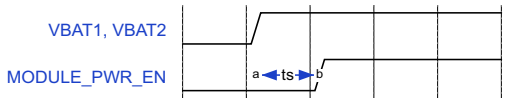


Figure 3-2: VBAT1, VBAT2, MODULE_PWR_EN Signals Timing Requirement for Cold Start

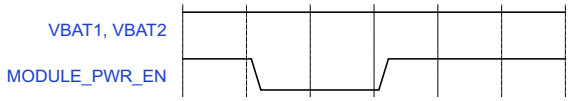


Figure 3-3: VBAT1, VBAT2, MODULE_PWR_EN Signals Timing Requirement for Warm Start

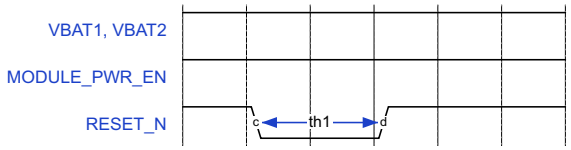


Figure 3-4: VBAT1, VBAT2, MODULE_PWR_EN and RESET_N Signals Timing Requirement for Reset Cycle

The timing minimum values are listed in Table 3-4.

Table 3-4: VBAT1, VBAT2 and RESET_N Signal Timing Values

Symbol	Description	Minimum Duration	Maximum Duration
ts	VBAT1 and VBAT2 setup time	0 ms	-
th1	RESET_N hold time	1 µs	-

A Acronyms

Acronym	Definition
CBRS	Citizens Broadband Radio Service
CPU	Central Processing Unit
DL	Downlink
ECCN	Export Control Classification Number
ECM	Ethernet Control Model, USB interface
EEM	Ethernet Emulation Model, USB interface
ESD	Electro-static discharge
GND	Ground
GPIO	General Purpose Input Output
HBM	Human Body Model (ESD)
I/O	Input/Output
IMEI	International Mobile Equipment Identity
IMS	Instant Messaging Service
IP	Internet Protocol
LTE	Long Term Evolution, or 4G. Standard is developed by the 3GPP www.3gpp.org.
PHY	Physical Layer
RB	Resource Block
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances

Acronym	Definition
Rx	Reception
S/N	or SN: Serial Number
SIM	Subscriber Identification Module
SMS	Short Message Service
SPI	Serial Peripheral Interface
Tx	Transmission
UE	User Equipment
UL	Uplink
USB	Universal Serial Bus

B PCB Layout Rules

This section provides general good practices in defining a PCB layout.

B.1 Placement

It is good to perform the placement of all the major components blocks before routing any section of the PCB design. The considerations here are:

- CB410L module
- RF interface
- Reset circuit

Initial placement of these parts allows assessment of the PCB floor plan usage and avoids any significant changes to final routed areas of the design if a placement issue is found.

The following information presents considerations when performing this placement:

1. Keep them in a similar quadrant to interface they connect to.
2. Consider orientation to avoid crossing traces when routing
3. Keep them as close as possible to the CB410L module where possible.

Note:	You can consider keeping 4mm from the perimeter of the module for component placement to allow possible update of alternative Sequans' module solution.

B.2 Trace Characteristic Design

This section explains some standard design rules when considering different types of signals involved (digital, power supply, RF).

B.2.1 Digital Traces

1. Careful and logical placement of digital signals are required to ensure separation of digital interference between each other and unrelated traces.
2. Consider the flow of ground currents during routing. Make sure that the grounding surrounding the traces (from source to load) remains continuous, with no cut or breaks. This will avoid long convoluted ground return currents which can create EMI-type problems.
3. Ensure the steps provided in Section Controlled Impedance Traces are taken into account for digital traces requiring specific impedance.
4. For those with no impedance requirements, be practical with the trace thickness. Keep them thin to avoid a buildup of capacitance, but make sure they are suitable to manufacture.
5. If routing traces on alternate layers, avoid paralleling them and keep them orthogonal. Good practice is to run traces on alternative layer from vertical to horizontal and so forth. This avoid traces directly coupling.
6. Important recommendation related to SIM connector placement can be found in Section ***UNRESOLVED***.

B.2.2 Power Supply Traces

1. Size the power supply traces appropriately for low impedance source. Pay attention to the number of vias used when routing traces across multiple layers. This is especially true for high current signals such as PA supply voltage.
2. For each power supply output, the decoupling capacitors ground pad must be connected to ground return of the power supply source.
3. Make sure that the digital traces remain well away from the power supply traces.
4. Appropriate dimensioning of the width and length of each supply track and the number of any interlayer connecting vias is needed to minimize the resistive losses in each supply track.

B.2.3 RF Traces

1. Avoid burying these traces as much as possible, because it increases RF losses compared with routing on the top.
2. Keep as short as possible to help reduce RF losses.
3. Design the impedance of the trace keeping in mind that the footprint of the RF components should be of similar width. This help avoid impedance discontinuities.
4. Ensure the steps provided in Section Controlled Impedance Traces are taken into account when making the trace width.

B.2.4 Controlled Impedance Traces

- Calculation of traces width and spacing:

  Use simple RF design tools to calculate the copper trace thicknesses based upon:

  a) Thickness of the dielectric substrate that is used between the RF copper trace and the ground plane
  b) Spacing between the copper trace and the adjacent ground plane (on the same layer)
  c) Dielectric constant of the substrate material being used for manufacture. It happens that the required trace width is impossible to manufacture. It must be reconsidered until feasible. In this case, consider implementation of one of the following:

     - Thicker substrate

     - Moving the ground plane reference to the next layer down by removing the ground plane under the transmission line of interest

- General good practice guidelines

  a) Careful placement is required to keep RF traces short and kink-free.
  b) Do not route RF traces on intermediate layers.
  c) Ground planes beneath RF traces should be continuous.
  d) The ground fill around RF traces should have sufficient clearance to maintain the desired impedance.

- RF matching component footprints

  Depending on the substrate thickness and the size of the components pads used can deviate the desired transmission impedance from the wanted (nominally 50 Ohm).

  For RF devices, if any copper pad in relation to RF signals is significantly larger than the transmission line width, then the ground reference could be moved to the next layer down.

B.2.5 Grounding

1. Stitch ground areas together with vias where flooded ground remains unterminated.
2. Stitch ground areas together in general to keep common ground impedance the same across the region.
3. RF ground planes should be as large and continuous as possible and not be cut into small islands. Check that strings of vias do not inadvertently create slots in ground or power planes.