FOREWORD TO THE OPERATIONAL DESCRIPTION

INTRODUCTION

This foreword to the full technical specifications of our module is meant to summarize the basic functions, frequency bands and modes supported by it and describe the followed strategy to get the FCC and ISED approval.

TECHNICAL SPECIFICATIONS

SUPPORTED MODES / FREQUENCY BANDS

The following table summarize the frequency bands and modes, which our module will support in the U.S and Canada.

These have been the modes/frequency bands tested in the lab according to FCC and ISED rules.

Band	UL	DL	LTE cat M1
2	1850 – 1910	1930 – 1990	Supported
4	1710 – 1755	2110 – 2155	Supported
5	824 – 849	869 – 894	Supported
12	699 – 716	729 – 746	Supported
13	777 – 787	746 – 756	Supported
25	1850 – 1915	1930 – 1995	Supported

As the device is LTE cat M1 the bandwidth of the transmitting channels is always 1.4 MHz.

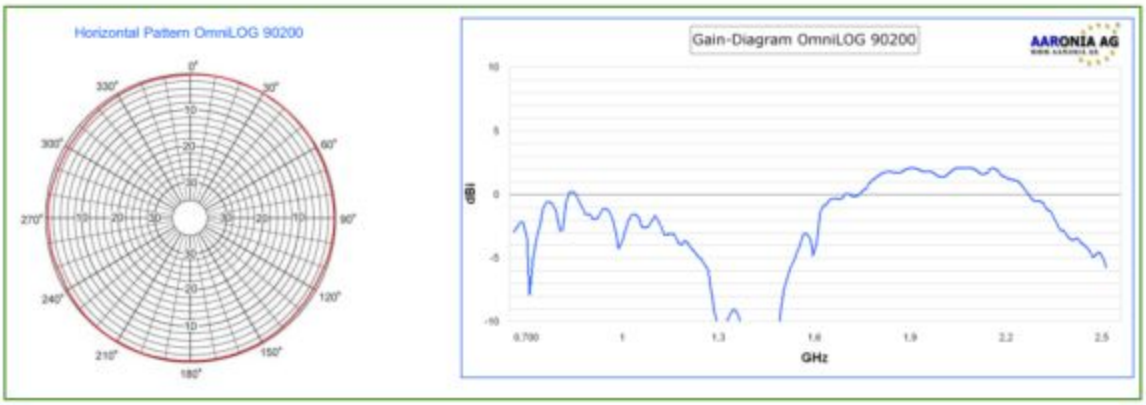
The device is meant to use only channels with bandwidth 5, 10, 15, and 20 MHz in each of the aforementioned bands.

Even when the full datasheet after this pages mentions LTE NB IoT we seek modular approval just for the device as LTE.

ANTENNAS

The antenna used for testing was the Broadband Antenna OmniLOG® 90200.

Frequency range 700MHz - 2,5GHz, specially for GSM, 3G, LTE and 2,4GHz WLAN.



In the RF exposure evaluation performed to the module, taking into account the tune-up values and procedure provided along with this application, we got the following results as ideal antennas which will be provided to our customers.

Technology / Mode	Band	Frequency (MHz)	Maximum Gain to comply with:			Maximum Gain (dBi)
			FCC MPE Limits (dBi)	ISED MPE Limits (dBi)	FCC/ISED EIRP Limits (dBi)	
LTE Cat-M1	2	1850 - 1910	11.0	7.5	7.0	**7.0**
LTE Cat-M1	4	1710 - 1755	11.0	7.2	4.0	**4.0**
LTE Cat-M1	5	824 - 849	8.4	5.1	14.6	**5.1**
LTE Cat-M1	12	699 - 716	7.6	4.6	10.9	**4.6**
LTE Cat-M1	13	777 - 787	8.1	4.9	10.9	**4.9**
LTE Cat-M1	25	1850 - 1915	11.0	7.5	7.0	**7.0**

PRELIMINARY DATA SHEET

SKY66430-11: LTE for IoT System-in-Package

Applications

- Wearables
- Personal trackers
- Asset trackers
- Alarm systems
- Security cameras
- Industrial monitoring devices
- Low-power IoT devices

Features

- Complete BB to RF solution in a single package:
  - Integrated baseband, transceiver, RF front end, RAM memory, and power management
  - 8.8 x 10.8 x 0.95 mm BGA package, 0.5 mm pitch
  - Device weight: 229 mg
- Compliant to 3GPP Rel-13 LTE Advanced Pro specifications, including VoLTE support
- Upgradable to 3GPP Rel-14
- Optimized for LTE half-duplex operation (HD-FDD) for LTE-M/NB-IoT
- Global frequency band support:
  - Low-band: B5, B8, B12, B13, B14, B17, B18, B19, B20, B26, B28, B85
  - Mid-band: B1, B2, B3, B4, B25, B66
- Two AUX ports to support additional bands
- Extended DRX and PSM features for long sleep duration cases
- Extremely low leakage internal PMU that enables operability for 10 years
- Smart PA biasing scheme to maximize efficiencies during low-output power operation
- Throughput:
  - LTE-M (1.4 MHz bandwidth) up to 300 kbps DL, 375 kbps UL
  - NB-IoT (200 kHz bandwidth):
    - NB1: 27.2 kbps DL, 62.5 kbps UL
    - NB2: 120 kbps DL, 170 kbps UL
- Single 3.1 V to 4.5 V supply operation
- Operating temperature range: -40 °C to +85 °C
- Skyworks conformal shielding
- Lead (Pb)-free and RoHS-compliant
- MSL3 @ 260 °C per JEDEC J-STD-020

Description

The SKY66430-11 is a multi-band multi-chip System-in-Package (SiP) supporting cellular LTE-M/NB-IoT (half-duplex FDD) platforms. The SiP integrates the entire RF front end, transceiver, power management, memory, and baseband modem for an LTE multi-band radio operating in the 698 to 2200 MHz frequency range. NOR flash, crystals, and a few passives external to the package complete the SiP implementation.

Front-End Section

The front-end section includes Rx low-pass filters, broadband PA with bias controller, Tx low-pass harmonic filter, and antenna switch.

Rx Section

Receive low-pass filters are integrated into the SIP along with the necessary matching to yield a 50 Ω single-ended impedance for the antenna. The filters provide a high level of rejection to out-of-band interferers, protecting the transceiver from high blocking signal levels and guaranteeing 3GPP LTE blocking test conformance. The Rx low-pass filters are cascaded with the low throw count switch to establish a lower insertion loss and noise figure than conventional LTE receivers.

Tx Section

The PA load-line is optimized for high efficiency while simultaneously meeting 3GPP ACLR and emissions mask specifications with LTE up to 6 RB. An integrated LPF is implemented to reject the PA and transceiver harmonics while at the same time minimizing any post PA loss for an optimized transmit current consumption. Out-of-band emissions performance is emphasized by the design to be 3GPP-compliant for low-band B5, B8, B12, B13, B14, B17, B18, B19, B20, B26, B28, B85 and mid-band B1/B2/B3/B4/B25/B66.

This SiP includes the Sequans Monarch 3330 chipset

Transceiver Section

A direct-conversion RF solution using low power technology has the following functional characteristics:

- Direct conversion in the Tx and Rx paths
- On-chip Fractional-N frequency synthesizers
- On-chip anti-alias filters
- On-chip AGC circuit
- On-chip reconstruction filters
- On-chip calibration including VCO and DC offset correction in the Rx paths
- Rx and Tx gain and phase correction loops between the RF and baseband
- Software control for synthesizer, Tx/Rx, adjustment, and gain control
- External clock reference of 38.4 MHz

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

Baseband Modem Section

- DL processing block, handling LTE downlink physical layer (Rx)
- UL processing block, handling LTE uplink physical layer (Tx)
- Synchronization processing block, handling frequency search and synchronization to LTE network
- Optimized for new Cat-M1 channels and operation of 3GPP Release 13
- An MCU with instruction and data cache, running LTE protocol stack at frequency up to 312 MHz
- A quad-IO SPI interface (QSPI) to 1.8 V serial NOR flash of 64 Mbit or 128 Mbit size, running at 104 MHz, with support of eXecute-in-Place (XIP) and critical word first wrapping reads
- A pSRAM controller interfacing with an embedded 64-Mbit pSRAM at 104 MHz
- Three high-speed UARTs with hardware flow control
- One I^2C master up to 3.4 Mbps
- One SPI master and slave up to 13 MHz
- Muxed GPIOs interruptible, with support of pulse counter and PWM functionality
- Two UICC interfaces compliant with ETSI TS 102 221 specification, including SIM card removal detection and support for 1.8 V and 3 V voltage levels
- Secured JTAG, with possibility of enabling or disabling the interface by hardware or secured software

NOTE: *This SiP includes the Sequans Monarch 3330 chipset. For more specific information related to that chipset, which is not included in this data sheet, refer to the data sheet for that product.*

A functional block diagram is shown in Figure 1. A typical application block diagram is shown in Figure 2. The pinout is shown in Figure 3. Signal pin assignments and functional pin descriptions are described in Table 1.

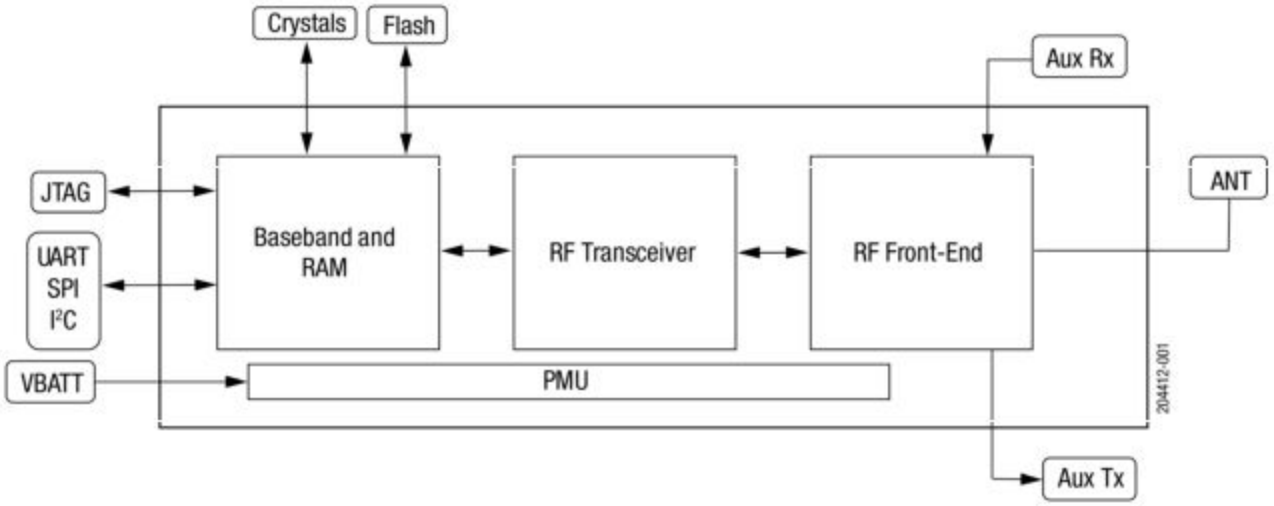


Figure 1. SKY66430-11 Functional Block Diagram

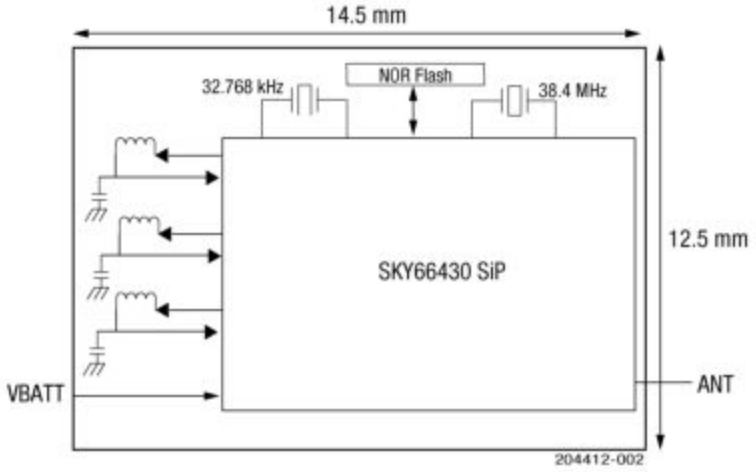
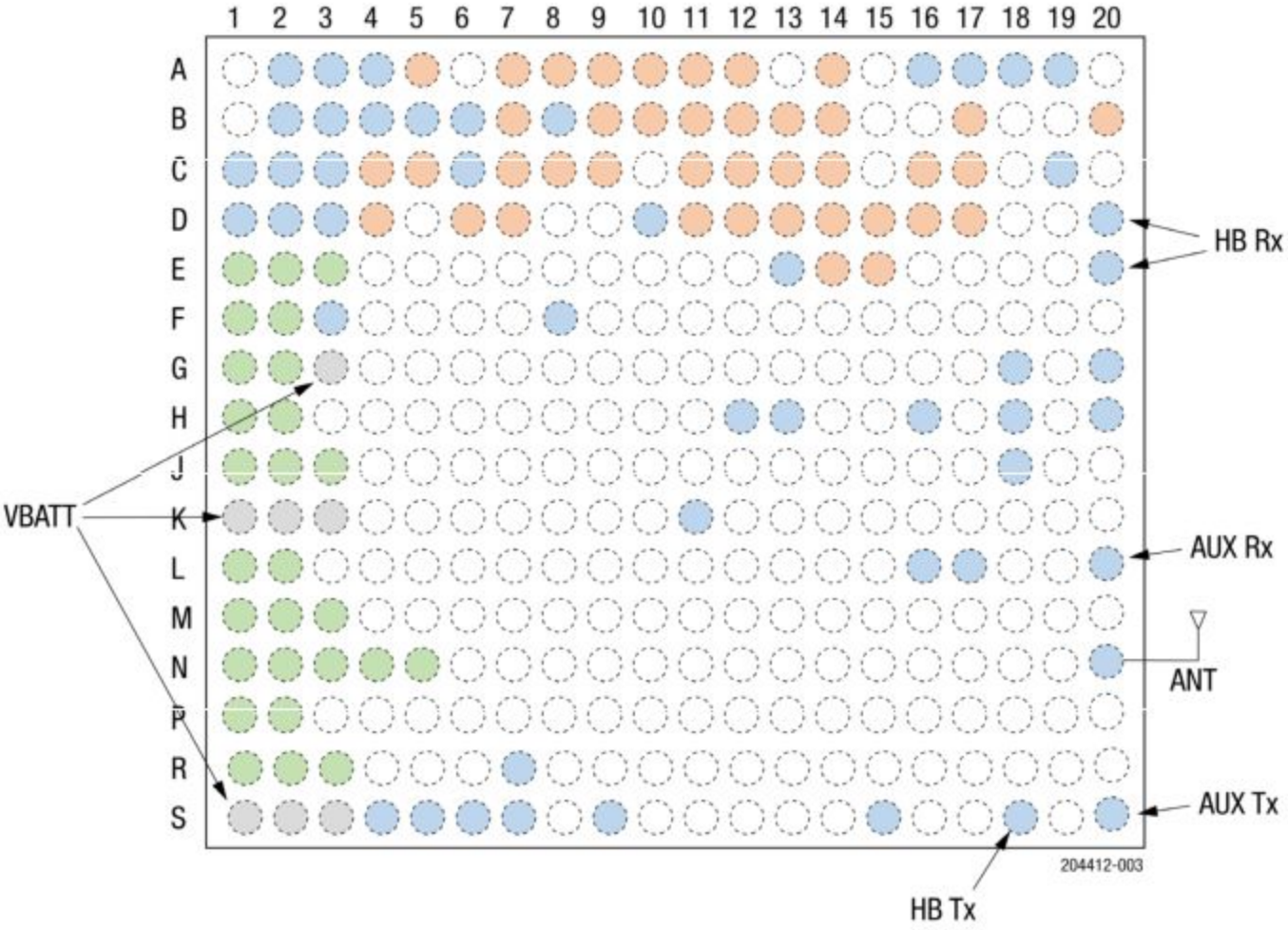


Figure 2. SKY66430-11 Typical Application Block Diagram



Color Coding Legend for Pinout

Group 1 – Interfaces							Group 2	Group 3	Group 4
UART0	UART1	UART2	QSPI	MSSPI	I2C	SCI	PMU	RF	VBATT

Figure 3. SKY66430-11 Signal Pin Assignments (Top View)

Table 1. SKY66430-11 Signal Pin Assignments and Functional Pin Descriptions (1 of 3)

Bump	Name	Description	Bump	Name	Description
A2	SAR_DETECT	Can be enabled to perform SAR detect function (input for external proximity detection interrupt). GPIO with wake capability (wake capability not enabled by default)	B9	SCI_EXT_RST_N	SIM external reset
A3	TDI	JTAG	B10	WAKE_SCI_EXT_DETECT	External SIM detect. Wake source
A4	TDO	JTAG	B11	WAKE_SCI_INT_DETECT	Internal SIM detect. Wake source
A5	WAKE_UART0_CTS_N	UART0. Wake source.	B12	SCI_INT_RST_N	SIM internal reset
A7	UART2_SOUT	UART2	B13	WAKE_UART1_CTS_N	UART1. Wake source.
A8	UART2_RTS_N	UART2	B14	UART1_CLK	UART1
A9	VCC_SCI0	No connection	B17	MSSPI_SDO	Master-Slave SPI data out
A10	SCI_EXT_DATA	SIM external data	B20	STATUS_LED	STATUS_LED
A11	VCC_SCI1	SIM supply	C1	Reserved	Reserved pad: it must be pulled up to external supply and connected to a test point.
A12	SCI_INT_CLK	SIM internal clock	C2	WAKE_GPIO_3	Wake source (wake capability not enabled by default)
A14	UART1_SOUT	UART1	C3	TMS	JTAG
A16	DCXOP	Reference crystal connection	C4	UART0_CLK	UART0
A17	RFDATA_8	RF control signal	C5	UART0_SIN	UART0
A18	RFDATA_6	RF control signal	C6	RFDATA_14	RF control signal
A19	WAKE_GPIO_0	Wake source (wake capability not enabled by default)	C7	UART2_CLK	UART2
B2	RING0	RING0 (OUT): it is recommended to pull-up this pin with the application host processor supply as it will become high impedance when module is in low power mode. GPIO with wake capability (wake capability not enabled by default)	C8	UART2_SIN	UART2
B3	TCK	JTAG	C9	SCI_EXT_CLK	SIM external clock
B4	TRST_N	JTAG	C11	SCI_INT_DATA	SIM internal data
B5	RFDATA_15	RF control signal	C12	QSPI_IO_1	Quad-SPI Flash I/O 1
B6	RFDATA_13	RF control signal	C13	QSPI_IO_2	Quad-SPI Flash I/O 2
B7	UART2_CTS_N	UART2	C14	UART1_SIN	UART1
B8	1V8_BBREG	1.8 V filtering	C16	PS_STATUS	Power Saving Status (OUT): indicates when the modem is in deep sleep

Color Coding Legend for Table 1

Group 1 – Interfaces							Group 2	Group 3	Group 4
UART0	UART1	UART2	QSPI	MSSPI	I2C	SCI	PMU	RF	VBATT

Table 1. SKY66430-11 Signal Pin Assignments and Functional Pin Descriptions (2 of 3)

Bump	Name	Description	Bump	Name	Description
C17	MSSPI_CLK	Master-Slave SPI clock	G1	PMU_1V1	SoC 1.1V supply (input)
C19	WAKE_PWR_OFF_GPIO	Wake source (wake capability not enabled by default)	G2	PMU_1V1	SoC 1.1V supply (input)
D1	WAKE_TIMESTAMP_SNAP_0	Wake source (wake capability not enabled by default)	G3	VBATT (PMU_VISNS)	VBATT Sense node
D2	WAKE_GPIO_2	Wake source (wake capability not enabled by default)	G18	1V2_RXVCO	Internal 1.2 V LDO output for external stability capacitor
D3	KHZ32_CLK_OUT	Output 32 kHz	G20	RFDATA_7	RF control signal
D4	UART0_SOUT	UART0	H1	PMU_LX1V1	1.1 V from DCDC switch node to external LC
D6	UART0_RTS_N	UART0	H2	PMU_LX1V1	1.1 V from DCDC switch node to external LC
D7	I2C_SCL	I^2C interface clock. Output only for I2C_SCL function. In/Out for GPIO function	H12	RFIC_BBREG2A5_EN	Internal 2V5 regulator enable(recommended to add 100K pull-down resistor)
D10	RFIC_LDO_EN	LDO enable	H13	RFIC_DCXO_REG1V8_EN	Internal 1V8 regulator enable
D11	QSPI_CS_N	Quad-SPI chip select	H16	AUXADC1	External connection to AUX ADC
D12	QSPI_IO_3	Quad-SPI I/O 3	H18	AUXADC2	External connection to AUX ADC
D13	QSPI_CLK	Quad-SPI clock	H20	RFDATA_3	RF control signal
D14	QSPI_IO_0	Quad-SPI I/O 0	J1	PMU_PGND2	1.1 V DCDC power ground
D15	UART1_RTS_N	UART1	J2	PMU_PGND2	1.1 V DCDC power ground
D16	MSSPI_CS_1_N	Master-Slave SPI chip select 1	J3	PMU_PGND2	1.1 V DCDC power ground
D17	MSSPI_SDI	Master-Slave SPI data in	J18	AUXADC3	External connection to AUX ADC
D20	RXHBP	Optional HB differential RX, positive	K1	VBATT (PMU_VI2)	1.8 V/3.0 V VBATT power input
E1	PMU_OSCO	32.8 kHz oscillator	K2	VBATT (PMU_VI2)	1.8 V/3.0 V VBATT power input
E2	PMU_LPM_N	Reserved, 1.8 V always-on enable	K3	VBATT (PMU_VI2)	1.8 V/3.0 V VBATT power input
E3	PMU_POWERON_PULSE	Active high power-on pulse	K11	1V2_TXVCO	Internal 1.2V LDO output for external stability capacitor
E14	QSPI_RST_N	Quad-SPI flash reset	L1	PMU_LX1V8	1.8 V from DCDC switch node to external LC
E15	MSSPI_CS_0_N	Master-Slave SPI chip select 0	L2	PMU_LX1V8	1.8 V from DCDC switch node to external LC
E20	RXHBN	Optional HB differential Rx, negative	L16	RFDATA_1_CAP	RFDATA MIPI decoupling
F1	PMU_OSCI	32.8 kHz oscillator	L17	RFDATA_2_CAP	RFDATA MIPI decoupling
F2	PMU_POWERON_PULSE_N	Active low power-on pulse	L20	FEM_AUX1_RX	Optional HB RX SP6T connection
F3	EXT_RST_N	Chip reset	M1	PMU_1V8	SoC 1.8 V supply (input)
F8	I2C_SDA	I^2C bus data			

Color Coding Legend for Table 1

Group 1 – Interfaces							Group 2	Group 3	Group 4
UART0	UART1	UART2	QSPI	MSSPI	I2C	SCI	PMU	RF	VBATT

Table 1. SKY66430-11 Signal Pin Assignments and Functional Pin Descriptions (3 of 3)

Bump	Name	Description	Bump	Name	Description
M2	PMU_1V8	SoC 1.8 V supply (input)	R7	3V0_FEM_VCC2	3.0 V FEM VCC2
M3	PMU_1V8	SoC 1.8 V supply (input)	S1	VBATT (PMU_VI1)	VBATT power input
N1	PMU_PGND1	1.8/3.0 V DCDC power ground	S2	VBATT (PMU_VI1)	VBATT power input
N2	PMU_PGND1	1.8/3.0 V DCDC power ground	S3	VBATT (PMU_VI1)	VBATT power input
N3	PMU_PGND1	1.8/3.0 V DCDC power ground	S4	1V8_FEM_VIO	1.8 V FEM VIO
N4	VP_1V8	PSRAM Power (connect to N5)	S5	3V0_FEM_VDD	3.0 V FEM VDD
N5	1V8_I_PSRAM	PSRAM Power (connect to N4)	S6	3V0_FEM_VCC1	3.0 V FEM VCC1
N20	FEM_ANT	Antenna	S7	3V0_FEM_VCC2	3.0 V FEM VCC2
P1	PMU_LX3V0	3.0 V from DCDC switch node to external LC	S9	RFDATA_5	RF control signal
P2	PMU_LX3V0	3.0 V from DCDC switch node to external LC	S15	FEM_VIO_CAP	RFDATA MIPI optional decoupling
R1	PMU_3V0	SoC 3.0 V supply (input)	S18	TXHB2	Optional HB TX
R2	PMU_3V0	SoC 3.0 V supply (input)	S20	FEM_AUX2_TX	Optional HB TX SP6T connection
R3	PMU_3V0	SoC 3.0 V supply (input)			
A15, B1, B15, C15, D8, E4, E5, E6, E7, E9, E10, E11, E12, E13, E16, E17, F5, F6, F7, F9, F10, F11, F12, F14, F15, F16, G4, G5, G6, G7, G10, G11, G12, G13, G14, G16, G17, H4, H5, H6, H9, H10, H11, H14, H15, H17, J5, J6, J7, J8, J9, J12, J15, K5, K6, K7, K9, K14, K16, L4, L5, L6, L7, L9, M4, M5, M6, M7, N6, N7, S13, and S14.					**These pins are designated as Do Not Connect.**
All other pins not specifically listed here are ground pins.					

Color Coding Legend for Table 1

Group 1 – Interfaces							Group 2	Group 3	Group 4
UART0	UART1	UART2	QSPI	MSSPI	I2C	SCI	PMU	RF	VBATT

UART Expected Usage

- **UART0:** main AT interface to be connected with host application. Wake from low power via HW flow control is active in this UART.
- **UART1:** secondary AT interface or debug interface. Wake from low power via HW flow control is active in this UART.
- **UART2:** modem console or debug interface.

Figure 3a represents the typical implementation for the hardware flow control for UART0, UART1, and UART2. TXD and RXD signals are mandatory.

CTS/RTS are mandatory in order to control SiP low power modes. The SKY66430 is designed for use as data communications equipment (DCE). Based on the conventions for DCE-DTE connections, the DCE device will communicate with the customer application (DTE) using the following signals:

- Port TXD on the Application send data to the SKY66430 SIN signal line.
- Port RX on the Application receives data from the SKY66430 SOUT signal line.

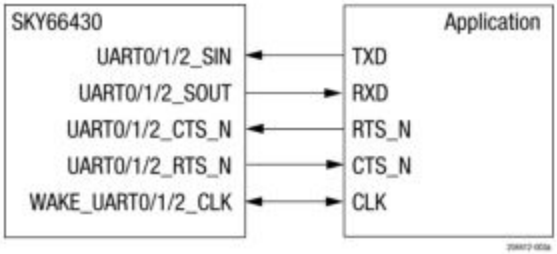


Figure 3a. UART0, UART1, and UART2 Signals Convention and Flow Control

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY66430-11 are shown in Table 2. Recommended operating conditions of the SKY66430-11 are provided in Table 3. SIP electrical specifications are shown in Table 4. The electrical specifications for low-band Tx are provided in Table 5. Table 6 shows the electrical specifications for mid-band Tx.

Table 7 shows the Rx electrical specifications for low-band and mid-band RX. Table 8 shows the AUX port electrical specifications.

Table 2. SKY66430-11 Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typ	Max	Units
RF input power (AUX Tx/Rx)	CW PIN			37.5	dBm
Supply voltages (with RF)	VBATT	-0.5		TBD	V
Operating case temperature	TCASE[2]	-40	25	+85	°C
Storage temperature	TSTG	-40		+150	°C

1 Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

2 TCASE refers to the temperature of the ground pad on the underside of the package.

ESD HANDLING: *Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.*

Table 3. SKY66430-11 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage	VBATT	3.1	3.8	5.5	V
Case operating temperature range	TRANGE	-40	+25	+85	°C

Table 4. SKY66430-11 Power Consumption Electrical Specifications
(V_{BATT} = 3.8 V, T_{CASE} = +25°C, QPSK/1.4 MHz BW / 6RB (MPR = 0), Unless Otherwise Specified)

Component	Supply Rail	Current or Loss	Heat Power
SKY66430-11, including DC-DC losses	1.1 V	470 mA	0.52 W
	1.8 V	260 mA	0.47 W
	3.0 V	490 mA	1.47 W
Flash	1.8 V	25 mA	0.05 W
Total			2.51 W

Table 5. SKY66430-11 Low-Band TX Electrical Specifications (1 of 2)
(V_{BATT} = 3.8 V, T_{CASE} = +25°C, LTE Low-Band, f = 782 MHz, QPSK/5 MHz BW/6RB, Unless Otherwise Specified)

Parameter		Symbol	Conditions	Min	Typ	Max	Units
Frequency		f		698		915	MHz
Maximum output power		P_{OUT_MAX}		24			dBm
		$P_{OUT\_MAX\_ETC}$[1]		23			
Power variation		DELTA_POUT	$P_{OUT} = P_{OUT\_MAX}$		2		dB
Adjacent channel leakage ratio (based on 5 MHz LTE channels) 6 RB transmitted signal on RB 19 through 24	EUTRA	EUTRA_ACLR1 (power measured in adjacent 5 MHz LTE channel)	$P_{OUT} = P_{OUT\_MAX}$		-35	-34	dBc
			$T_{CASE} = T_{RANGE}$			-33	
	UTRA1	UTRA_ACLR1 (power measured in adjacent 3.84 MHz UTRA channel)	$P_{OUT} = P_{OUT\_MAX}$		-38	-37	
			$T_{CASE} = T_{RANGE}$			-36	
Modulation accuracy		EVM_QPSK	Load = 50 Ω, P_{OUT} = +23 dBm		3	5	%
Harmonics	Second	2fo	$P_{OUT} = P_{OUT\_MAX}$		-40	-35	dBm/MHz
	Second (B13)	2fo			-54	-52	dBm/MHz
	Second (B28)	2fo			-40	-38	dBm/MHz
	Third	3fo			-40	-35	dBm/MHz
	Third (B28)	3fo			-55	-50	dBm/MHz
	Fourth and higher	4fo			-65	-60	dBm/MHz

Table 5. SKY66430-11 Low-Band TX Electrical Specifications (2 of 2)
(VBATT = 3.8 V, TCASE = +25°C, LTE Low-Band, f = 782 MHz, QPSK/5 MHz BW/6RB, Unless Otherwise Specified)

Parameter		Symbol	Conditions	Min	Typ	Max	Units
Noise during B13 TX	LB (B13) noise in B13 Rx band	$P_{NOISE\_Emissions\_Bands}$	f_{MEAS} = 756 MHz[2]		-65		dBm/MHz
	LB (B13) noise in B14 Rx band		f_{MEAS} = 768 MHz[2]		-60		dBm/MHz
	LB (B13) noise in public safety (NS_07)		f_{MEAS} = 775 MHz[2]		-60		dBm/6.25kHz
	LB (B13) noise in GPS Band		f_{MEAS} = 1574.42 to 1576.42 MHz[3]		-75		dBm/MHz
	LB (B13) noise in GNSS band		f_{MEAS} = 1559.00 MHz to 1574.42 MHz[3] f_{MEAS} = 1576.42 MHz to 1610.00 MHz[3]		-50 -75		dBm/MHz dBm/MHz
ANT port return loss		RL_{ANT}	P_{IN} = -30 dBm		10		dB
Stability		S	No oscillations, all spurious: < -36 dBm/100 kHz @ 30 MHz~1 GHz < -30 dBm/MHz @ 1 GHz ~ 12.5 GHz T_{CASE} = T_{RANGE}	6:1			VSWR
Ruggedness		Ru	No permanent damage to module P_{OUT} = P_{OUT_MAX} @ Load = 50 Ω T_{CASE} = T_{RANGE}	10:1			VSWR

[1] ETC = Extreme Temperature Condition, T_{CASE} = -40 °C and T_{CASE} = +85 °C.

[2] Measured with +24 dBm TX on 5 MHz LTE channel centered at 779.5 MHz, lowest 6RB.

[3] Measured with +24 dBm TX on 5 MHz LTE channel centered at 784.5 MHz, highest 6RB.

Table 6. SKY66430-11 Mid-Band TX Electrical Specifications
(VBATT = 3.8 V, TCASE = +25°C, LTE Mid-band, f = 1732 MHz, QPSK/1.4 MHz BW/6RB, Unless Otherwise Specified)

Parameter		Symbol	Conditions	Min	Typ	Max	Units
Frequency		f		1710		1980	MHz
Maximum output power		POUT_MAX		24			dBm
		POUT_MAX_ETC[1]		TBD			dBm
Power variation		DELTA_POUT	POUT = POUT_MAX		2		dB
Adjacent channel leakage ratio (based on 5 MHz LTE channels) 6 RB transmitted signal on RB 19 through 24	EUTRA	EUTRA_ACLR1 (power measured in adjacent 5 MHz LTE channel)	POUT = POUT_MAX		-35	-34	dBc
			TCASE = TRANGE			-33	dBc
	UTRA1	UTRA_ACLR1 (power measured in adjacent 3.84 MHz UTRA channel)	POUT = POUT_MAX		-38	-37	dBc
			TCASE = TRANGE			-36	dBc
Modulation accuracy		EVM_QPSK	Load = 50 Ω, POUT = +23 dBm		3	5	%
Harmonics	Second	2fo	POUT = POUT_MAX		-40	-35	dBm/MHz
	Third	3fo			-40	-35	dBm/MHz
	Fourth and higher	4fo			-40	-35	dBm/MHz
Noise	Noise in B4 Rx band	PNOISE_Emissions_Bands	fMEAS = 2110 MHz[2]		-50		dBm/MHz
	Noise in GPS Band		fMEAS = 1574.42 to 1576.42 MHz[3]		-70		dBm/MHz
	Noise in GNSS band		fMEAS = 1559.00 MHz to 1574.42 MHz[3] fMEAS = 1576.42 MHz to 1610.00 MHz[3]		-70		dBm/MHz
ANT port return loss		RL_ANT	PIN = -30 dBm		10		dB
Stability		S	No oscillations, all spurious: < -36 dBm/100 kHz @ 30 MHz–1 GHz < -30 dBm/MHz @ 1 GHz – 12.5 GHz TCASE = TRANGE	6:1			VSWR
Ruggedness		Ru	No permanent damage to module POUT = POUT_MAX @ Load = 50 Ω TCASE = TRANGE	10:1			VSWR

[1] ETC = Extreme Temperature Condition, TCASE = -40 °C and TCASE = +85 °C.

[2] Measured with +24 dBm TX on 5 MHz LTE channel centered at 1752.5 MHz, highest 6 RB.

[3] Measured with +24 dBm TX on 5 MHz LTE channel centered at 1712.5 MHz, lowest 6 RB.

Table 7. SKY66430-11 Low-Band and Mid-Band Rx Electrical Specifications
(V_{BATT} = 3.8 V, T_{CASE} = +25°C, Unless Otherwise Specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low-Band						
Operating frequency	f		729		960	MHz
ANT port return loss	RL_{ANT}	In/Out, 50 Ω, 729 to 960 MHz	7	10		dB
RSSI	$RSSI_{LB}$	TBD		-109.7		dBm
Mid-Band						
Operating frequency	f		1805		2200	MHz
ANT port return loss	RL_{ANT}	In/Out, 50 Ω, 1805 to 2200 MHz	7	10		dB
RSSI	$RSSI_{MB}$	TBD		-109.7		dBm

Table 8. SKY66430-11 AUX Port Electrical Specifications
(V_{BATT} = 3.8 V; T_{CASE} = +25°C, Unless Otherwise Specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AUX1_RX port insertion loss	IL_{AUX}	0.7 to 1.0 GHz 1.4 to 2.0 GHz 2.0 to 2.7 GHz		0.4 0.5 0.6		dB
AUX1_RX port return loss	RL_{AUX}	In/Out, 50 Ω, 0.7 to 2.7 GHz	7	10		dB
AUX1_RX port compression point, P0.1dB	$P0.1dB_{AUX}$	0.7 to 2.7 GHz		38		dBm
AUX1_RX port third order input intercept point	$IP3_{AUX}$	0.7 to 2.7 GHz		70		dBm
AUX2_TX port insertion loss	IL_{AUX}	0.7 to 1.0 GHz 1.4 to 2.0 GHz 2.0 to 2.7 GHz		0.4 0.5 0.6		dB dB dB
AUX2_TX port return loss	RL_{AUX}	In/Out, 50 Ω, 0.7 to 2.7 GHz	7	10		dB
AUX2_TX port compression point, P0.1dB	$P0.1dB_{AUX}$	AUX1 port, 0.7 to 2.7 GHz		38		dBm
AUX2_TX port third order input intercept point	$IP3_{AUX}$	AUX1 port, 0.7 to 2.7 GHz		70		dBm

Evaluation Board Description

The SKY66430-11 Evaluation Board is used to test the performance of the SKY66430-11 SiP. The schematic diagrams for the SKY66430-11 are shown in Figures 4a through 4d.

An assembly diagram of the Evaluation Board is shown in Figure 5.

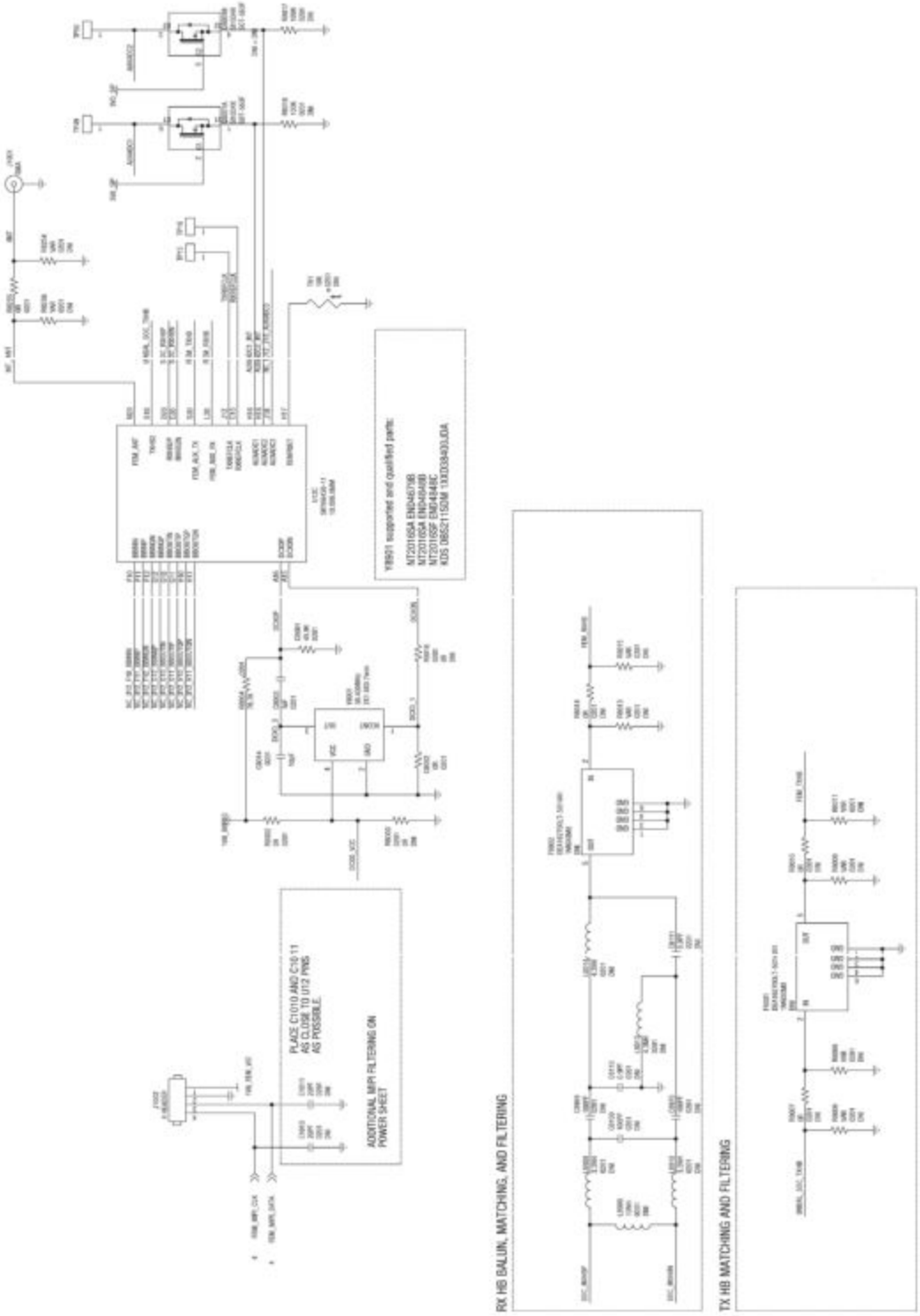


Figure 4a. SKY66430-11 Evaluation Board Schematic - Analog/RF

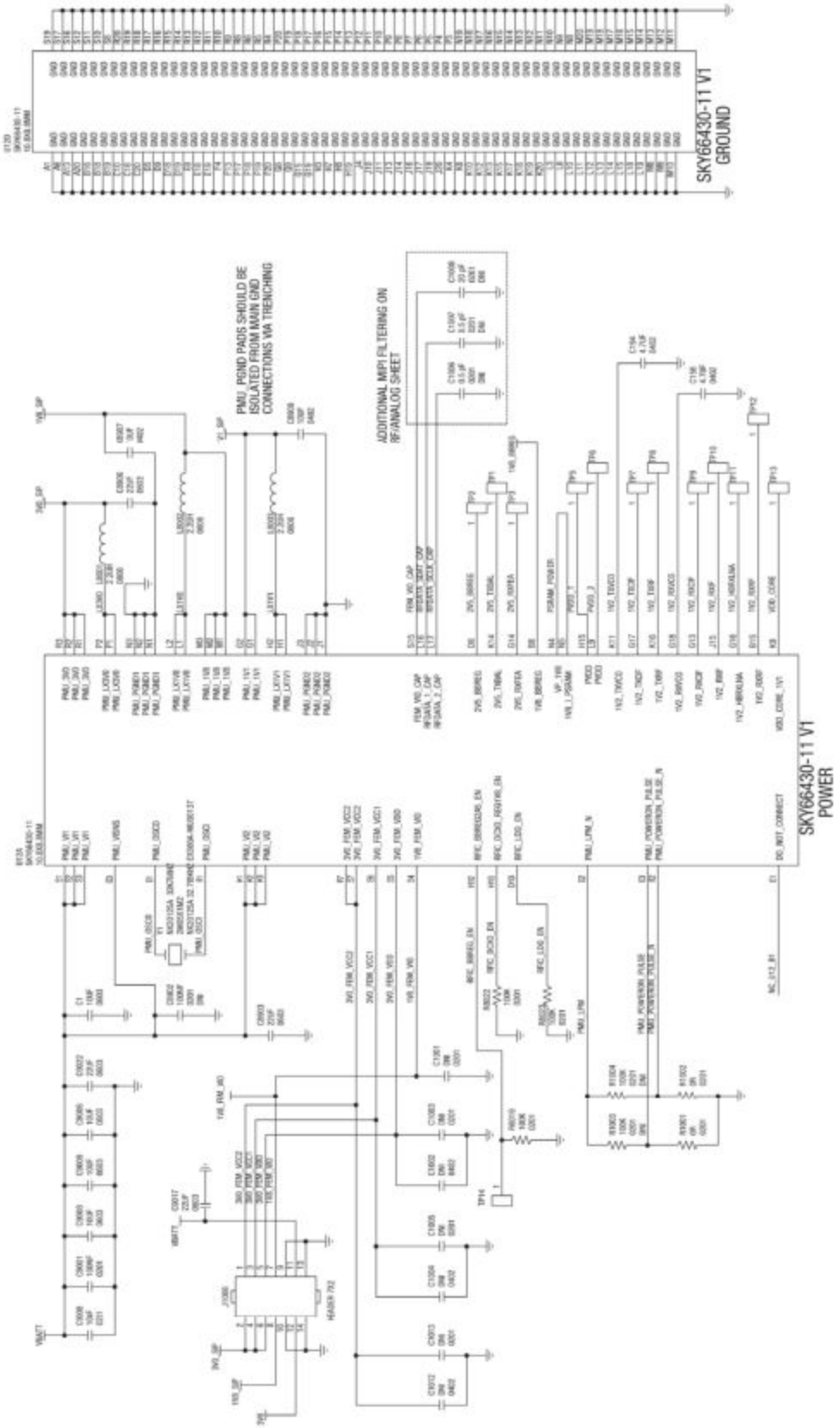


Figure 4b. SKY66430-11 Evaluation Board Schematic - Power

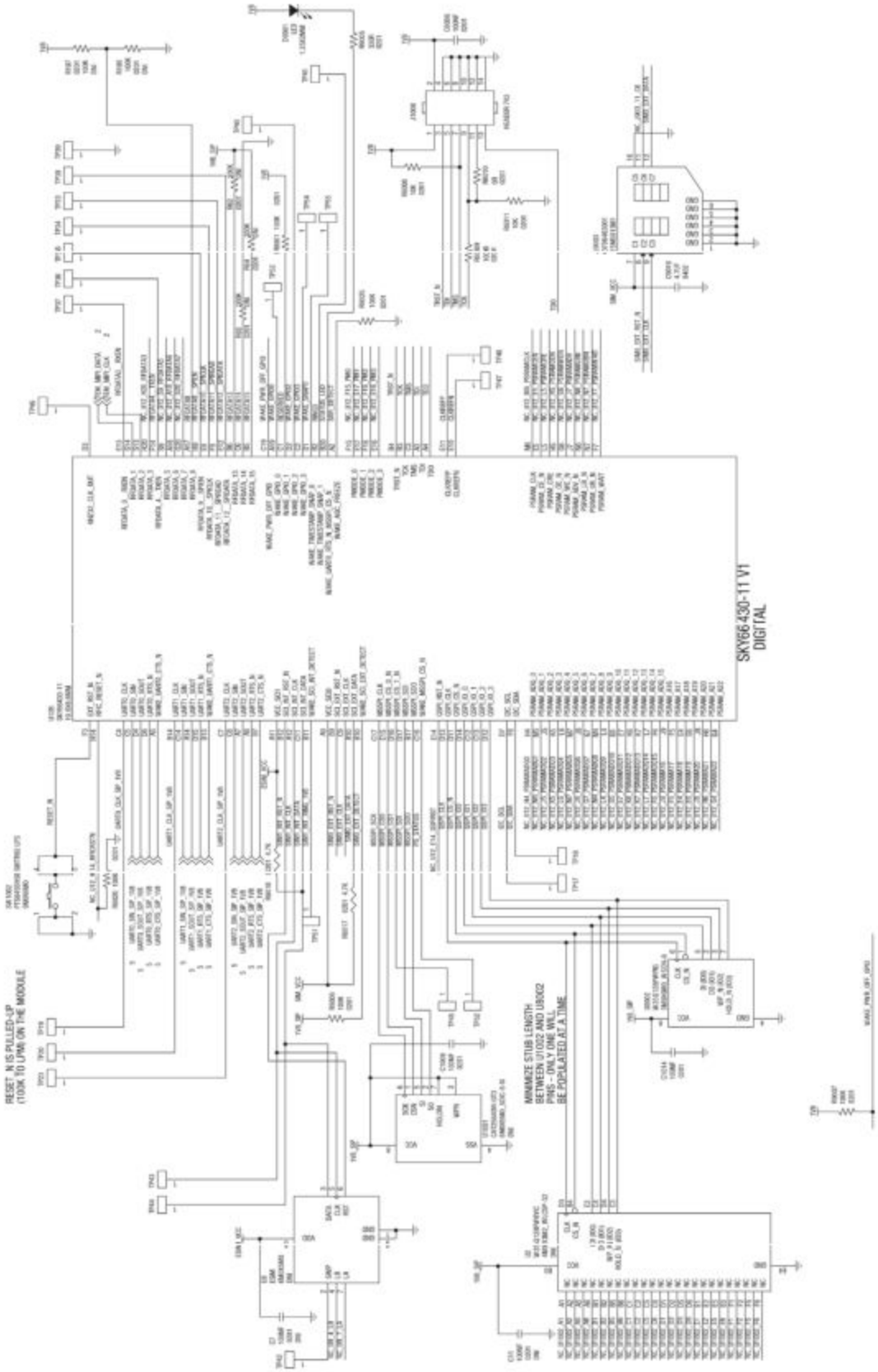


Figure 4c. SKY66430-11 Evaluation Board Schematic - Digital

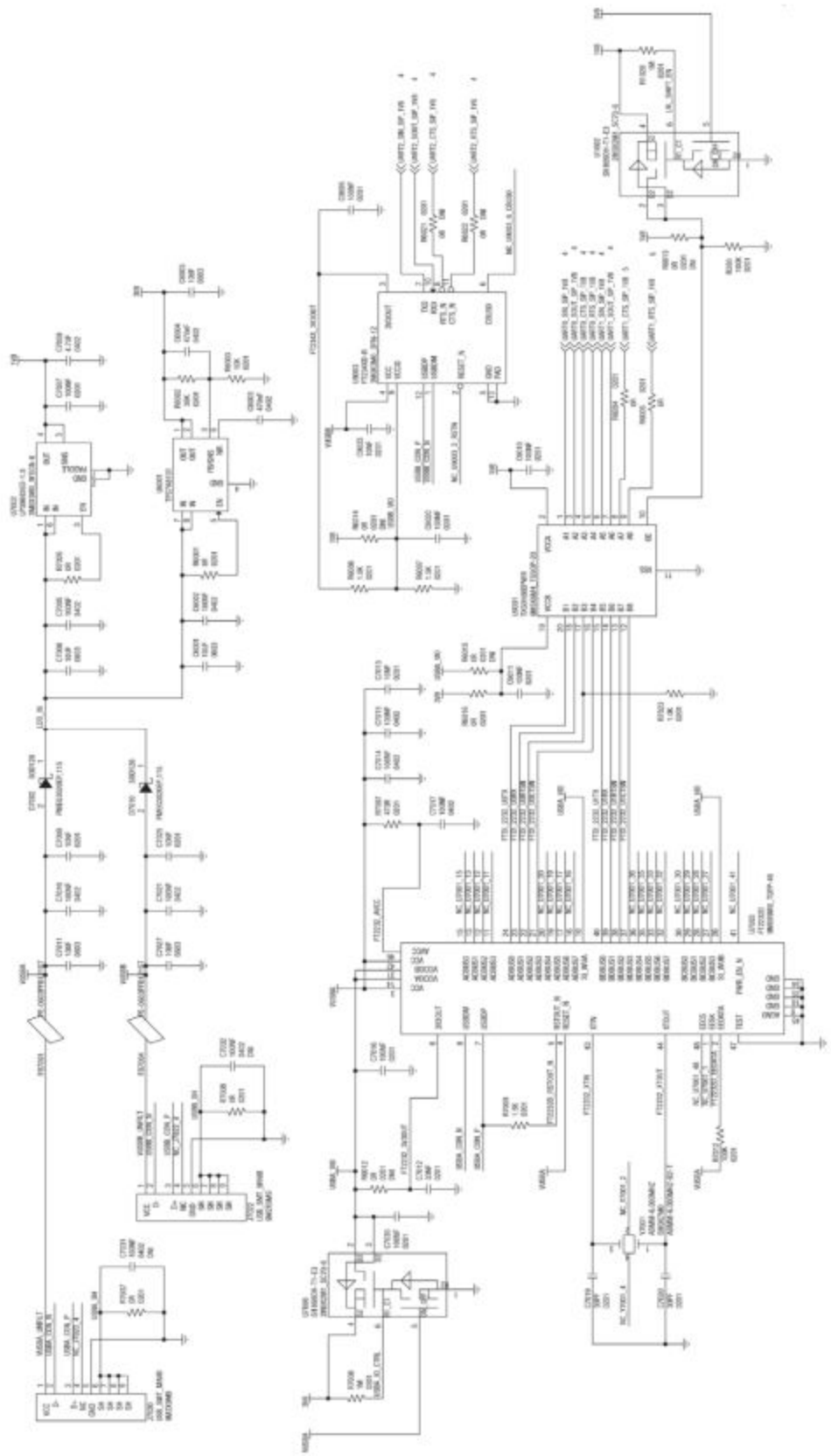
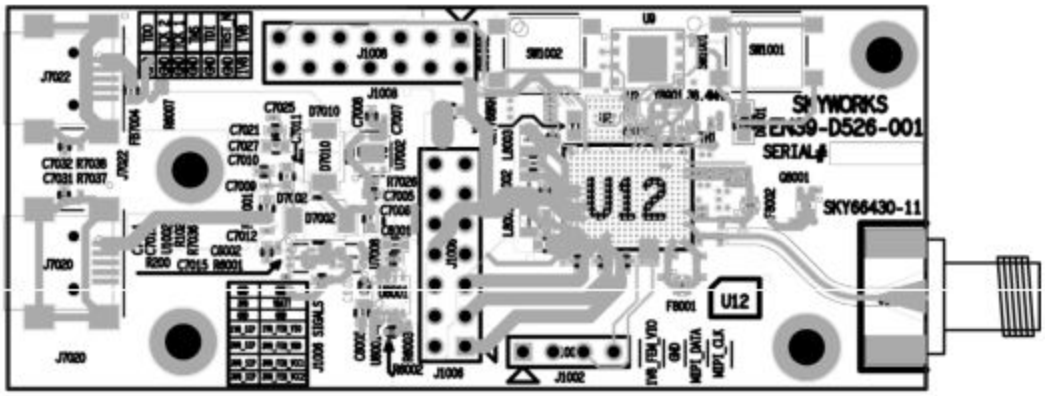
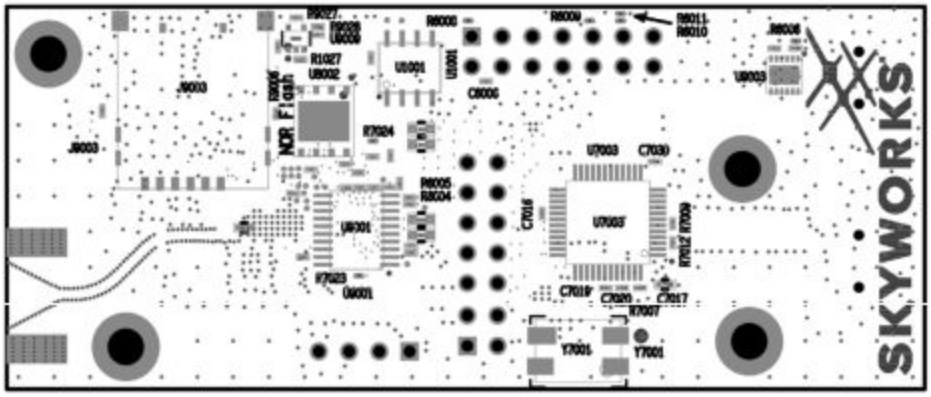


Figure 4d. Evaluation Board Schematics - Miscellaneous



Top View



Bottom View

Figure 5. SKY66430-11 Application Board Assembly Diagram

Package Dimensions

The typical part marking for the SKY66430-11 is shown in Figure 6. The PCB layout footprint for the SKY66430-11 is shown in Figure 7. Package dimensions are shown in Figure 8, and tape and reel dimensions are provided in Figure 9.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY66430-11 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

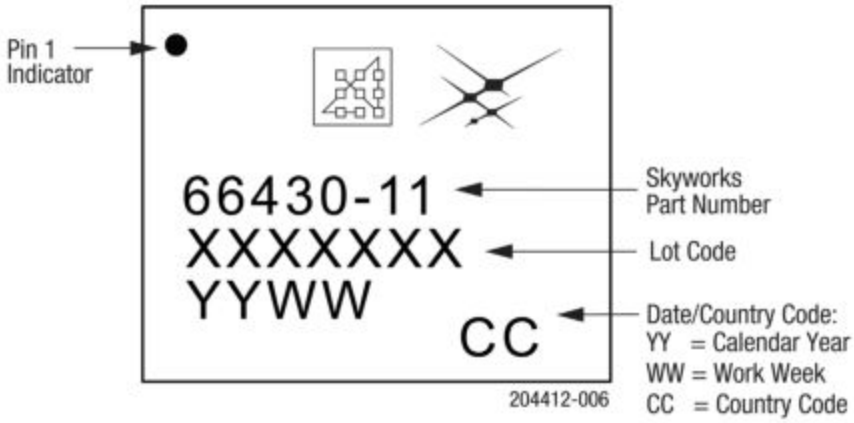
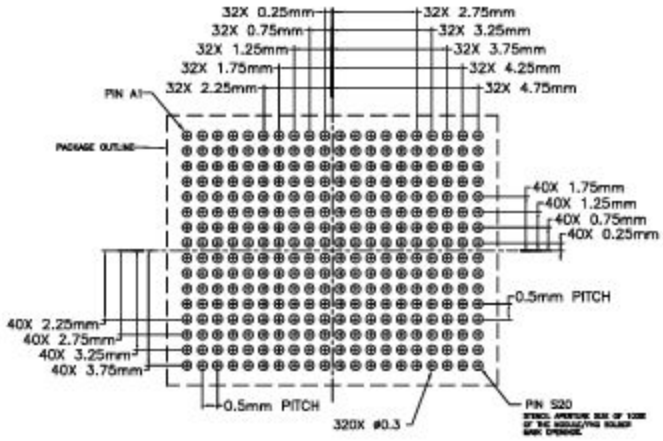
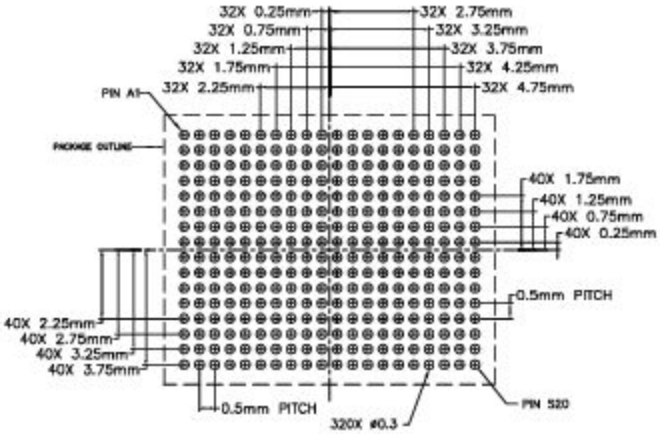


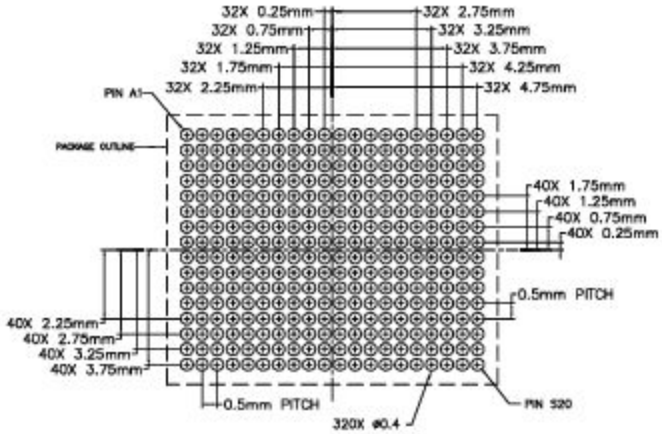
Figure 6. SKY66430-11 Typical Part Marking



STENCIL APERTURE
Top View



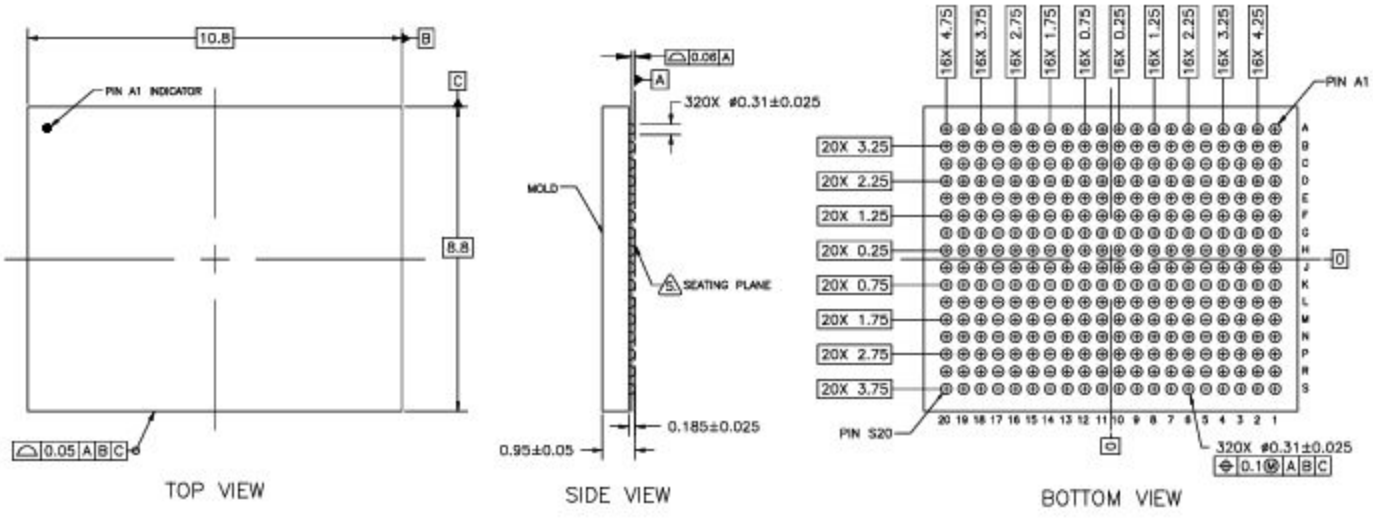
METALLIZATION
Top View



SOLDER MASK OPENING
Top View

NOTE: THERMAL VIAS SHOULD BE RESIN FILLED AND CAPPED IN ACCORDANCE WITH IPC-4761 TYPE VII VIAS. 30-35UM Cu THICKNESS IS RECOMMENDED.

Figure 7. SKY66430-11 PCB Layout Footprint



NOTES: UNLESS OTHERWISE SPECIFIED.

1. DIMENSIONING AND TOLERANCING IN ACCORDANCE WITH ASME Y14.5M–1994.
2. SEE APPLICABLE BONDING DIAGRAM AND DEVICE ASSEMBLY DRAWING FOR DIE AND COMPONENT PLACEMENT.
3. PAD DEFINITIONS PER DETAILS ON DRAWING.
4. PCB TYPE 6L NS SSV 40 GS 250.
5. PRIMARY DATUM A AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE IS COMPATIBLE WITH TRANSFER AND COMPRESSION MOLD.
7. THIS PACKAGE CONFORMAL SHIELDING.

204412-008

Figure 8. SKY66430-11 Package Dimensions

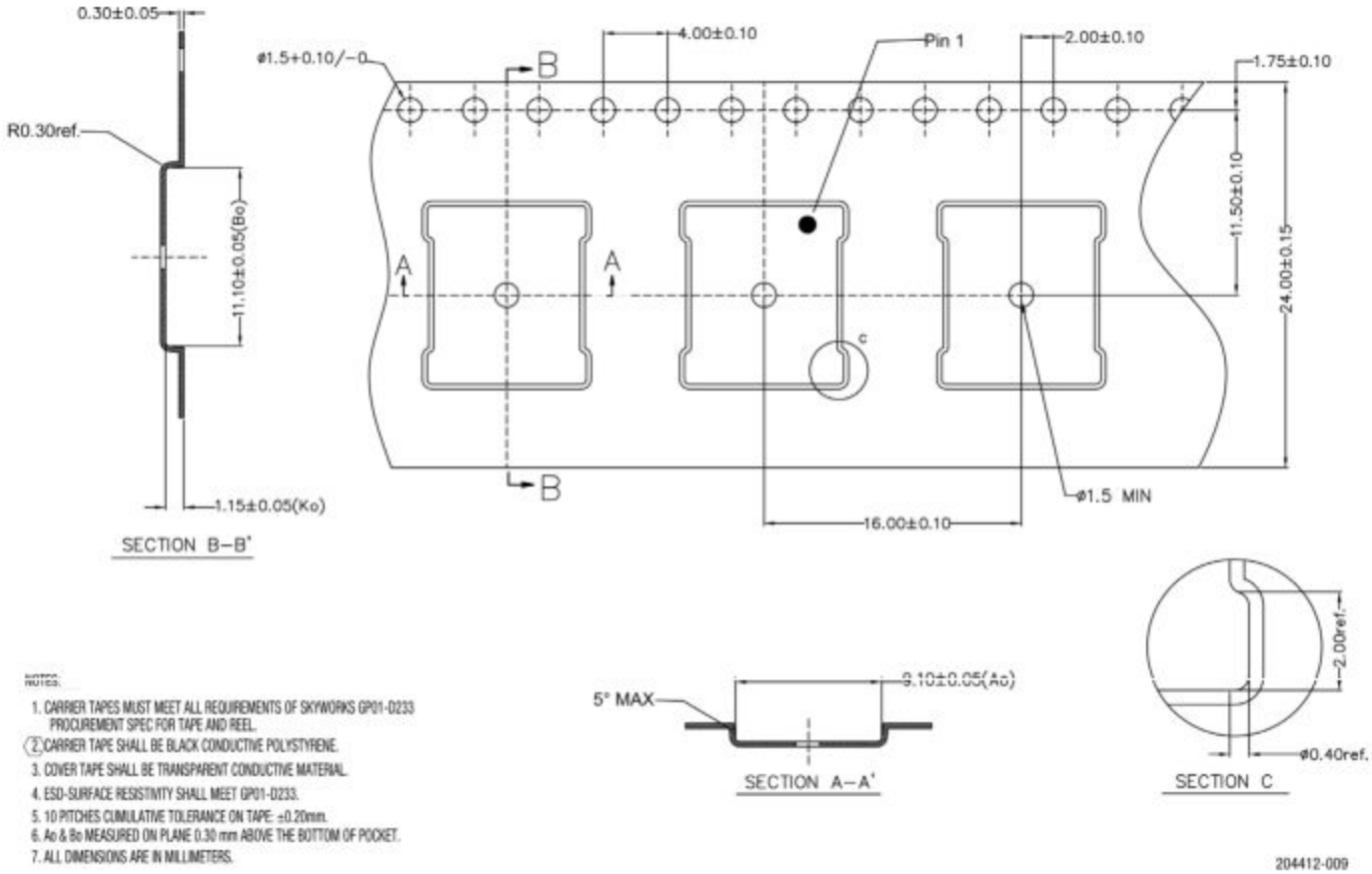


Figure 9. SKY66430-11 Tape and Reel Dimensions

Ordering Information

Part Number	Product Description	Evaluation Board Part Number
SKY66430-11 / SQN66430-11	LTE for IoT System-in-Package	SKY66430-11EK1

Data sheet

Rev 1.8
02.12.2013

Broadband Antenna OmniLOG® 90200

Frequency range 700MHz - 2,5GHz, specially for GSM, 3G, LTE and 2,4GHz WLAN

Highlights:

- Highly isotropic from 700MHz to 2,5GHz
- Optimal for usage with spectrum analyzer for omni-directional measurements
- 90° knuckle base with SMA connector
- Small weight and very small dimensions
- **10 years warranty**

AARONIA AG
WWW.AARONIA.DE

Made in Germany

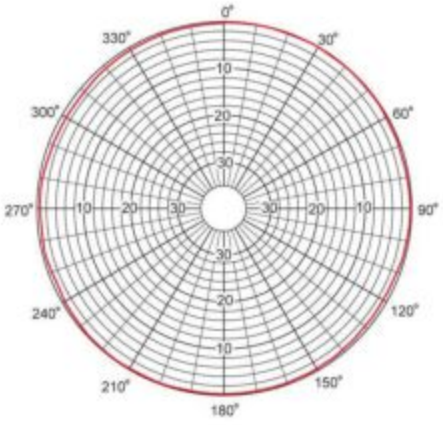
Specifications

OmniLOG® 90200

- Design: Omni-Directional
- Nominal impedance: 50 Ohms
- Frequency range: 700MHz - 2,5GHz
- VSWR (typ): < 3:1
- RF-connection: SMA (male)
- Temperature range: - 20°C to +70°C Shock: 40G at 10msek
- Thermal Shock: - 20°C to +70°C:10 cycles
- Dimensions (L/W): 210 x 20mm
- Weight: 70gr
- **Warranty: 10 years**

OmniLOG 90200 Antenna with Spectran HF-60100 V4.
The antenna is directly supported by the V4 series. It can be used for the GSM and UMTS frequency range with the Rev.3 units too (measurement uncertainty only 2dB).

Horizontal Pattern OmniLOG 90200



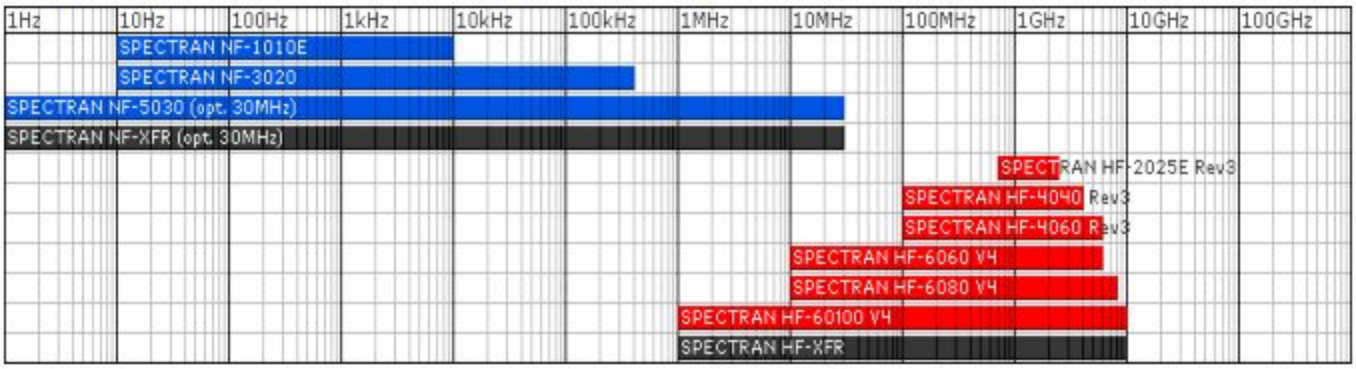
Front view OmniLOG 90200 Broadbandantenna

Rear view

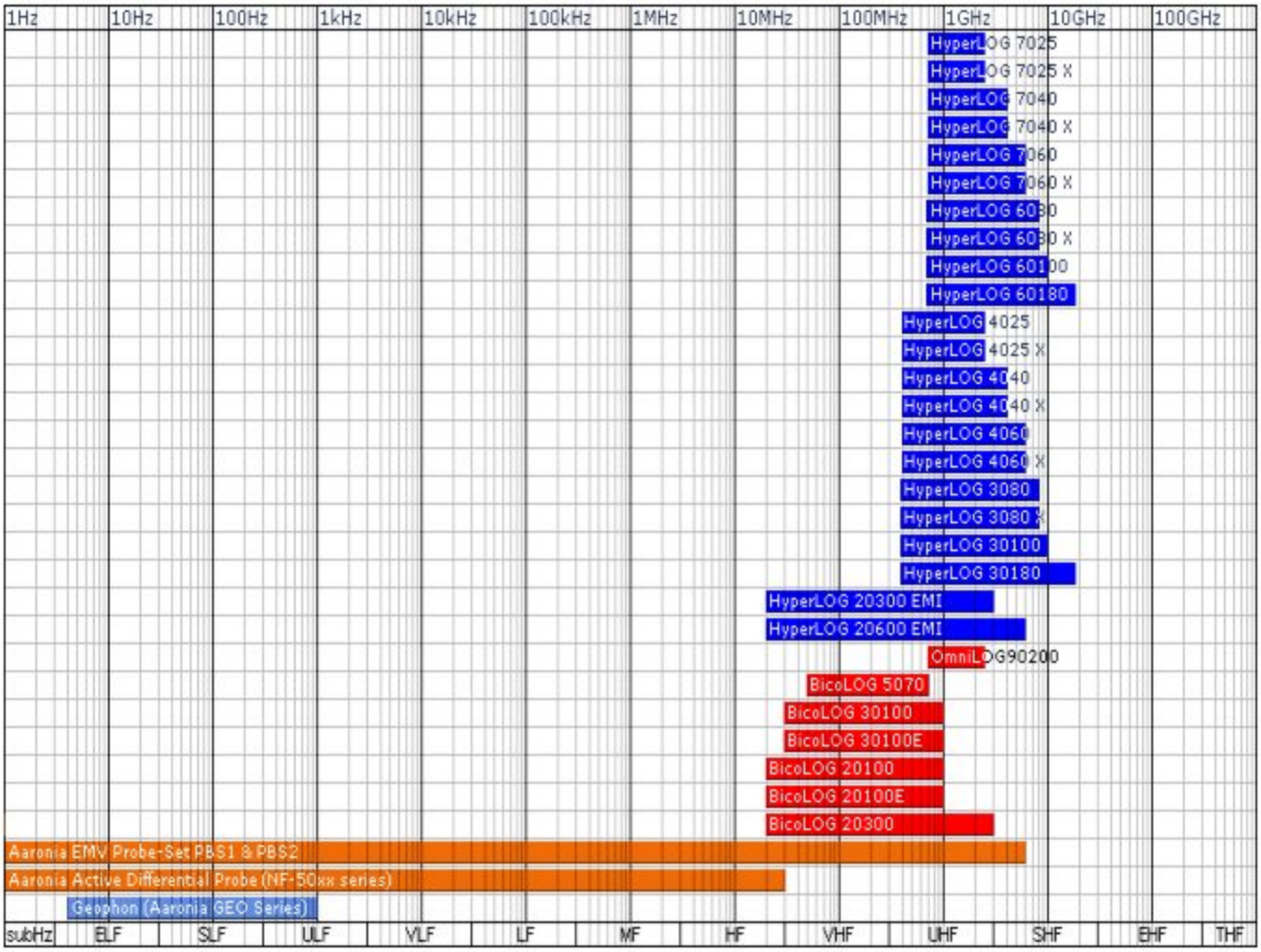
OmniLOG with Spectran HF-XFR (OmniLOG 90200 Antenna already included with the Spectran HF-XFR)

Frequency overview Analyzer & Antennas

Frequency Overview SPECTRAN Spectrum Analyzer



Frequency Overview HyperLOG and BicoLOG Antennas and Probes



References

User of Aaronia Antennas and Spectrum Analyzers (Examples)

Government, Military, aeronautic, astronautic

- NATO, Belgien
- Boeing, USA
- Airbus, Hamburg
- Bund (Bundeswehr), Leer
- Bundeswehr (Technische Aufklärung), Hof
- Lufthansa, Hamburg
- DLR (Deutsches Zentrum für Luft- und Raumfahrt, Stuttgart
- Eurocontrol (Flugüberwachung), Belgien
- Australian Government Department of Defence, Australien
- EADS (European Aeronautic Defence & Space Company) GmbH, Ulm
- Institut für Luft- und Raumfahrtmedizin, Köln
- Deutscher Wetterdienst, Tauche
- Polizeipräsidium, Bonn
- Landesamt für Umweltschutz Sachsen-Anhalt, Halle
- Zentrale Polizeitechnische Dienste, NRW
- Bundesamt für Verfassungsschutz, Köln
- BEV (Bundesamt für Eich- und Vermessungswesen)

Research/Development, Science and Universitys

- Deutsches Forschungszentrum für Künstliche Intelligenz, Kaiserslautern
- Universität Freiburg
- Indonesien Institute of Sience, Indonesien
- Max-Planck-Institut für Polymerforschung, Mainz
- Los Alamos National Labratory, USA
- University of Bahrain, Bahrain
- University of Florida, USA
- Universität Erlangen, Erlangen
- Universität Hannover, Hannover
- University of Newcastle, Großbritannien
- Universität Strasbourg, Frankreich
- Universität Frankfurt, Frankfurt
- Uni München – Fakultät für Physik, Garching
- Technische Universität Hamburg, Hamburg
- Max-Planck Institut für Radioastronomie, Bad Münstereifel
- Max-Planck-Institut für Quantenoptik, Garching
- Max-Planck-Institut für Kernphysik, Heidelberg
- Max-Planck-Institut für Eisenforschung, Düsseldorf
- Forschungszentrum Karlsruhe, Karlsruhe

Industry

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- Fedex, USA
- Walt Disney, Kalifornien, USA
- Agilent Technologies Co. Ltd., China
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- IBM, Schweiz
- Audi AG, Neckarsulm
- BMW, München
- Daimler Chrysler AG, Bremen
- BASF, Ludwigshafen
- Deutsche Bahn, Berlin
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- Siemens AG, Erlangen
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- Pro Sieben – SAT 1, Unterföhring
- Channel 6, Großbritannien
- WDR, Köln
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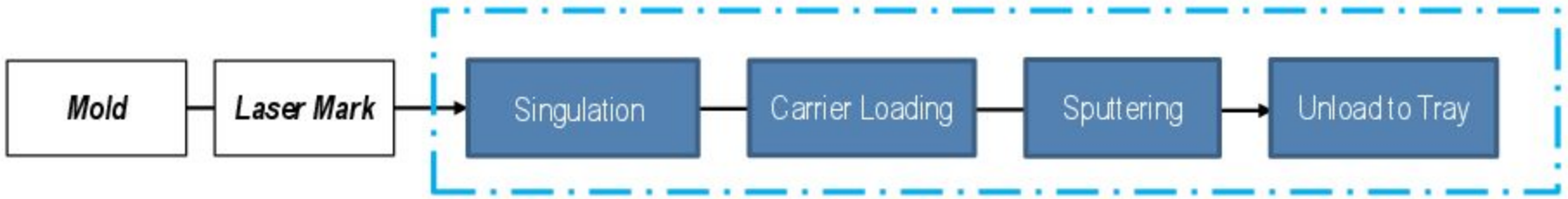
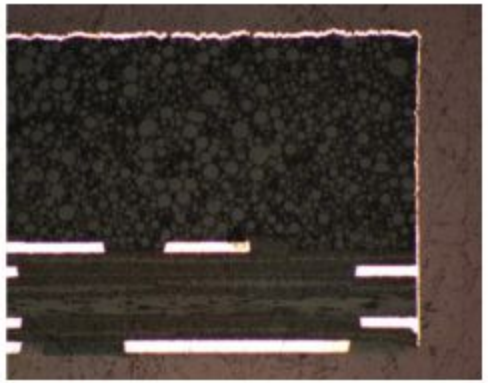
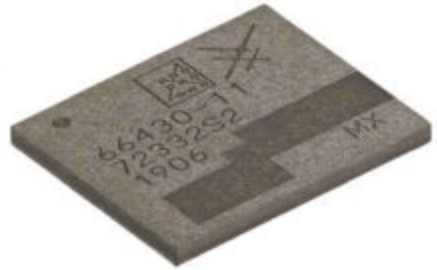
Email:mail@aaronia.de URL:www.aaronia.com

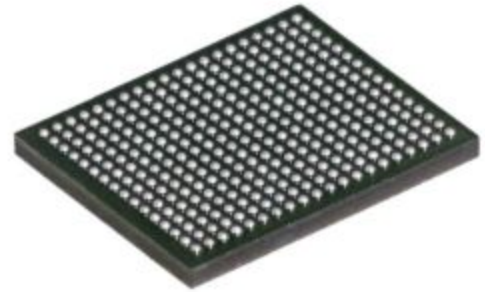
Conformal Shielding Process Flow

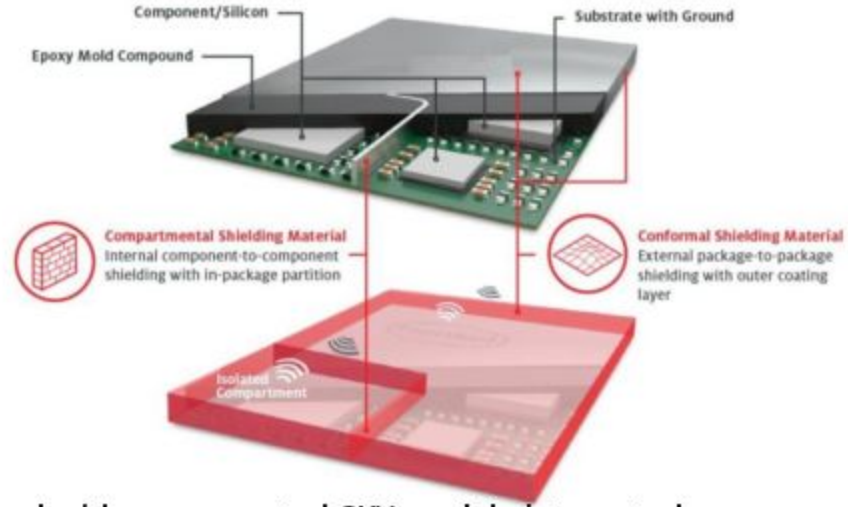


Item	Standard
Number of Coated Sides	5
Coating Process	PVD
Metal Layers (Top) Metal Layers (Side)	0.2um Ti /3um Cu /0.4um Ti 0.08um Ti /1.2um Cu /0.16um Ti
Ground Connection	Sidewall (Min. 2 PCB ground layers)

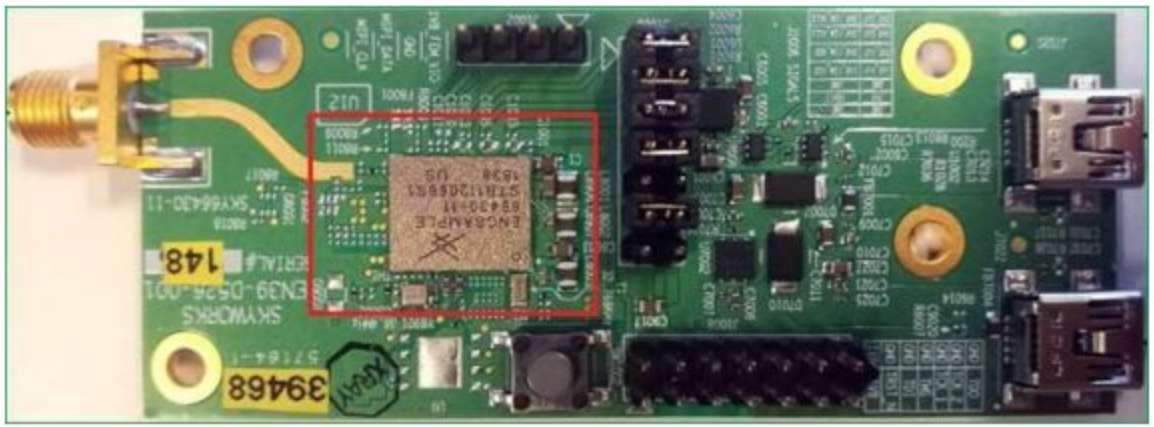








Picture 1.
Dev board with SKY module integrated
(module with conformal coating)



Comparison

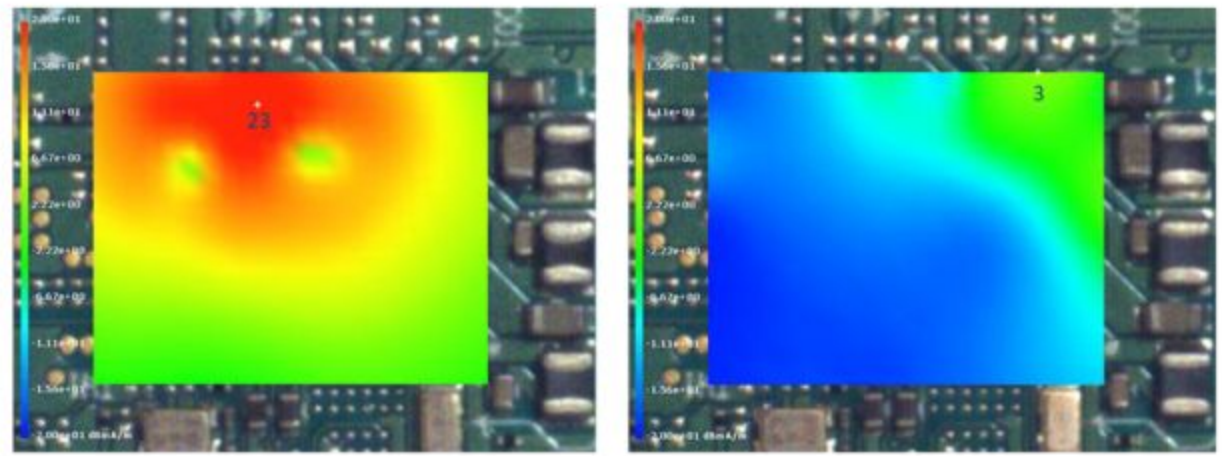
Left side,

Measures of same dev board with a non-coated SKY module integrated

Right side,

Measures of same board with a coated SKY module integrated

Without Shield **With Shield**



2fo Scan B4: 20dB difference with vs. without Shield.

Conformal Shield
Production Release

02/12/15

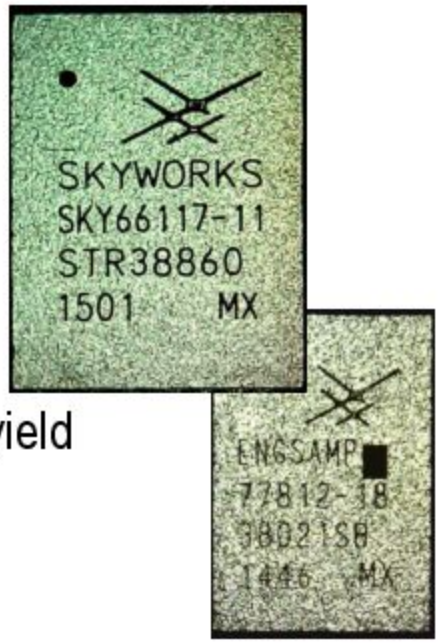
SkyShield Ultra Conformal Shield

Batch Process/Tango Solution

- **Objective**

  Develop and Qualify **an improved** package level EMI shield process in Skyworks Mexicali, to differentiate our product portfolio by enabling a conformal shield solution to maximize EMI protection by depositing a stack up of metal layers (Ti-Cu-Ti) around 5 of 6 of the sides of our MCM/SIP packages an scale it up at a high volume - lower cost model to benefit our customers by allowing the removal of system level shielding and avoiding cost retuning in the system environment

- **Target Products**: All RF products, as applicable

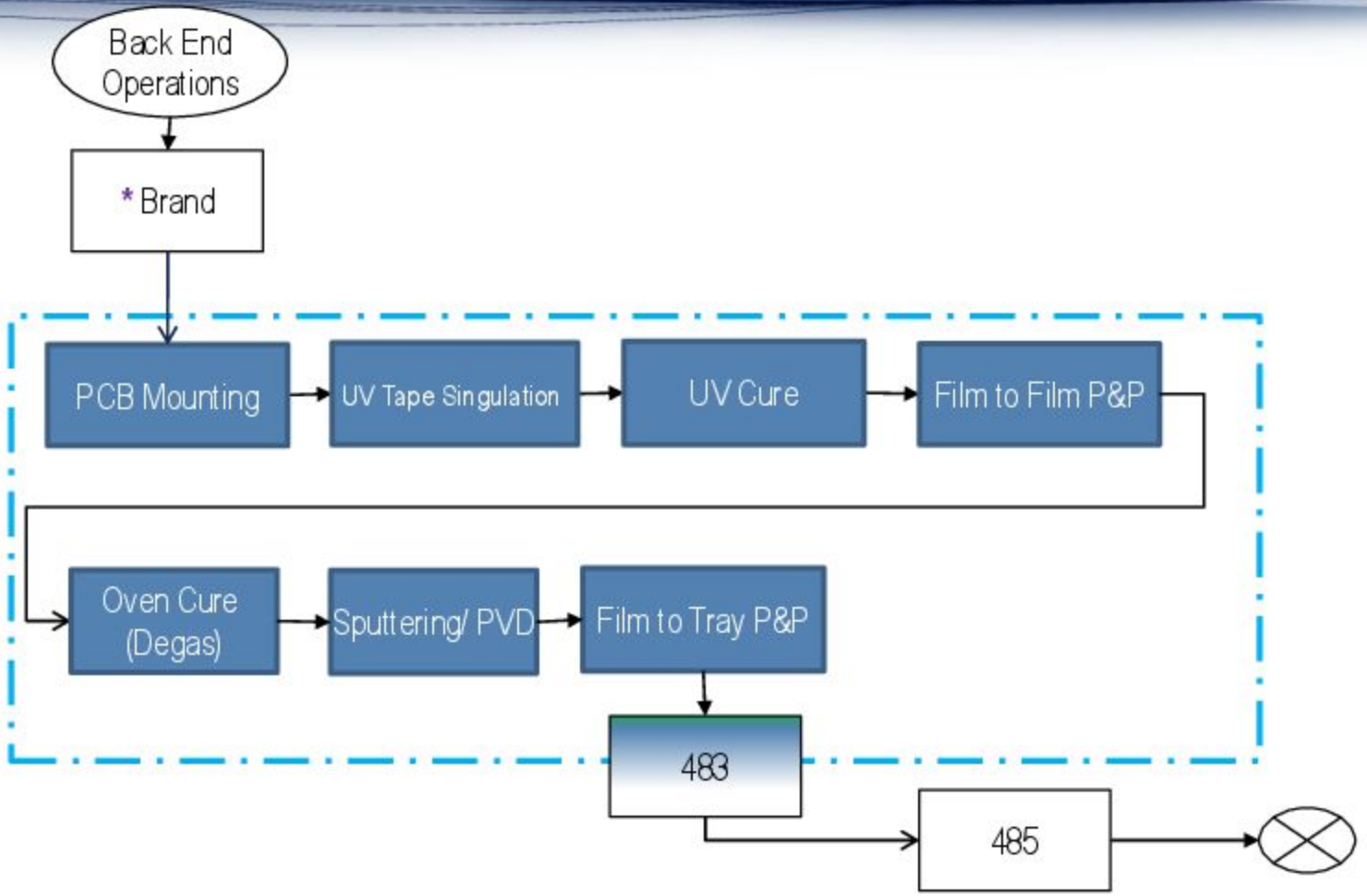


- **Approach**
  - Perform Conformal Shield Process Development
    - Characterize best manufacturing practices/methods
    - Achieve highest possible package density-design rules & yield
    - Validate package level reliability (functional and RTV)

Differences Between Wire Shielding & Conformal Shielding

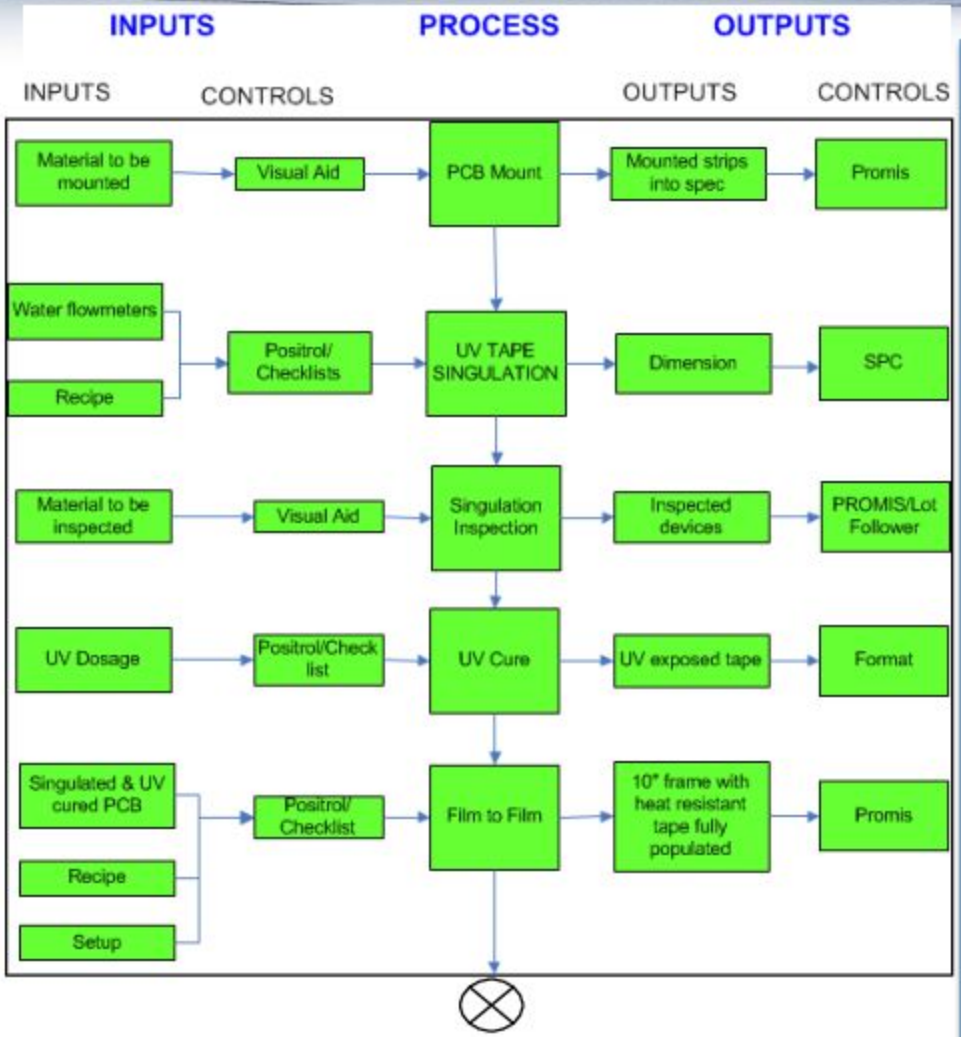
Item	Conformal Shielding _Batch Process/Tango Solution_
Number of Coated Sides	5 (Top & 4 sidewalls)
Coating Process	Sputtering
Qty of Metal Layers	3 (Ti+Cu+Ti)
Metal Layer Thickness	Top 3.4 +/- 1 um (Ti=0.2um, Cu=3um, Ti=0.2um) Side 45+/-15% of Top (1.53um)
Shielding Contact Zone	Sidewall (Cu Layer embedded on PCB)
Pictures	

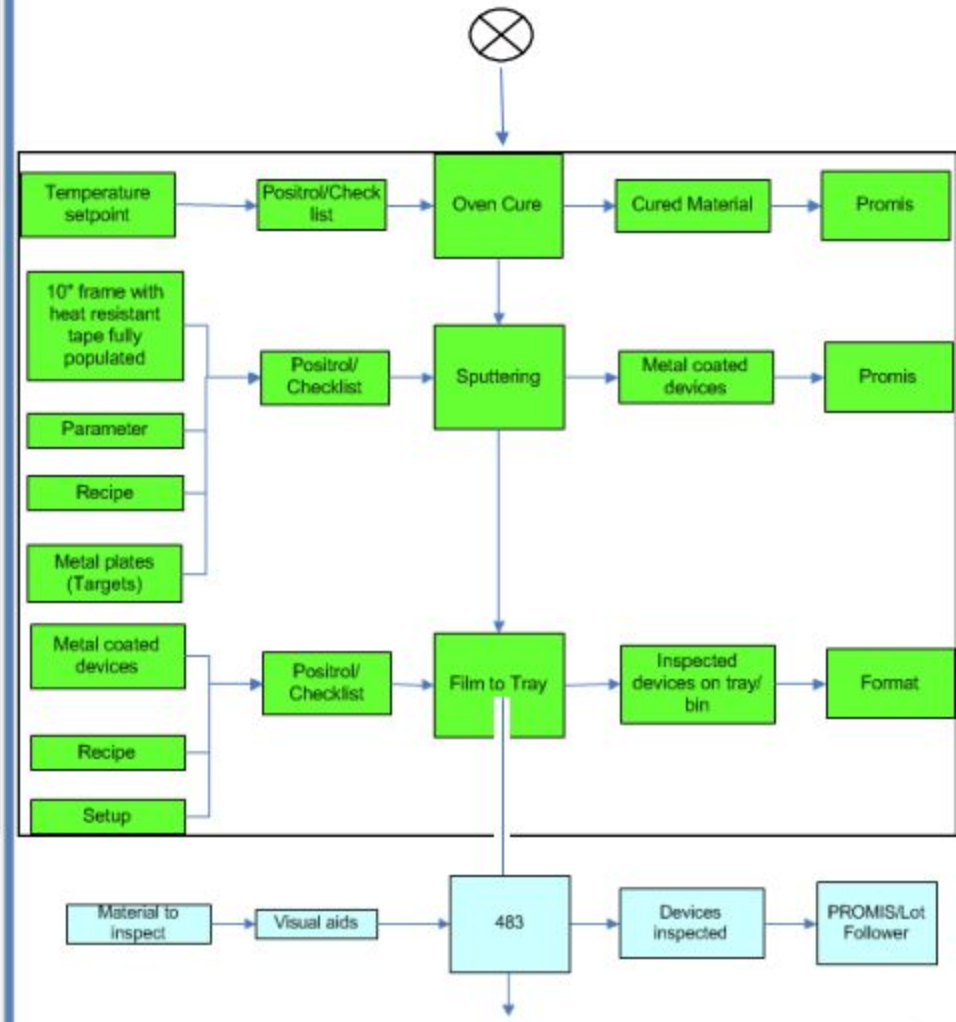
Conformal Shielding Process Flow



- ✓ *After branding, starts "Conformal shielding" process*
- ✓ *483 will be executed on 5 sides for FT2000 and topside manually inspection*
- ✓ *485 is standard QA gate of Back End operations*

Conformal Shielding Control Plan/ IPO





Pilot Release Success Criteria

Step	Critical Process Output	Success Criteria	Sample Size	Result
PCB Mounting	Mounting Quality	According to MXVA-3827	30 STR (10 PCB, each)	PASS
	PCB Breakage/ Damage	Not allowed	30 STR (10 PCB, each)	PASS
	Yield	100%	30 STR (10 PCB, each)	PASS
UV Tape Singulation	Dimension	Pkg size +/- 125 um	10 STR (50 meas, each)	PASS
	X, Y Offset	+/- 50 um	10 STR (50 meas, each)	PASS
	Incomplete Cut	Not allowed	30 STR (10 PCB, each)	PASS
	PCB Breakage/ Damage	Not allowed	30 STR (10 PCB, each)	PASS
UV Cure	UV Dosage	400mJ/ cm2 +/- 20%	5 PCB (19 units, each)	PASS
	Pick up force	< 200gr/cm2	5 lots (5 PCB, each)	PASS
Film to Film	Device breakage/ damage	< 1%	20+ STR (20 PCB, each)	PASS
	Inspected devices	GR& R < 10%	3 Golden units, 10 times	PASS
	Separation between devices	1mm +/- 200um	14 Frames (10 Units, each)	PASS
Sputtering/ PVD	Metal layer adhesion	No peeling off allowed	70+ STR (4 units, each)	PASS
	Metal layer thickness (Top)	0.2umTi +3um Cu +0.2 um Ti	10 lots (5 units, each)	PASS
	Metal layer thickness (Sidewall)	45 +/- 15% of Top	20 lots (5 units, each)	PASS
Film to Tray	Shielding damage	< 1%	20+ STR (20 PCB, each)	PASS
	Inspected devices	GR& R < 10%	270 Data	PASS

Sputtering Results

Scratch test

SKY778xx

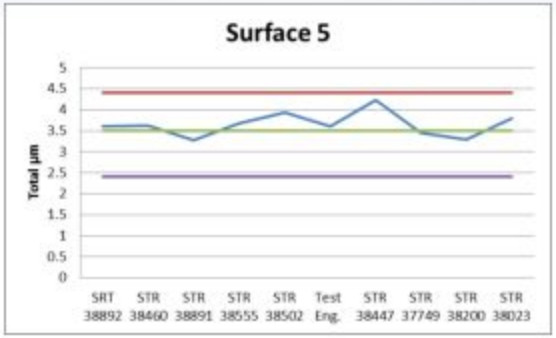
SKY773xx

+70 STR were scratch tested with good results

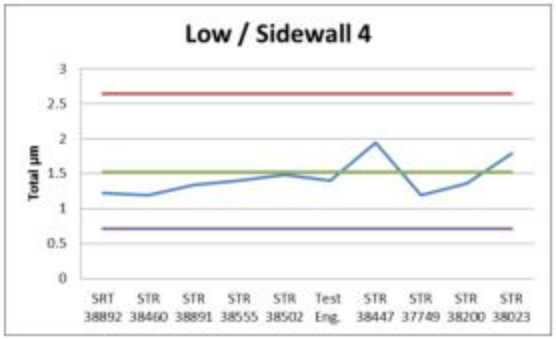
Sputtering Results

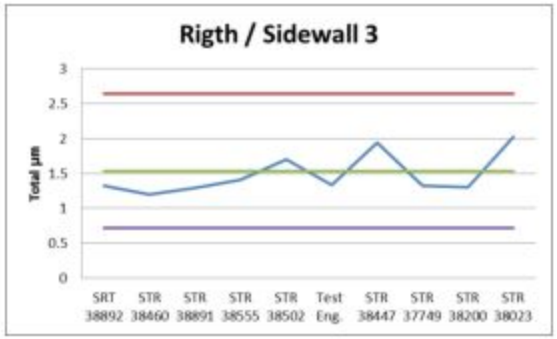
Metal layer thickness (3um recipe)

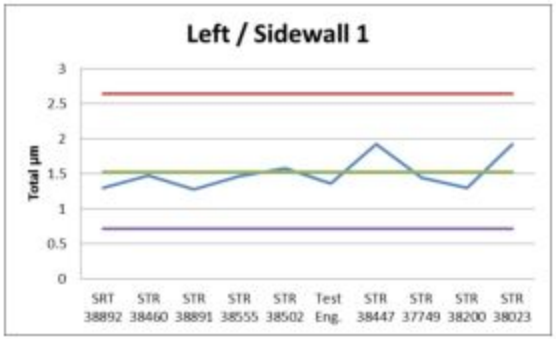
STR	Device Side	Ti 1	Cu 2	Ti 3	Total Thickness µm.	Sidewall/Surface
SRT 38892	Left / Sidewall 1	0.097	1.108	0.092	1.297	36%
3 µm	Top/ Sidewall 2	0.112	1.074	0.059	1.245	35%
	Rigth / Sidewall 3	0.103	1.142	0.075	1.32	37%
	Low/ Sidewall 4	0.1	1.079	0.051	1.23	34%
	Surface 5	0.122	3.123	0.356	3.601	
STR 38460	Left / Sidewall 1	0.109	1.291	0.078	1.478	41%
3 µm	Top/ Sidewall 2	0.108	1.22	0.076	1.404	39%
	Rigth / Sidewall 3	0.1	1.048	0.054	1.202	33%
	Low/ Sidewall 4	0.078	1.047	0.068	1.193	33%
	Surface 5	0.174	3.248	0.208	3.63	
STR 38891	Left / Sidewall 1	0.097	1.08	0.099	1.276	39%
3 µm	Top/ Sidewall 2	0.102	1.207	0.107	1.416	43%
	Rigth / Sidewall 3	0.103	1.093	0.097	1.293	39%
	Low/ Sidewall 4	0.104	1.142	0.09	1.336	41%
	Surface 5	0.176	2.864	0.235	3.275	
STR 38555	Left / Sidewall 1	0.107	1.28	0.077	1.464	40%
3 µm	Top/ Sidewall 2	0.104	1.281	0.083	1.468	40%
	Rigth / Sidewall 3	0.109	1.216	0.078	1.403	38%
	Low/ Sidewall 4	0.109	1.216	0.078	1.403	38%
	Surface 5	0.17	3.249	0.255	3.674	
STR 38502	Left / Sidewall 1	0.184	1.149	0.242	1.575	40%
3 µm	Top/ Sidewall 2	0.191	1.589	0.165	1.945	49%
	Rigth / Sidewall 3	0.166	1.353	0.186	1.705	43%
	Low/ Sidewall 4	0.191	1.05	0.249	1.49	38%
	Surface 5	0.431	3.099	0.409	3.939	
Test Eng.	Left / Sidewall 1	0.107	1.171	0.079	1.357	38%
3 µm	Top/ Sidewall 2	0.102	1.122	0.078	1.302	36%
	Rigth / Sidewall 3	0.096	1.145	0.091	1.332	37%
	Low/ Sidewall 4	0.104	1.226	0.074	1.404	39%
	Surface 5	0.155	3.222	0.224	3.601	
STR 38447	Left / Sidewall 1	0.181	1.579	0.162	1.922	45%
3 µm	Top/ Sidewall 2	0.204	1.533	0.203	1.94	46%
	Rigth / Sidewall 3	0.189	1.556	0.2	1.945	46%
	Low/ Sidewall 4	0.224	1.478	0.241	1.943	46%
	Surface 5	0.404	3.385	0.44	4.229	
STR 37749	Left / Sidewall 1	0.105	1.234	0.101	1.44	42%
3 µm	Top/ Sidewall 2	0.116	1.299	0.093	1.508	44%
	Rigth / Sidewall 3	0.102	1.127	0.094	1.323	38%
	Low/ Sidewall 4	0.09	1.021	0.084	1.195	35%
	Surface 5	0.187	3.086	0.183	3.456	
STR 38200	Left / Sidewall 1	0.108	1.115	0.079	1.302	39%
3 µm	Top/ Sidewall 2	0.096	1.026	0.086	1.208	37%
	Rigth / Sidewall 3	0.116	1.127	0.064	1.307	40%
	Low/ Sidewall 4	0.109	1.162	0.093	1.364	41%
	Surface 5	0.176	2.943	0.181	3.3	
STR 38023	Left / Sidewall 1	0.103	1.714	0.11	1.927	51%
3 µm	Top/ Sidewall 2	0.108	1.22	0.076	1.404	37%
	Rigth / Sidewall 3	0.106	1.792	0.124	2.022	53%
	Low/ Sidewall 4	0.099	1.582	0.107	1.788	47%
	Surface 5	0.151	3.325	0.314	3.79	

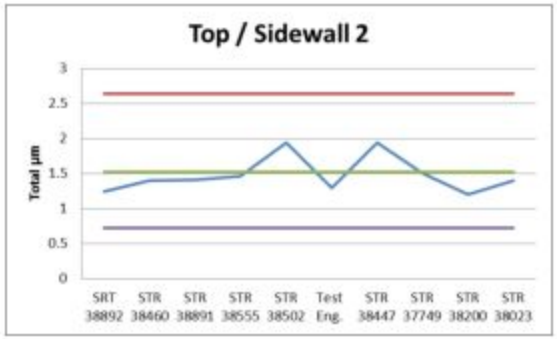


- **Production metal thickness measured by XRF technique**
  - 5 units/lot
  - Units measured top and sides
  - Specification
    - Top 3.4 +/- 1um
    - Side: 45 +/- 15 % of Top







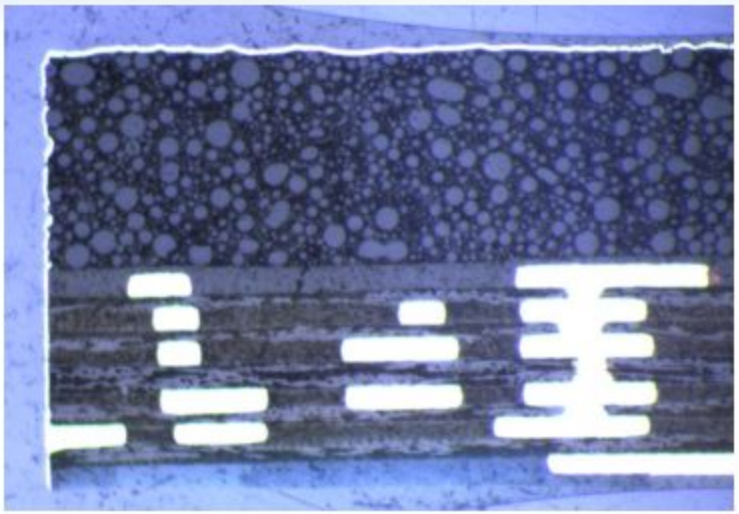


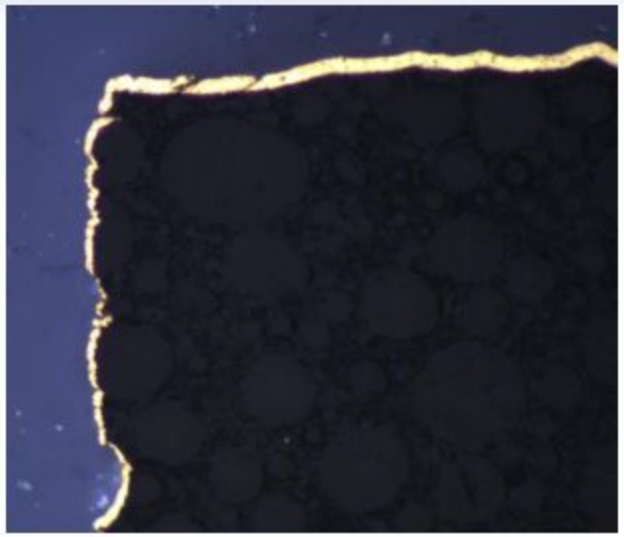
Sidewall coverage 45 +/- 15% of Top coverage

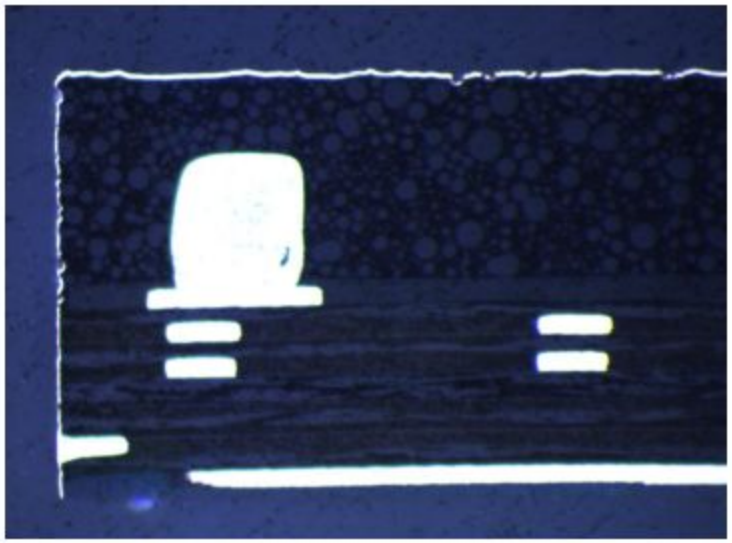
Sputtering Results (Continue)

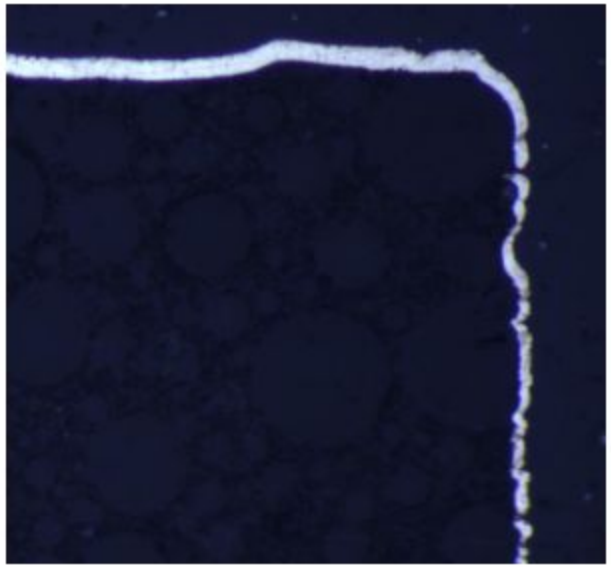
Target:
Top: 3.4 ±1um
Side: 45 +/- 15 % of Top

Average Measured Data (Cross Section)
Top: 3.64um
Side: 1.47um





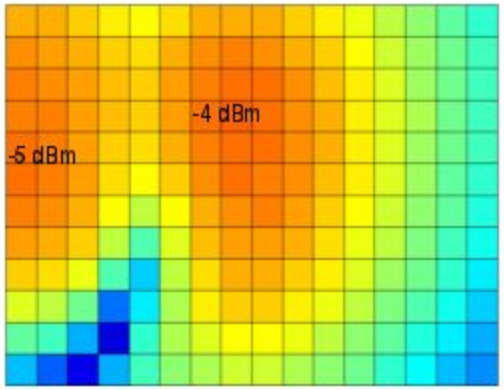




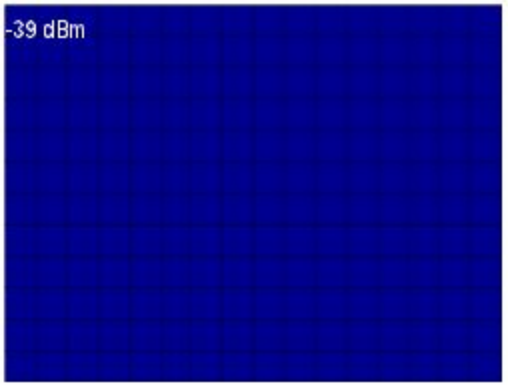
Supporting EMI measurements and Reliability Data

EMI Comparison of Different Shield Method

77608



No Shield



SkyShield Ultra

#	Shield Type	EMI Attenuation
1	Without Shield	-4 dBm
2	SkyShield Ultra	-39 dBm

Package Qualification Report

Report No: Qual-QP-14-01722

SKYWORKS

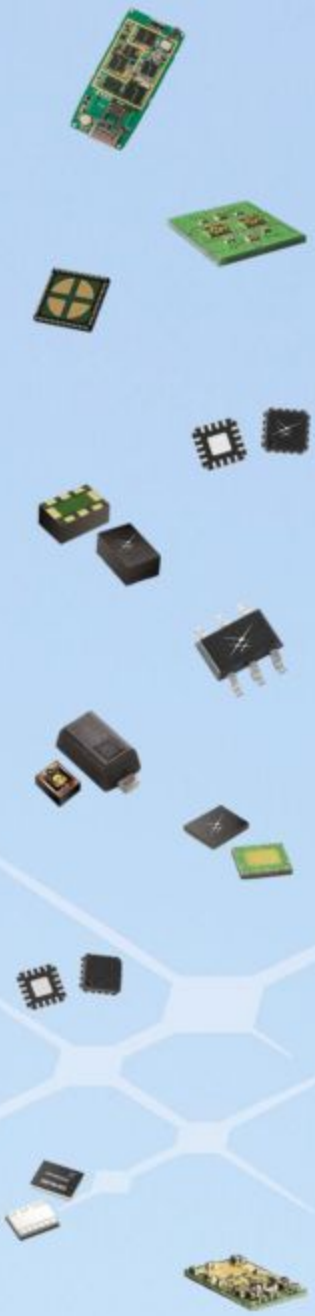
Reliability:

Technology: SKYSHIEL Ultra-Conformal Shielding coating on MCM at Mexicali
Test Vehicle: SKY65746-14
Package Type: 1.6X2.0, 6 Terminals.

Test [1]	Qty	Endpoints (ATE)	Accept Criteria	Results
Acoustic Imaging (J-STD-035)	11 x 4 lots (from preconditioning)	Pre- and Post-preconditioning	0 Fail / 11 (criteria per SQ03-0024)	Pass
Preconditioning [2] MSL1-260ºC (JESD22-A113)	240 x 4 lots	Bake 125C 24 Hours Moisture Soak 3x Reflow ATE electrical test Visual inspection	0 Fail / 240 No peeling	Pass
Temperature Cycling -65 ºC to +150 ºC (JESD22-A104)	77 x 4 lots (from preconditioning)	PASS	0 Fail / 77 No peeling	Pass
HAST 130 ºC, 85 %RH, 33 PSIA, bias (JESD22-A110)	77 x 4 lots (from preconditioning)	96 hours ATE electrical test Visual inspection	0 Fail / 77 No peeling	EV1: 10 fails[3] QL1: 2 fails[4] QL2: 0 fail QL3: 1 fail[5]
High Temp Storage 150 ºC (JESD22-A103)	77 x 2 lots QL1 & QL2 (without preconditioning)	1000 hours ATE electrical test Visual inspection	0 Fail / 77 No peeling	Pass

[1] All stress tests are performed by the procedures referenced in SQ03-0025.
[2] Preconditioning is required before TC, HAST, and HTS stresses.
3 FA58751: 10 fail due to Iqc/VCC_leak. FA showed moisture ingression around MIM cap, and other area of LNA die (MG8006-X1, Win Semi PD25). Many units are recovered after decap. X-ray /CSAM shows no anomaly. This failure is not related with Skyshield Ultra (conformal coating) process qualification.
4 FA58752: 2 fail due to Iqc/VCC_leak. This is same reason as item 3.
5 FA58754: 1 fails due to Iqc/VCC_leak. This is same reason as item 3.

✓ *SKY66107-11 Data shows there is issue on "Conformal shielding". Pending to receive official report*



BREAKTHROUGH SIMPLICITY

SKYWORKS™

Package Qualification Report

Technology: 3µm Skyshield Ultra – Conformal coating process on MCM at MxI

Test Vehicles: SKY66105-11, SKY66107-11

Package Type: 6x8mm MCM, 7.6x9.6mm MCM

Report No: Qual-QR-14-01970

Qualification Team

Requestor: Wayne Nguyen

Package Engineer: Tony LoBianco

Product/Package Reliability: Rebecca Luk

Prepared by: Edward Yoon

Skyworks Solutions, Inc.

Product & Package Reliability

20 Sylvan Rd. Woburn, MA 01801

REVISION HISTORY			
Rev	**Description of Change**	**Author**	**Submit Date**
1	Initial Release	Edward Yoon	2-27-2015

Table of Contents

1 Summary

This document summarizes the package qualification requirements and result for 3µm Cu coating thickness of conformal coating process (Skyshield Ultra) on MCM at Mexicali assembly line. 7µm coating thickness of conformal coating process has already been qualified (QUAL-QR-14-01722), and the scope of this qualification is for reduction on Cu thickness using same coating process.

Coating

	Current	New
Coating Equipment	Tango Onyx 350mm	Tango Onyx 350mm
1st layer (Ti)	4000 Å	4000 Å
2nd layer (Cu)	7 µm	3 µm
3rd layer (Ti)	4000 Å	4000 Å
Minimum total thickness	6.0µm Top 2.0um Side	2.5µm Top 1.0µm Side

EMI performance has been verified on various coating thickness on SKY66105 and SKY77357, and equivalent EMI performance was observed on 3µm and 7µm coating thickness.

One of key failure mechanism is peeling of coating material post stress, and this will degrade EMI performance. Scratch/Peel test has been carried out to check adhesion of coating material post stresses.

All reliability have been completed and passed. 3µm conformal coating (Skyshield Ultra) process on MCM at Mexicali meets Skyworks' reliability requirements for production and is rated at JEDEC MSL3 – 260C for moisture sensitivity.

2 Reference Documents

2.1 Skyworks Documents

SQ02-0013	Qualification Standard
SQ03-0023	Wafer Process Qualification Requirements
SQ03-0024	Package and Assembly Qualification Requirements
SQ03-0025	Product Qualification Requirements

2.2 Other Supporting Documents

JESD22	JEDEC Standard Test Methods
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
MIL-STD-883	Department of Defense Test Method Standard, Microcircuits

3 Product Description and Information

3.1 Reliability File Number: 320345

3.2 Product Information

Test Vehicle: SKY66107-11
Product Function/Frequency: 100 mW ZigBee® Solution in Package

3.3 Die Information

	Mask Info		Wafer Fabrication Information			Die Attach
Die	Qty	Mask	Company	Location	Process	Material
EM358 (TMDP73B)	1	SiLabs	TSMC	Camas, WA	0.18 embedded flash	1290WB
Cedar 3.3	1	405C01	IBM	Burlington	5PAE	1290WB
Gatineau 2.0	1	450A01	IBM	Burlington	7RF	1290WB

3.4 Assembly and Package Information

Package Supplier: Skyworks, Mexicali
Package Family & Name: 7x9 Skyshield Ultra MCM, 62 Terminals + center ground
Package Body Dimensions : 7.0 mm x 9.0 mm x 0.95 mm
Substrate Technology: TW72-D396-001 (4L PPG SSV-EO MCM(60))

3.5 Material Information and Selected Dimensions

PCB or Lead Plating Material: NiPdAu (ENEPIG)
Bond Wire Size & Material: 20um Cu
Mold Compound: Nitto GE-100-LFCSK
Branding method: Laser

4 Product Description and Information

4.1 Reliability File Number: 321023

4.2 Product Information

Test Vehicle: SKY66105-11
Product Function/Frequency: 902 to 931 MHz High-Power RF Front-End Module

4.3 Die Information

	Mask Info		Wafer Fabrication Information			Die Attach
Die	Qty	Mask	Company	Location	Process	Material
U1: 449A01	1	FNW-00375	IBM	Vermont	5PAE	1290WB
U2: 02B	1	MK5022C	TowerJazz	Newport Beach	CS18Q1	1290WB

4.4 Assembly and Package Information

Package Supplier: Skyworks, Mexicali
Package Family & Name: 6x8 MCM, Skyshield Ultra, 13 terminals
Package Body Dimensions : 6.0 mm x 8.0 mm x 1.05 mm
Substrate Technology: TW61-D174-004 (4L PPG TEV MCM(150))

4.5 Material Information and Selected Dimensions

PCB or Lead Plating Material: NiPdAu (ENEPIG)
Bond Wire Size & Material: 30um Au
Mold Compound: Sumitomo EME G770HF
Branding method: Laser

5 Package/Assembly Reliability Testing Requirements

General Information

Total sample requirements (#parts x # lots):	300 x 2 lots
Part Number:	QL1: SKY66107-11 QL2: SKY66105-11
Package:	7x9mm, 6x8mm MCM

5.1 Manufacturability Requirements for Qualification

Test [1]	Qty	Accept Criteria [2]	Results
Process Yield (Coating process)	All	Equal or better than 7um coating process	Pass
Physical dimension (JESD22-B100)	10 units x2 lots	Per physical specification, Cpk > 1.66	Pass
Solderability (JESD22-B102)	5 units x 2 lots	Test and criteria per JESD22-B102 0 Fail	Pass
Coating thickness	10 units x 2 lots	**Min 2µm for top Min 1µm for side**	Pass
Scratch test	10 units x 2 lots	Visual inspection 0 fail	Pass
Scratch test post stress (TC & HAST)	10 units x 2 lots	Visual inspection 0 fail	Pass

[1] Electrical reject devices may be used for manufacturability testing when no electrical endpoint measurements are required. All stress tests are performed by the procedures referenced in SQ03-0024.

[2] In the event of sample failure, the cause of failure will be investigated.

5.2 Package/Assembly Reliability Requirements for Qualification

Test [1]	Qty	Endpoints (ATE)	Accept Criteria	Results
Acoustic Imaging (J-STD-035)	11 x 2 lots (from preconditioning)	Pre- and Post-preconditioning	0 Fail / 11 (criteria per SQ03-0024)	QL1: Pass QL2: Pass
Preconditioning [2] MSL3-260°C (JESD22-A113)	160 x 2 lots	Bake 125C 24 Hours Moisture Soak 3x Reflow ATE electrical test	0 Fail / 160	QL1: Pass QL2: Pass
Temperature Cycling -65 °C to +150 °C (JESD22-A104)	77 x 2 lots (from preconditioning)	500 cycles (condition C) ATE electrical test	0 Fail / 77	QL1: Pass [3] QL2: Pass
HAST 130 °C, 85 %RH, 33 PSIA, max operating DC bias (JESD22-A110)	77 x 2 lots (from preconditioning)	96 hours ATE electrical test	0 Fail / 77	QL1: Pass QL2: Pass

[1] All stress tests are performed by the procedures referenced in SQ03-0025.

[2] Preconditioning is required before TC, HAST, and HTS stresses.

[3] FA 60663: 8 fails due to high sleep current issue. Decap showed lifted bond at stich bond due to die attach epoxy delamination. CAR has been issued to Mexicali factory (MS-CAR-3405). As corrective action DAF process for SiLab die has been implemented. This failure is removal for 3 µm conformal coating thickness qualification for Skyshield process.