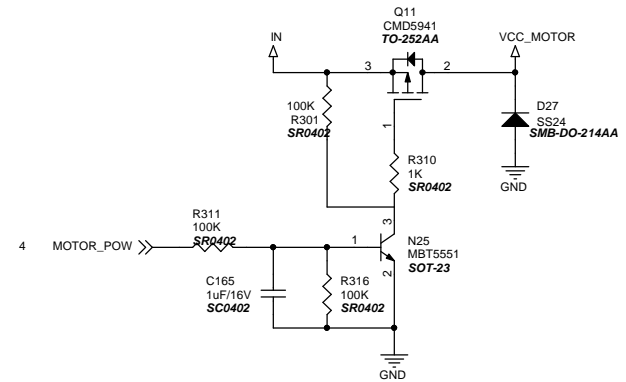
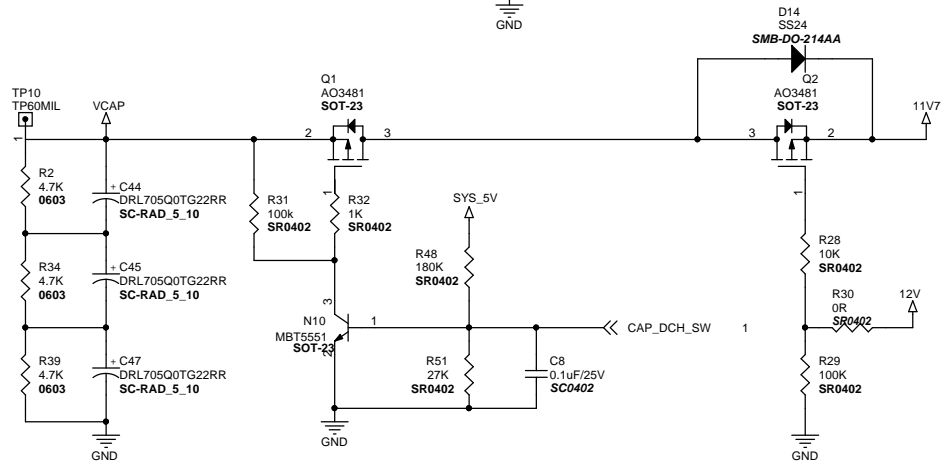
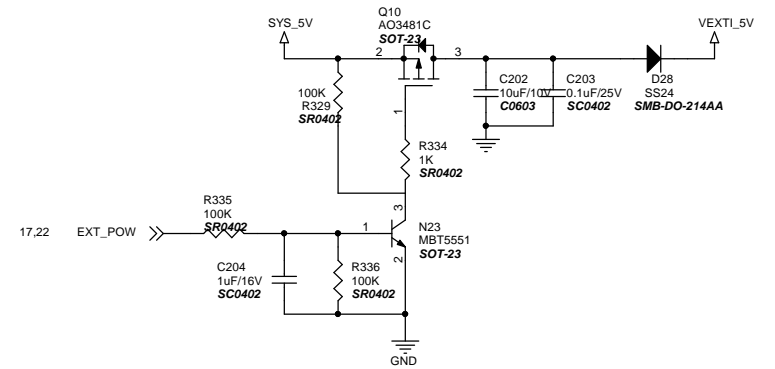
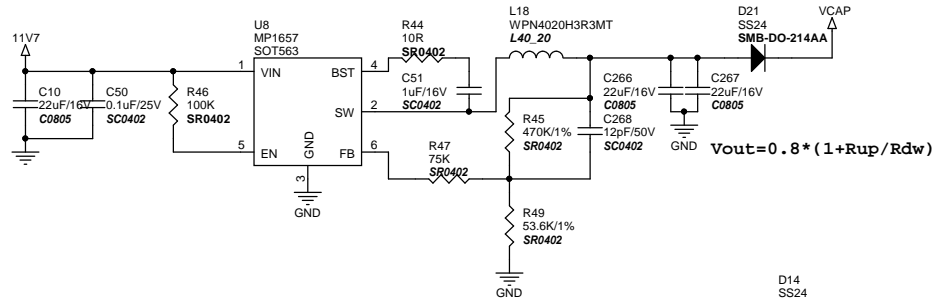
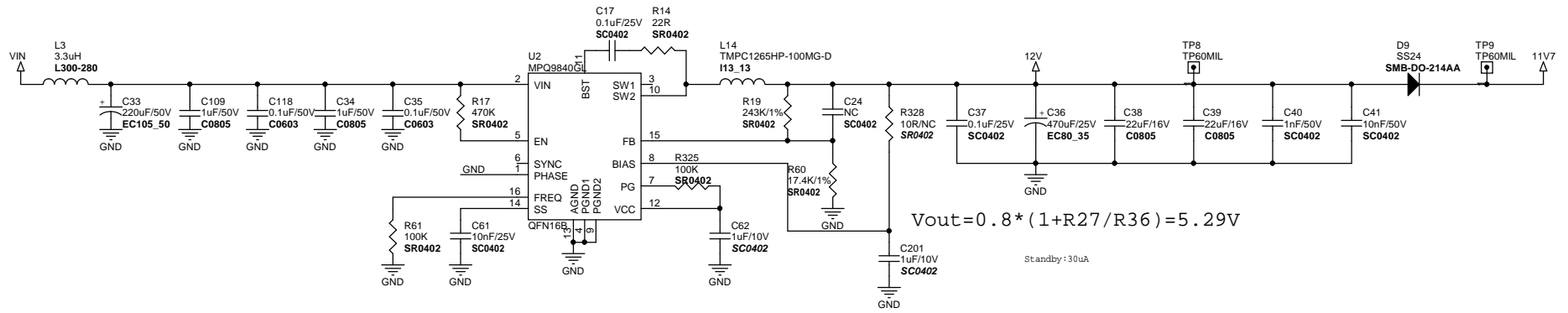
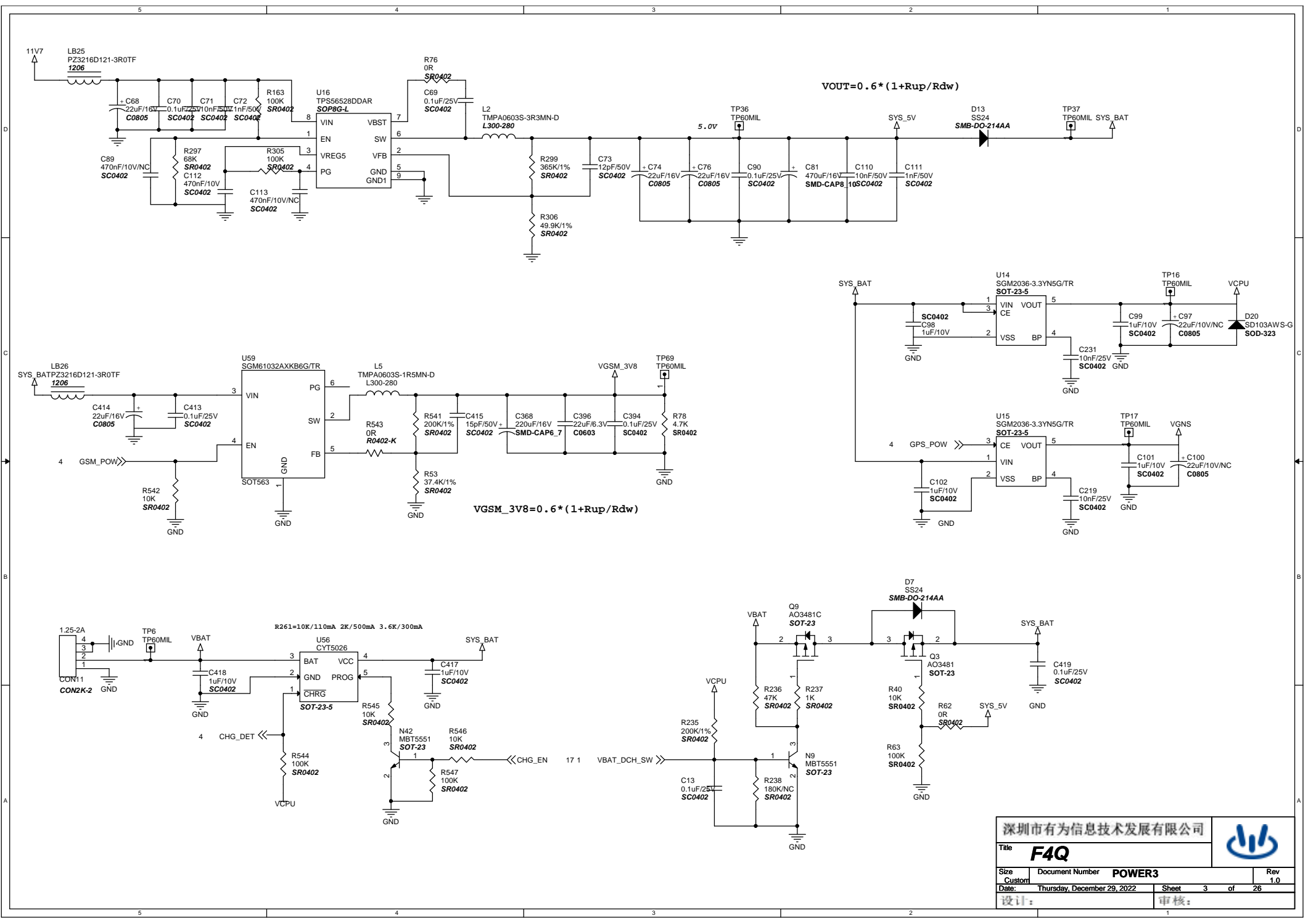


共模电感底下要净空, 不能覆铜, 不能走线

增大电容容量, 应对传导低频

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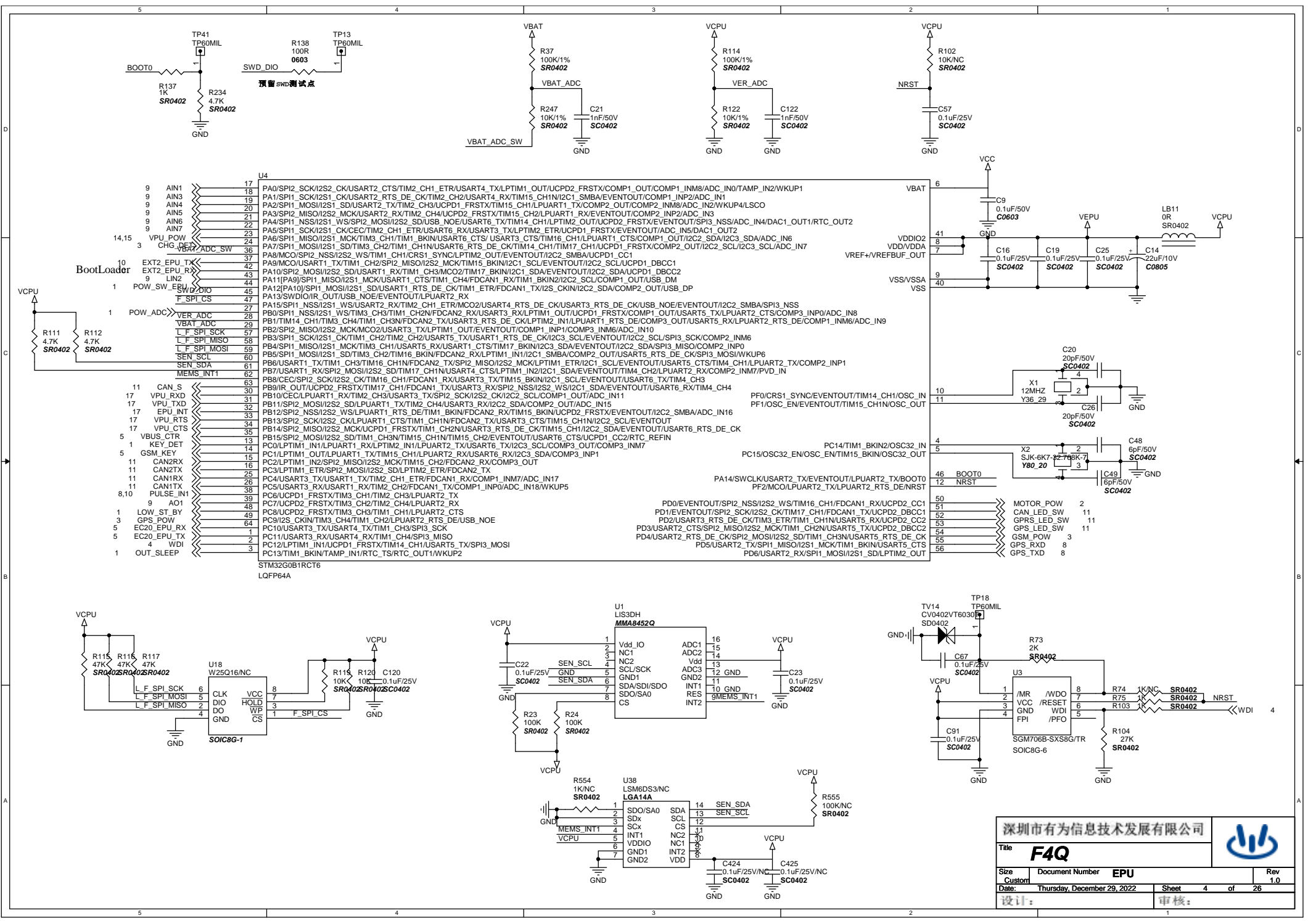





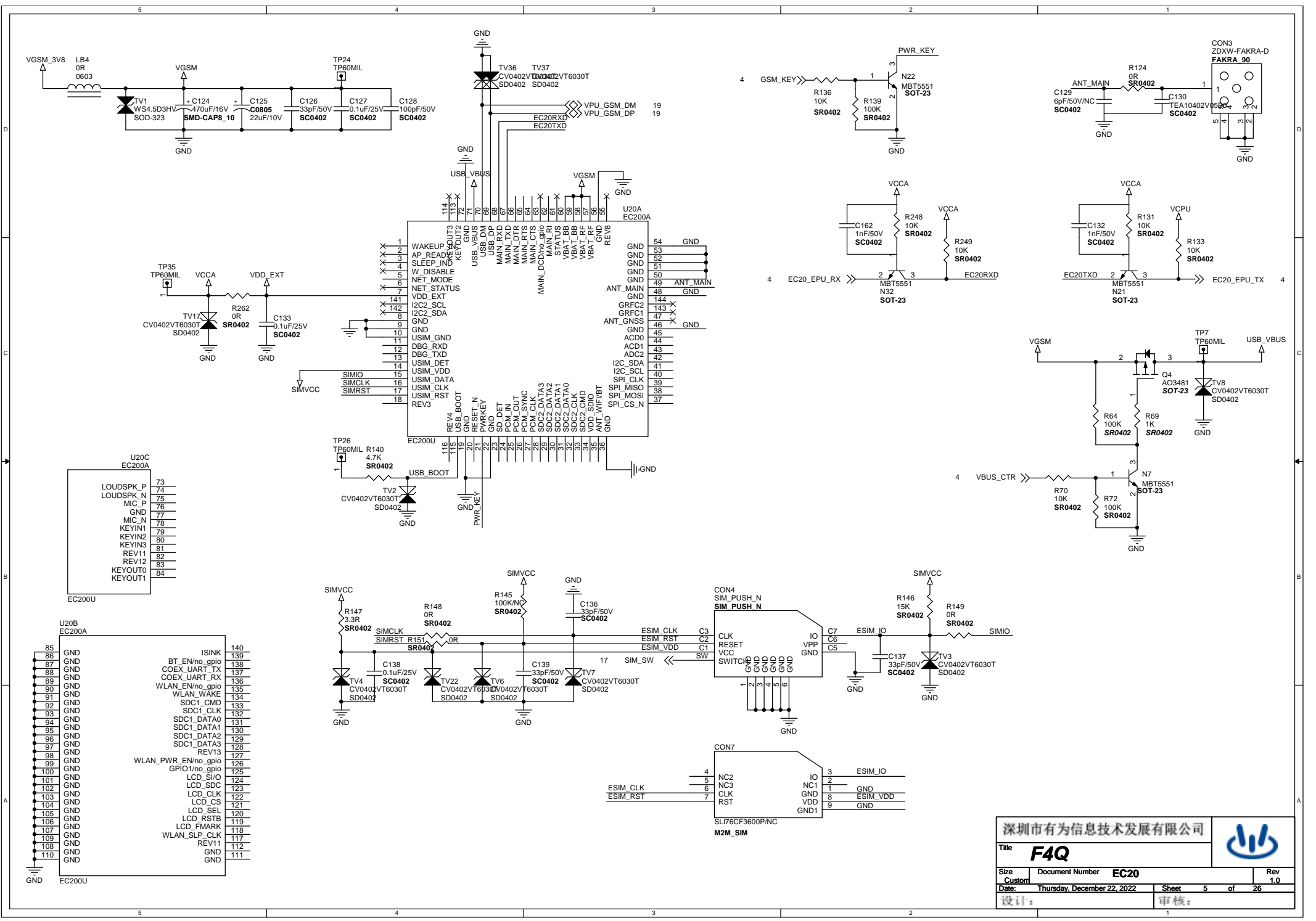
$$VOUT = 0.6 * (1 + R_{up} / R_{dw})$$

$$V_{GSM_3V8} = 0.6 * (1 + R_{up} / R_{dw})$$

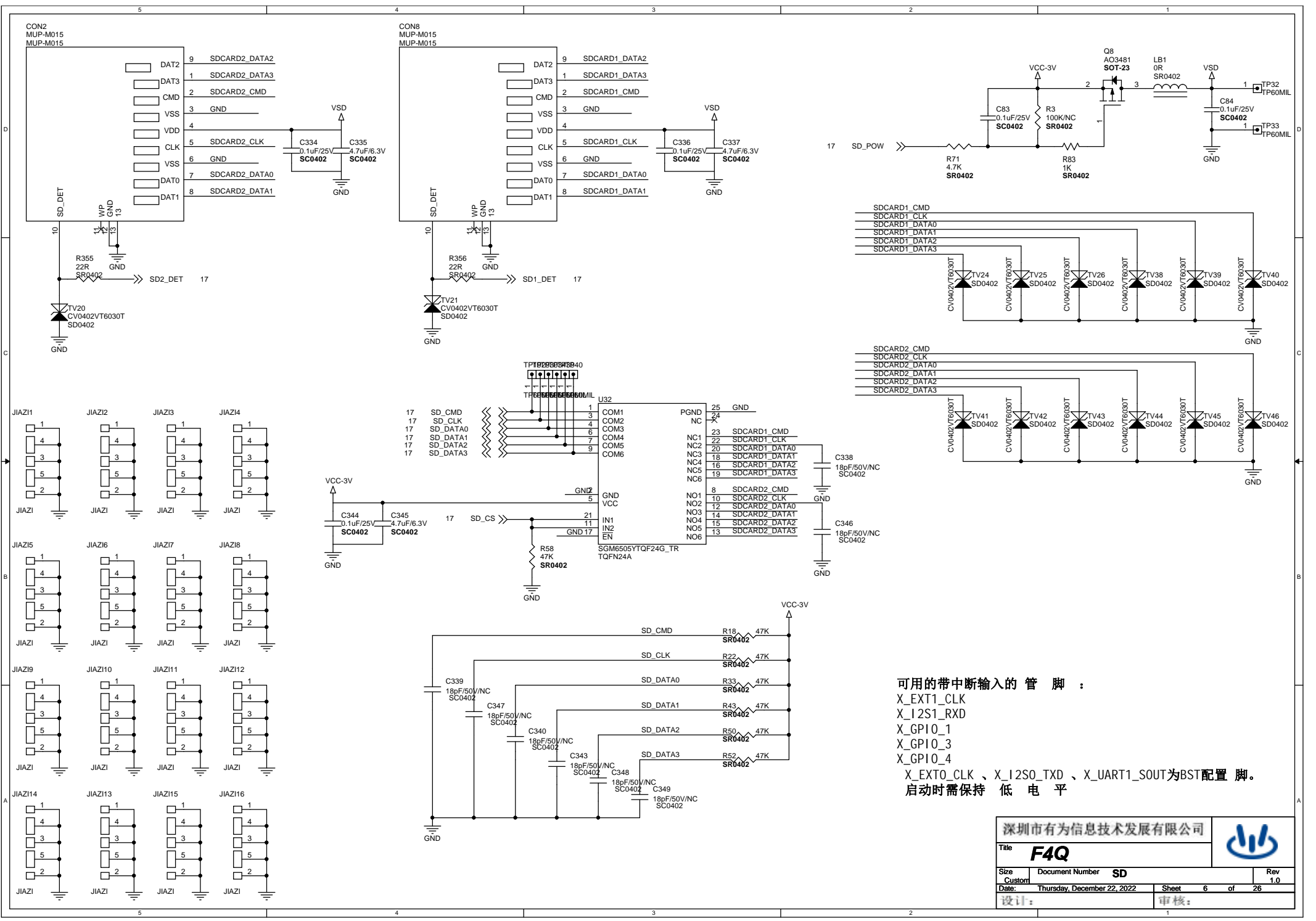
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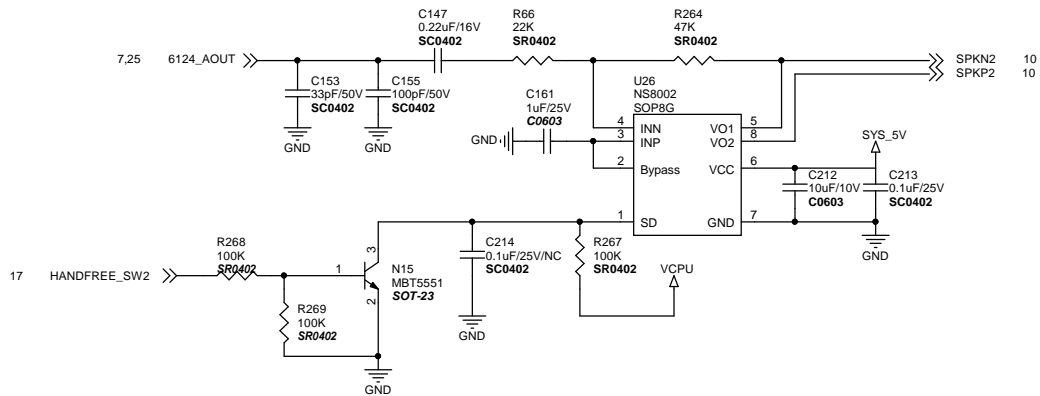
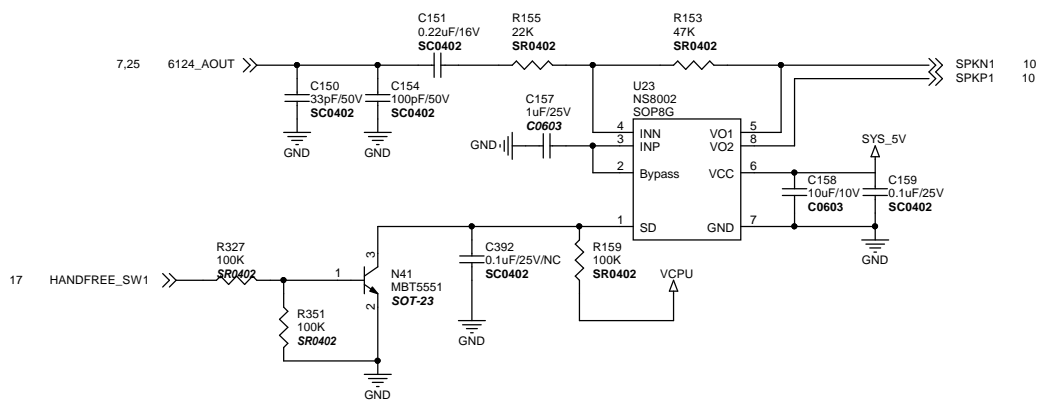
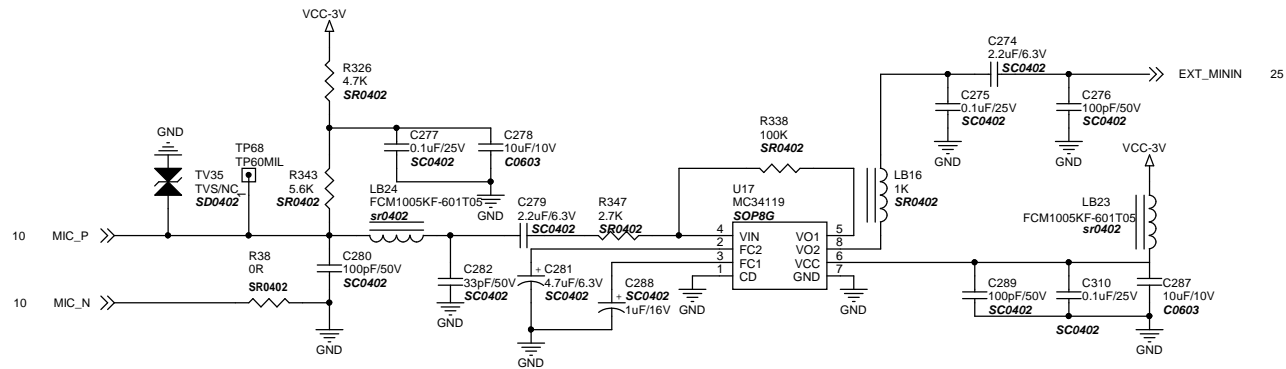


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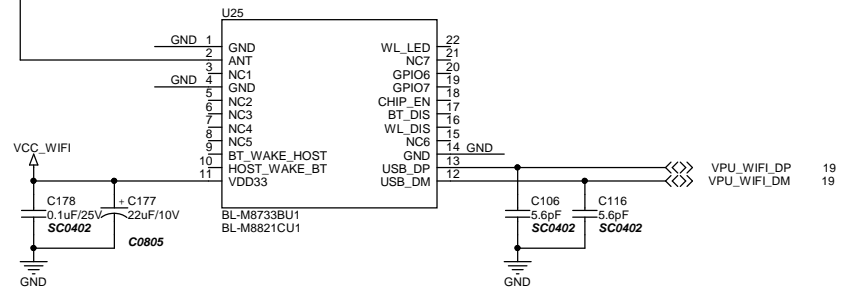
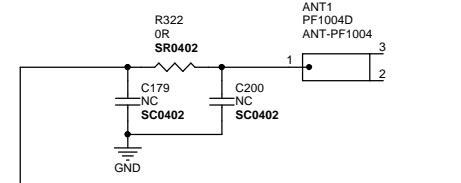
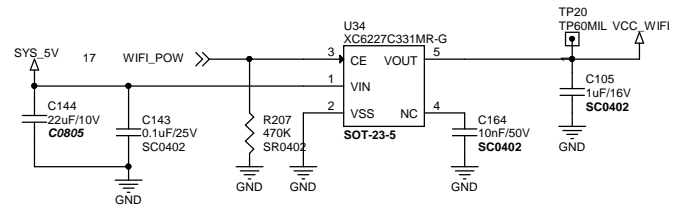
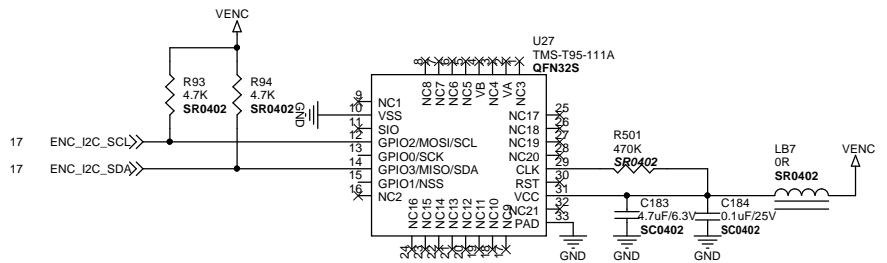
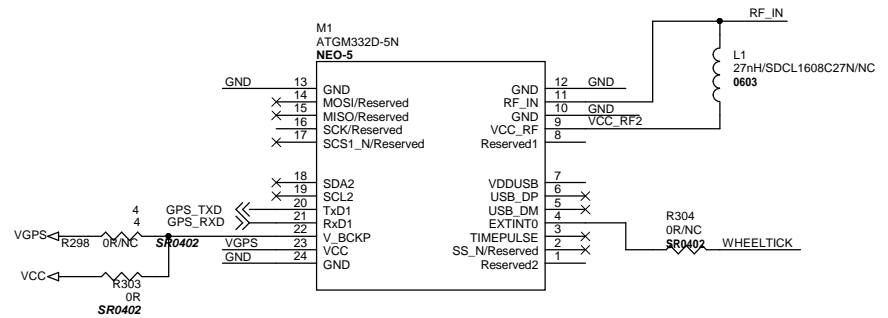
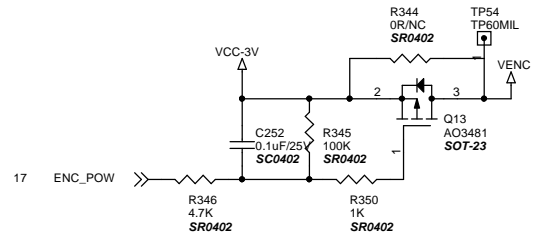
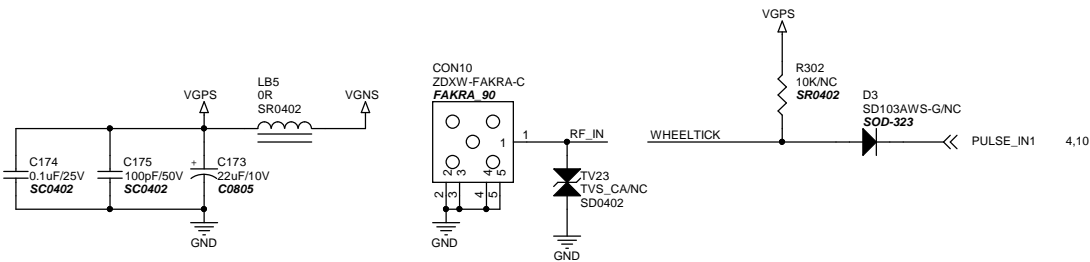


可用的带中断输入的 管脚：
 X_EXT1_CLK
 X_I2S1_RXD
 X_GPIO_1
 X_GPIO_3
 X_GPIO_4
 X_EXT0_CLK、X_I2S0_TXD、X_UART1_SOUT为BST配置脚。
 启动时需保持 低 电平

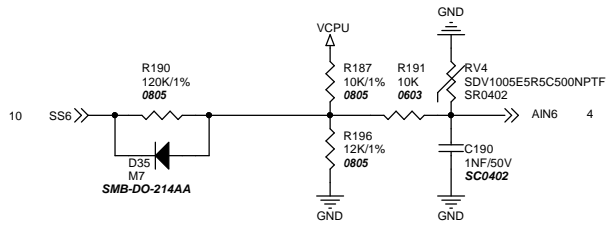
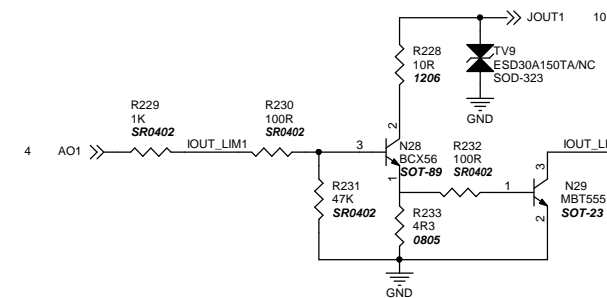
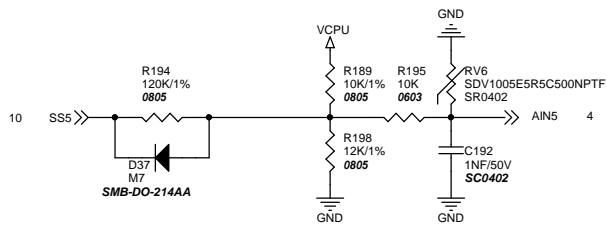
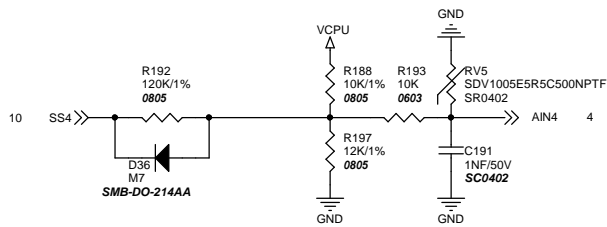
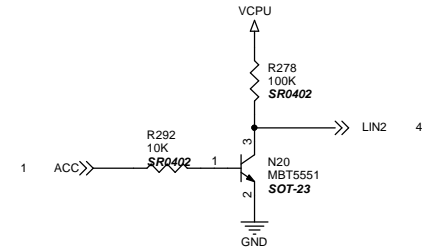
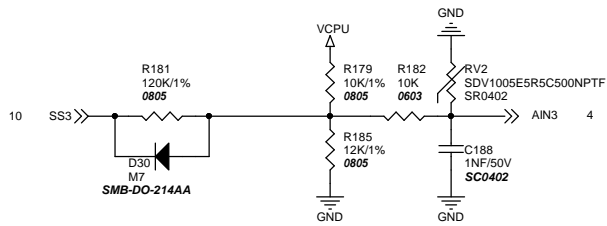
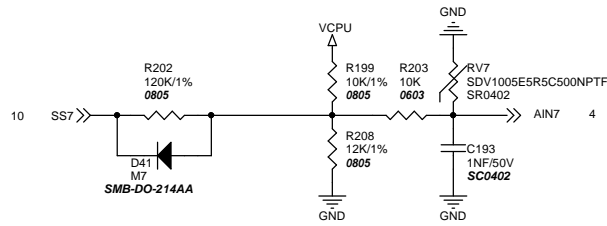
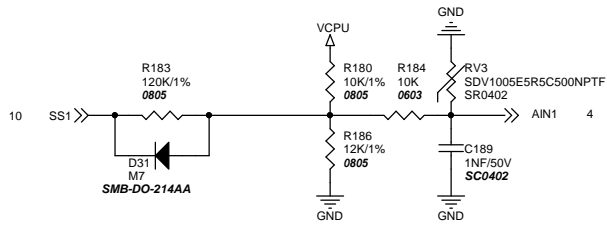
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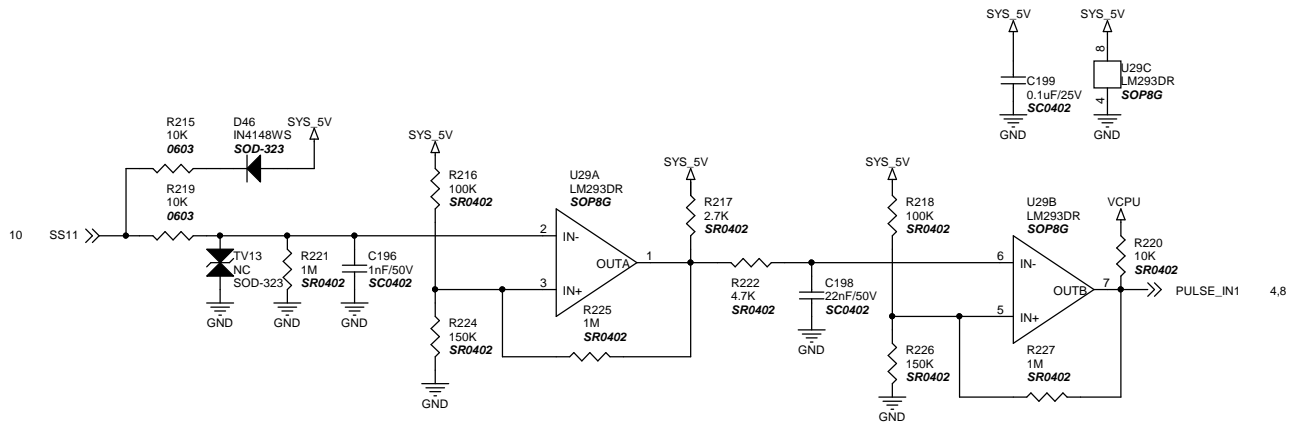
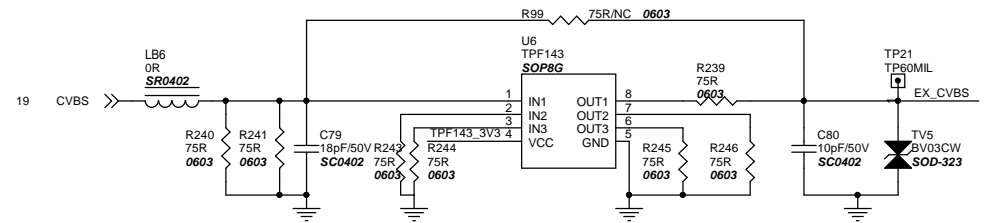
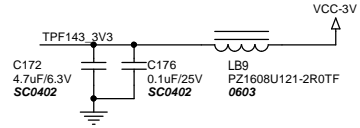
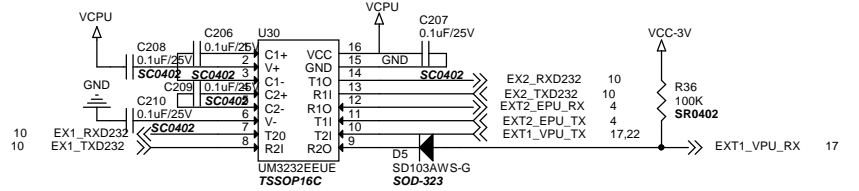
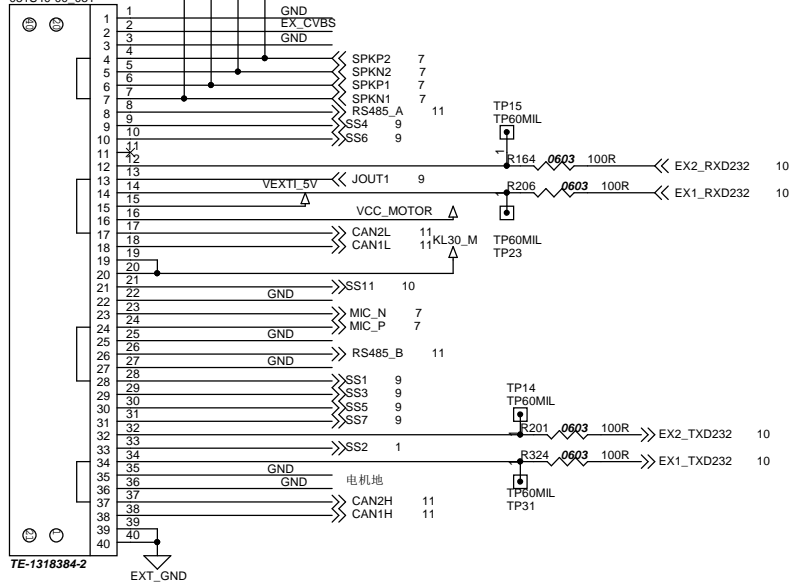
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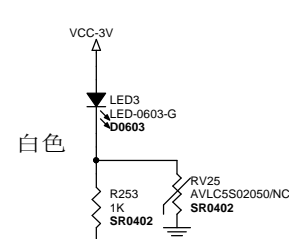
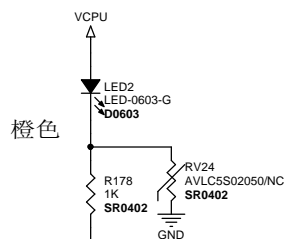
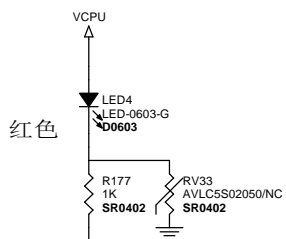
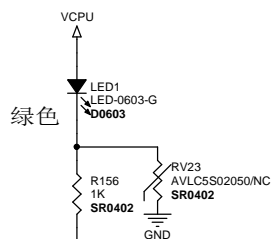
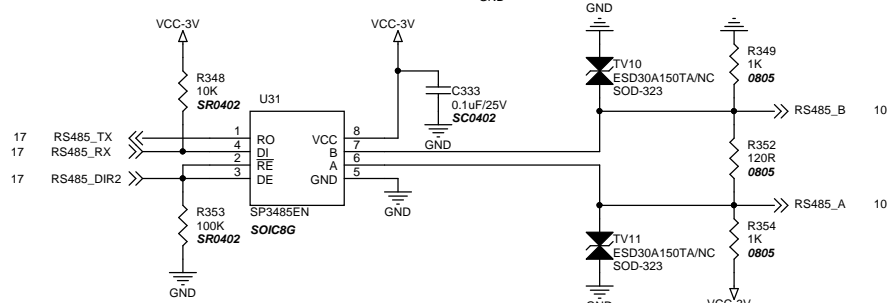
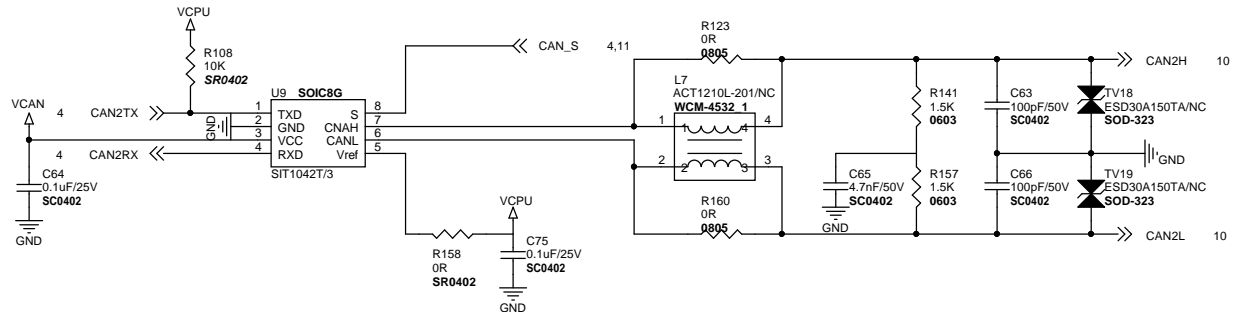
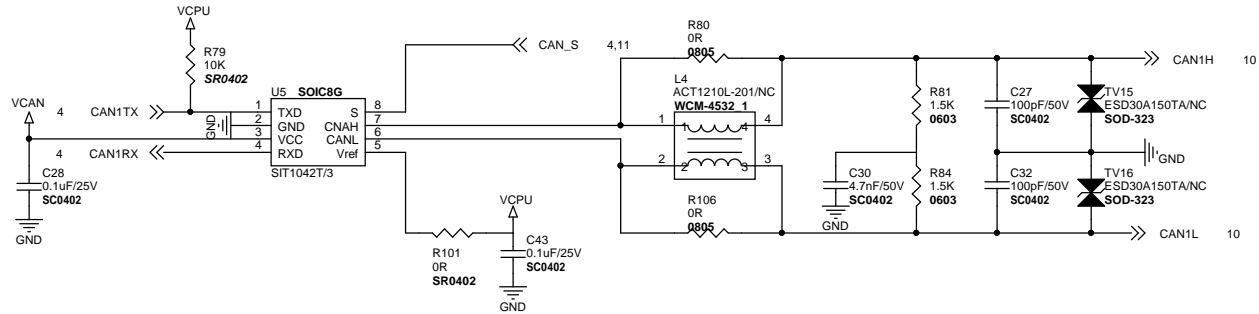
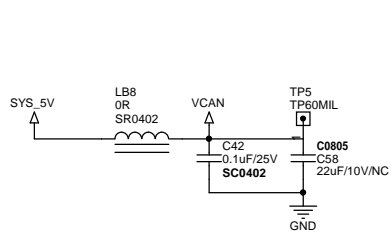
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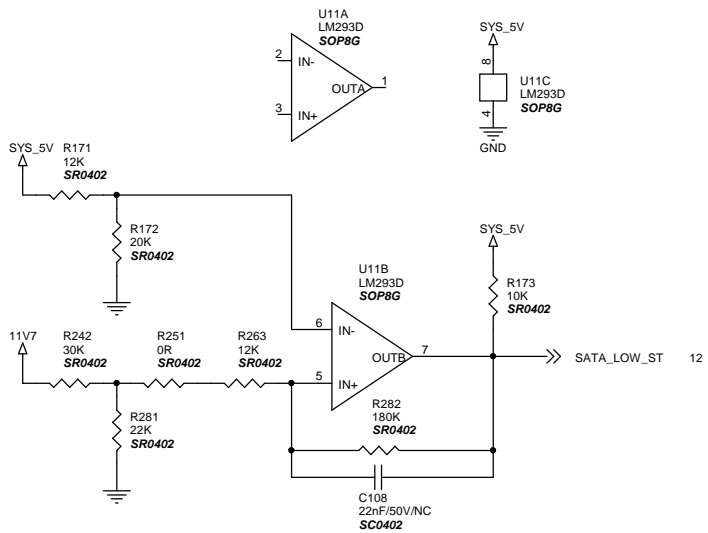
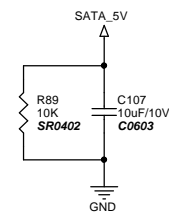
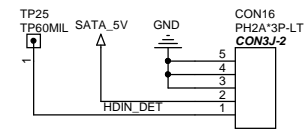
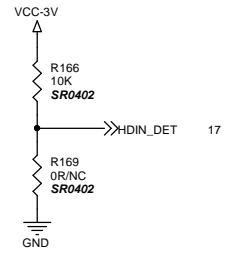
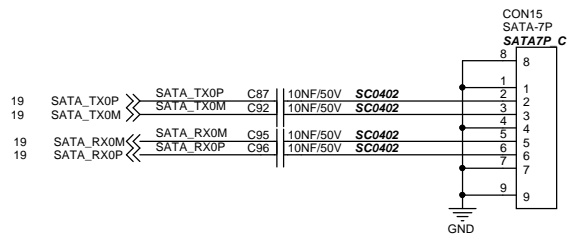
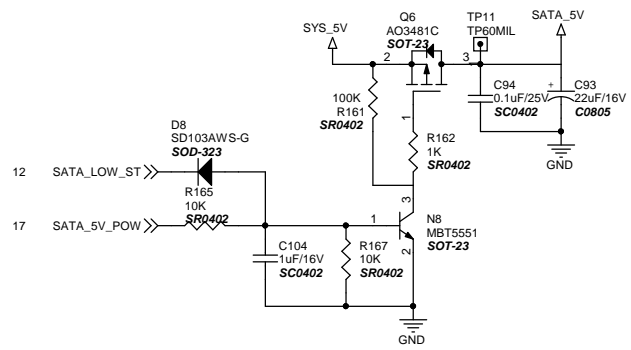
CON5
031S40-00_031



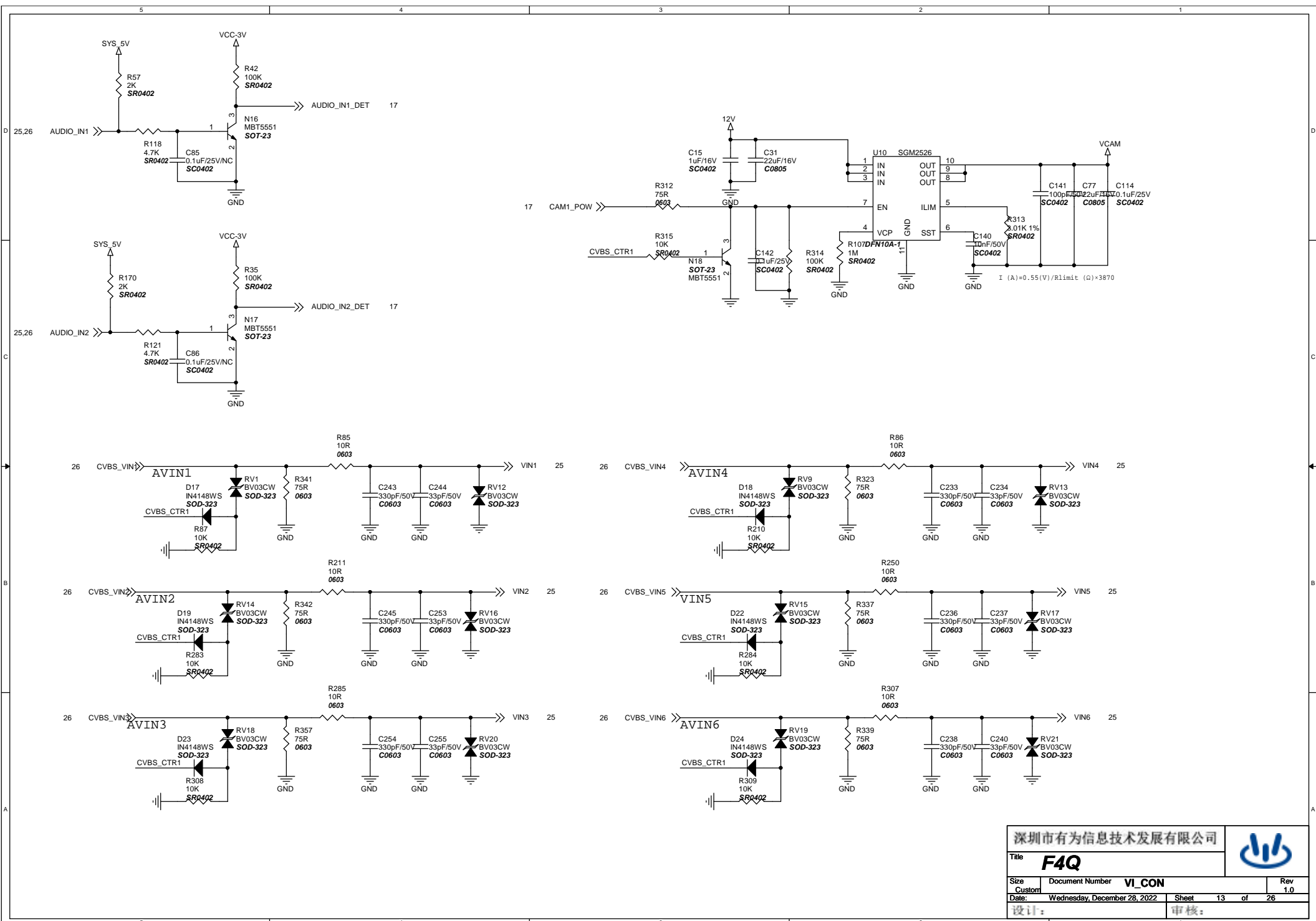
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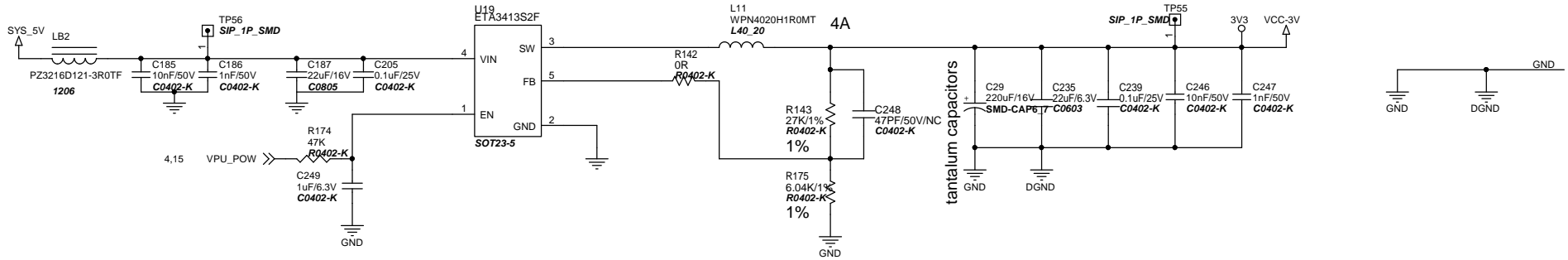


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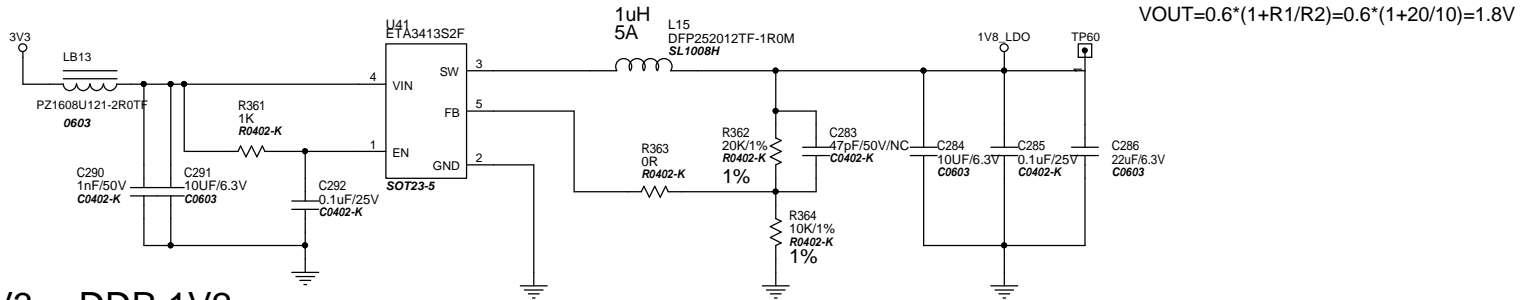


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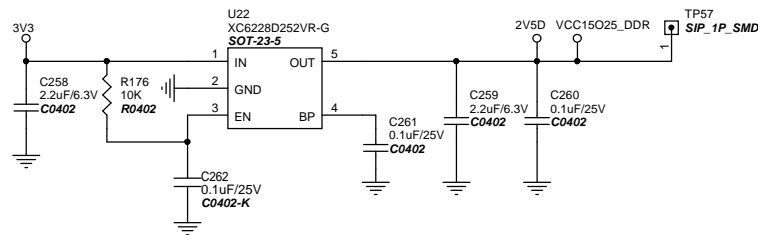
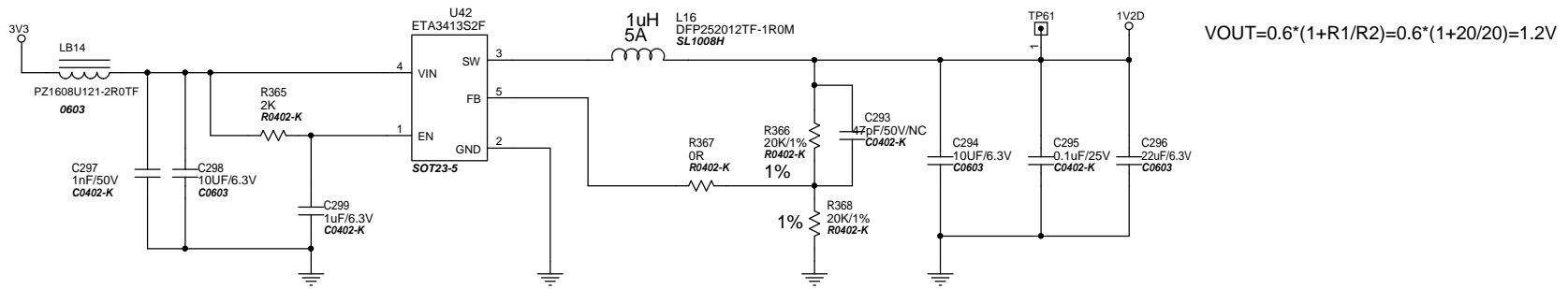
5V-->3V3



3V3-->1V8

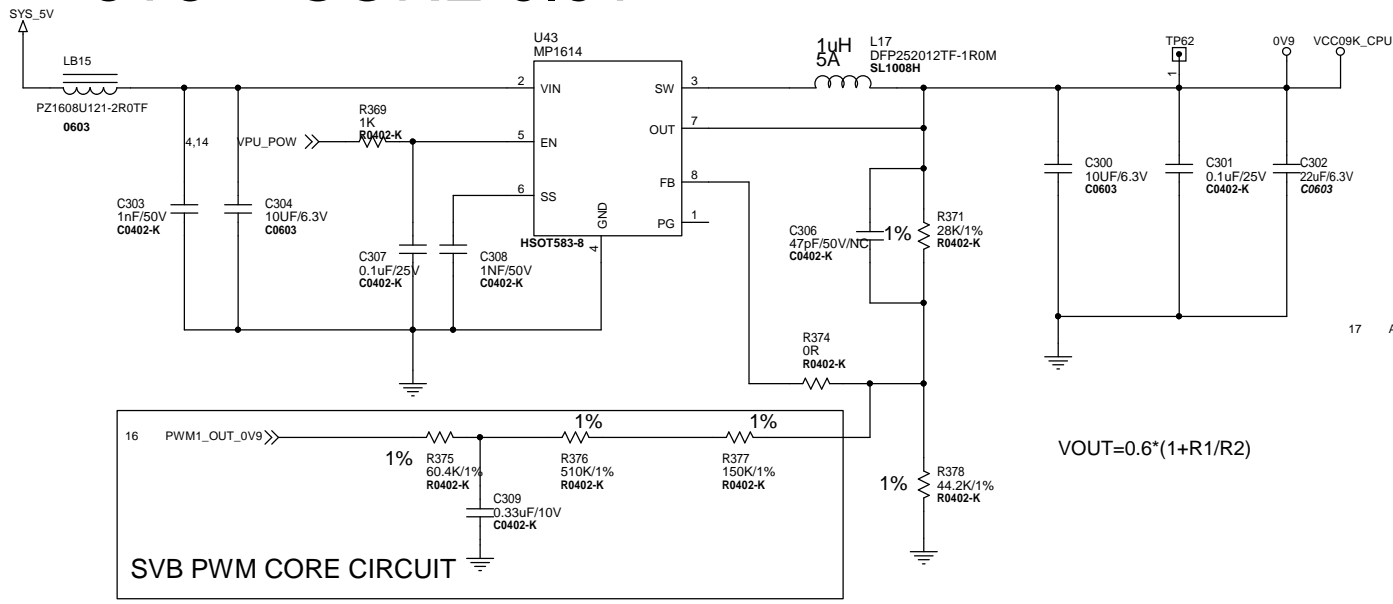


3V3-->DDR 1V2



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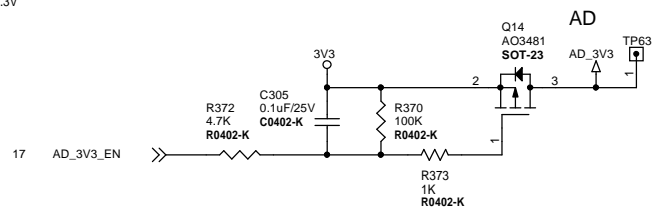
3V3-->CORE 0.9V



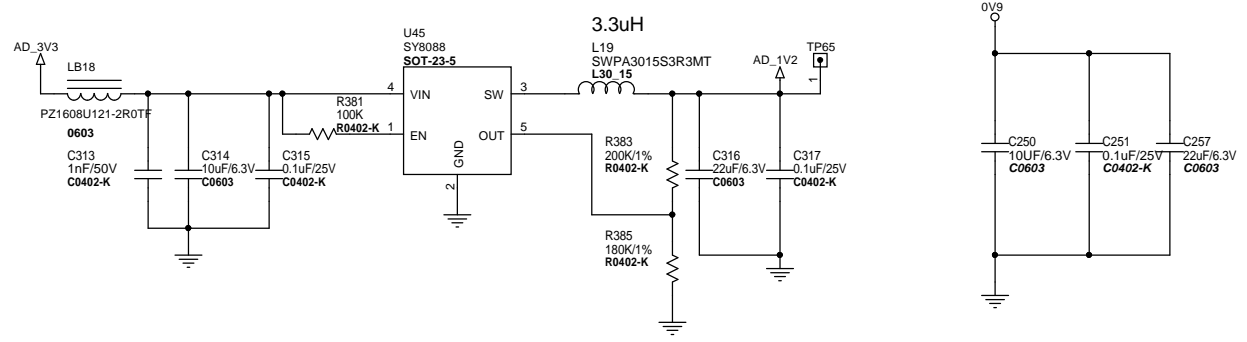
NOTES:the precision of these resistors must be +/-1%

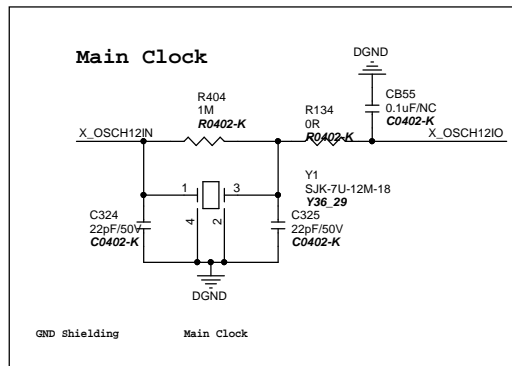
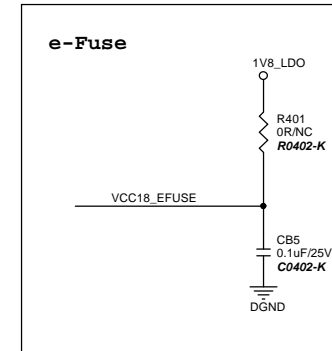
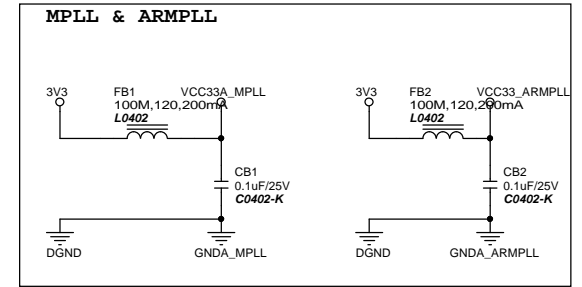
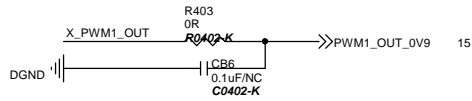
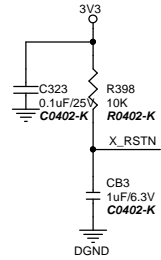
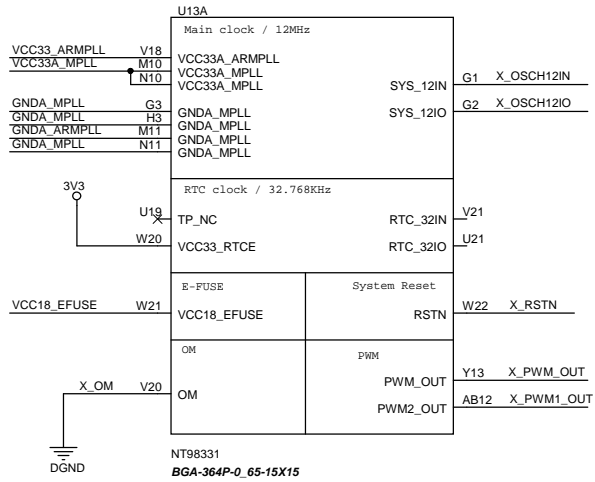
$$VOUT=0.6*(1+R1/R2)$$

3V3-->NXP6124



1V2-->NXP6124

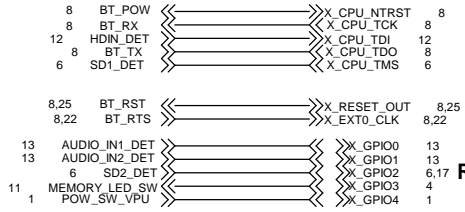




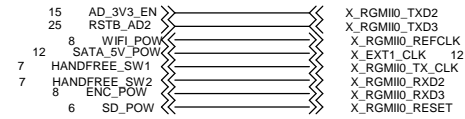
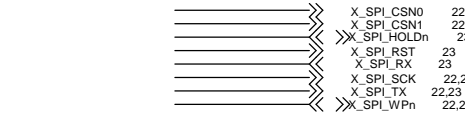
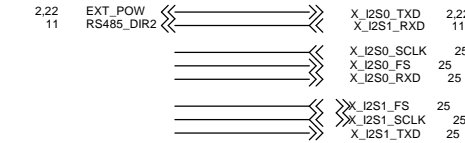
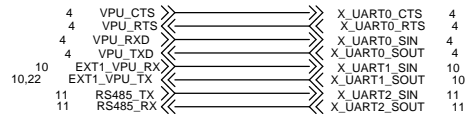
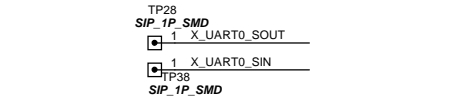
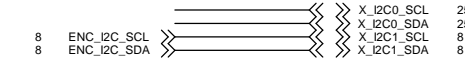
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可用的带中断输入的 管脚 :

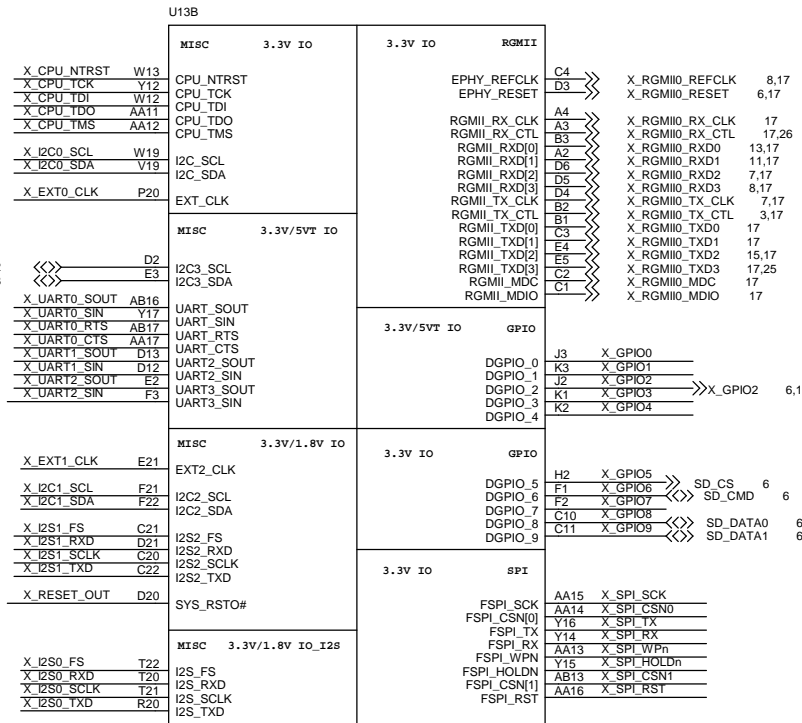
X_EXT1_CLK
X_I2S1_RXD
X_GPIO_1
X_GPIO_3
X_GPIO_4



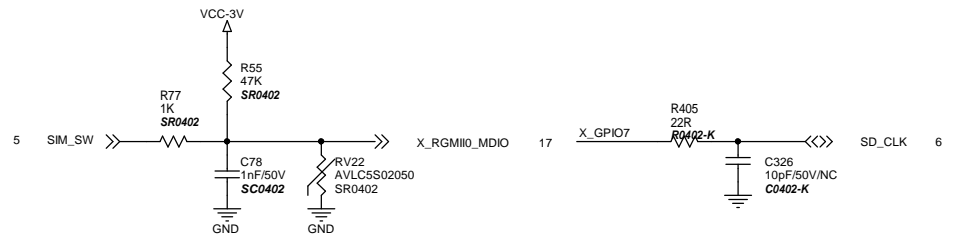
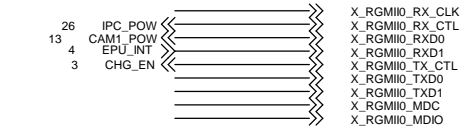
RSV for IR



RSV for 100Base-T1



NT98331
BGA-364P-Q_65-15X15



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```

>>>X_DDR0_MDQ[0..15] 24
>>>X_DDR0_MDM[0..1] 24
>>>X_DDR0_MDQS[0..1] 24
>>>X_DDR0_MDQSn[0..1] 24

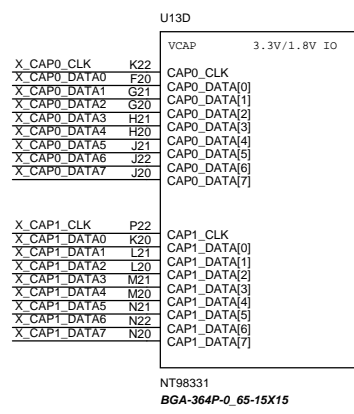
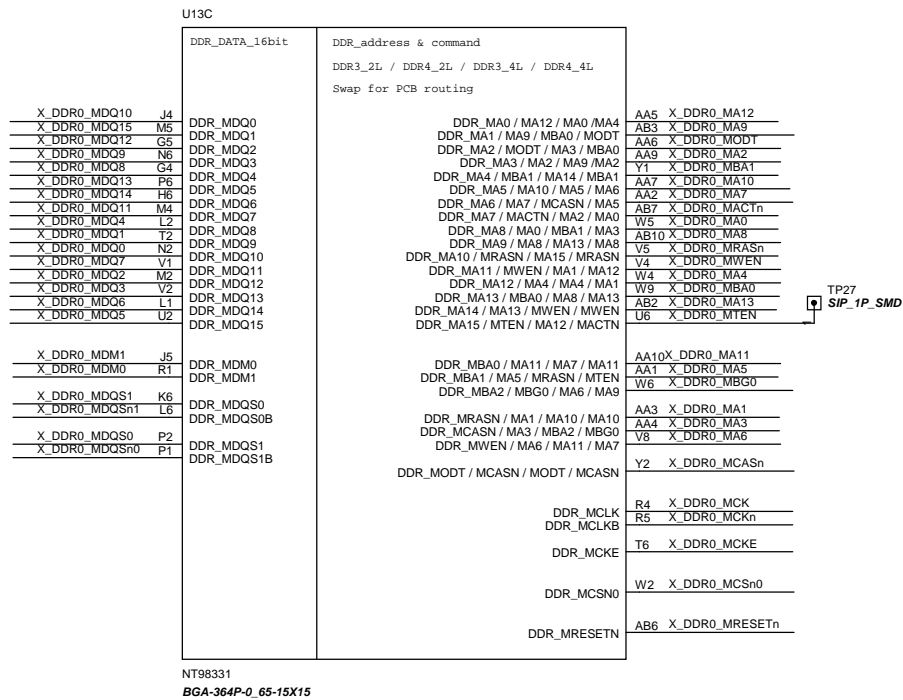
>>>X_DDR0_MA[0..13] 24
>>>X_DDR0_MCK 24
>>>X_DDR0_MCKN 24
>>>X_DDR0_MCKE 24
>>>X_DDR0_MRASn 24
>>>X_DDR0_MACTN 24
>>>X_DDR0_MRESETr 24
>>>X_DDR0_MBA[0..1] 24
>>>X_DDR0_MODT 24
>>>X_DDR0_MBG0 24
>>>X_DDR0_MWEN 24
>>>X_DDR0_MTEN 24
>>>X_DDR0_MCASn 24
>>>X_DDR0_MCSn0 24

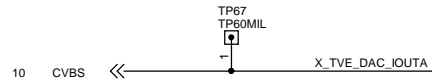
>>>X_CAP0_CLK 25
>>>X_CAP1_CLK 25

>>>X_CAP0_DATA[0..7] 25
>>>X_CAP1_DATA[0..7] 25

```

High & Low bytes signal is exchanged for balancing the trace's length. DDR DQ signal could be exchanged each other in the same byte (high byte or low byte).





GPIO_3[8]

RSV

- 26 MDL_BN <<< X_EPHY_RN A10
- 26 MDL_BP <<< X_EPHY_RP B10
- 26 MDL_AN <<< X_EPHY_TN C8
- 26 MDL_AP <<< X_EPHY_TP B8

X_TVE_DAC_IOUTA B22

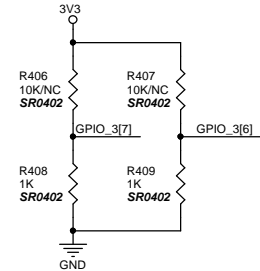
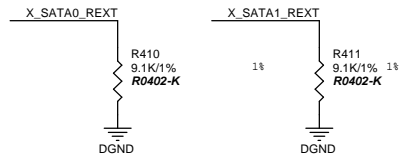
- X_USB0_DP B7
- X_USB0_DM A7
- X_USB1_DP B6
- X_USB1_DM C6

- X_VGA_DAC_HS A21
- X_VGA_DAC_OPB A20
- X_VGA_DAC_OPG C19
- X_VGA_DAC_OPR B19
- X_VGA_DAC_VS B21

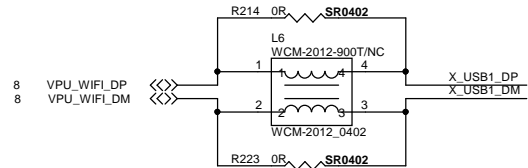
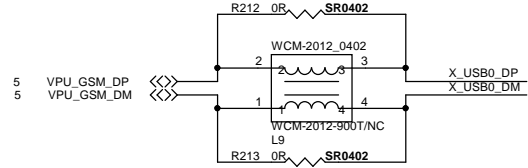
U13E

EPHY	X_EPHY_RN A10	EPHY_RXN	HDMI	HDMI_HPD	A18 GPIO_3[8]
	X_EPHY_RP B10	EPHY_RXP		HDMI_I2C_SCL	B18 GPIO_3[6]
CVBS	X_EPHY_TN C8	EPHY_TXN	HDMI_I2C_SDA	C17 GPIO_3[7]	
	X_EPHY_TP B8	EPHY_TXP	HDMI_TX0	B15	
TVE_OUT	X_TVE_DAC_IOUTA B22	TVE_OUT	HDMI_TX0_N	A15	
			HDMI_TX1	B13	
USB	X_USB0_DP B7	USB20_DP	HDMI_TX1_N	B14	
	X_USB0_DM A7	USB20_DM	HDMI_TX2	A12	
SATA0	X_USB1_DP B6	USB20_2_DP	HDMI_TX2_N	B12	
	X_USB1_DM C6	USB20_2_DM	HDMI_TXC	B16	
VGA	X_VGA_DAC_HS A21	VGA_HS	HDMI_TXC_N	C16	
	X_VGA_DAC_OPB A20	VGA_OPB			
SATA1	X_VGA_DAC_OPG C19	VGA_OPG			
	X_VGA_DAC_OPR B19	VGA_OPR			
	X_VGA_DAC_VS B21	VGA_VS			

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BGA-364P-0_65-15X15



版本识别



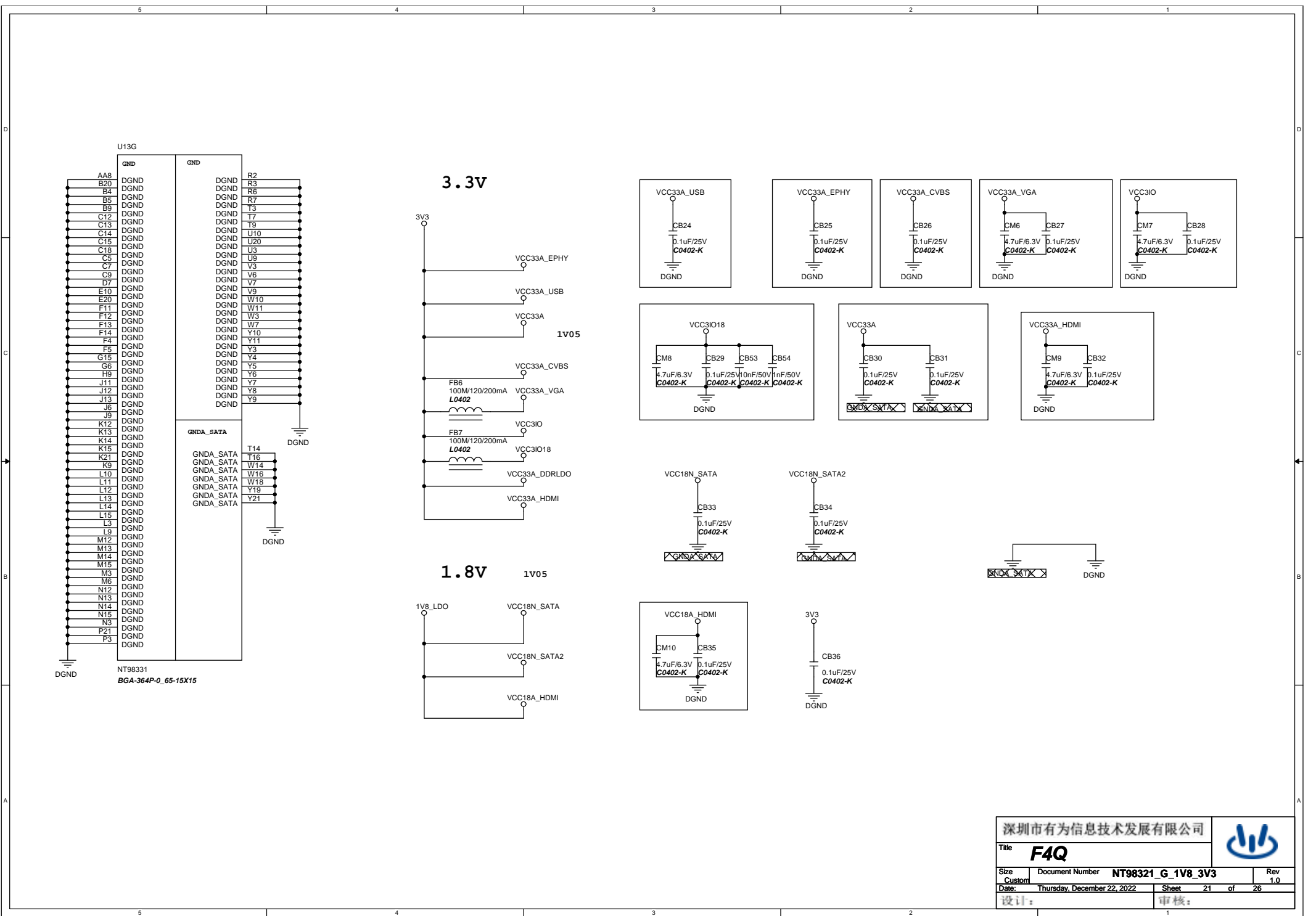
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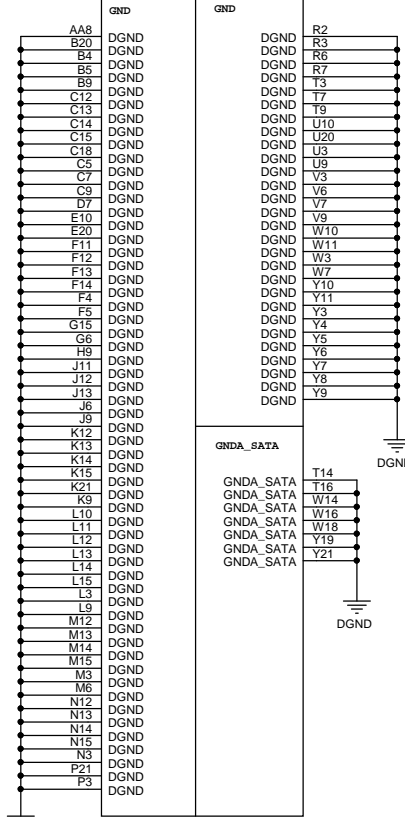
Size Custom Document Number **NT98321_E Display_Anglog** Rev 1.0

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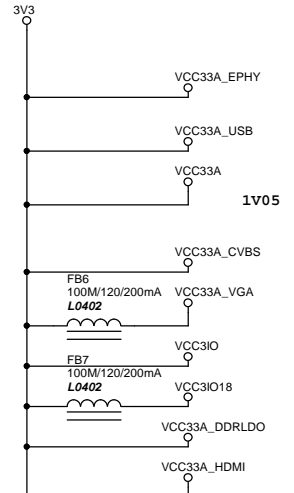
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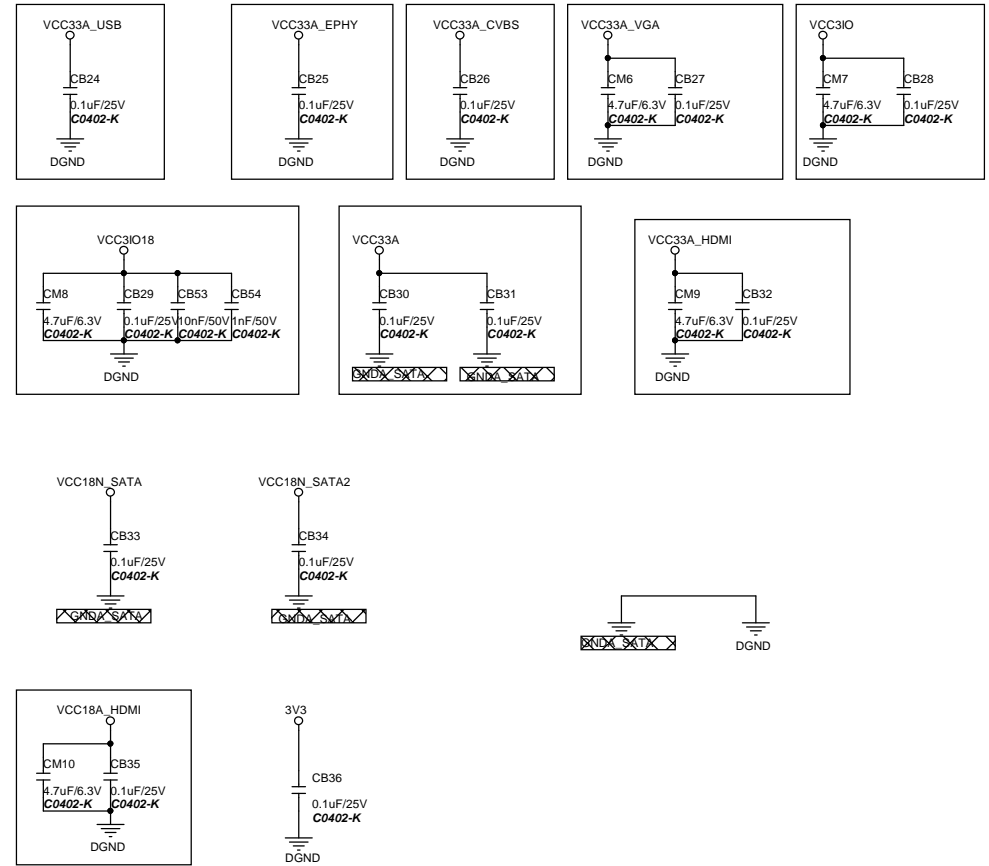
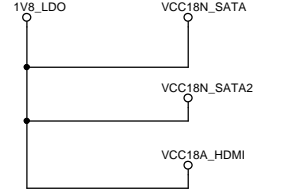
U13G



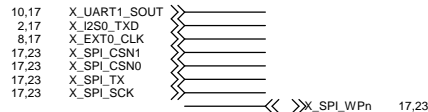
3.3V



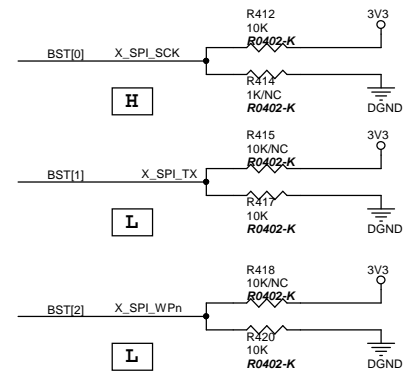
1.8V



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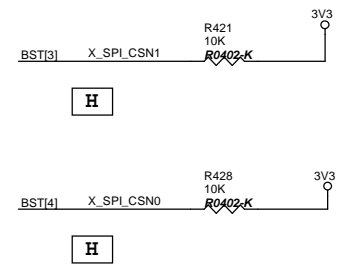
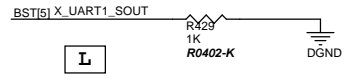


BST[2--0]	Function
Boot sequence switch	
0x0:	SPI NOR
0x1:	SPI NAND
0x2:	USB high speed
0x3:	ETHERNET
0x4:	UART
0x5:	SDIO
0x6:	BMC (SPI)
Others: Reserved	

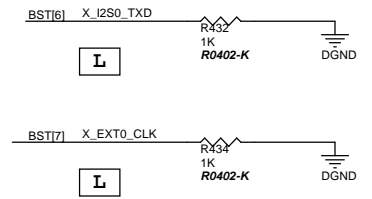


BST[5]	Function
EJTAG select	
0:	GPIO
1:	EJTAG

BST[4--3]	Function
0:	RMII (refclk output mode) - MAC0
1:	RMII (refclk input mode) - MAC0
2:	RGMII - MAC0
3:	Embedded PHY - MAC1



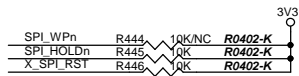
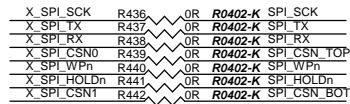
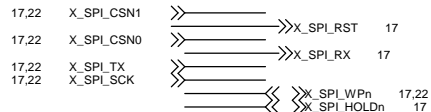
BST[7--6]	Function
CPU_DEBUG_MODE_SEL	
2'b00:	Normal mode
2'b01:	CPU debug mode 0
2'b10:	CPU debug mode 1
2'b11:	CG debug mode



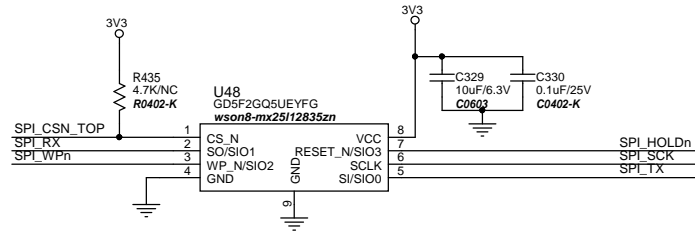
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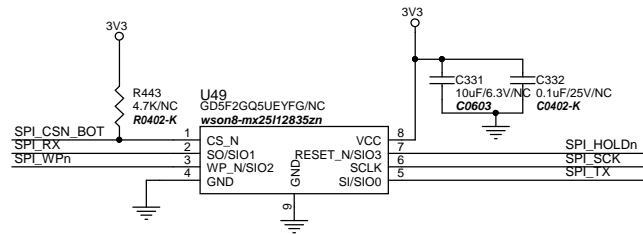
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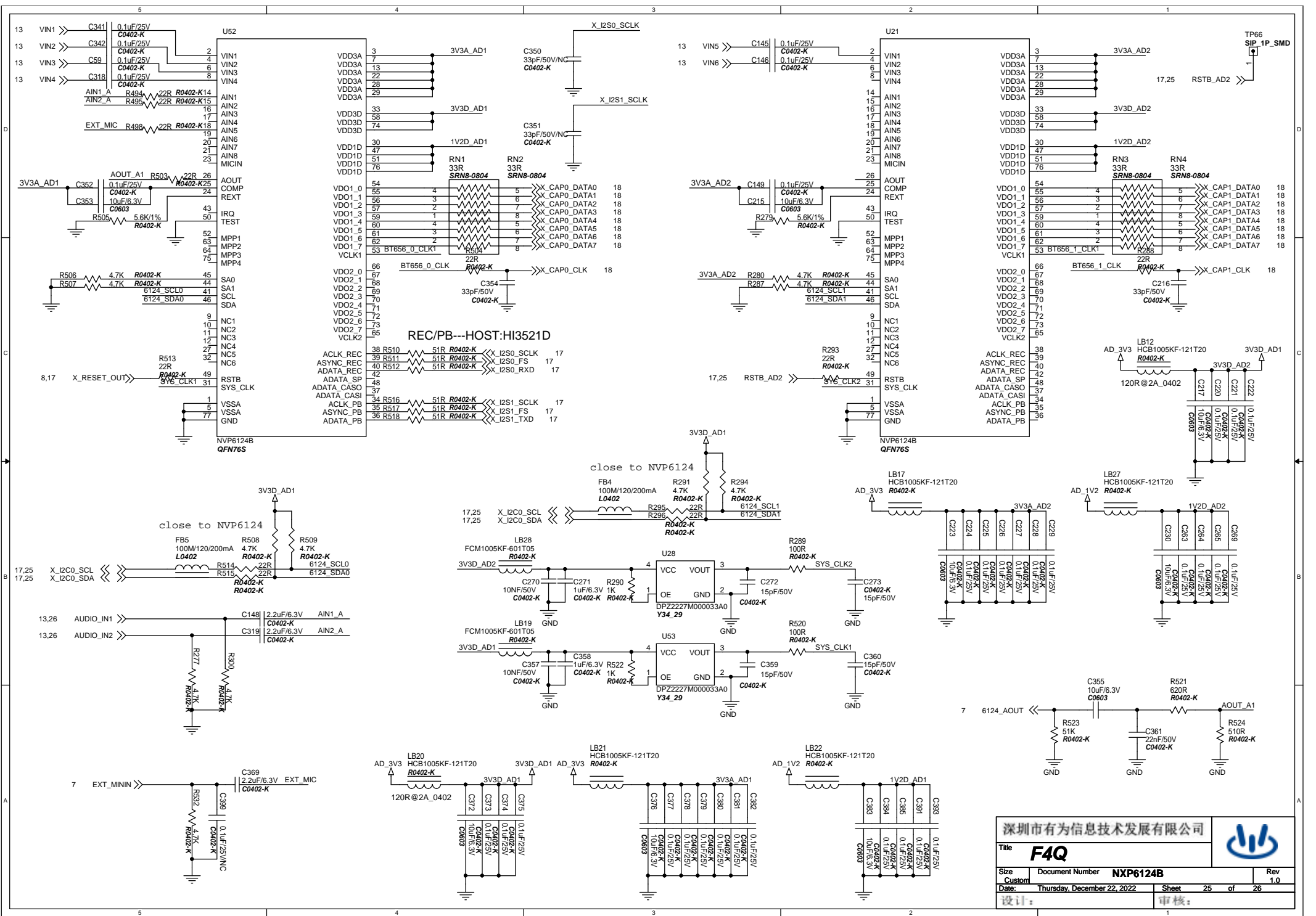


SPI NAND FLASH



SPI NAND FLASH





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设计:	审核:

