

W-LAN+Bluetooth Combo Module LBEE5ZZ1GV-893 Manual

**Broadcom Chipset
for 802.11b/g/n + Bluetooth 4.1/EDR**

The revision history of the product specification

Issued Date	Revision Code	Revision Page	Changed Items	Change Reason
Oct.23, 2015	-	-	First Issue	
Oct.28, 2015	02	P32	Add chapters of WLAN operation and Bluetooth Operation	By a request from a customer
Nov.2, 2015	03		Change order of the chapters. And remove "Taping and Reel Pacing", "NOTICE", and "PRECONDITION TO USE OUR PRODUCTS"	To meet the format to the reference Material.
Nov.10, 2015	04		Remove "Block Diagram"	Not to disclose on certification page.
		P7,8,9	Correct Pin Name on Terminal Configurations, Power up Sequence	Fix
Nov.20, 2015	05	Cover Page	Changed Part Number to MP Part Number.	Fix
		P4	Changed Marking information	Fix
		P18-P24	Deleted DC/RF Characteristics, land pattern, and Reference circuit.	Fix
		P18(new)	Added Notice without contents	Add a new chapter
Dec. 17, 2015	06	Header, Footer, and etc.	Remove manufacturer's name.	By a request from a customer
		P4	Modified Marking information	Fix
		P18,19,20	Added contents of the 11.Notice.	Add notices

TABLE OF CONTENTS

1. WLAN Function Start Guide	3
1.1. Hardware Setup	3
1.2. Software Setup	3
2. Bluetooth Function Start Guide	3
2.1. Hardware Setup	3
2.2. Software Setup	3
3. Features	3
4. Part Number	3
5. Dimensions, Marking and Terminal Configurations	4
6. Rating	8
7. Operating Condition	8
7.1. Operating condition	8
7.2. Power Up Sequence.....	8
Power On Sequence for WLAN ON and BT ON	8
Power On Sequence for WLAN OFF and BT ON	9
Power On Sequence for WLAN OFF and BT OFF.....	9
8. Digital I/O Requirements	12
9. External LPO Specification.....	12
10. Interface Timing	13
10.1. SDIO Timing (Default Mode)	13
10.2. SDIO Timing (High Speed Mode)	14
10.3. Bluetooth UART Timing (Default Mode)	14
10.4. PCM Timing Short Frame Sync, Master Mode.....	15
10.5. PCM Timing Short Frame Sync, Slave Mode	16
10.6. PCM Timing Long Frame Sync, Master Mode.....	16
10.7. PCM Timing Long Frame Sync, Slave Mode	17
11. Notice	18
11.1. FCC.....	18
11.2. IC	19

Please be aware that an important notice concerning availability, standard warranty and use in critical applications of the products and disclaimers thereto appears at the end of this specification sheet.

1. WLAN Function Start Guide

1.1. Hardware Setup

1. Connect Power input pins (VBAT, VDDIO) to power supply circuit.
2. Connect SDIO interface pins (WL_SDIO_CLK, WL_SDIO_CMD, WL_SDIO_D0 to WL_SDIO_D3) to an SDIO interface of host processor like Micro Controller Unit or PC. (See [5. Dimensions, Marking and Terminal Configurations.](#))
3. Connect Other IO lines (for ex. WL_REG_ON) to the host processor IO terminal.
4. Connect 32kHz LPO to the input pin of the module.
5. Turn on the module with following [7.2. Power Up Sequence.](#)

1.2. Software Setup

6. Loading WLAN driver from the host processor.
In case of “linux”,
`insmod dhd.ko firmware_path=aaa.bin nvram_path=bbb.txt`
Specify Manufacturing firmware for RF testing provided by Broadcom Corporation.
7. Operate RF test commands with using “wl” command.

2. Bluetooth Function Start Guide

2.1. Hardware Setup

1. Connect Power input pins (VBAT, VDDIO) to power supply circuit.
2. Connect UART interface pins (BT_UART_TXD, BT_UART_RXD, BT_UART_RTS_N, BT_UART_CTS_N) to an UART interface of host processor like Micro Controller Unit or PC. (See [5. Dimensions, Marking and Terminal Configurations.](#))
3. Connect Other IO lines (for ex. BT_REG_ON) to the host processor IO terminal.
4. Connect 32kHz LPO to the input pin of the module.
5. Turn on the module with following [7.2. Power Up Sequence.](#)

2.2. Software Setup

6. Download a patchram file (so-called hcd file) provided from Broadcom Corporation to the module.
7. Input HCI commands through UART interface from the host processor, and initialize the BT function on the module.
8. Input HCI commands for RT testing.

3. Features

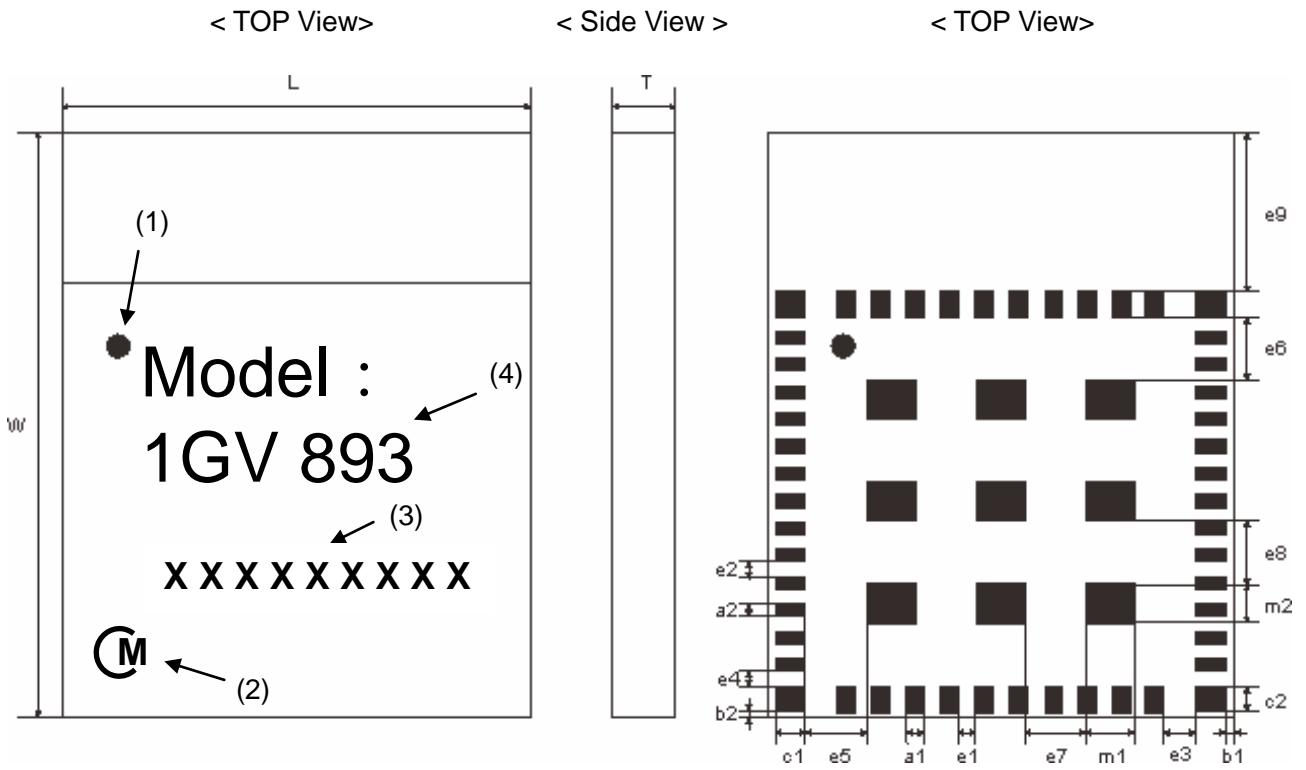
This Manual is applied to the IEEE802.11b/g/n W-LAN + Bluetooth 4.1+EDR module named LBEE5ZZ1GV-***.

- Interface : SDIO (WLAN), UART (BT)
- IC/Firmware : Broadcom/BCM4343W
- Reference Clock : Reference clock is embedded.
- MSL : Level 3
- RoHS : This module is compliant with the RoHS directive.

4. Part Number

Sample Part Number	LBEE5ZZ1GV-TEMP
EVK Part Number	LBEE5ZZ1GV-TEMP-D
	LBEE5ZZ1GV-893

5. Dimensions, Marking and Terminal Configurations



Dimensions

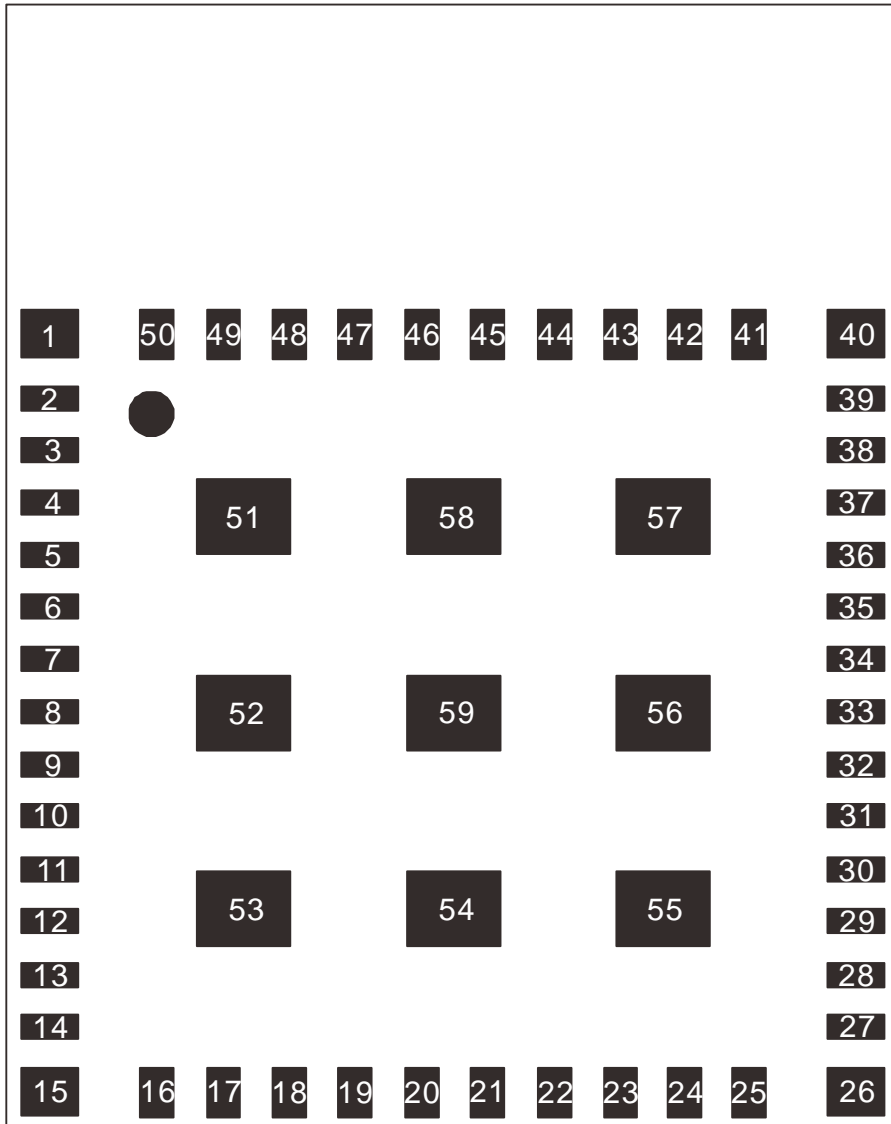
(unit : mm)

Mark	Dimensions	Mark	Dimensions	Mark	Dimensions
L	9.5 +/- 0.2	W	15 +/- 0.2	T	1.80 max.
a1	0.35 +/- 0.1	a2	0.35 +/- 0.1	b1	0.20 +/- 0.15
b2	0.20 +/- 0.15	c1	0.65 +/- 0.1	c2	0.65 +/- 0.1
e1	0.35 +/- 0.1	e2	0.35 +/- 0.1	e3	0.625 +/- 0.1
e4	0.375 +/- 0.1	e5	1.225 +/- 0.1	e6	1.625 +/- 0.1
e7	1.225 +/- 0.1	e8	1.625 +/- 0.1	e9	4.05 +/- 0.1
m1	1.0 +/- 0.1	m2	1.0 +/- 0.1		

Marking

Marking	Meaning
(1)	Pin 1 Marking
(2)	Manufacturer's Logo
(3)	Inspection Number
(4)	Module Type

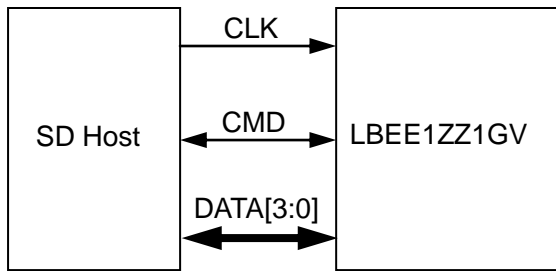
Terminal Configurations



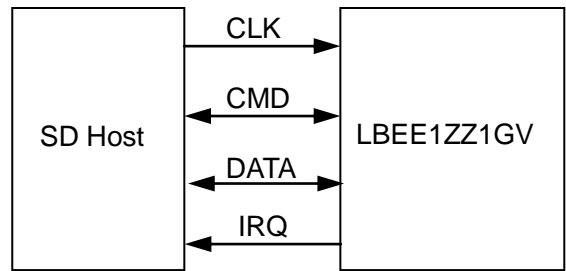
Pin#	Pin Name	Type	Description
1	GND	—	Ground
2	GND	—	Ground
3	WLAN_BT_ANT	I/O	WLAN/BT Transmit/Receive Antenna Port
4	GND	—	Ground
5	GND	—	Ground
6	WL_GPIO_2	I/O	This pin can be programmed by software to be a GPIO
7	GND	—	Ground
8	WL_SDIO_CLK	I	SDIO Bus clock input
9	GND	—	Ground
10	WL_SDIO_D2	I/O	SDIO Bus data line 2
11	WL_SDIO_CMD	I/O	SDIO Bus command line
12	WL_SDIO_D0	I/O	SDIO Bus data line 0
13	WL_SDIO_D3	I/O	SDIO Bus data line 3
14	WL_SDIO_D1	I/O	SDIO Bus data line 1
15	GND	—	Ground
16	WL_HOST_WAKE(WL_GPIO_0)	I/O	This pin can be programmed by software to be a GPIO or a WLAN_HOST_WAKE output indicating that host wake-up should be performed.
17	WL_GPIO_1	I/O	This pin can be programmed by software to be a GPIO
18	WL_REG_ON	I	Used by PMU to power up or power down the internal BCM4343W regulators used by the WLAN section. This pin has an internal 200kOhm pull-down resistor that is enabled by default. It can be disabled through programming.
19	VDDIO	I	Digital I/O supply input
20	GND	—	Ground
21	VBAT	I	Battery supply input
22	VBAT	I	Battery supply input
23	GND	—	Ground
24	BT_REG_ON	I	Used by PMU to power up or power down the internal BCM4343W regulators used by the BT/FM section. This pin has an internal 200kOhm pull-down resistor that is enabled by default. It can be disabled through programming.
25	LPO_IN	I	External sleep clock input (32.768 kHz)
26	GND	—	Ground
27	GND	—	Ground
28	BT_PCM_CLK	I/O	PCM clock can be master (output) or slave (input).
29	BT_PCM_SYNC	I/O	PCM sync signal can be master (output) or slave (input).
30	BT_PCM_OUT	O	PCM data output.
31	BT_PCM_IN	I	PCM data input.
32	BT_UART_RTS_N	O	Bluetooth UART request-to-send. Active-low request-to-send signal for the HCI UART interface.
33	BT_UART_CTS_N	I	Bluetooth UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
34	BT_UART_TXD	O	Bluetooth UART serial output. Serial data output for the HCI UART Interface.
35	BT_UART_RXD	I	Bluetooth UART serial input. Serial data input for the HCI UART Interface.
36	GND	—	Ground
37	BT_DEV_WAKE	I	Bluetooth DEV_WAKE
38	BT_HOST_WAKE	O	Bluetooth HOST_WAKE
39	GND	—	Ground
40	GND	—	Ground
41~50	GND	—	Ground
H1~H9	GND	—	Ground

SDIO Pin Description

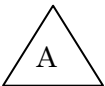
No.	Pin Name	(i) SD 4-bit Mode		(ii) SD 1-bit Mode	
20	WL_SDIO_CLK	CLK	Clock	CLK	Clock
24	WL_SDIO_D0	DATA0	Data line 0	DATA	Data line
26	WL_SDIO_D1	DATA1	Data line 1 /Interrupt	IRQ	Interrupt
23	WL_SDIO_D2	DATA2	Data line 2	NC	Not used
25	WL_SDIO_D3	DATA3	Data line 3	NC	Not used
22	WL_SDIO_CMD	CMD	Command line	CMD	Command line



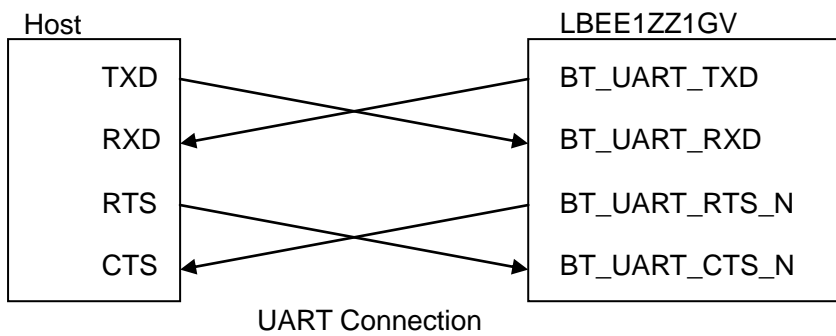
(i) SD 4-bit Mode



(ii) SD 1-bit Mode



Note : 10 to 100kΩ pull-ups are required on the four DATA lines and the CMD line. This requirement must be met during all operating states by using external pull-up resistors or properly programming internal SDIO host pull-ups.



6. Rating

		min.	max.	unit
Storage Temperature		-40	+85	deg.C
Supply Voltage	VBAT	-0.5	5.0	V
	VDDIO	-0.5	3.9	V

* Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability. No damage assuming only one parameter is set at limit at a time with all other parameters are set within operating condition.

7. Operating Condition

7.1. Operating condition

		min.	typ.	max.	unit
Operating Temperature Range		-30	+25	+70	deg.C
Specification Temperature Range		-10	+25	+55	deg.C
Supply Voltage	VBAT	3.2	3.6	4.8	V
	VDDIO	1.71	1.8 or 3.3	3.63	V

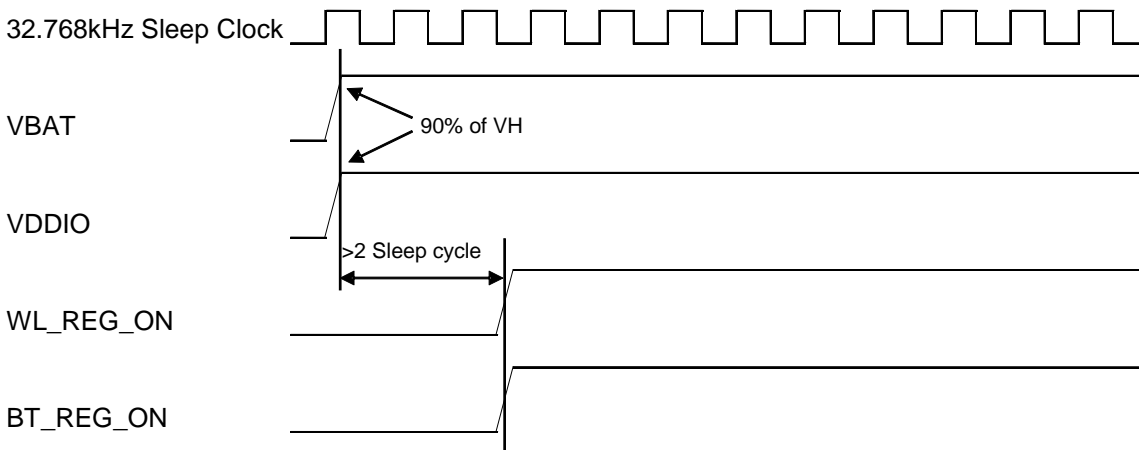
* Functionality is guaranteed but specifications require derating at extreme temperatures.

7.2. Power Up Sequence

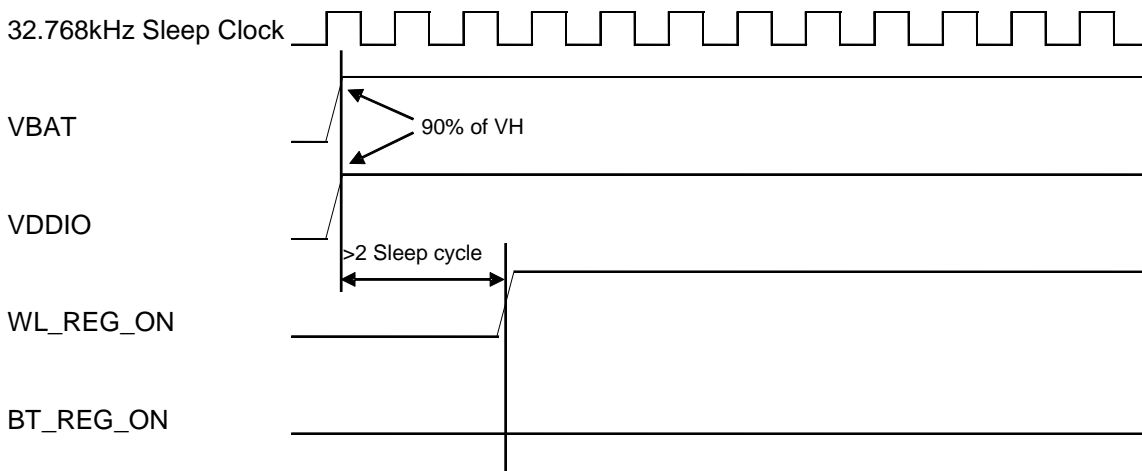
-VBAT should not rise 10%-90% faster than 40 microsecond.

-VBAT should be up before or at the same time as VIO. VIO should NOT be present fast or be held high before VBAT is high.

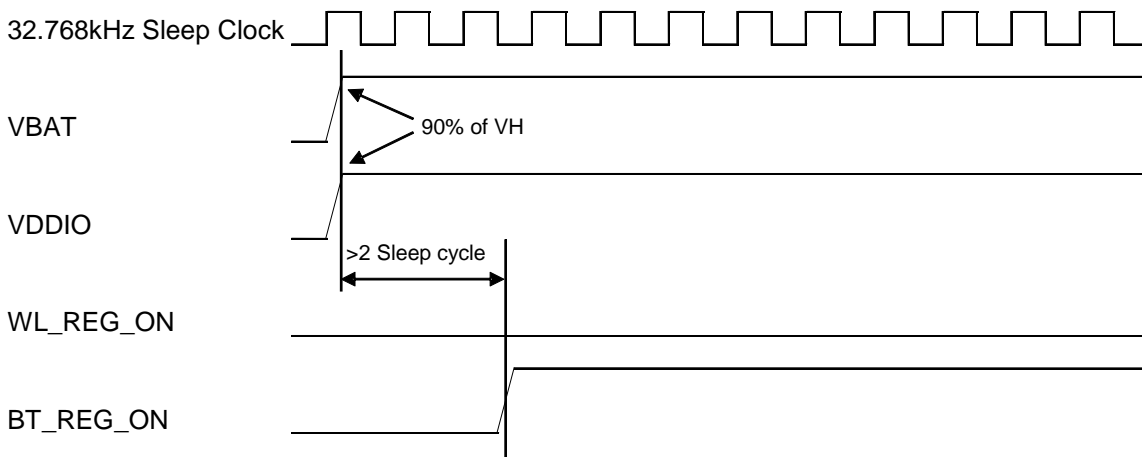
Power On Sequence for WLAN ON and BT ON



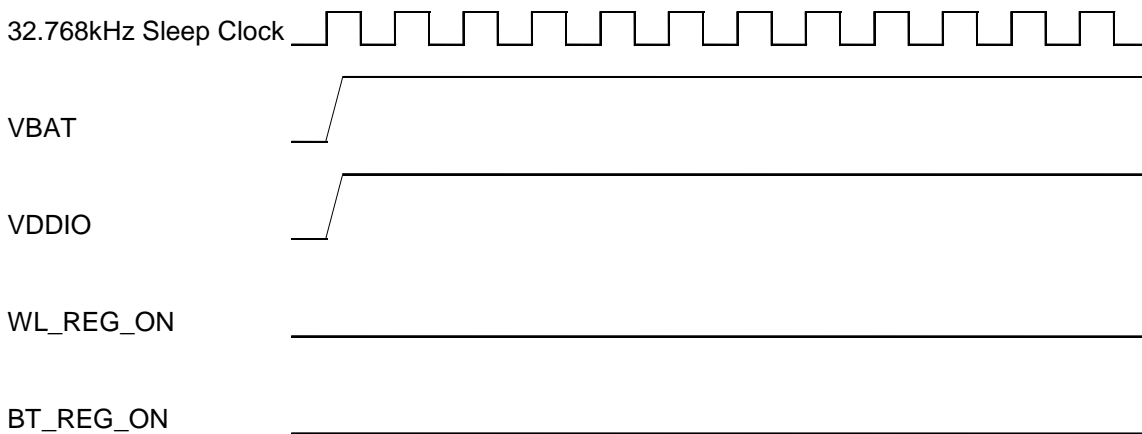
Power On Sequence for WLAN ON and BT Off



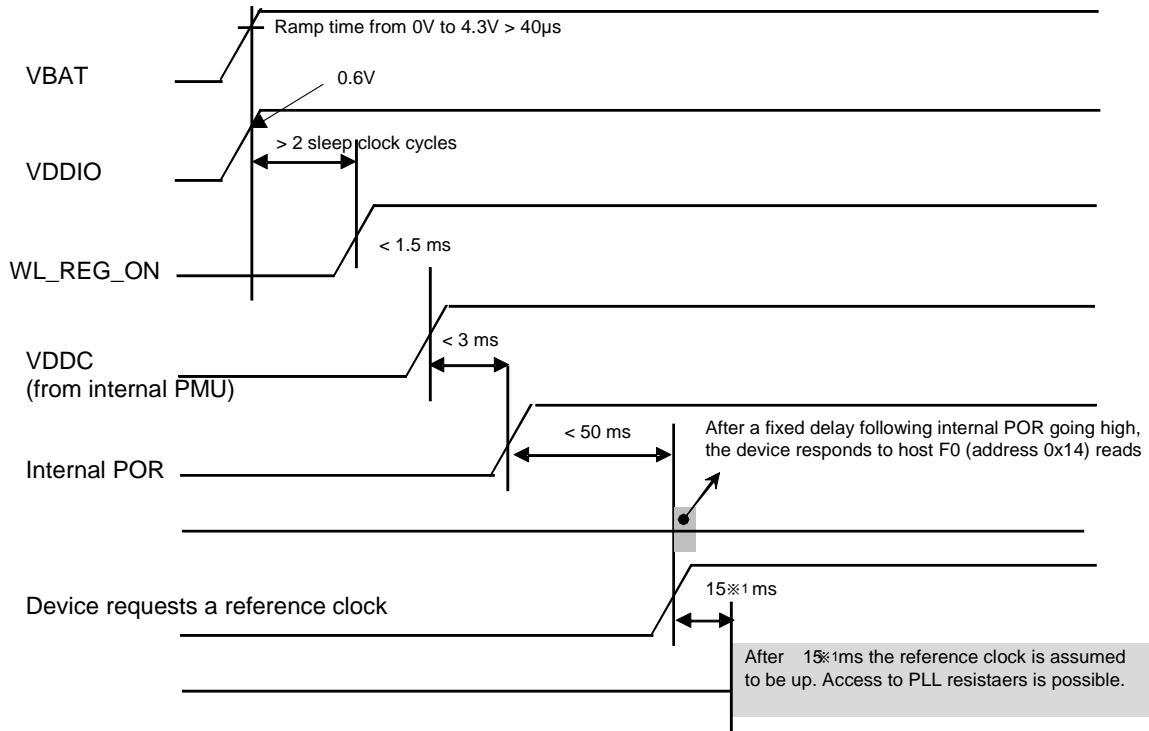
Power On Sequence for WLAN OFF and BT ON



Power On Sequence for WLAN OFF and BT OFF

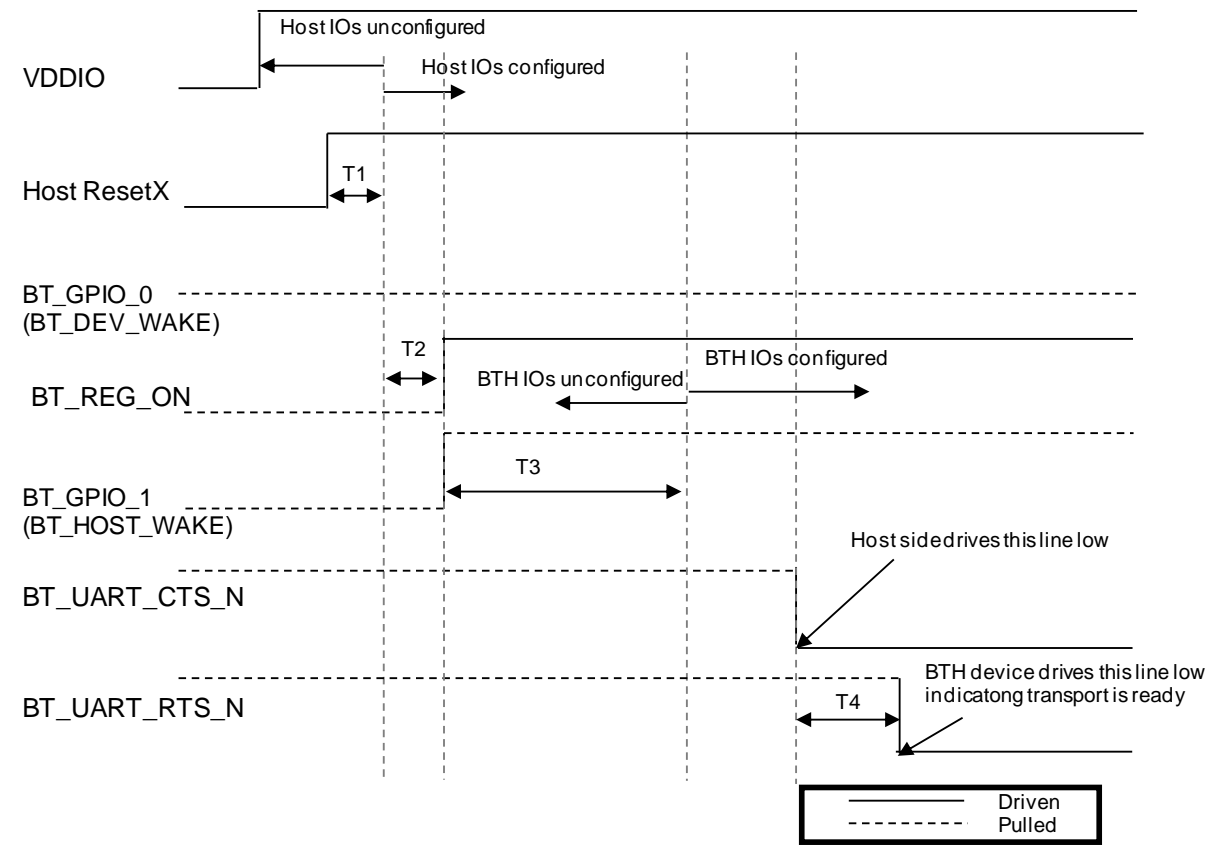


WLAN Boot up Sequence



※1 This wait time is programmable in sleep-clock increments from 1 to 255 (30us to 15ms)

Startup Signaling Sequence



T1 is the time for host to settle it's I/Os after a reset.

T2 is the time for host to drive BT_REG_ON high after the Host I/Os are configured.

T3 is the time for BTH(Bluetooth) device to settle its I/Os after a reset and reference clock settling time has elapsed.

T4 is the time for BTH device to drive BT_UART_RTS_N low after the host drives BT_UART_CTS_N low. This assumes the BTH device has already completed initialization.

Timing diagram assumes VBAT is present.

8. Digital I/O Requirements

SDIO Interface I/O Pins	Sym	min.	max.	unit
Input low voltage (VDDIO = 3.3V)	V _{IL}	-	0.25*VDDIO	V
Input high voltage (VDDIO = 3.3V)	V _{IH}	0.625*VDDIO	-	V
Input low voltage (VDDIO = 1.8V) ¹	V _{IL}	-	0.58	V
Input high voltage (VDDIO = 1.8V)	V _{IH}	1.27	-	V
Output low voltage (VDDIO = 3.3V)	V _{OL}	-	0.125*VDDIO	V
Output high voltage (VDDIO = 3.3V)	V _{OH}	0.75*VDDIO	-	V
Output low voltage (VDDIO = 1.8V)	V _{OL}	-	0.45	V
Output high voltage (VDDIO = 1.8V)	V _{OH}	1.40	-	V

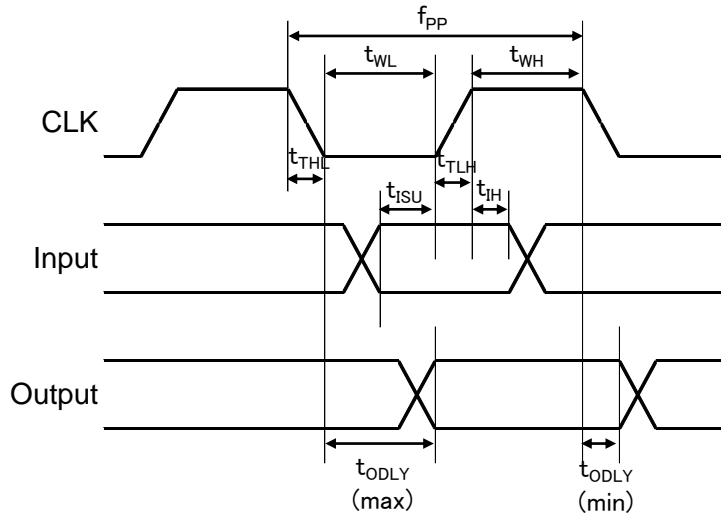
Other Digital I/O Pins	Sym	min.	max.	Unit
Input low voltage (VDDIO = 3.3V)	V _{IL}	-	0.8	V
Input high voltage (VDDIO = 3.3V)	V _{IH}	2.0	-	V
Input low voltage (VDDIO = 1.8V) ¹	V _{IL}	-	0.35*VDDIO	V
Input high voltage (VDDIO = 1.8V)	V _{IH}	0.65*VDDIO	-	V
Output low voltage (VDDIO = 3.3V)	V _{OL}	-	0.40	V
Output high voltage (VDDIO = 3.3V)	V _{OH}	VDDIO-0.4	-	V
Output low voltage (VDDIO = 1.8V)	V _{OL}	-	0.45	V
Output high voltage (VDDIO = 1.8V)	V _{OH}	VDDIO-0.45	-	V

9. External LPO Specification

Parameter	Condition/Notes	Specification			
		Minimum	Typical	Maximum	Units
Frequency	-	-	32.768	-	KHz
Frequency accuracy		-200	-	+200	ppm
Duty cycle	-	30	-	70	%
Input amplitude		200	-	3300	mV, p-p
Signal type	Square wave or sine wave	-	-	-	-
Input impedance ^a	Resistive	100	-	-	kΩ
	Capacitive	-	-	5	pF
Clock jitter		-	-	10,000	ppm

a. When power is applied or switched off.

10. Interface Timing
10.1. SDIO Timing (Default Mode)

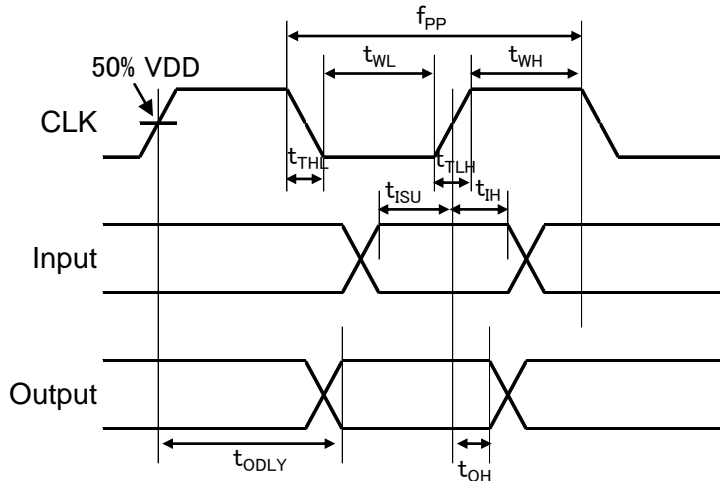


Parameter	Symbol	Min ⁽¹⁾	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
Clock CLK (All values are referred to min. VIH and max. VIL ⁽²⁾)					
Frequency-Data Transfer Mode	fPP	0	-	25	MHz
Frequency-Identification Mode	fOD	0	-	400	kHz
Clock Low Time	tWL	10	-	-	ns
Clock High Time	tWH	10	-	-	ns
Clock Rise Time	tTLH	-	-	10	ns
Clock Fall Time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input Setup Time	tISU	5	-	-	ns
Input Hold Time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output Delay time-Data Transfer Mode	tODLY	0	-	14	ns
Output Delay time-Identification Mode	tODLY	0	-	50	ns

(1). Timing is based on $CL \leq 40pF$ load on CMD and Data.

(2). Min (Vih) = $0.7 \cdot VDDIO$ and max (Vil) = $0.2 \cdot VDDIO$.

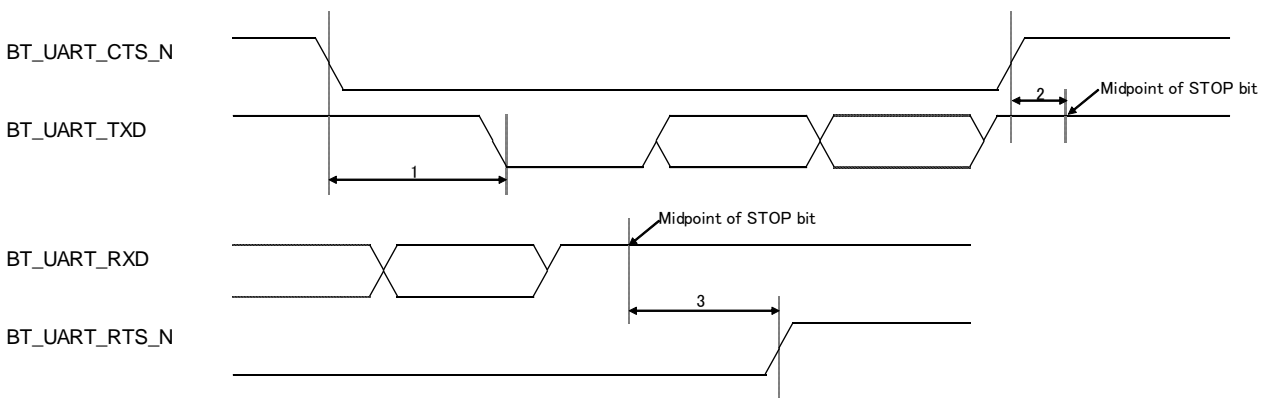
10.2. SDIO Timing (High Speed Mode)



Parameter	Symbol	Min ⁽¹⁾	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
Clock CLK (All values are referred to min. VIH and max. VIL ⁽²⁾)					
Frequency-Data Transfer Mode	fPP	0	-	50	MHz
Frequency-Identification Mode	fOD	0	-	400	kHz
Clock Low Time	tWL	7	-	-	ns
Clock High Time	tWH	7	-	-	ns
Clock Rise Time	tTLH	-	-	3	ns
Clock Fall Time	tTHL	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input Setup Time	tISU	6	-	-	ns
Input Hold Time	tIH	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output Delay time-Data Transfer Mode	tODLY	-	-	14	ns
Output Hold time	tOH	2.5	-	-	ns
Total System Capacitance (each line)	CL	-	-	40	pF

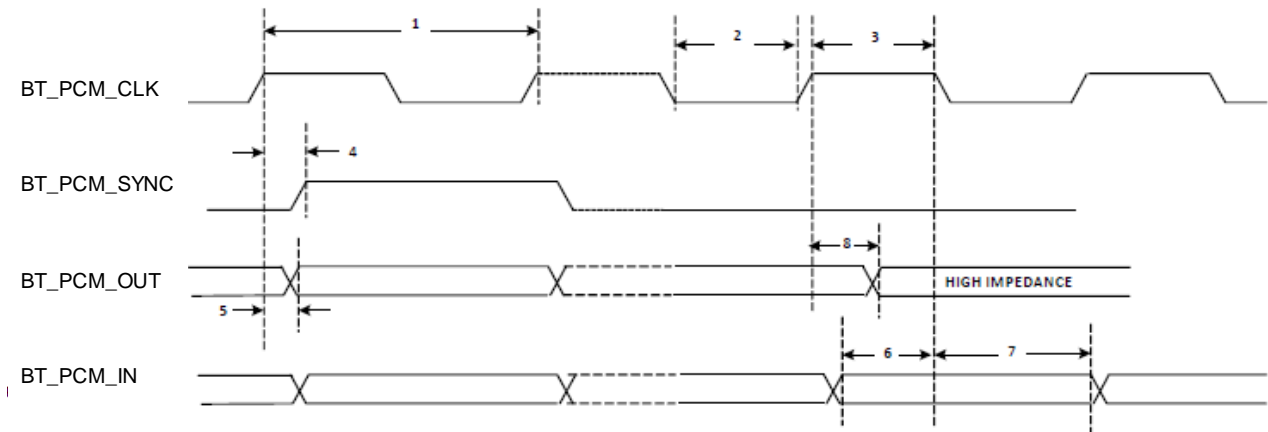
(1). Timing is based on $CL \leq 40pF$ load on CMD and Data.
 (2). Min (Vih) = $0.7 \cdot VDDIO$ and max (Vil) = $0.2 \cdot VDDIO$.

10.3. Bluetooth UART Timing (Default Mode)



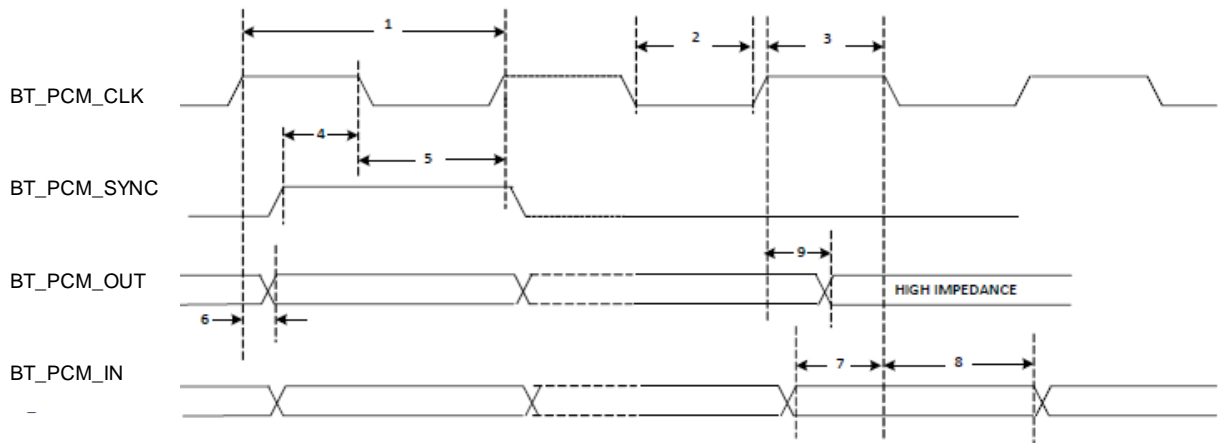
Reference	Description	Min	Typ	Max	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	-	-	1.5	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	-	-	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	-	-	0.5	Bit periods

10.4. PCM Timing Short Frame Sync, Master Mode



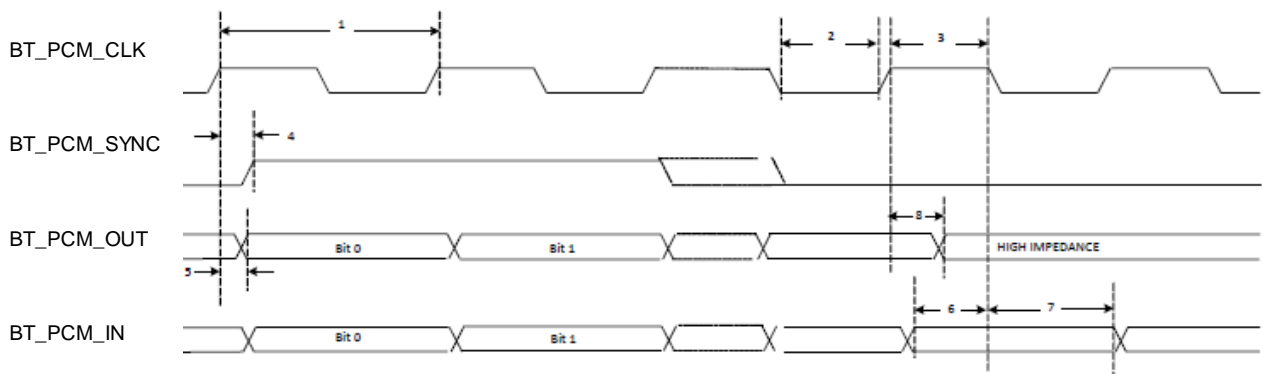
Reference	Description	Min	Typ	Max	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	PCM_SYNC delay	0	-	25	ns
5	PCM_OUT delay	0	-	25	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
8	Delay from rising edge of PCM_CLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

10.5. PCM Timing Short Frame Sync, Slave Mode



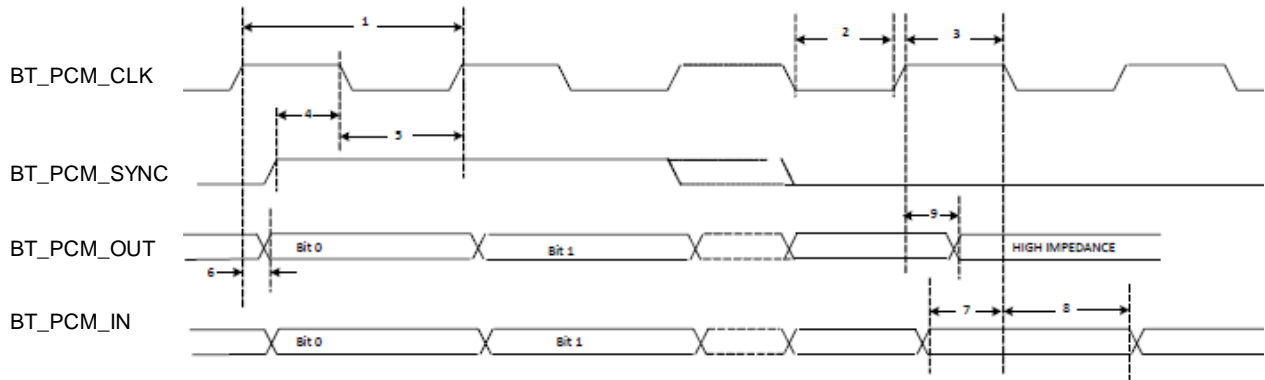
Reference	Description	Min	Typ	Max	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock Low	41	-	-	ns
3	PCM bit clock High	41	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	0	-	25	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns
9	Delay from rising edge of PCM_CLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

10.6. PCM Timing Long Frame Sync, Master Mode



Reference	Description	Min	Typ	Max	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	PCM_SYNC delay	0	-	25	ns
5	PCM_OUT delay	0	-	25	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
8	Delay from rising edge of PCM_CLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

10.7. PCM Timing Long Frame Sync, Slave Mode



Reference	Description	Min	Typ	Max	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	0	-	25	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns
9	Delay from rising edge of PCM_CLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

11. **Notice**

Please describe the following warning on the final product which contains this module.

11.1. **FCC**

Class B: (Section 15.105)

FEDERAL COMMUNICATIONS COMMISSION INTERFERENCE STATEMENT

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/ TV technician for help.

(Section 15.21)

CAUTION:

Any changes or modifications not expressly approved by the grantee of this device could void the user's authority to operate the equipment.

(Section 15.19)(a)(3)

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

RF Exposure Information (SAR)

This device meets the government's requirements for exposure to radio waves. This device is designed and manufactured not to exceed the emission limits for exposure to radio frequency (RF) energy set by the Federal Communications Commission of the U.S. Government.

The exposure standard employs a unit of measurement known as the Specific Absorption Rate, or SAR. The SAR limit set by the FCC is 1.6 W/kg. Tests for SAR are conducted using standard operating positions accepted by the FCC with the EUT transmitting at the specified power level in different channels.

The FCC has granted an Equipment Authorization for this device with all reported SAR levels evaluated as in compliance with the FCC RF exposure guidelines. SAR information on this device is on file with the FCC and can be found under the Display Grant section of www.fcc.gov/eot/ea/fccid after searching on FCC ID: 2AAD3JA0MOP0

To ensure that RF exposure levels remain at or below the tested levels, use a belt-clip, holster, or similar accessory that maintains a minimum separation distance of 5mm between your body and the device.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 5 mm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains FCC ID: 2AAD3JA0M0P0 "

Information for the OEMs and Integrators

The following statement must be included with all versions of this document supplied to an OEM or integrator, but should not be distributed to the end user.

- 1) This device is intended for OEM integrators only.
- 2) Please see the full Grant of Equipment document for other restrictions.

11.2. IC

Canada, Industry Canada (IC) Notices

This device complies with Canada licence-exempt RSS standard(s).

Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Canada, avis d'Industry Canada (IC)

Cet appareil est conforme avec Industrie Canada exemptes de licence RSS standard(s).

Son fonctionnement est soumis aux deux conditions suivantes : (1) cet appareil ne doit pas causer d'interférence et (2) cet appareil doit accepter toute interférence, notamment les interférences qui peuvent affecter son fonctionnement.

Radio Frequency (RF) Exposure Information

The radiated output power of the Wireless Device is below the Industry Canada (IC) radio frequency exposure limits. The Wireless Device should be used in such a manner such that the potential for human contact during normal operation is minimized.

This device has been evaluated for and shown compliant with the IC Specific Absorption Rate ("SAR") limits when operated in portable exposure conditions.

Informations concernant l'exposition aux fréquences radio (RF)

La puissance de sortie émise par l'appareil de sans fil est inférieure à la limite d'exposition aux fréquences radio d'Industry Canada (IC). Utilisez l'appareil de sans fil de façon à minimiser les contacts humains lors du fonctionnement normal.

Ce dispositif a été évalué pour et démontré conforme à la Taux IC d'absorption spécifique ("SAR") des limites lorsqu'il est utilisé dans des conditions d'exposition portatifs.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 5 mm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains IC: 4634A -6152EC “.

Information for the OEMs and Integrators

The following statement must be included with all versions of this document supplied to an OEM or integrator, but should not be distributed to the end user.

- 1) This device is intended for OEM integrators only.

- 2) Please see the full Grant of Equipment document for other restrictions.

—