Freeott GA-OTT

S C H E M A T I C Version 1.0

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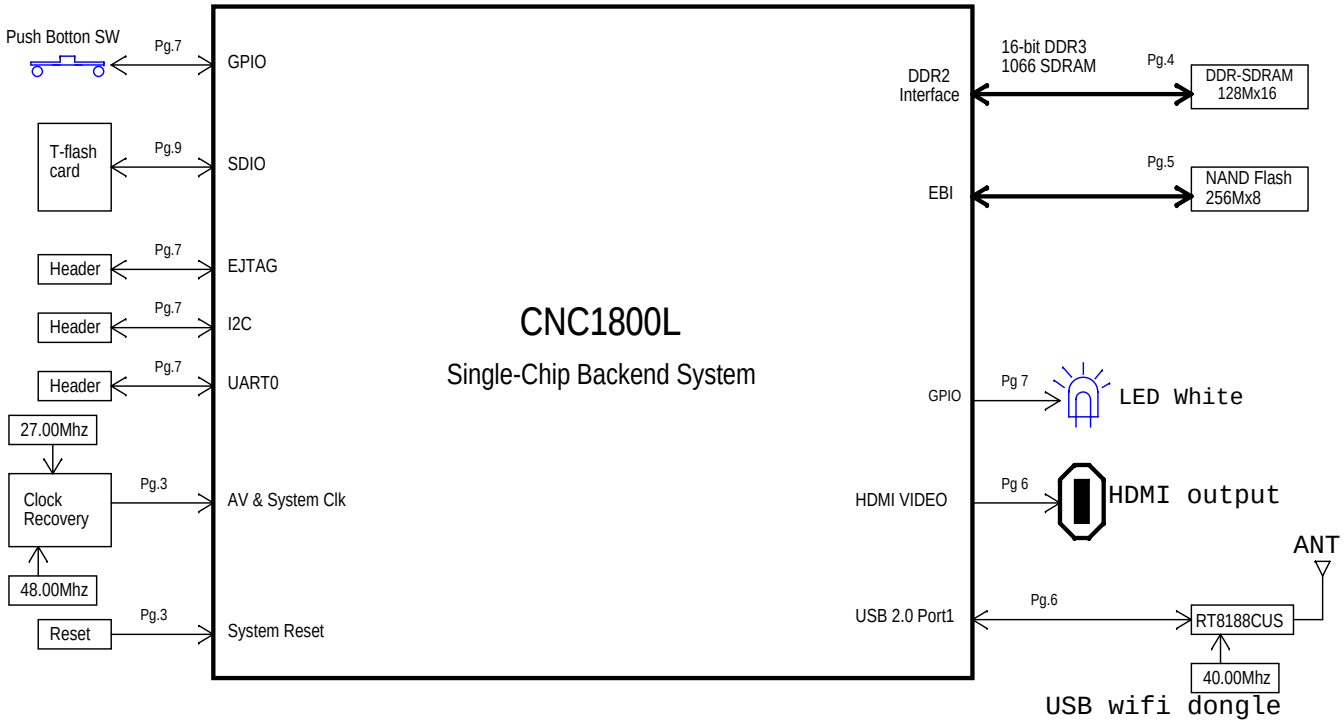
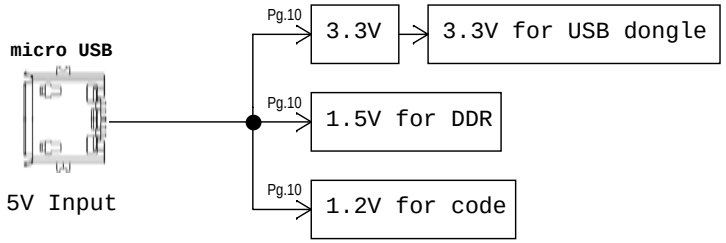
FreeOTT Block Diagram





Power Block

Revision History:

Rev	Description	Date	Approved
1	Preliminary Release	2012/03/14	

Layout Notes:

1. Discrete (especially resistors) should be placed close to Large components which are on the same schematic page

NOTES, UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES IN OHMS.
2. CAPACITANCE VALUES IN MICROFARADS.
3. REFERENCE DESIGNATORS USED.
4. ALL 0.1 uF CAPACITORS ARE DECOUPLING CAPS UNLESS OTHERWISE NOTED. THEY ARE SHOWN ON THE PAGE WITH THE INTEGRATED CIRCUITS THEY SHOULD BE PLACED NEAR.
5. BOARD PROPERTIES:
   - A. FR-4 RoHS COMPLIANT MATERIAL PER IPC-4101/129 OR BETTER
   - B. ALL SIGNAL LAYERS - 0.5 OZ CU
   - C. PLANE LAYERS - 0.5 OZ CU
   - D. IMPEDENCE CONTROL:
     50 OHMS +/- 10% SINGLE ENDED TRACES
     60 OHMS +/- 10% SINGLE ENDED TRACES
     90 OHMS +/- 10% SINGLE ENDED TRACES
     100 OHMS +/- 10% DIFFERENTIAL TRACES
   - E. LAYER STACKUP:

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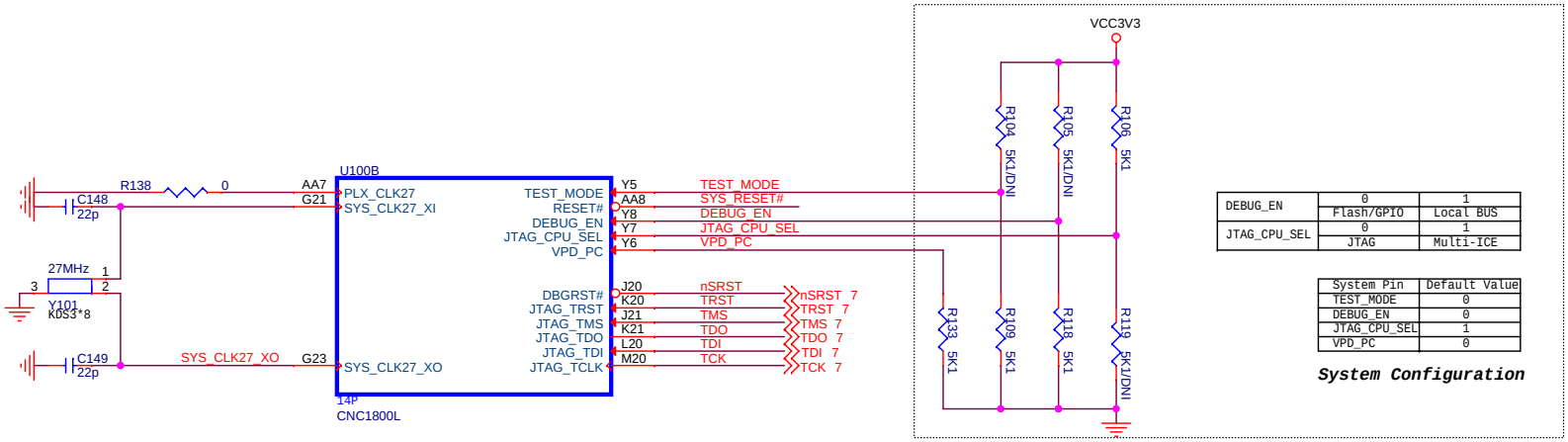
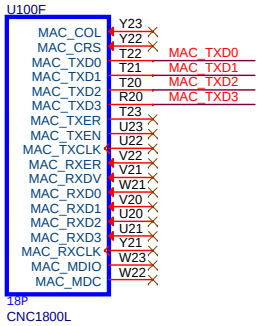


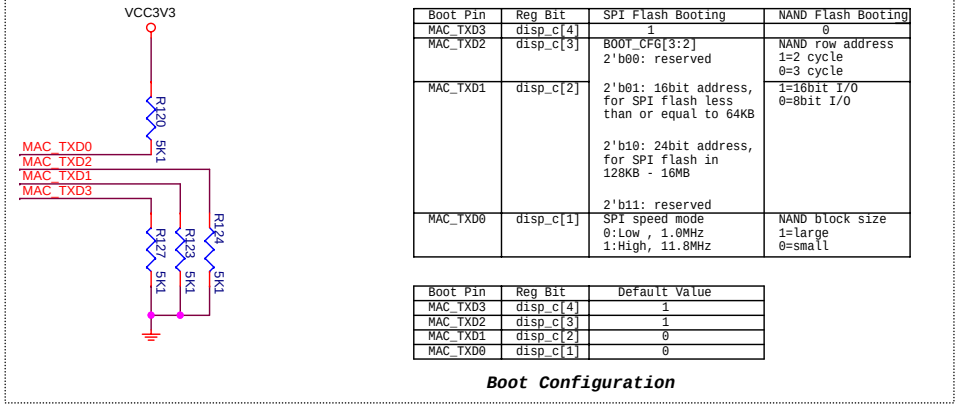
DEBUG_EN	0	1
	Flash/GPIO	Local BUS
JTAG_CPU_SEL	0	1
	JTAG	Multi-ICE

System Pin	Default Value
TEST_MODE	0
DEBUG_EN	0
JTAG_CPU_SEL	1
VPD_PC	0

System Configuration

Ethernet Interface

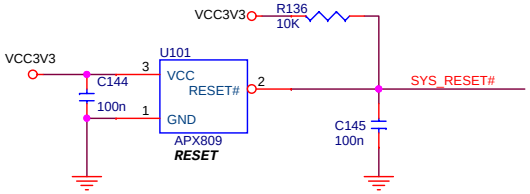




Boot Pin	Reg Bit	SPI Flash Booting	NAND Flash Booting
MAC_TXD3	disp_c[4]	1	0
MAC_TXD2	disp_c[3]	BOOT_CFG[3:2] 2'b00: reserved	NAND row address 1=2 cycle 0=3 cycle
MAC_TXD1	disp_c[2]	2'b01: 16bit address, for SPI flash less than or equal to 64KB 2'b10: 24bit address, for SPI flash in 128KB - 16MB 2'b11: reserved	1=16bit I/O 0=8bit I/O
MAC_TXD0	disp_c[1]	SPI speed mode 0:Low , 1.0MHz 1:High, 11.8MHz	NAND block size 1=large 0=small

Boot Pin	Reg Bit	Default Value
MAC_TXD3	disp_c[4]	1
MAC_TXD2	disp_c[3]	1
MAC_TXD1	disp_c[2]	0
MAC_TXD0	disp_c[1]	0

Boot Configuration



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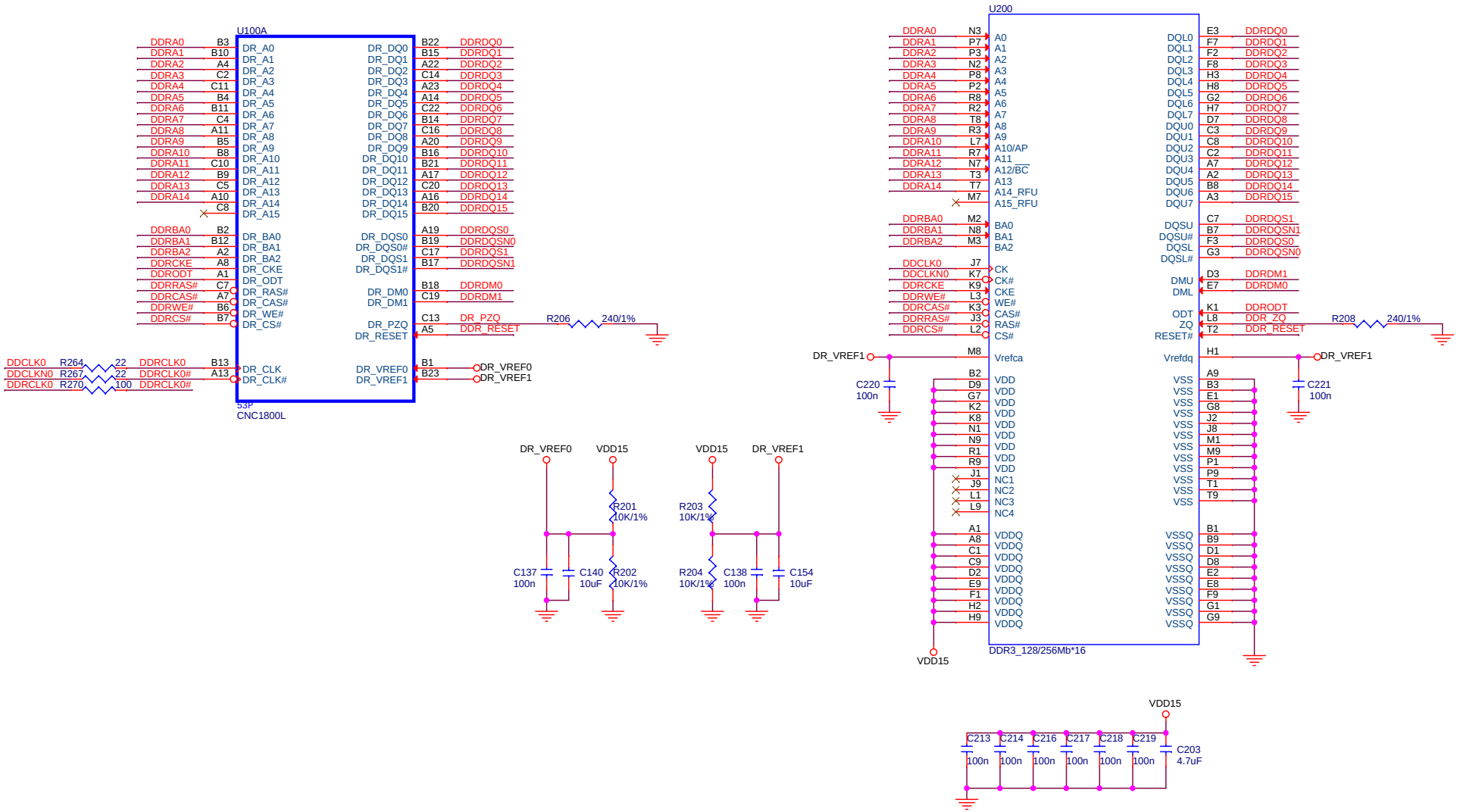

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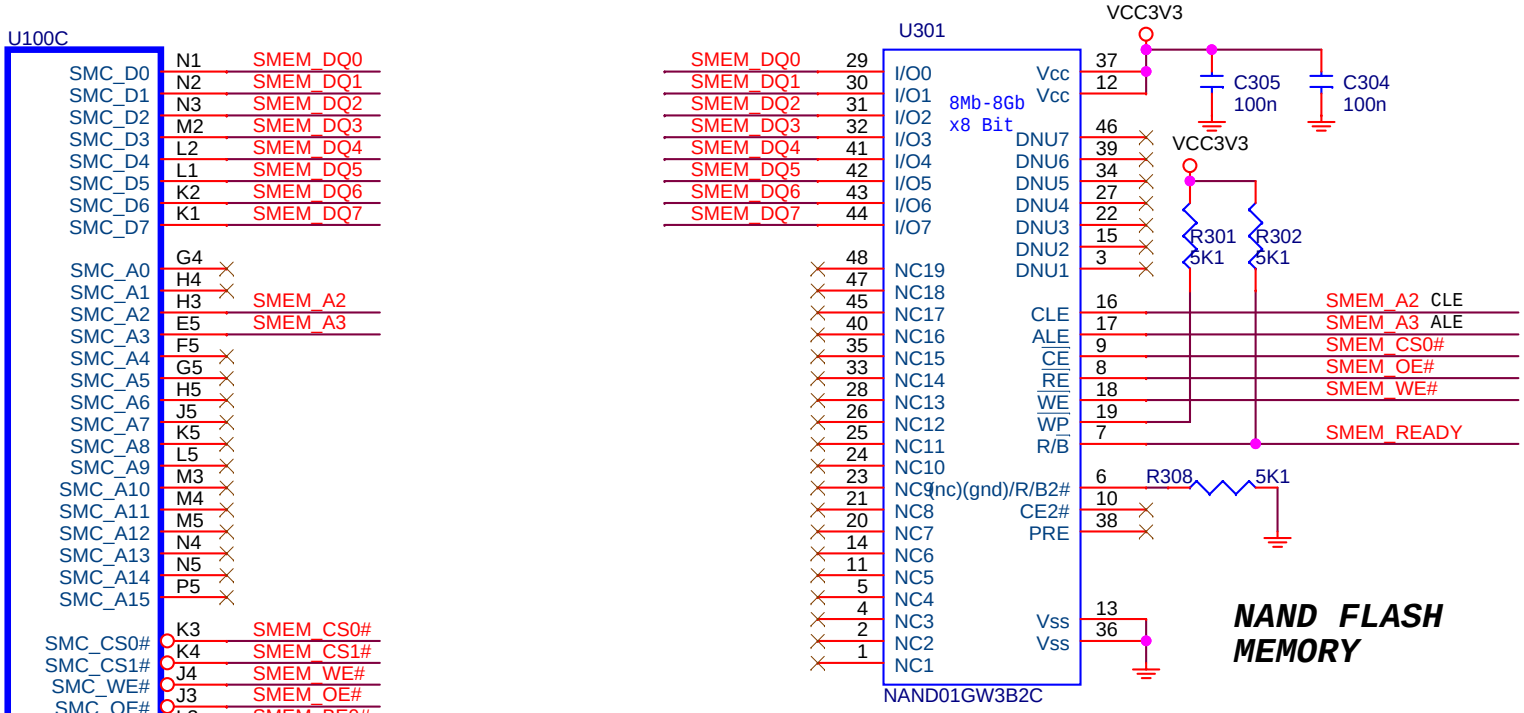

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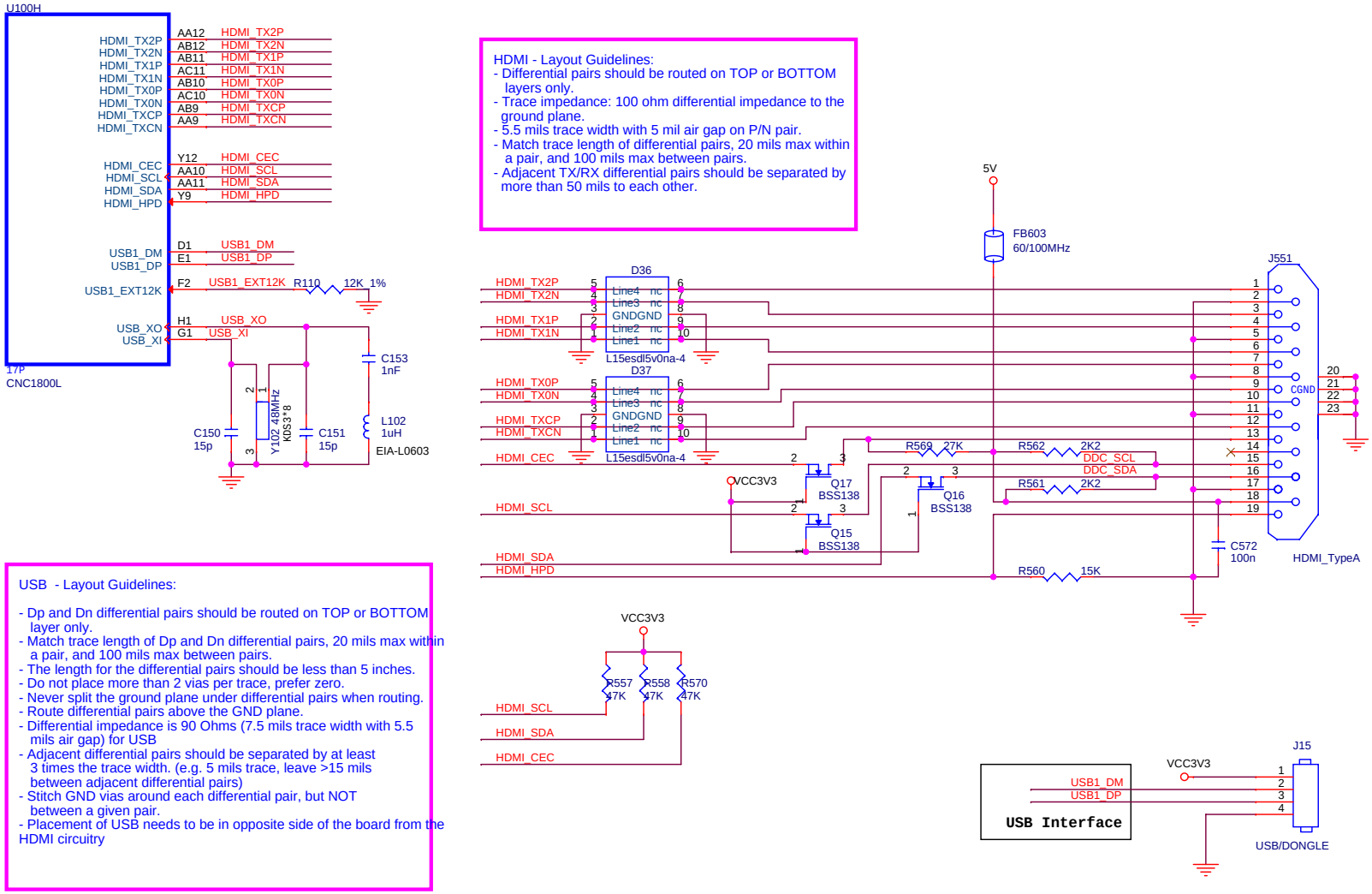

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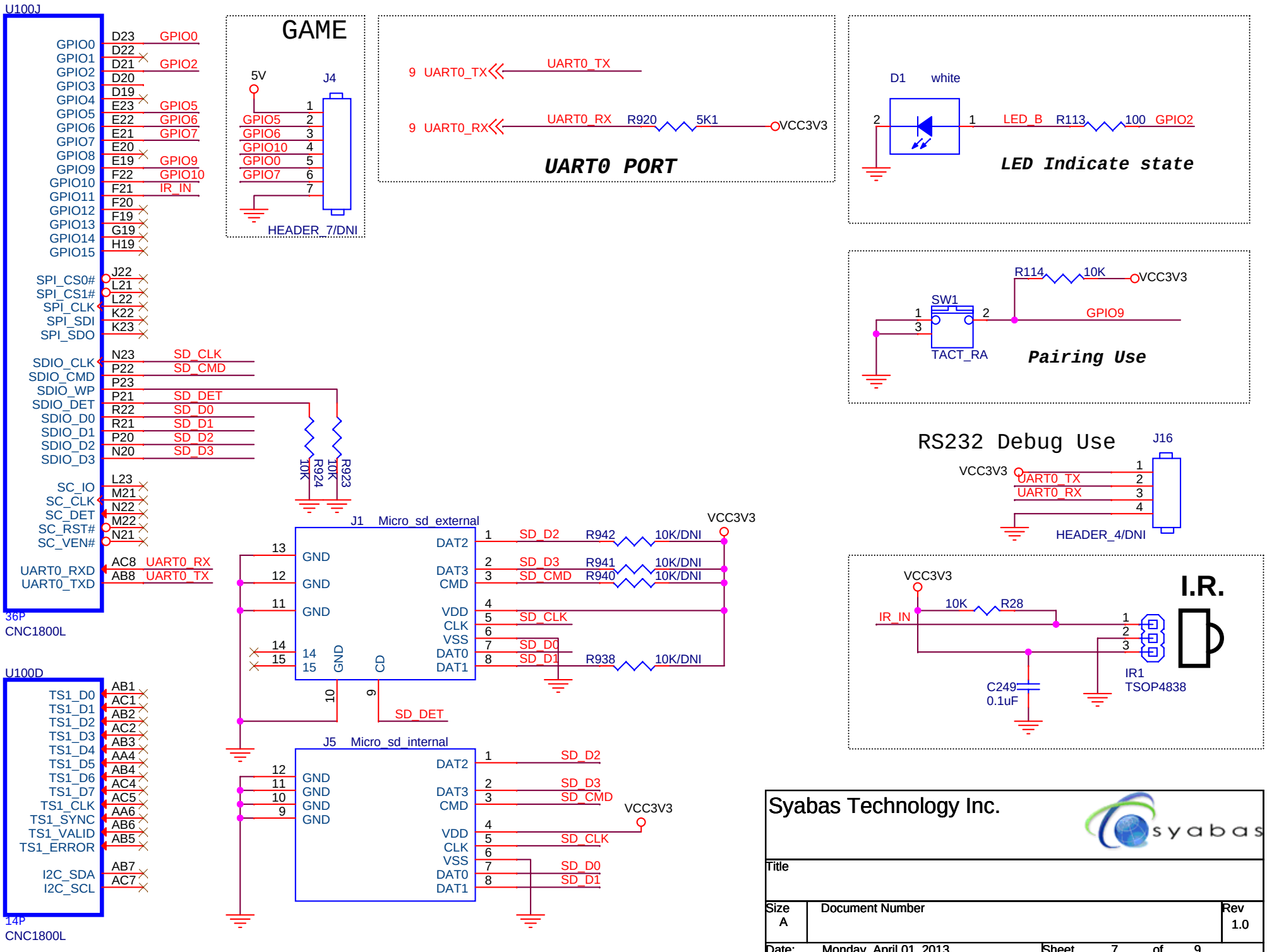
U100J
GPIO0 D23 GPIO0
GPIO1 D22
GPIO2 D21 GPIO2
GPIO3 D20
GPIO4 D19
GPIO5 E23 GPIO5
GPIO6 E22 GPIO6
GPIO7 E21 GPIO7
GPIO8 E20
GPIO9 E19 GPIO9
GPIO10 F22 GPIO10
GPIO11 F21 IR_IN
GPIO12 F20
GPIO13 F19
GPIO14 G19
GPIO15 H19
SPI_CS0# J22
SPI_CS1# L21
SPI_CLK L22
SPI_SDI K22
SPI_SDO K23
SDIO_CLK N23 SD_CLK
SDIO_CMD P22 SD_CMD
SDIO_WP P23
SDIO_DET P21 SD_DET
SDIO_D0 R22 SD_D0
SDIO_D1 R21 SD_D1
SDIO_D2 P20 SD_D2
SDIO_D3 N20 SD_D3
SC_IO L23
SC_CLK M21
SC_DET N22
SC_RST# M22
SC_VEN# N21
UART0_RXD AC8 UART0_RX
UART0_TXD AB8 UART0_TX
36P
CNC1800L
U100D
TS1_D0 AB1
TS1_D1 AC1
TS1_D2 AB2
TS1_D3 AC2
TS1_D4 AB3
TS1_D5 AA4
TS1_D6 AB4
TS1_D7 AC4
TS1_CLK AC5
TS1_SYNC AA6
TS1_VALID AB6
TS1_ERROR AB5
I2C_SDA AB7
I2C_SCL AC7
14P
CNC1800L
GAME
5V
J4
GPIO5 1
GPIO6 2
GPIO10 3
GPIO0 4
GPIO7 5
6
7
HEADER_7/DNI
9 UART0_TX
UART0_TX
9 UART0_RX
UART0_RX R920 5K1 VCC3V3
UART0 PORT
D1 white
2
1 LED_B R113 100 GPIO2
LED Indicate state
R114 10K VCC3V3
SW1
1
3
2
GPIO9
TACT_RA
Pairing Use
R924 10K
R923 10K
J1 Micro_sd_external
13 GND
12 GND
11 GND
14 GND
15 GND
CD
10
9
SD_DET
DAT2 1 SD_D2 R942 10K/DNI
DAT3 2 SD_D3 R941 10K/DNI
CMD 3 SD_CMD R940 10K/DNI
VDD 4
CLK 5 SD_CLK
VSS 6
DAT0 7 SD_D0
DAT1 8 SD_D1 R938 10K/DNI
VCC3V3
J5 Micro_sd_internal
12 GND
11 GND
10 GND
9 GND
DAT2 1 SD_D2
DAT3 2 SD_D3
CMD 3 SD_CMD
VDD 4
CLK 5 SD_CLK
VSS 6
DAT0 7 SD_D0
DAT1 8 SD_D1
VCC3V3
RS232 Debug Use
J16
VCC3V3
1
UART0_TX 2
UART0_RX 3
4
HEADER_4/DNI
VCC3V3
10K R28
IR_IN
1
2
3
C249
0.1uF
IR1
TSOP4838
I.R.
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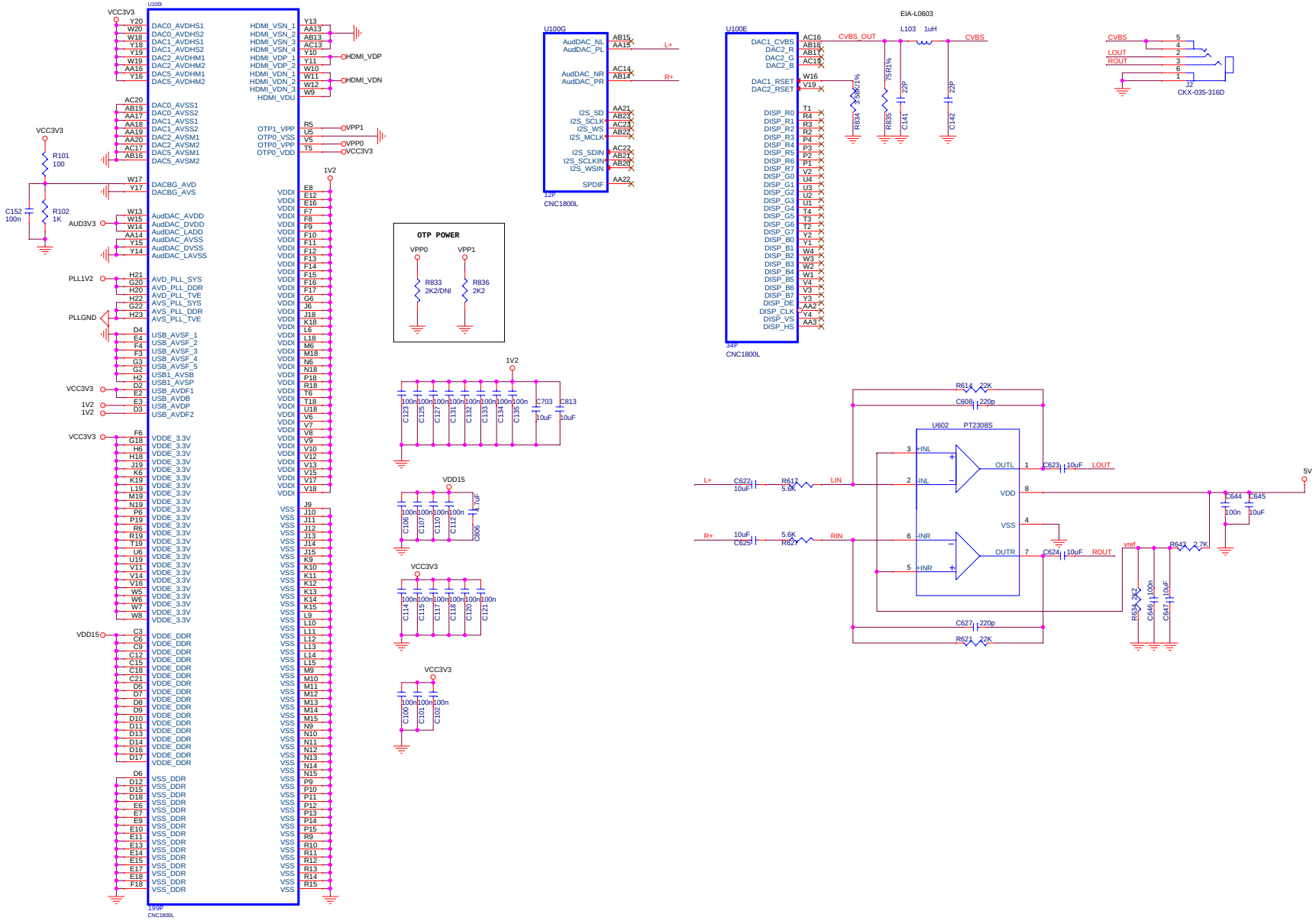

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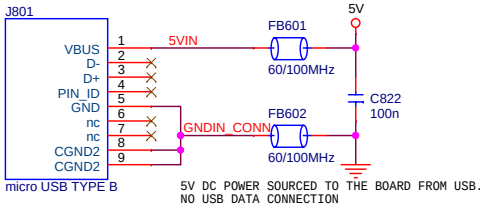
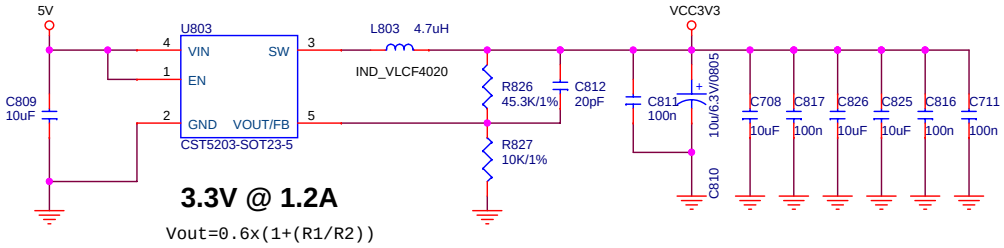
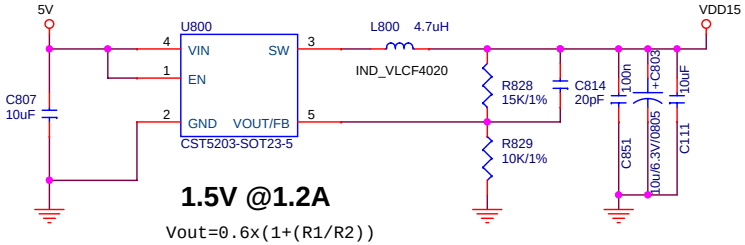
5V @ 500mA





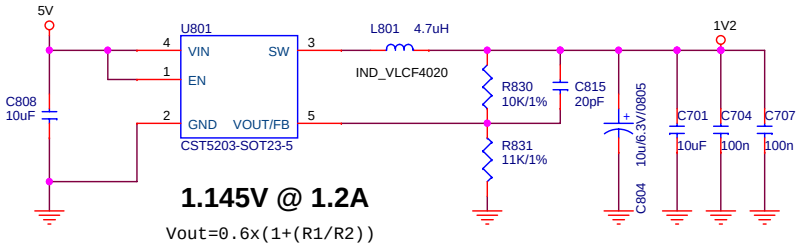
3.3V @ 1.2A

Vout=0.6x(1+(R1/R2))



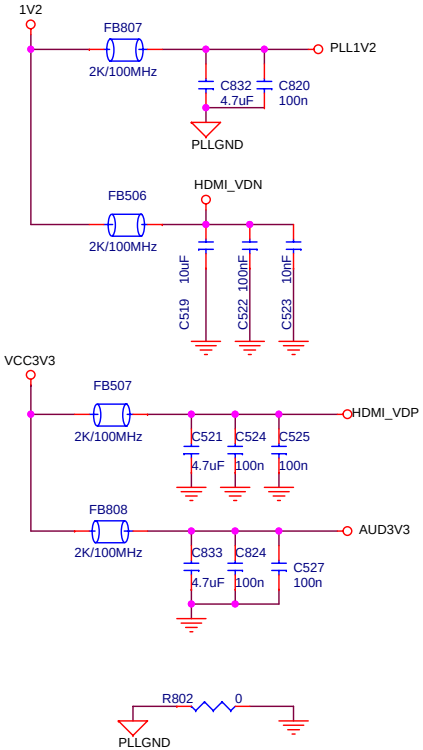
1.5V @1.2A

Vout=0.6x(1+(R1/R2))



1.145V @ 1.2A

Vout=0.6x(1+(R1/R2))



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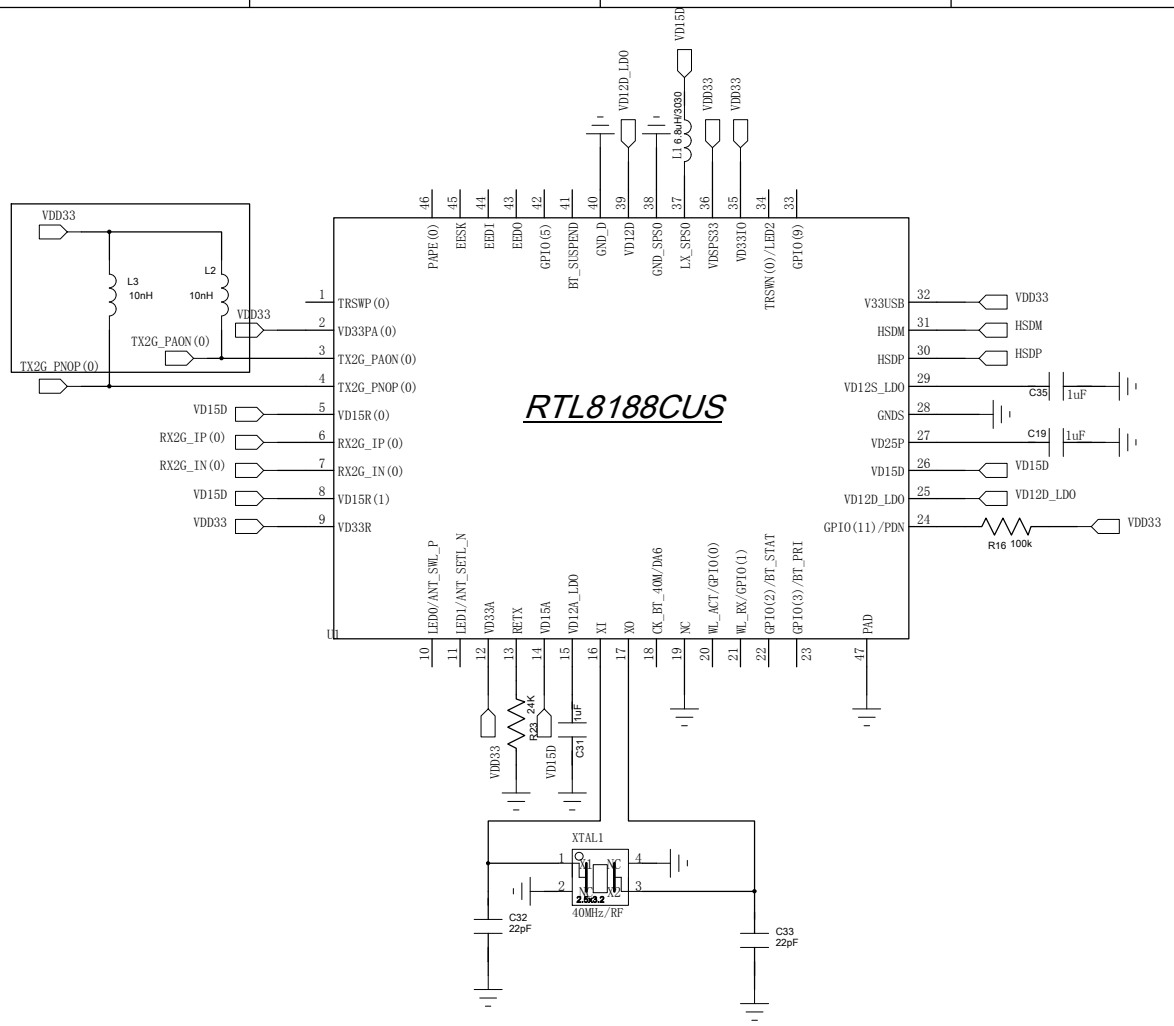

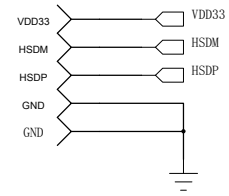

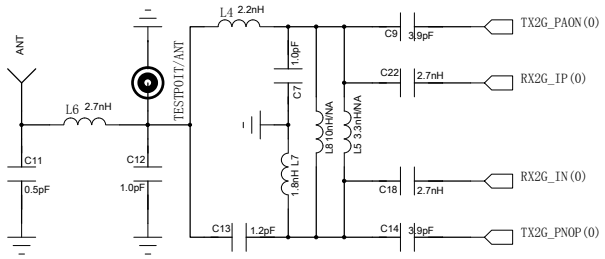

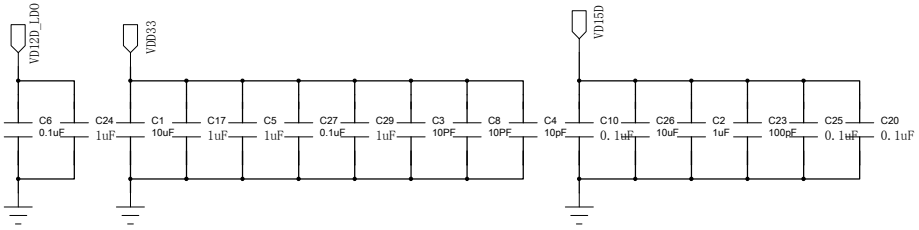

REVISION RECORD			
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DRAWN: Lavender	DATED: 2011.3.18	
CHECKED:	DATED:	
QUALITY CONTROL:	DATED:	
RELEASED:	DATED:	

COMPANY: RL-LINK			
TITLE: RL-UM02BS-8188CUSB			
CODE:	SIZE: B	DRAWING NO: R&D 2011-3-18-01	REV: 1.0
SCALE:	SHEET: 1 OF 1		