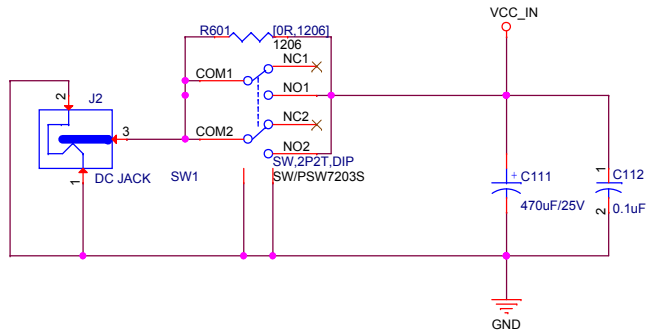
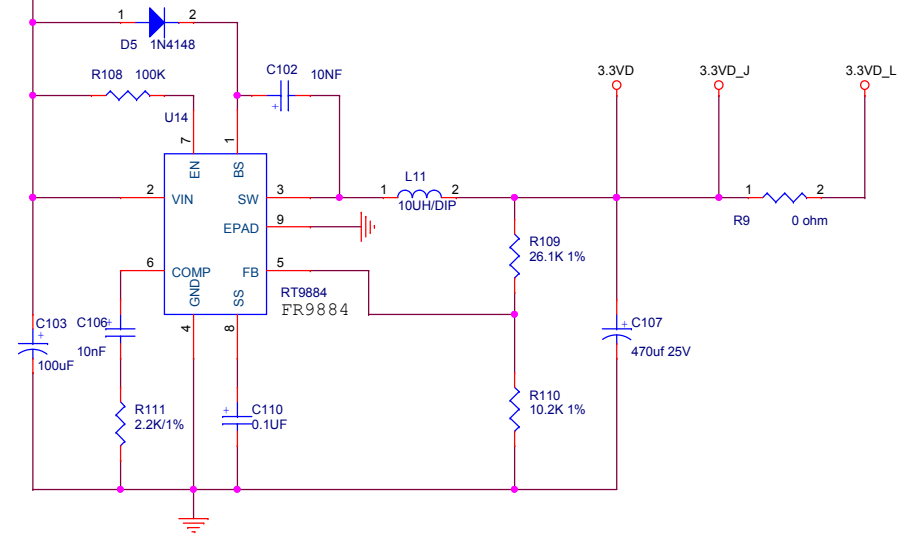


### 7.5V~~12V DC INPUT



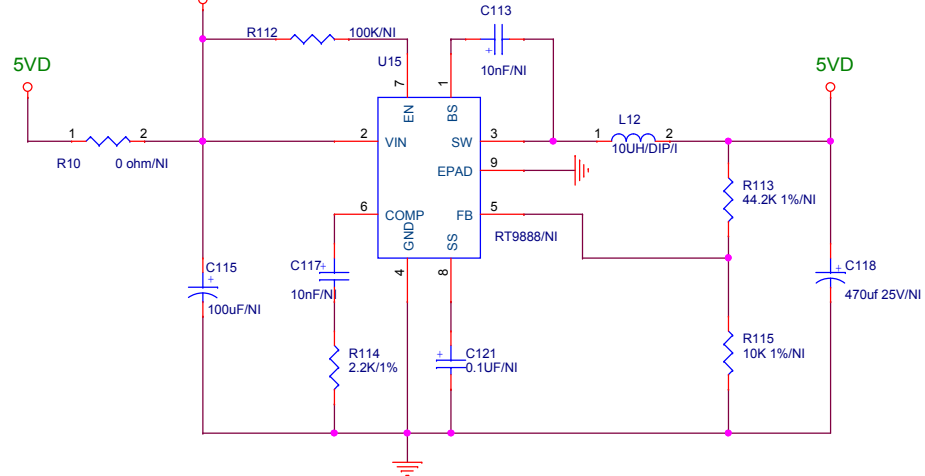
### 7.5V~~12V DC ADAPTER

### VCC\_IN



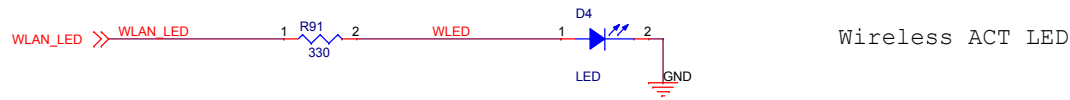
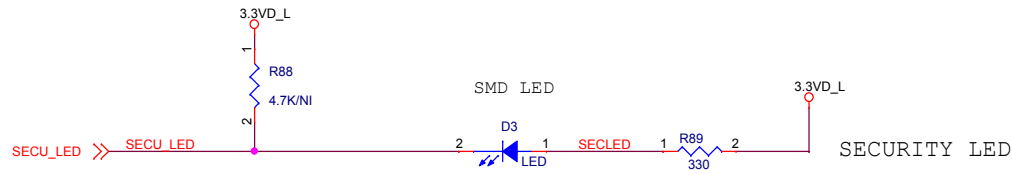
$$0.925V * (1 + 26.1 / 10.2) = 3.3V$$

### VCC\_IN

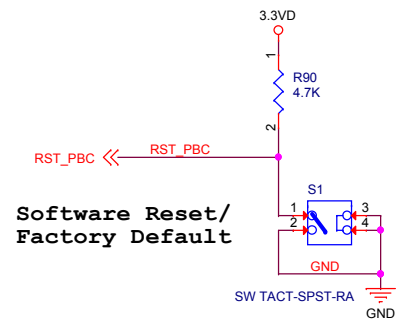


$$0.925V * (1 + 44.2 / 10) = 5V$$

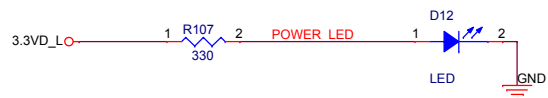
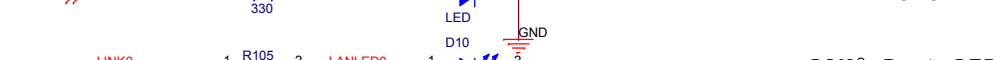
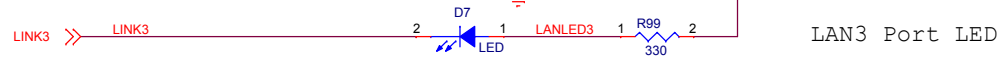
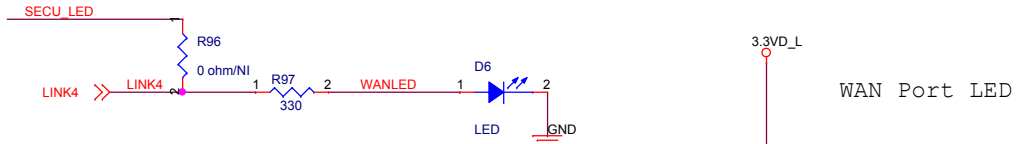
GPIO13



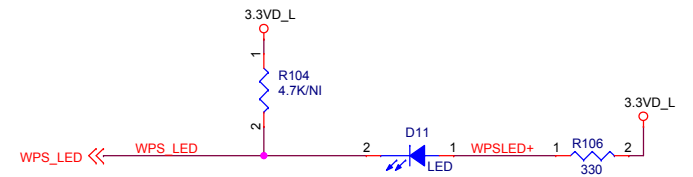
GPIO10

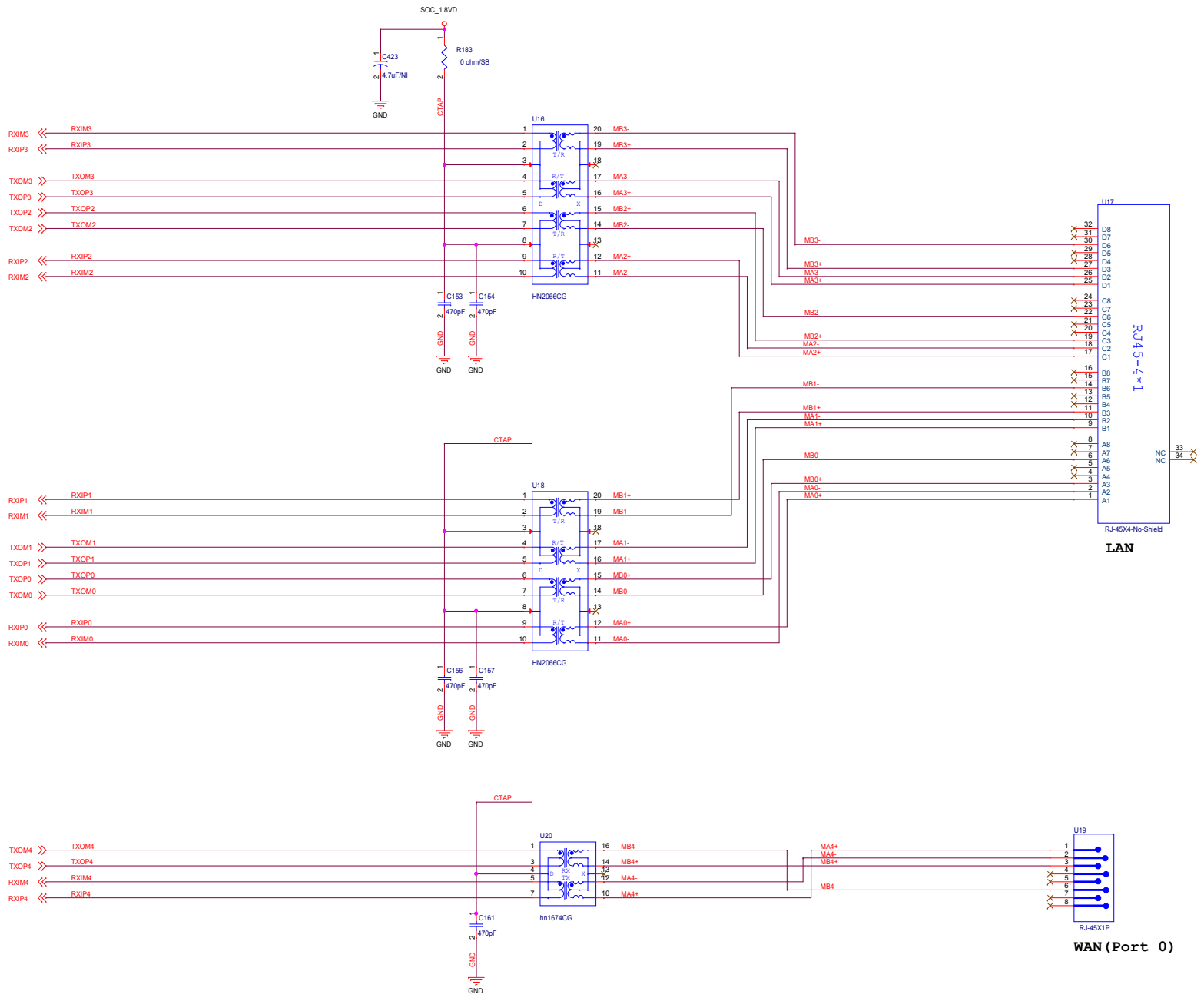


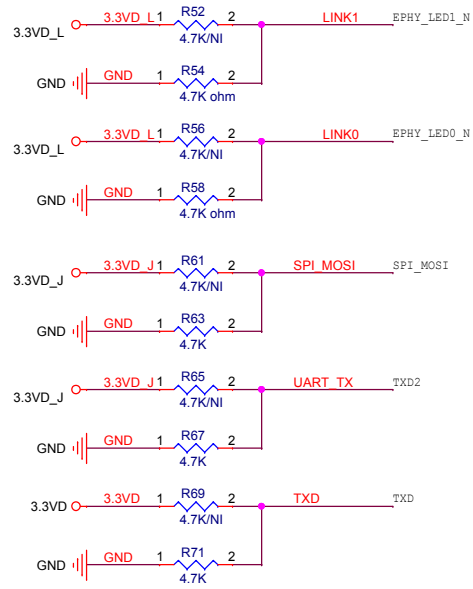
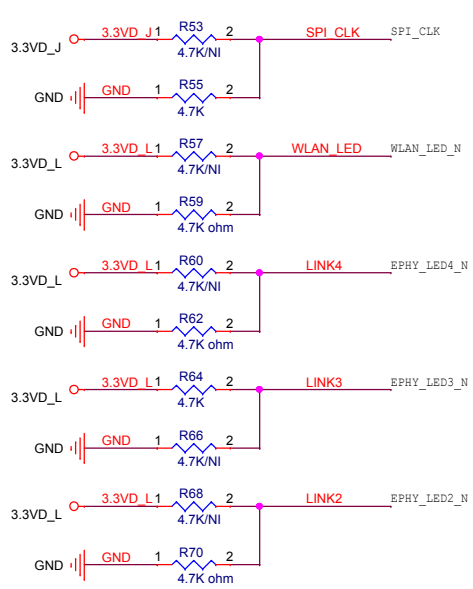
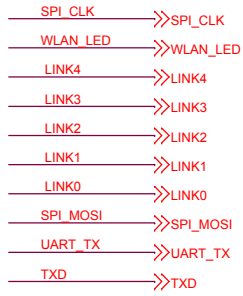
GPIO9



GPIO14

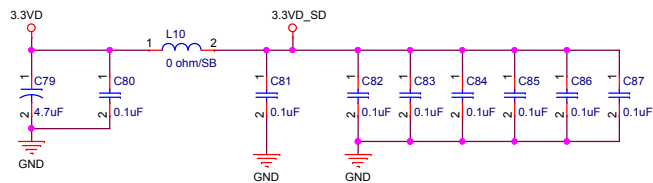
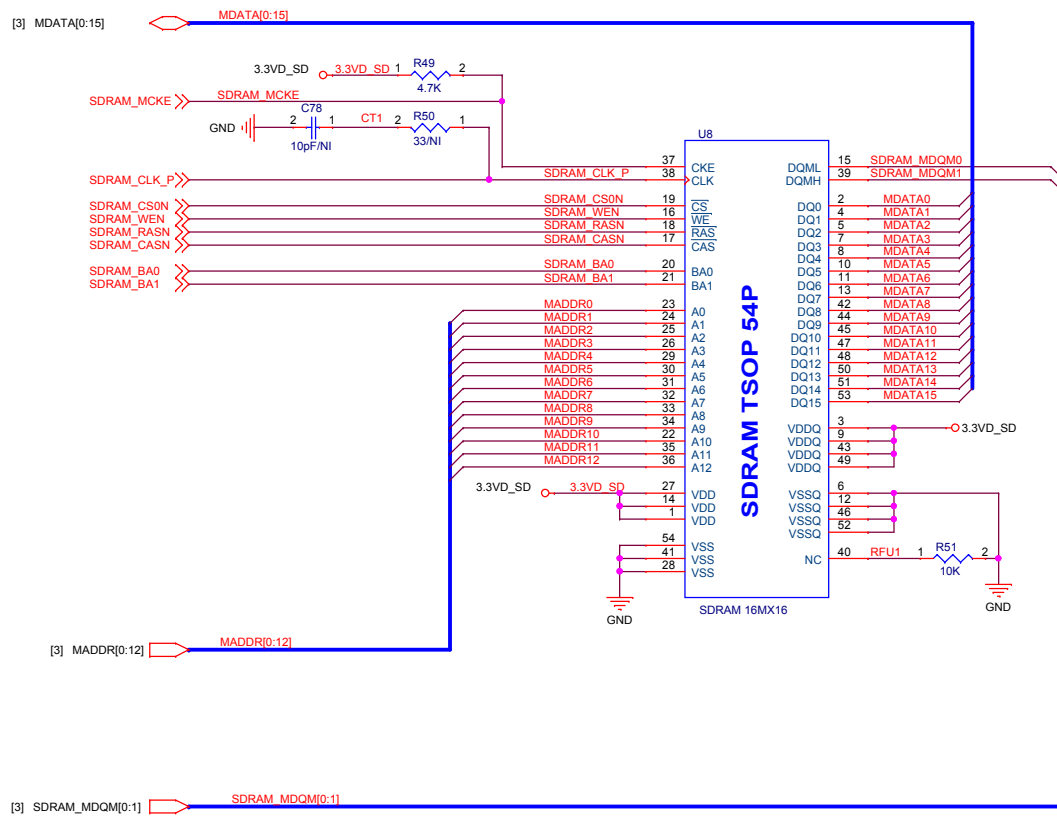


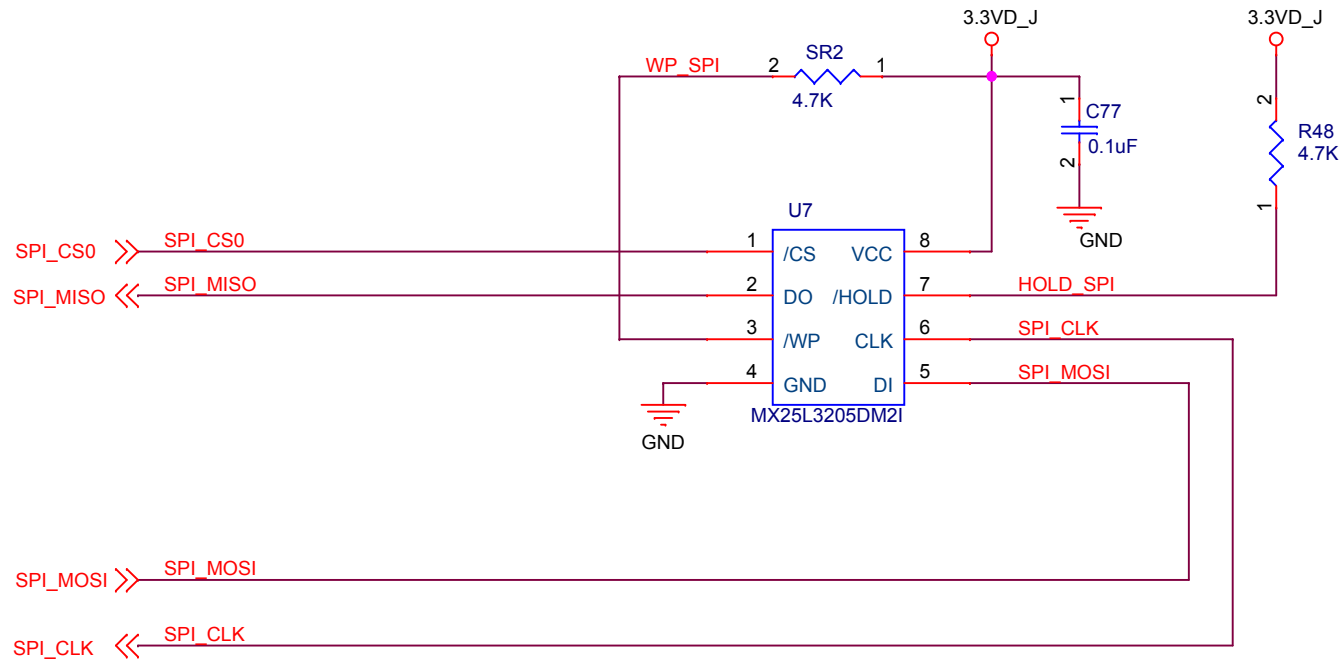


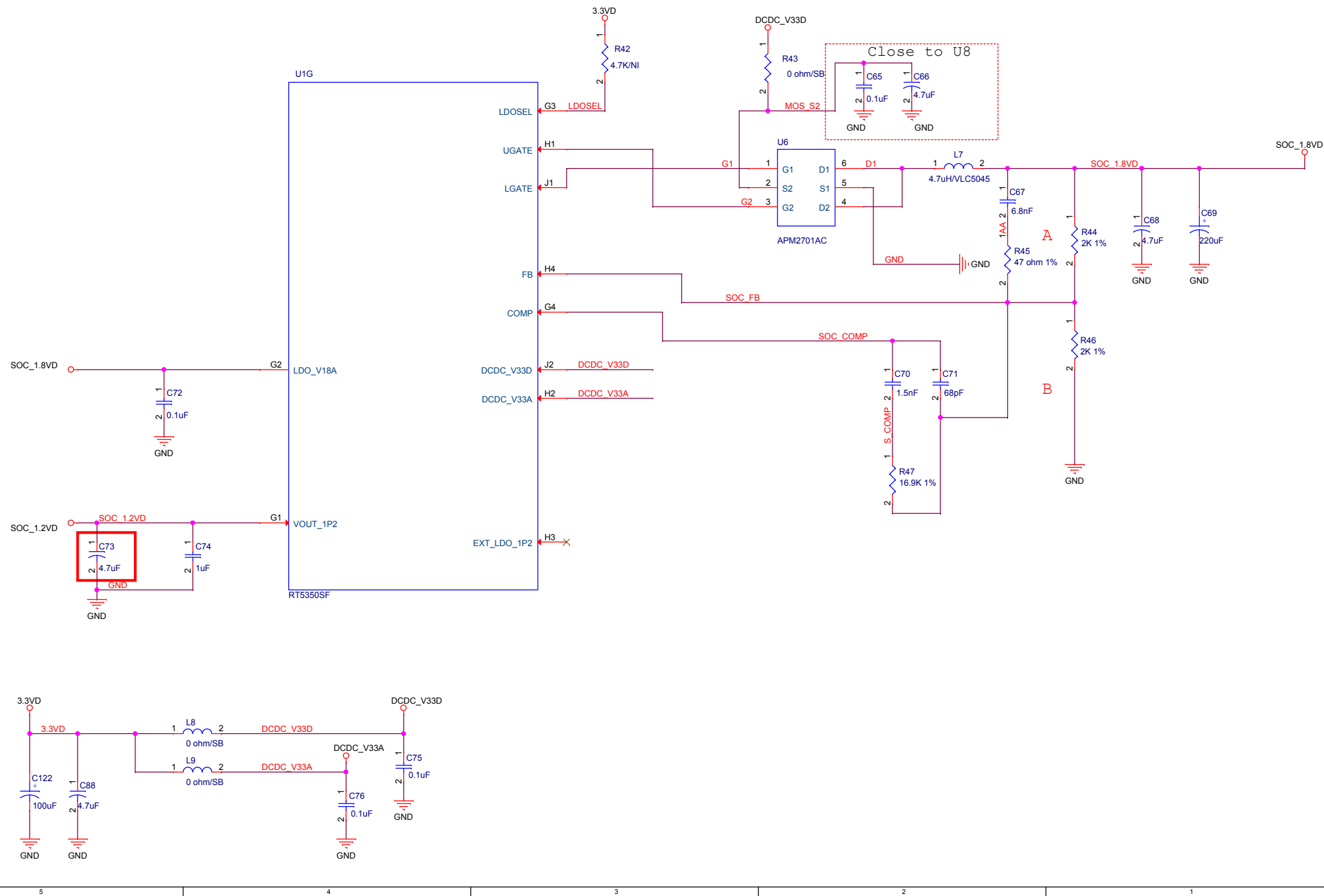


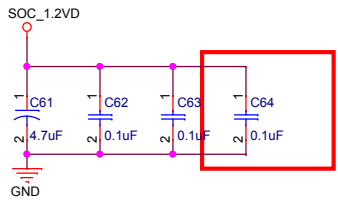
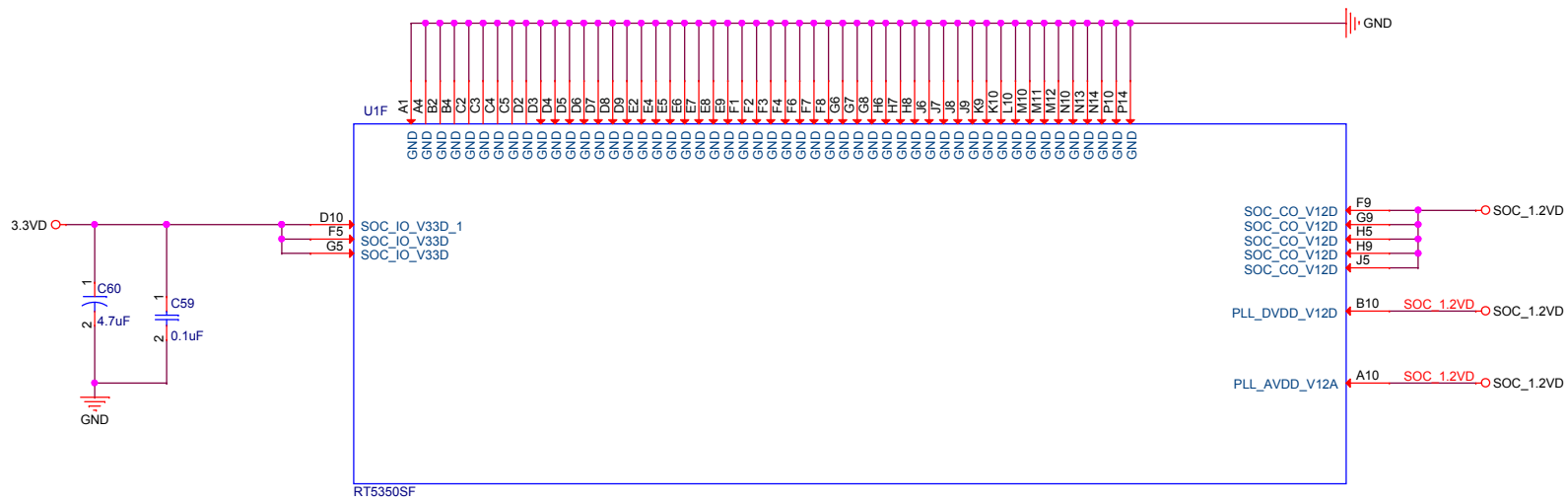
## RT5350 Boot Up Strapping

Pin Name	Description	Value=0	Value=1
SPI_CLK	XTAL_FREQ_HI	20MHz	40MHz
WLAN_LED_N	Big Endian	Little Endian	Big Endian
EPHY_LED4_N	DRAM_FROM_EE	from boot strapping	from EEPROM
{EPHY_LED3_N, EPHT_LED2_N}	DRAM_SIZE	INIC/AP(SDR) 0: 2MB/8MB 1: 8MB/16MB 2: 16MB/32MB 3: 32MB/64MB	
{EPHY_LED1_N, EPHT_LED0_N}	CPU_CLK_SEL	CPU clock select 0: 360MHz 1: Reserved 2: 320MHz 3: 300MHz	
{SPI_MOSI, TXD2, TXD}	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes 0 : Normal mode(boot fromSPI serial flash) 1 : iNIC-USB mode 2 : Reserved 3 : Reserved 4 : Reserved 5 : iNIC-PHY mode 6 : SCAN mode 7 : TEST/DEBUG mode	

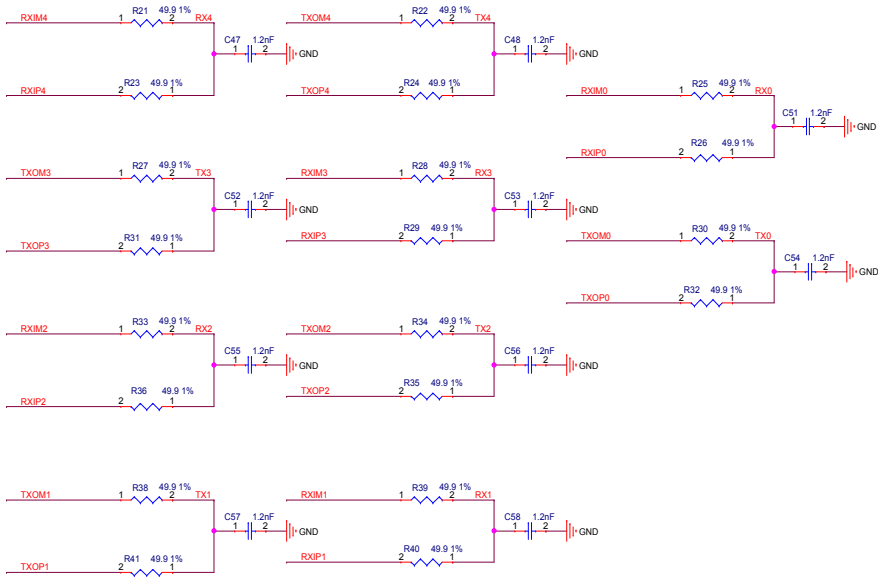
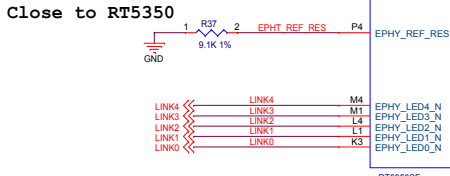
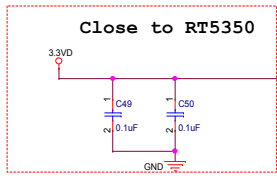












PHY address 5~d0 -> Internal PHY for port 0

PHY address 5~d1 -> Internal PHY for port 1

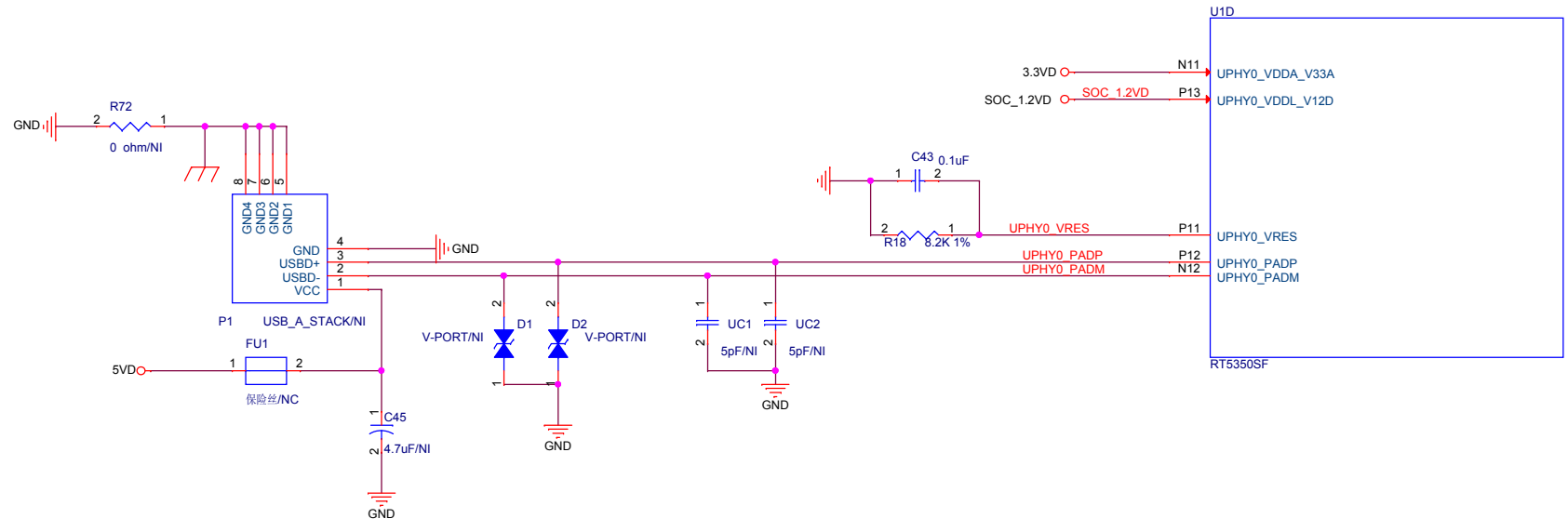
PHY address 5~d2 -> Internal PHY for port 2

PHY address 5~d3 -> Internal PHY for port 3

PHY address 5~d4 -> Internal PHY for port 4

PHY address 5~d5 -> default for the external Port 5

PHY address 5~d5 ~ 5~d31 are free for the external PHY.



R72  
0 ohm/N1

GND4  
GND3  
GND2  
GND1

GND  
USB+  
USB-  
VCC

P1  
USB\_A\_STACK/N1  
FU1  
保險絲/NC

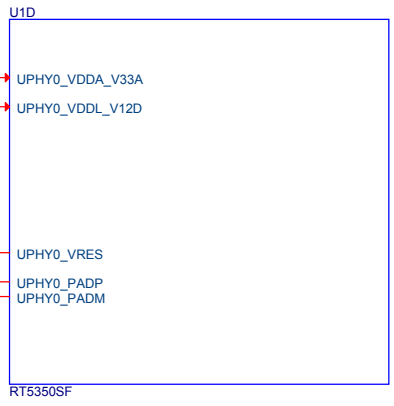
C45  
4.7uF/N1

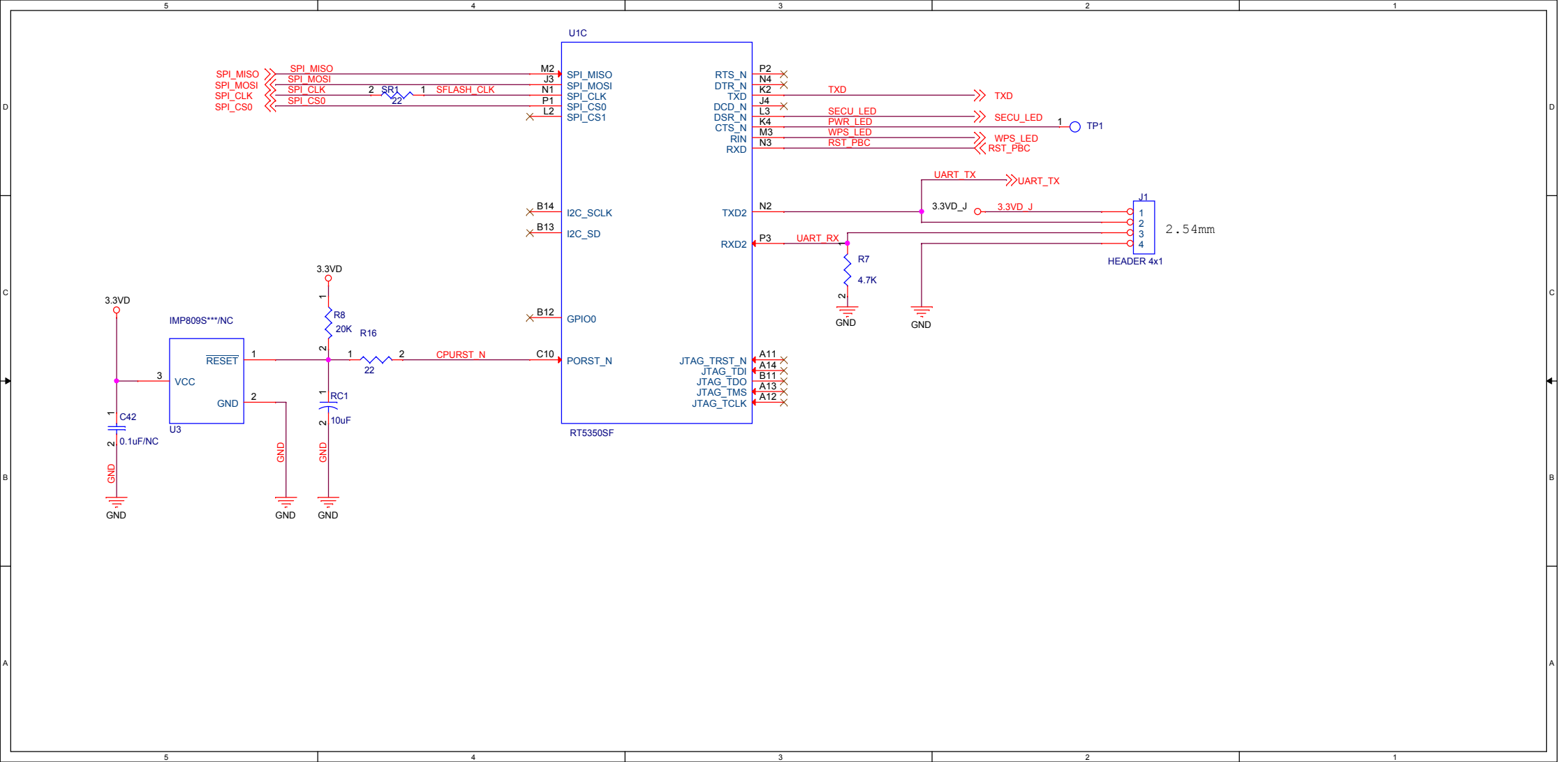
V-PORT/N1  
D1  
D2  
V-PORT/N1

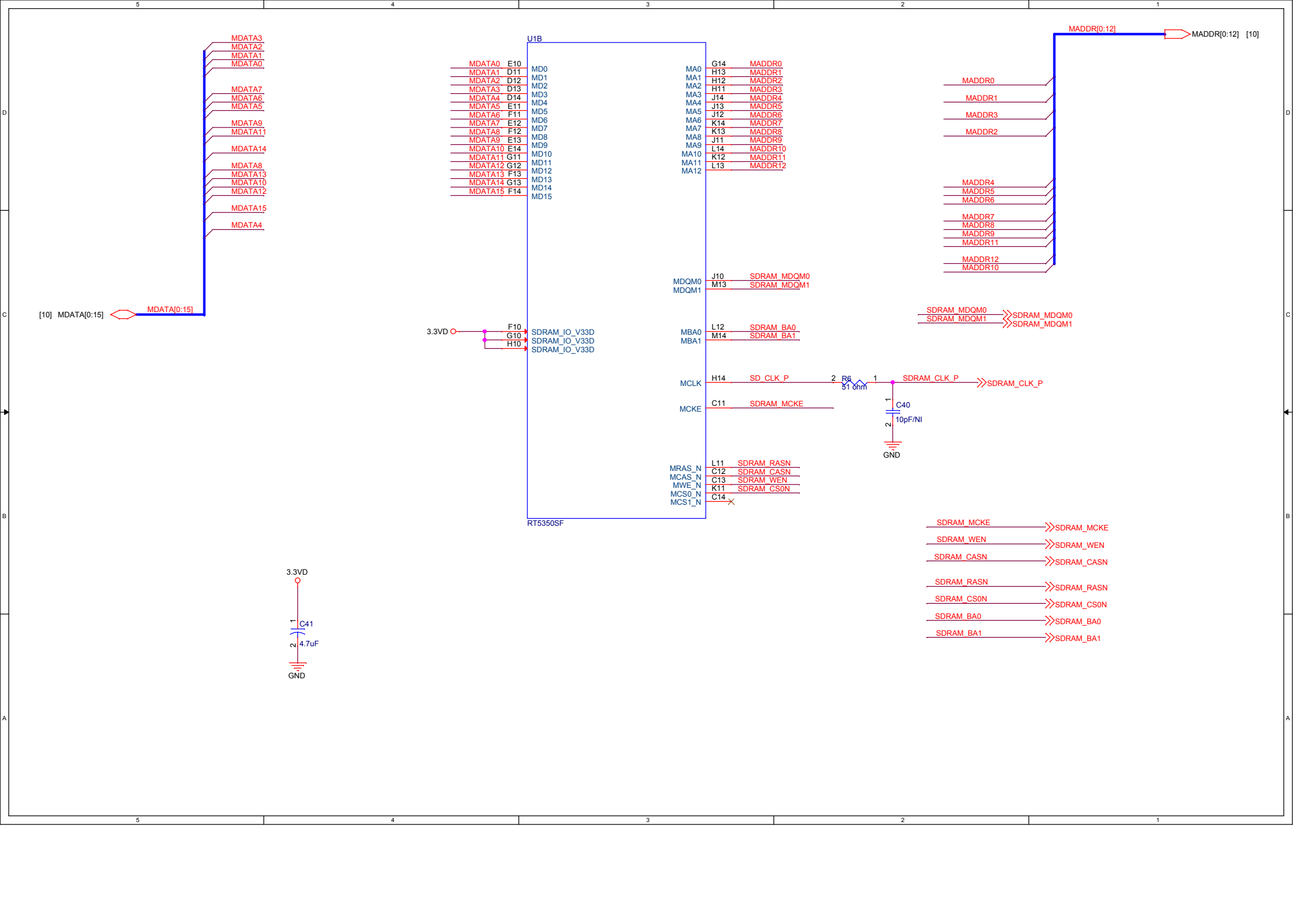
C43  
0.1uF  
R18  
8.2K 1%

3.3VD  
SOC\_1.2VD

UPHY0\_VRES  
UPHY0\_PADP  
UPHY0\_PADM

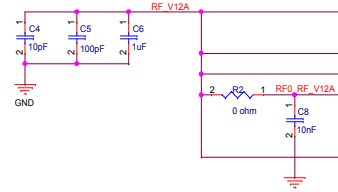






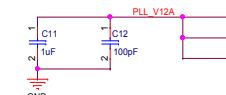
LDORF\_Out

C8 layout close D8

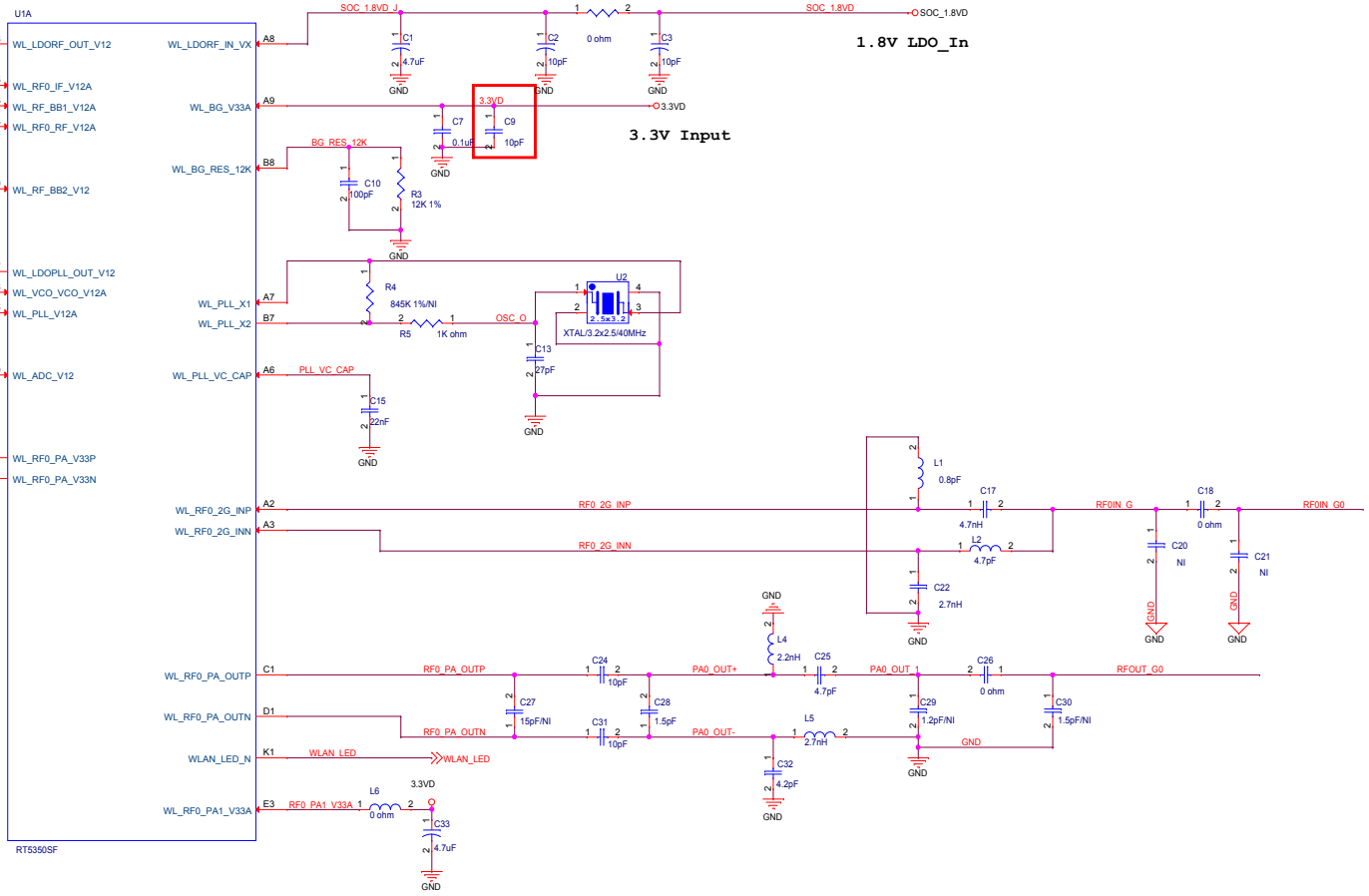
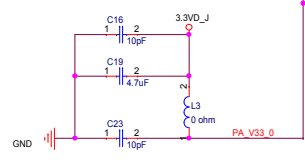


C11 layout close C7

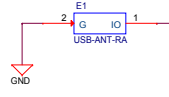
LDOPLL\_Out



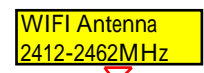
L34 ,C252 layout close C1 and F1



(ANTENNA1) (RX1)



(ANTENNA1) (TX0/RX0)



(ANTENNA0) (TX0/RX0)

