Theory Description

MT-SA-WR752

Date: 2013-08-28

Approved	Tested
Director	RD
Lode	Liuchiyuan

Revision History:

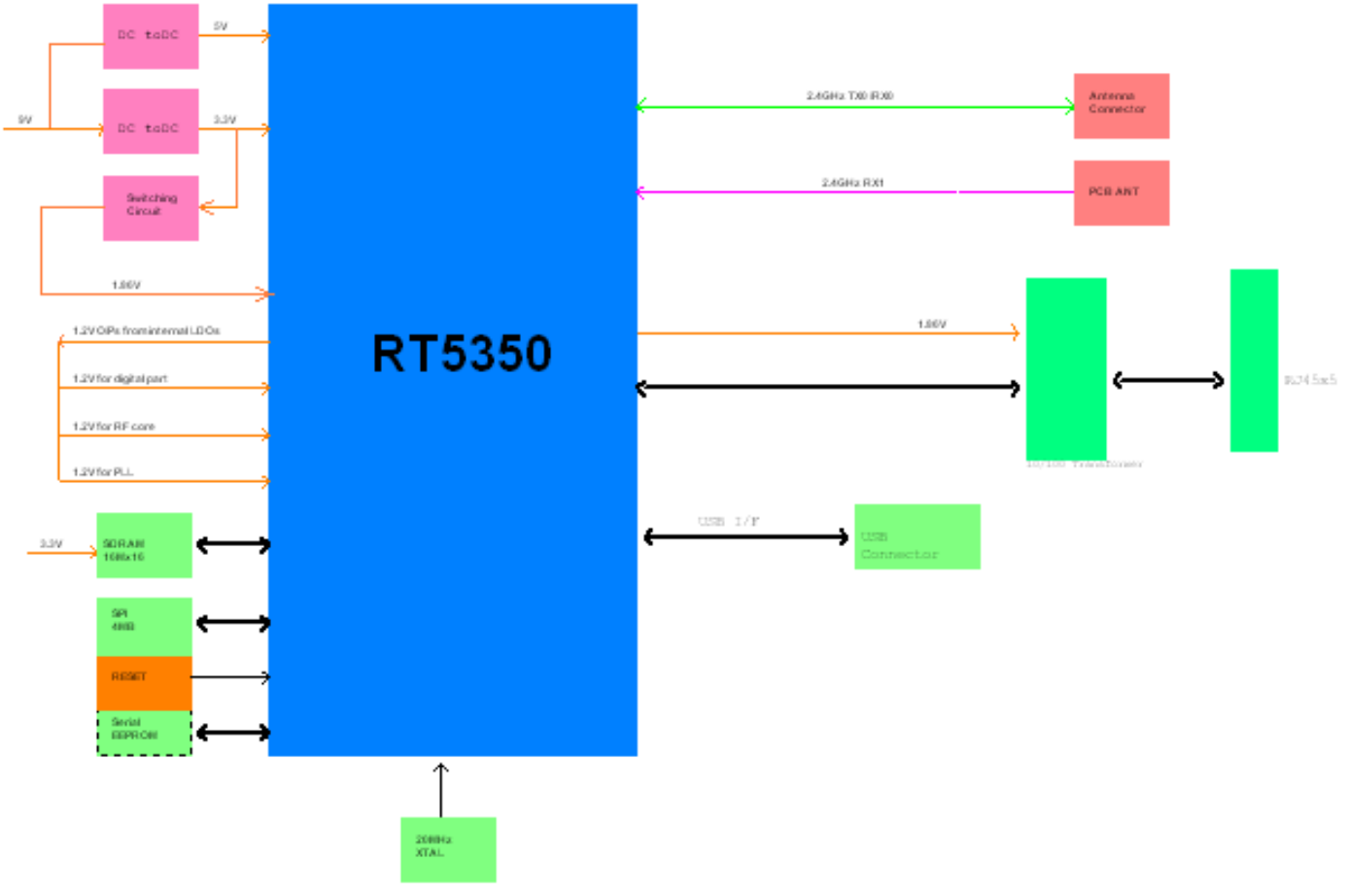
Version	Date	Change Description
V1.0	2013-08-28	Initial draft

Table of Contents:

1.Overview

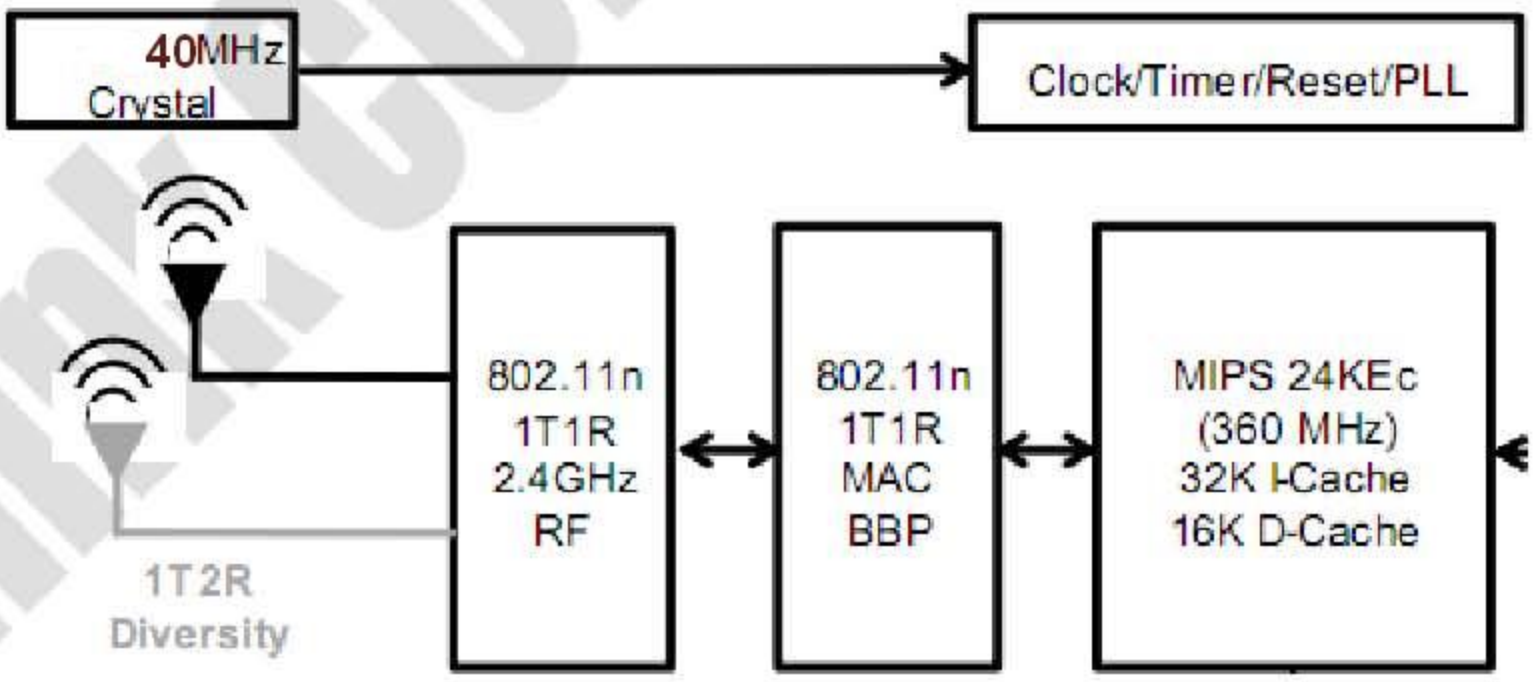
MT-SA-WR752's CPU is Ralink RT5350, The RT5350 SOC combines Ralink's 802.11n draft compliant 1T1R MAC/BBP/PA/RF, a high performance 360MHz MIPS24KEc CPU core, 5-ports integrated 10/100 Ethernet Swtich/PHY and an USB Host/Device. With the RT5350, there are very few external components required for 2.4GHz 11n wireless products. The RT5350 employs Ralink 2nd generation 11n technologies for longer range and better throughput. The embedded high performance CPU can process advanced applications effortlessly, such as WIFI data processing without overloading the host processor. In addition, the RT5350 has rich hardware interfaces (SPI/ I2S/ I2C/ PCM/ UART/ USB) to enable many possible applications.

2.Block Diagram



3.RF interface description

The RT5350 SoC embeds Ralink's market proven 802.11n 1T1R MAC/BBP/RF to provide a 300Mbps PHY rate on the wireless LAN interface. The MAC design employs a highly efficient DMA engine and hardware data processing accelerators, which free the CPU for user applications. The 802.11n 1T1R MAC/BBP/RF is designed to support standards based features in the area of security, quality of service and international regulation resulting in an enhanced end user experience.



4.Ethernet interface Description

Support IEEE 802.3 full duplex flow control

5 10/100Mbps PHY

Support Spanning Tree port states

Support 1K-MAC address table with direct or XOR hash

QoS

Four priorities queues per port

Packet classification based on incoming port, IEEE 802.1p or IP ToS/DSCP

Strict-Priority Queue (PQ) and Weighted Round Robin (WRR)

VLAN

Port Base VLAN

Double VLAN tagging

802.1q tag VLAN

16 VIDs

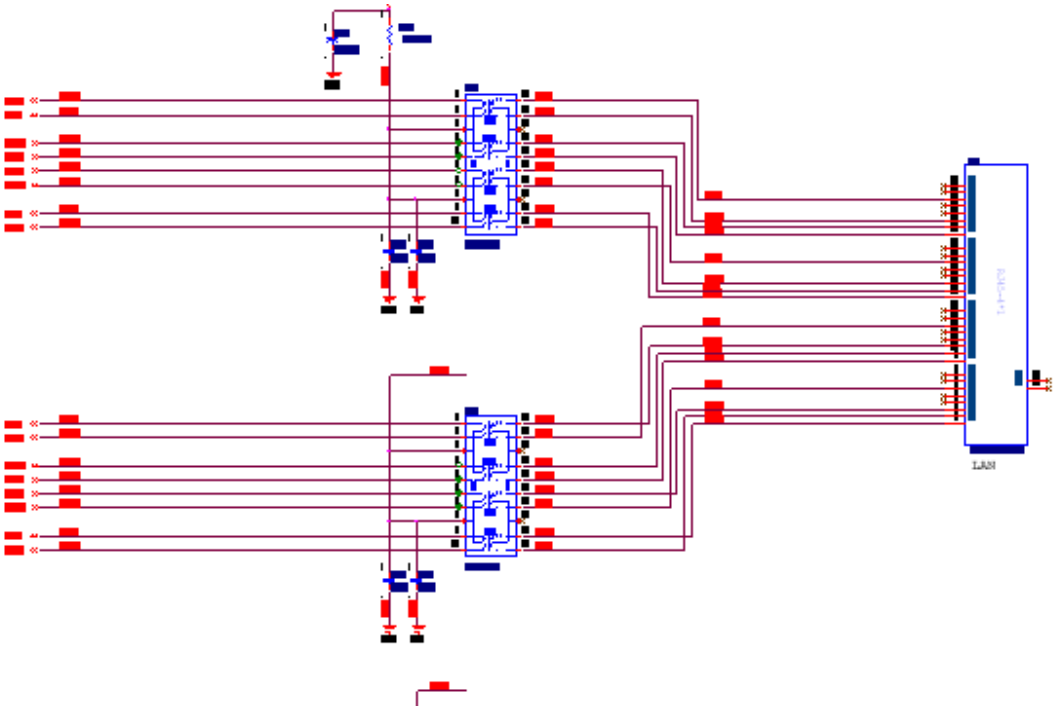
MAC address table read and write-able

MAC security – Locking a MAC address to an incoming port

MAC clone support – hash with VID

IGMP and MLD support

Per-Port Broadcast storm prevention



5.SDRAM interface description

Support 2 SDRAM(16b) chip select

Support 1 SRAM (8/16b) chip selects

Support 32MB/SDRAM per chip select

Support SDRAM transaction overlapping by early active and hidden pre-charge

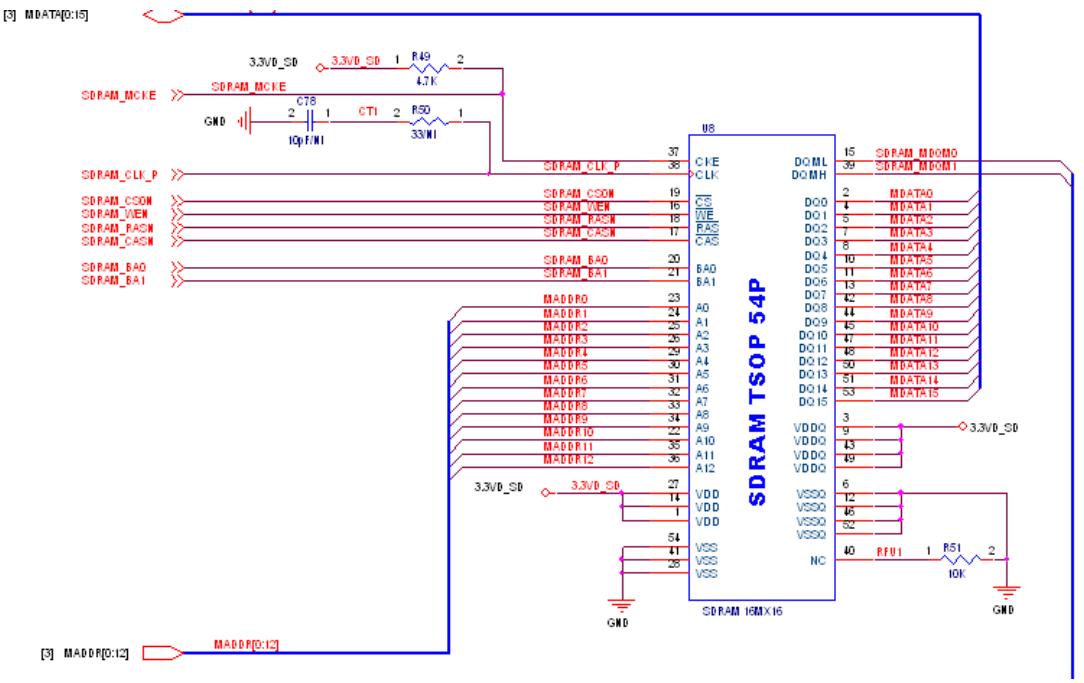
Support user SDRAM Init commands

Support 4 banks per SDRAM chip select

SDRAM burst length: 4 (fixed)

Support Wrap-4 transfer

Support Bank-Raw-Column and Raw-Bank-Column address mapping



6. SPI interface description

Supports up to 2 SPI master operations

Programmable clock polarity

Programmable interface clock rate

Programmable bit ordering

Firmware-controlled SPI enable

Programmable payload (address + data) length