EJEK Technology

SPECIFICATION

SPEC. NO. : _____ REV : 1.0

DATE : 2022.09.14

PRODUCT NAME : AI00400

	APPROVED	CHECKED	PREPARED	DCC ISSUE
NAME				

EJEK

AI00400

WiFi 11a/b/g/n/ac & Bluetooth 5.0
Module Data Sheet

Revision History

Date	Revision Content	Revised By	Version
2022/09/14	- Preliminary	Eric	1.0

Contents

1. Introduction

EJEK Technology would like to announce a performance and low-power consumption module which has all of the Wi-Fi, Bluetooth functionalities. The highly integrated module makes the possibilities of web browsing, VoIP, Bluetooth headsets applications. With seamless roaming capabilities and advanced security, also could interact with different vendors' 802.11a/b/g/n/ac Access Points in the wireless LAN.

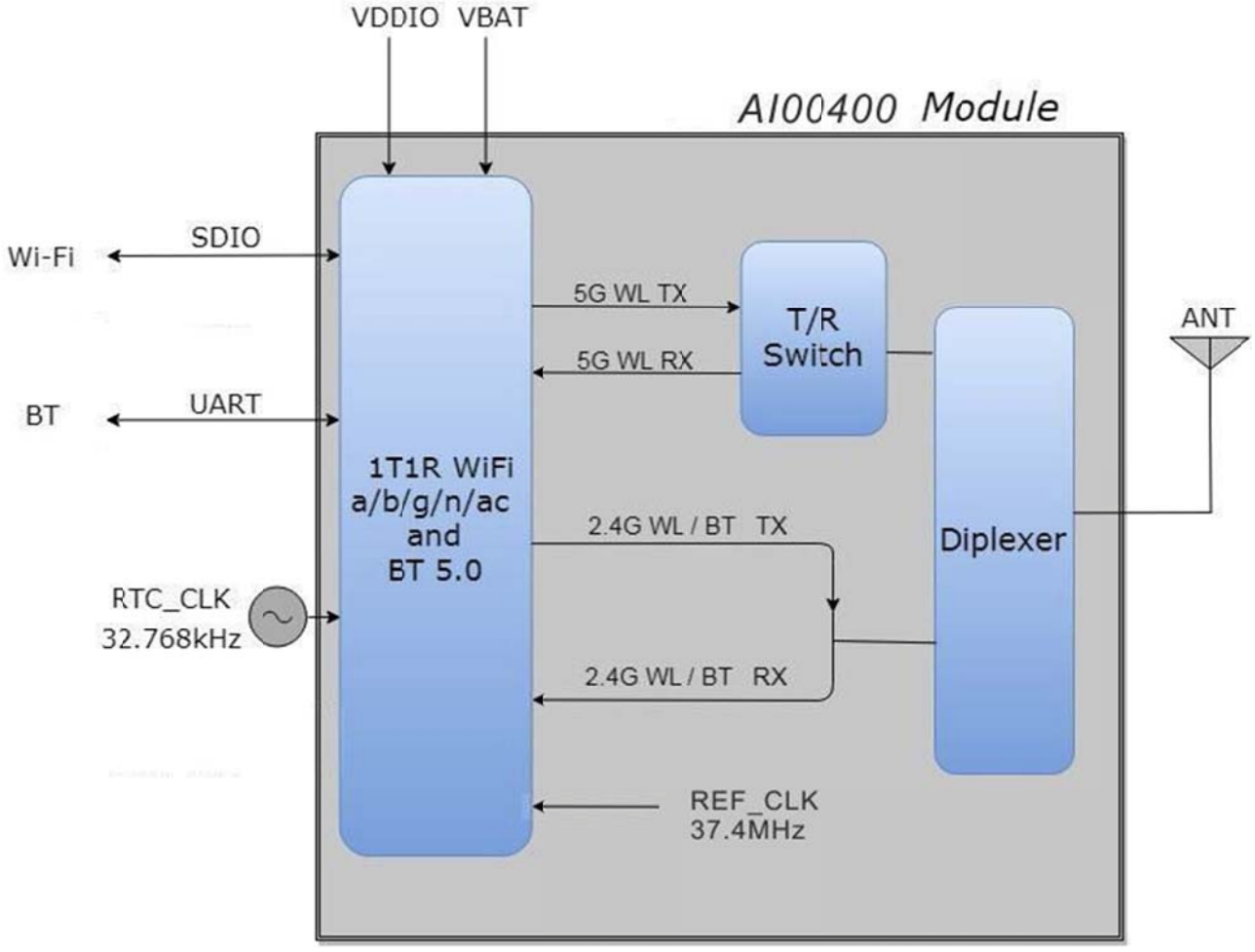
The wireless module complies with IEEE 802.11a/b/g/n/ac standard to connect to the wireless LAN. The integrated module provides SDIO interface for Wi-Fi, UART / PCM interface for Bluetooth.

This compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for Smart console and electronic devices which with IoT function.

2. Features

- IEEE 802.11a/b/g/n/ac dual-band radio with virtual-simultaneous dual-band operation
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- Single-stream spatial multiplexing up to 433.3 Mbps data rate.
- Supports 20, 40, 80 MHz channels with optional SGI (256 QAM modulation)
- Supports 1antenna with one for WLAN & Bluetooth shared port. Also, shared Bluetooth and WLAN receive signal path eliminates the need for an external power splitter while maintaining excellent sensitivity for both Bluetooth and WLAN.
- Supports standard SDIO v3.0 and backward compatible with SDIO v2.0 host interfaces.
  - SDIO v3.0(4-bit) — up to 208 MHz clock rate in SDR104 mode
- BT host digital interface:
  - UART (up to 4 Mbps)
  - PCM for audio data
- Complies with Bluetooth Core Specification Version 5.0 with provisions for supporting future specifications. With Bluetooth Class 1 or Class2 transmitter operation.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.

A simplified block diagram of the module is depicted in the figure below.



3. General Specification

3-1. General Specification

Model Name	AI00400
Product Description	1Tx/1Rx 802.11 a/b/g/n/ac Wi-Fi + BT 5.0 Module
Dimension	L x W x H: 37.6(inc. pin) x 36.6 x 7.3 (typical) mm
WiFi Interface	SDIO v2.0/v3.0
BT Interface	UART / PCM
Operating temperature	-30℃ to 85℃
Storage temperature	-40℃ to 125℃
Humidity	Operating Humidity 10% to 95% Non-Condensing

3-2. Voltages

3-2-1. Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
WIFI-VCC	Input supply Voltage	-0.5	5	V
VCC-IO-WIFI	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	3.9	V

3-2-2. Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

	Min.	Typ.	Max.	Unit
Operating Temperature	-30	25	85	℃
WIFI-VCC	3.2	3.3	4.8	V
VCC-IO-WIFI	1.6	1.8/3.3	3.6	V

4. Wi-Fi RF Specification

4-1. 2.4GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25℃

Feature	**Description**
WLAN Standard	IEEE 802.11b/g/n & Wi-Fi compliant
Frequency Range	2.412 GHz ~ 2.462 GHz (2.4GHz ISM Band)
Number of Channels	2.4GHz：Ch1 ~ Ch11
Modulation	802.11b : DQPSK、DBPSK、CCK 802.11 g/n : OFDM/64-QAM、16-QAM、QPSK、BPSK

Output Power , tolerance ± 1.5 dB
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 **standard**

802.11b	1Mbps	2Mbps	5.5Mbps	11Mbps	
	17	17	17	17	
802.11g	6、9Mbps	12、18Mbps	24Mbps	36Mbps	48Mbps
	16	16	16	16	15
	54Mbps				
	15				
802.11n 20MHz	MCS0~2	MCS3	MCS4	MCS5	MCS6
	17	17	16	15	14
	MCS7				
	14				

Note： The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance ± 2 dB
CCK modulation PER ≦ 8% 、OFDM modulation PER ≦ 10%

802.11b	Data Rate	Spec.(dBm)		
	1Mbps	-96		
	2Mbps	-90		
	5.5Mbps	-88		
802.11g	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-91	24Mbps	-83
	9Mbps	-88	36Mbps	-80
	12Mbps	-87	48Mbps	-76
	18Mbps	-85	54Mbps	-73
802.11n_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS4	-77
	MCS1	-85	MCS4	-75
	MCS2	-84	MCS6	-72
	MCS3	-80	MCS7	-71

Maximum Input Leve	802.11b : -10 dBm
	802.11g/n : -20 dBm

4-2. 5GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25℃

Feature	**Description**
WLAN Standard	IEEE 802.11a/n/ac & Wi-Fi compliant
Frequency Range	5.15~5.24GHz、5.725~5.85GHz (5GHz UNII Band)
Number of Channels	5.18~5.24GHz：Ch36 ~ Ch48 5.745~5.825GHz：Ch149 ~ Ch165
Modulation	802.11a : OFDM /64-QAM、16-QAM、QPSK、BPSK 802.11n : OFDM /64-QAM、16-QAM、QPSK、BPSK 802.11ac : OFDM /256-QAM、OFDM /64-QAM、16-QAM、QPSK、BPSK

Output Power , tolerance ± 2 dB
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard

802.11a	Frequency (MHz)	6~9Mbps	12~18Mbps	24Mbps	36Mbps
	5180~5240	17	17	17	16
	5745~5825	17	17	17	16
	Frequency (MHz)	48Mbps	54Mbps		
	5180~5240	16	15		
	5745~5825	16	15		
802.11n 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5180~5240	17	17	16	16
	5745~5825	17	17	16	16
	Frequency (MHz)	MCS6	MCS7		
	5180~5240	15	14		
	5745~5825	15	14		
802.11n 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5180~5240	17	17	16	16
	5745~5825	17	17	16	16
	Frequency (MHz)	MCS6	MCS7		
	5180~5240	15	14		
	5745~5825	15	14		
802.11ac 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5180~5240	17	17	16	16
	5745~5825	17	17	16	16
	Frequency (MHz)	MCS6	MCS7	MCS8	
	5180~5240	15	14	12	
	5745~5825	15	14	12	
802.11ac 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5180~5240	17	17	16	16
	5745~5825	17	17	16	16
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5180~5240	15	14	12	10.5

	5745~5825	15	14	12	10.5
802.11ac 80MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5180~5240	17	17	16	16
	5745~5825	17	17	16	16
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5180~5240	15	14	12	10.5
	5745~5825	15	14	12	10.5

Note：The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance ±2 dB
OFDM modulation PER ≦ 10%

802.11a	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-92	24Mbps	-82
	9Mbps	-89	36Mbps	-79
	12Mbps	-88	48Mbps	-75
	18Mbps	-86	54Mbps	-74
802.11n_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-91	MCS4	-78
	MCS1	-88	MCS5	-74
	MCS2	-85	MCS6	-73
	MCS3	-82	MCS7	-72
802.11n_40MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-89	MCS4	-76
	MCS1	-85	MCS5	-71
	MCS2	-83	MCS6	-70
	MCS3	-79	MCS7	-68
802.11ac_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS5	-73
	MCS1	-87	MCS6	-71
	MCS2	-84	MCS7	-70
	MCS3	-81	MCS8	-67
802.11ac_40MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS5	-70
	MCS1	-83	MCS6	-68
	MCS2	-81	MCS7	-66
	MCS3	-78	MCS8	-65
802.11ac_80MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-85	MCS5	-69
	MCS1	-82	MCS6	-65
	MCS2	-78	MCS7	-63
	MCS3	-74	MCS8	-61

Maximum Input Level	802.11a/n : -20 dBm
	802.11ac : -30 dBm
Antenna Reference	Small antennas with 0~2 dBi peak gain

5. Bluetooth Specification

5-1. Bluetooth Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25℃

Feature	Description	
General Specification		
Bluetooth Standard	GFSK、DQPSK、8DPSK、LE(1Mbps)、2LE(2Mbps)	
Host Interface	UART	
Frequency Band	2402 MHz ~ 2480 MHz	
Number of Channels	79 channels for classic、40 channels for BLE	
Modulation	FHSS, GFSK, DPSK, DQPSK	
RF Specification		
	CL1 level	**CL2 level**
BDR Output Power	**6**	2
EDR Output Power	4	2
LE Output Power	5	2
	Typical.	
Sensitivity @ BER=0.1% for GFSK (1Mbps)	-86 dBm	
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)	-87 dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)	-83 dBm	
Sensitivity @ BER=0.01% for LE (1Mbps)	-90 dBm	
Sensitivity @ BER=0.01% for LE (2Mbps)	-90 dBm	
Maximum Input Level	GFSK (1Mbps):-20dBm	
	π/4-DQPSK (2Mbps) :-20dBm	
	8DPSK (3Mbps) :-20dBm	

Note*：The Bluetooth output power is able to be configured by firmware (hcd file).

6. Pin Assignments

6-1. Pin Outline

< BOTTOM VIEW >

6-2. Pin Definition

NO	Name	Type	Description
1	GND	-	Ground connections
2	GND	-	Ground connections
3	WL-REG-ON	I	Power up/down internal regulators used by WiFi section
4	WL-HOST-WAKE	O	WLAN to wake-up HOST
5	WL-CMD	I/O	SDIO command line
6	WL-CLK	I/O	SDIO clock line
7	WL-D3	I/O	SDIO data line 3
8	WL-D2	I/O	SDIO data line 2
9	WL-D0	I/O	SDIO data line 0
10	WL-D1	I/O	SDIO data line 1
11	IO-VCC	P	I/O Voltage supply input
12	WL-VCC	P	Main power voltage source input
13	GND	-	Ground connections
14	CLK32K	I	External Low Power Clock input (32.768KHz)
15	GND	-	Ground connections
16	BT-RST	I	Power up/down internal regulators used by BT section
17	BT-UART-TX	O	Bluetooth UART interface
18	BT-UART-RX	I	Bluetooth UART interface

19	BT-UART-RTS	O	Bluetooth UART interface
20	BT-UART-CTS	I	Bluetooth UART interface
21	GND	-	Ground connections
22	BTHOST-WAKE	O	Bluetooth device to wake-up HOST
23	GND	-	Ground connections
24	GND	-	Ground connections

7. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-30	ppm
Duty cycle	30 - 70	%
Input signal amplitude	400 to 3300	mV, p-p
Signal type	Square-wave or sine-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7Vio - Vio	V

Input signal amplitude follow VDDIO (1.8V or 3.3V)

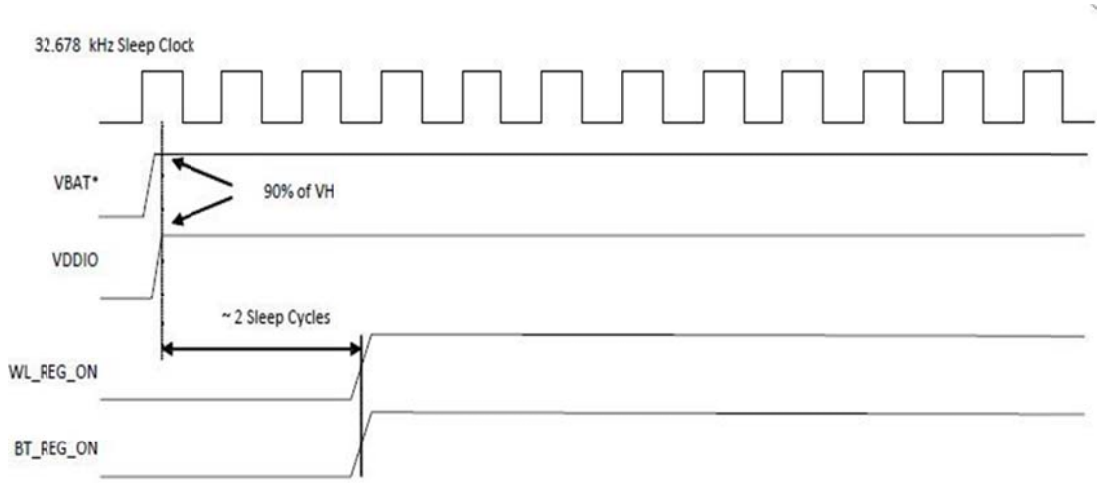
8. Host Interface Timing Diagram

8-1. Power-up Sequence Timing Diagram

The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

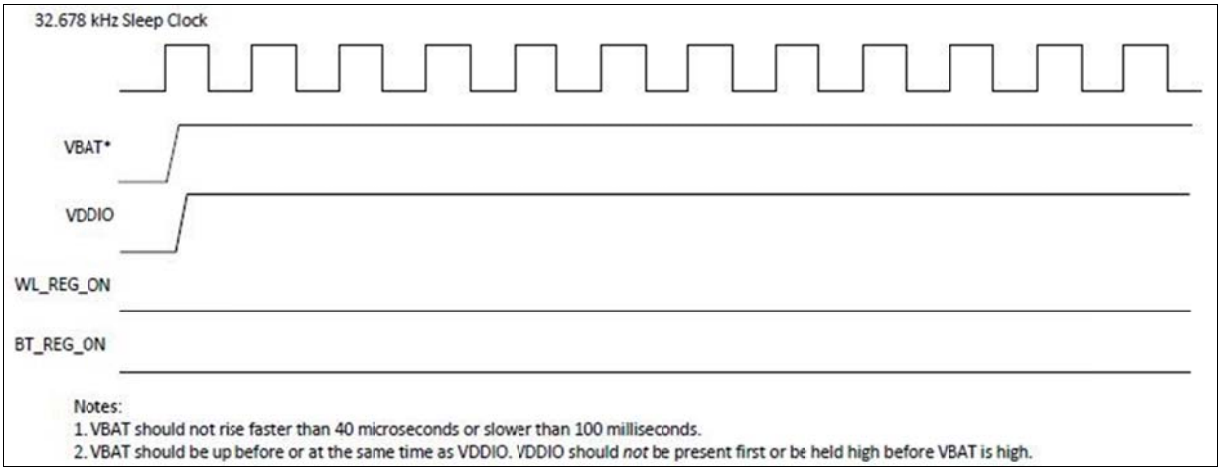
Additionally, diagrams are provided to indicate proper sequencing of the signals for carious operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

- WL_REG_ON: Used by the PMU to power up or power down the internal regulators used by the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- BT_REG_ON: Used by the PMU to power up or power down the internal regulators used by the BT section. Low asserting reset for Bluetooth. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



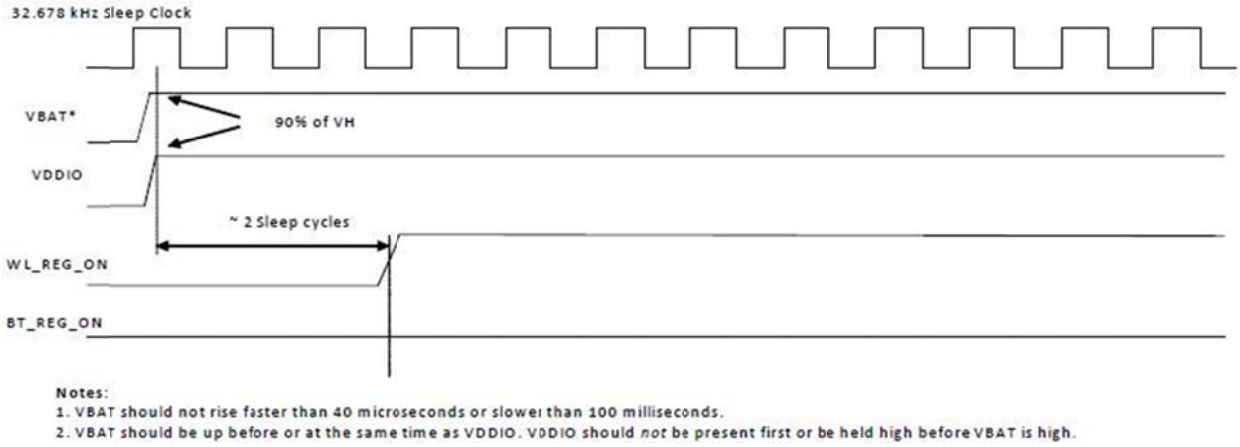
Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should *not* be present first or be held high before VBAT is high.

WLAN=ON, Bluetooth=ON

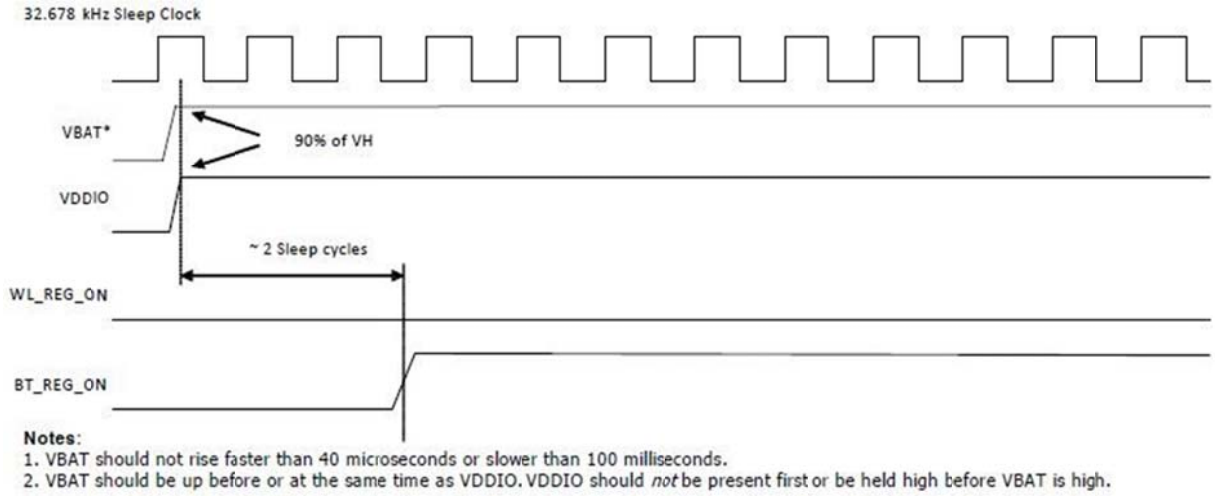


Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should *not* be present first or be held high before VBAT is high.

WLAN=OFF, Bluetooth=OFF



WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

8-2. SDIO Pin Description

The module supports SDIO version 3.0 for all 1.8V 4-bit UHSI speeds: SDR50(100 Mbps),SDR104(208MHz) and DDR50(50MHz, dual rates) in addition to the 3.3V default speed(25MHz) and high speed (50 MHz). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

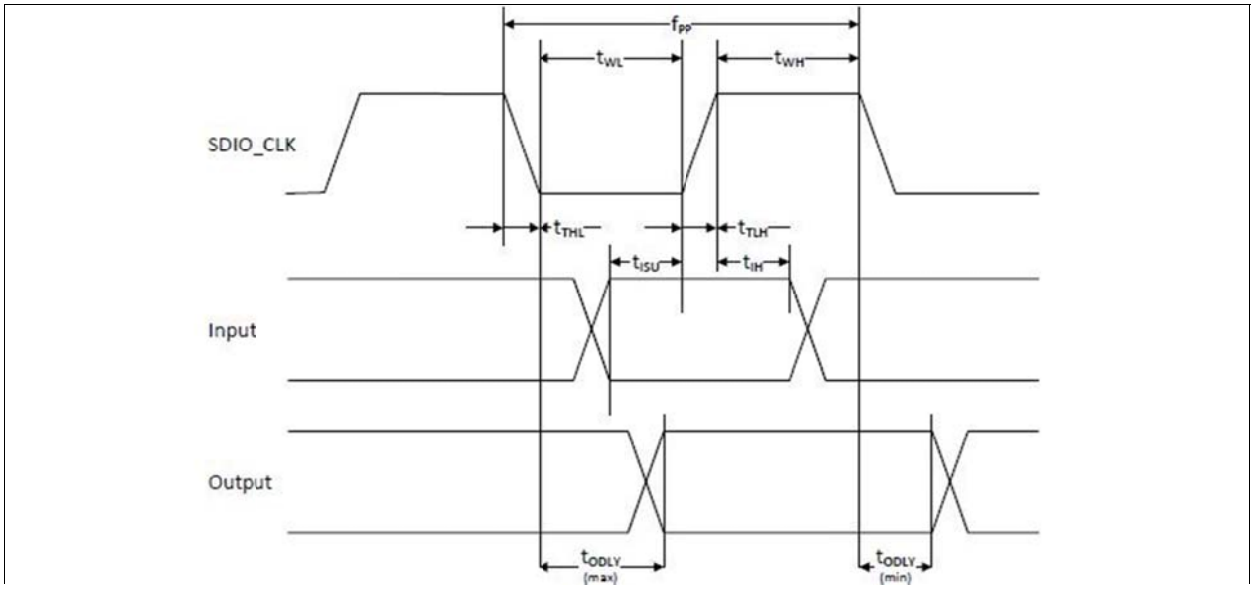
The following three functions are supported:

- Function 0 Standard SDIO function (Max Block Size / Byte Count = 32B)
- Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max Block Size / Byte Count = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max Block Size/Byte Count=512B)

8-2-1. SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

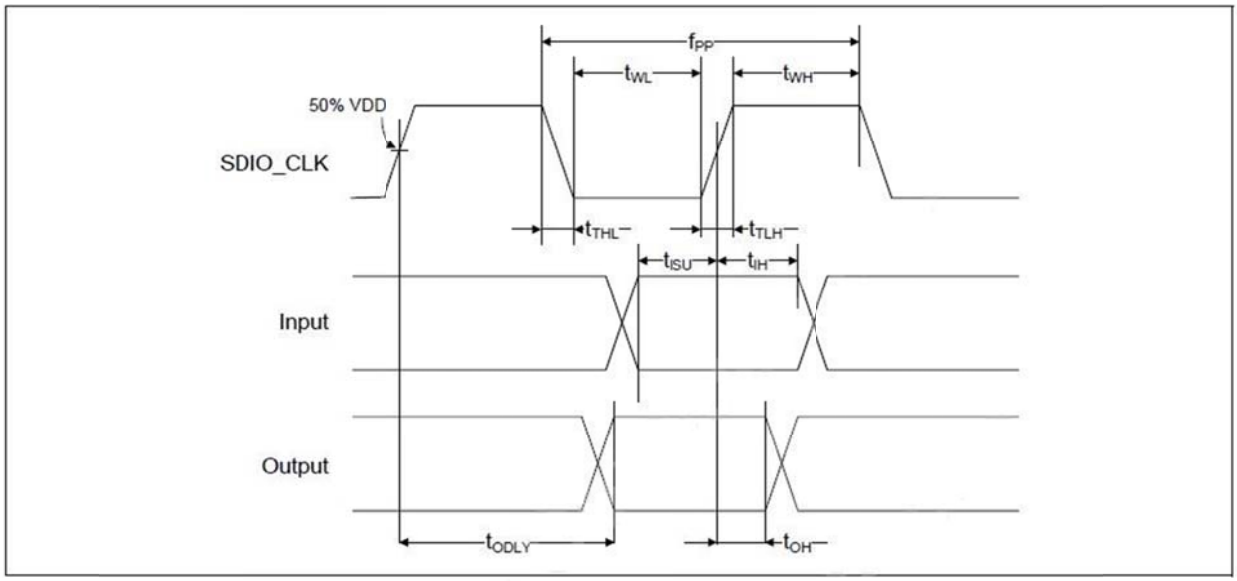
8-2-2. SDIO Default Mode Timing Diagram



Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	fPP	0	–	25	MHz
Frequency – Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock low time	tTHL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	–	14	ns
Output delay time – Identification mode	tODLY	0	–	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

8-2-3. SDIO High Speed Mode Timing Diagram

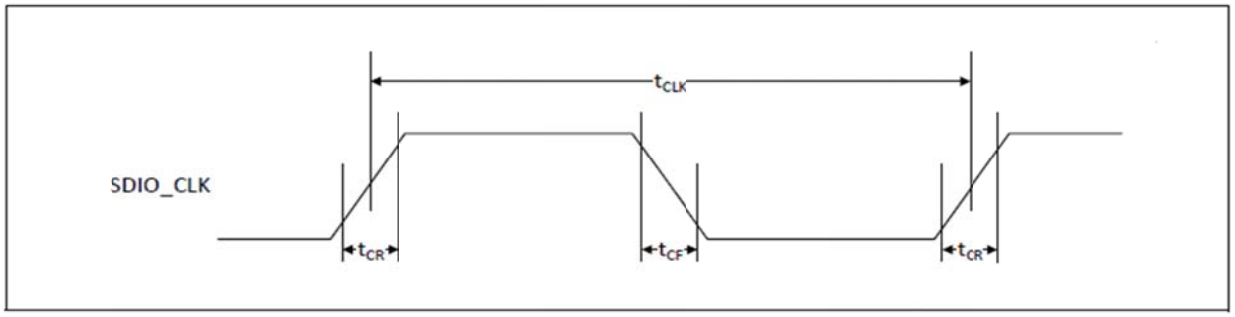


Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock low time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	tISU	6	–	–	ns
Input hold Time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on CL ≤ 40 pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

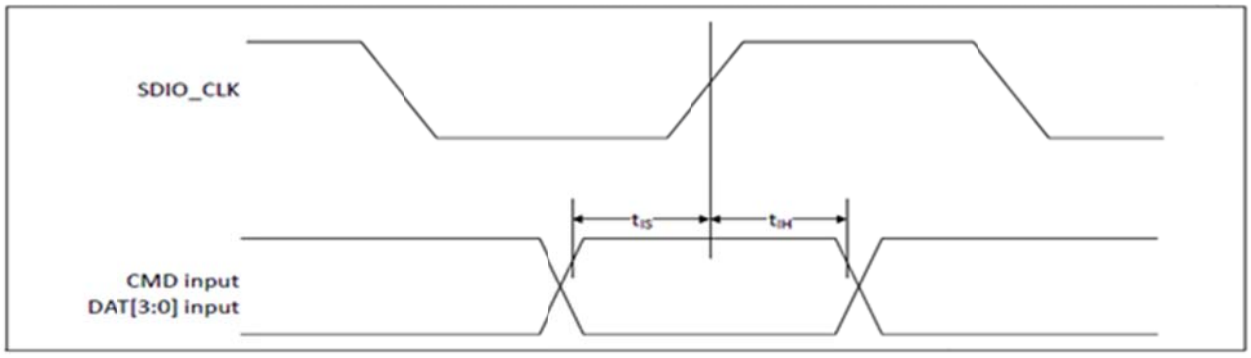
8-2-4. SDIO Bus Timing Specifications in SDR Modes

Clock timing (SDR Modes)



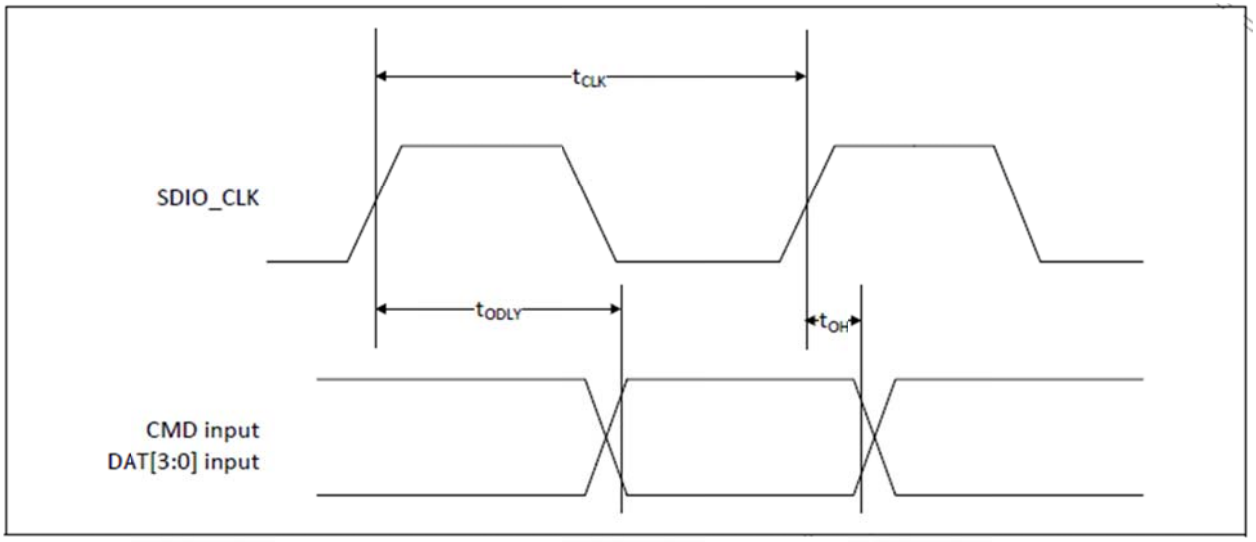
Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
		10	–	ns	SDR50 mode
		4.8	–	ns	SDR104 mode
–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 2.00 ns (max) @100 MHz, C_{CARD} = 10 pF t_{CR}, t_{CF} < 0.96 ns (max) @208 MHz, C_{CARD} = 10 pF
Clock duty	–	30	70	%	–

SDIO Bus Input timing (SDR Modes)



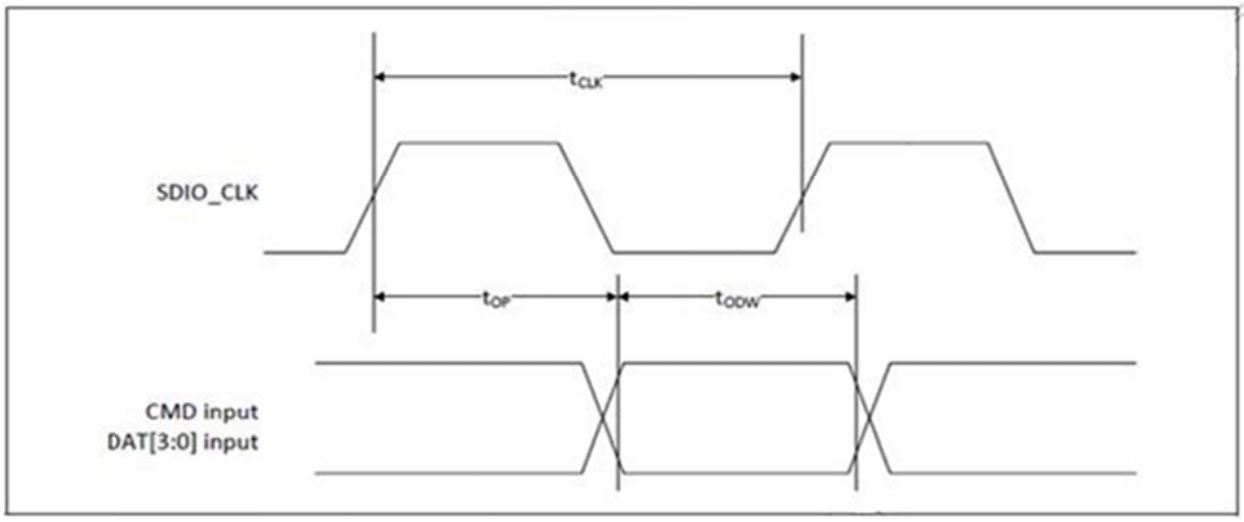
Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.4	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975V
SDR50 Mode				
t_{IS}	3.00	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975V

SDIO Bus output timing (SDR Modes up to 100MHz)



Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	7.5	ns	$t_{CLK} \geq 10$ ns $C_L = 30$ pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	$t_{CLK} \geq 20$ ns $C_L = 40$ pF using for SDR12, SDR25

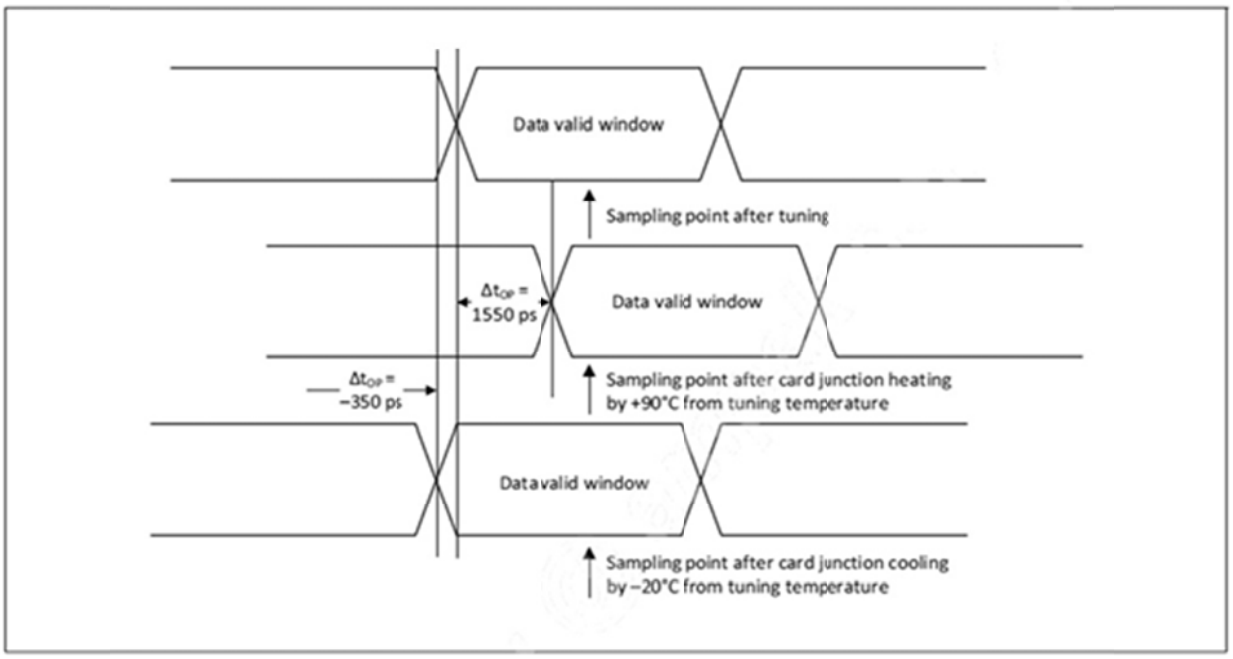
Card output timing (SDR Modes 100MHz to 208MHz)



Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	−350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	–	UI	t_{ODW}=2.88 ns @208 MHz

- Δt_{OP} = +1550 ps for junction temperature of Δt_{OP} = 90 degrees during operation
- Δt_{OP} = −350 ps for junction temperature of Δt_{OP} = −20 degrees during operation
- Δt_{OP} = +2600 ps for junction temperature of Δt_{OP} = −20 to +125 degrees during operation

Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)

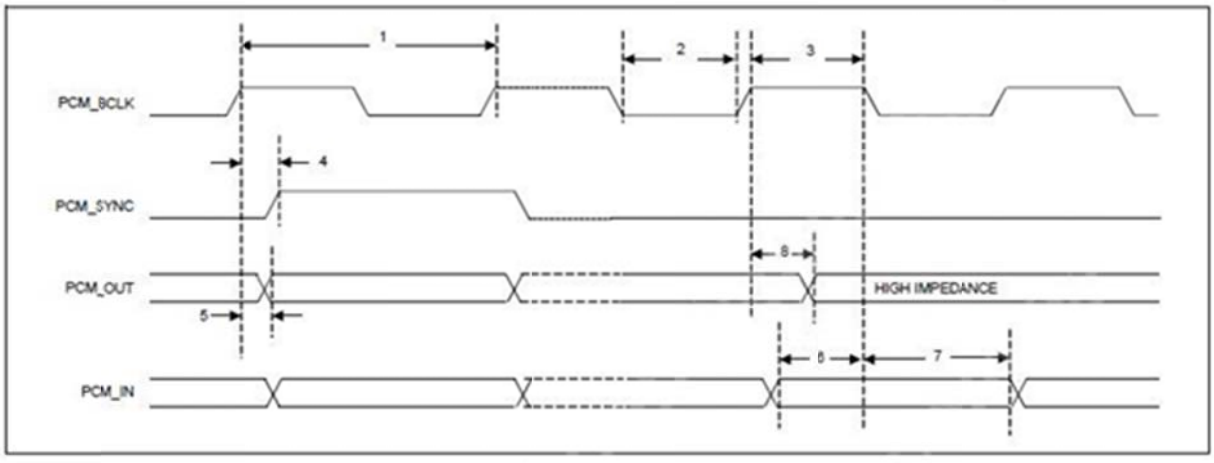


8-3. PCM Interface Description

The PCM Interface on the BCM43456 can connect to linear PCM Codec devices in master or slave mode. In master mode, the BCM43456 generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the BCM43456.The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Short Frame Sync, Master Modem

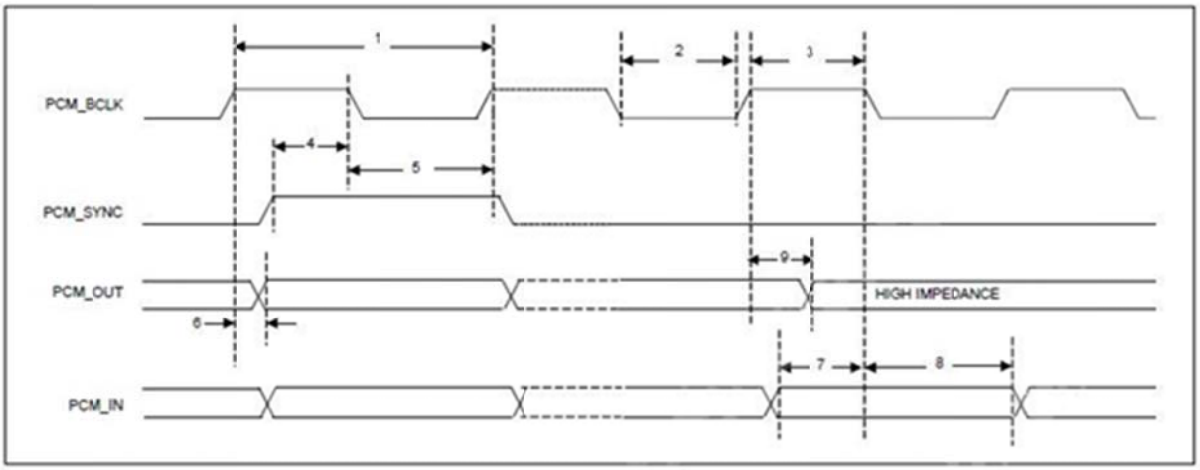
PCM Timing Diagram (Short Frame Sync, Master Mode)



Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Slave Mode

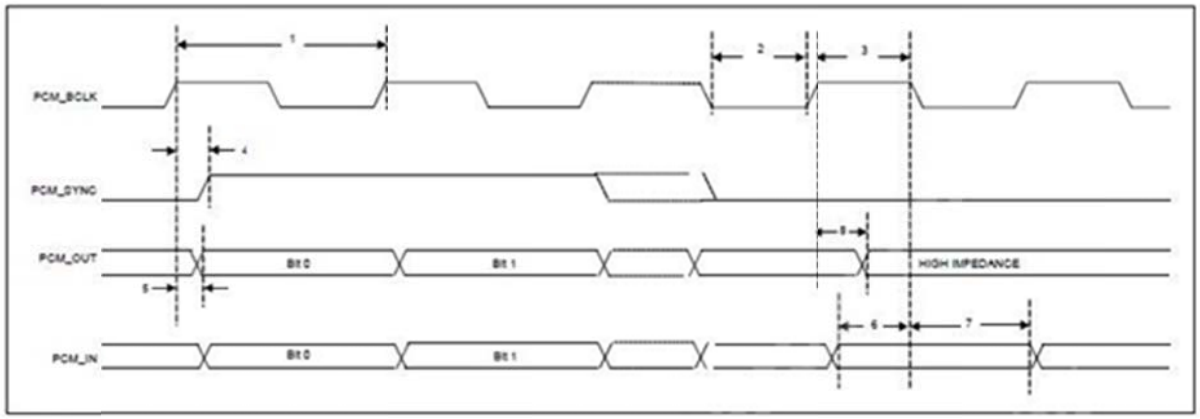
PCM Timing Diagram (Short Frame Sync, Slave Mode)



Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Master Mode

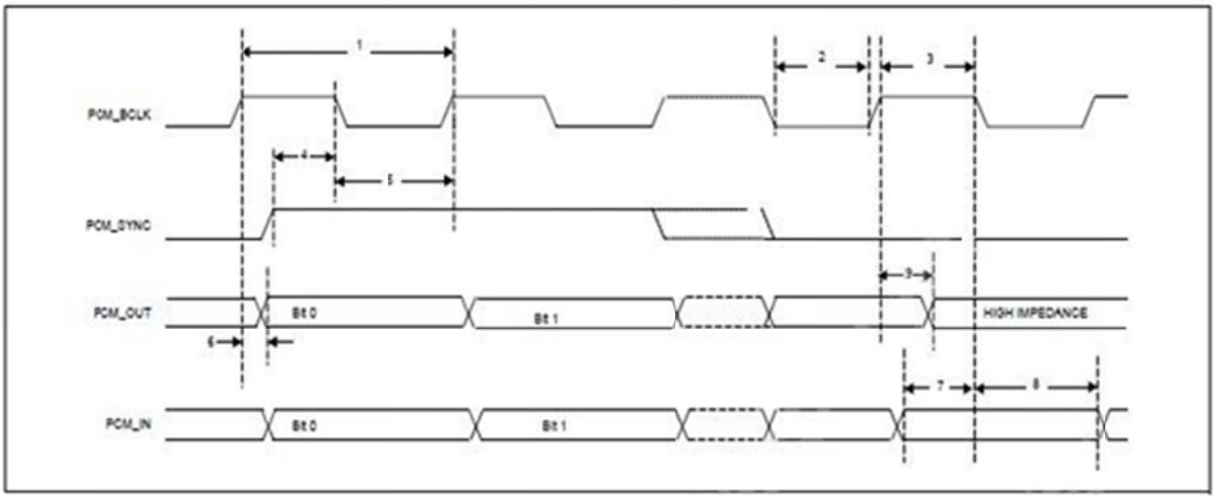
PCM Timing Diagram (Long Frame Sync, Master Mode)



Reference	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Slave Mode

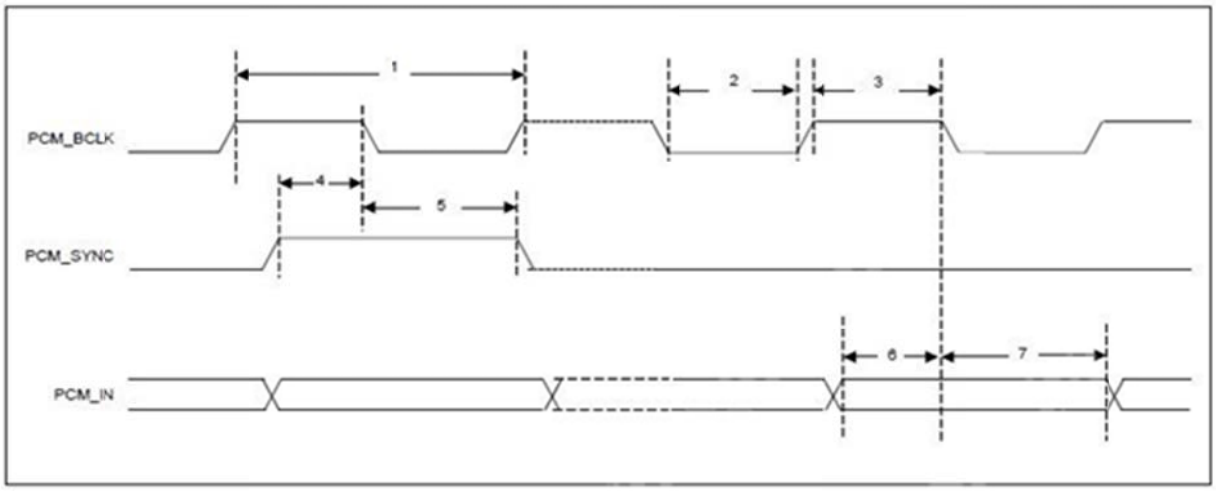
PCM Timing Diagram (Long Frame Sync, Slave Mode)



Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Burst Mode

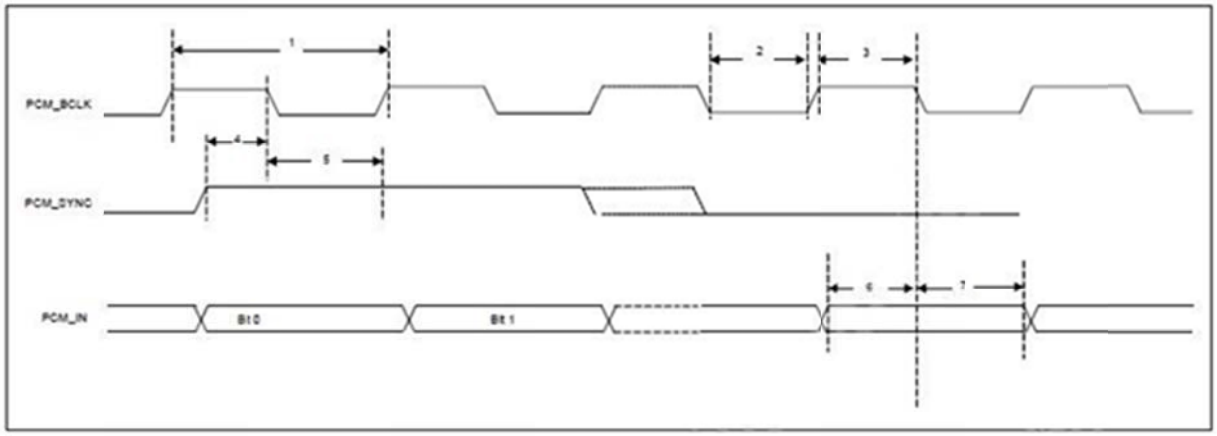
PCM Burst Mode Timing (Receive Only, Short Frame Sync)



Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

Long Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Long Frame Sync)



Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

8-4. UART Interface Description

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

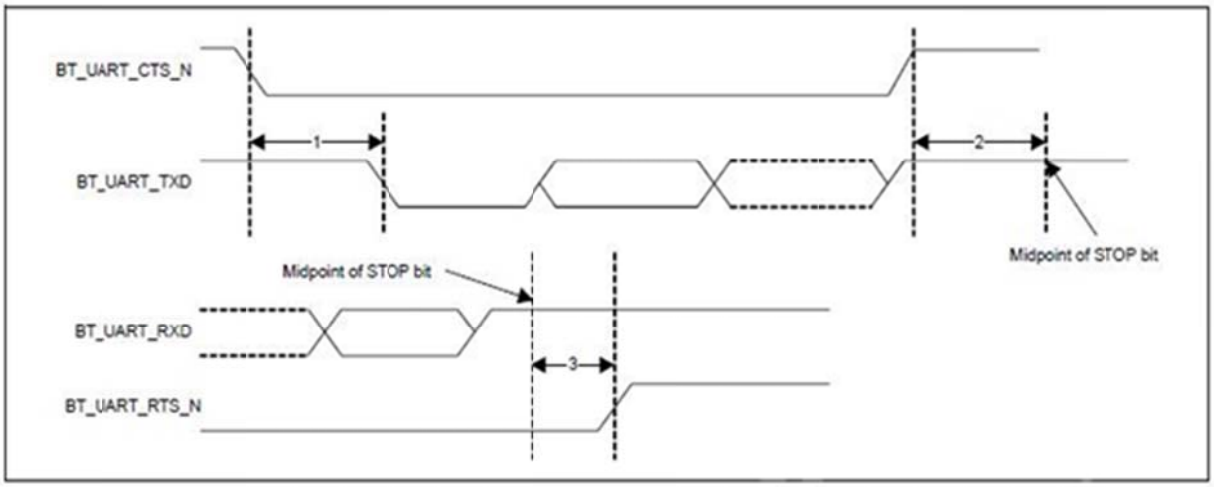
UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 5.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The BCM43456 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The BCM43456 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Example of Common Baud Rates

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

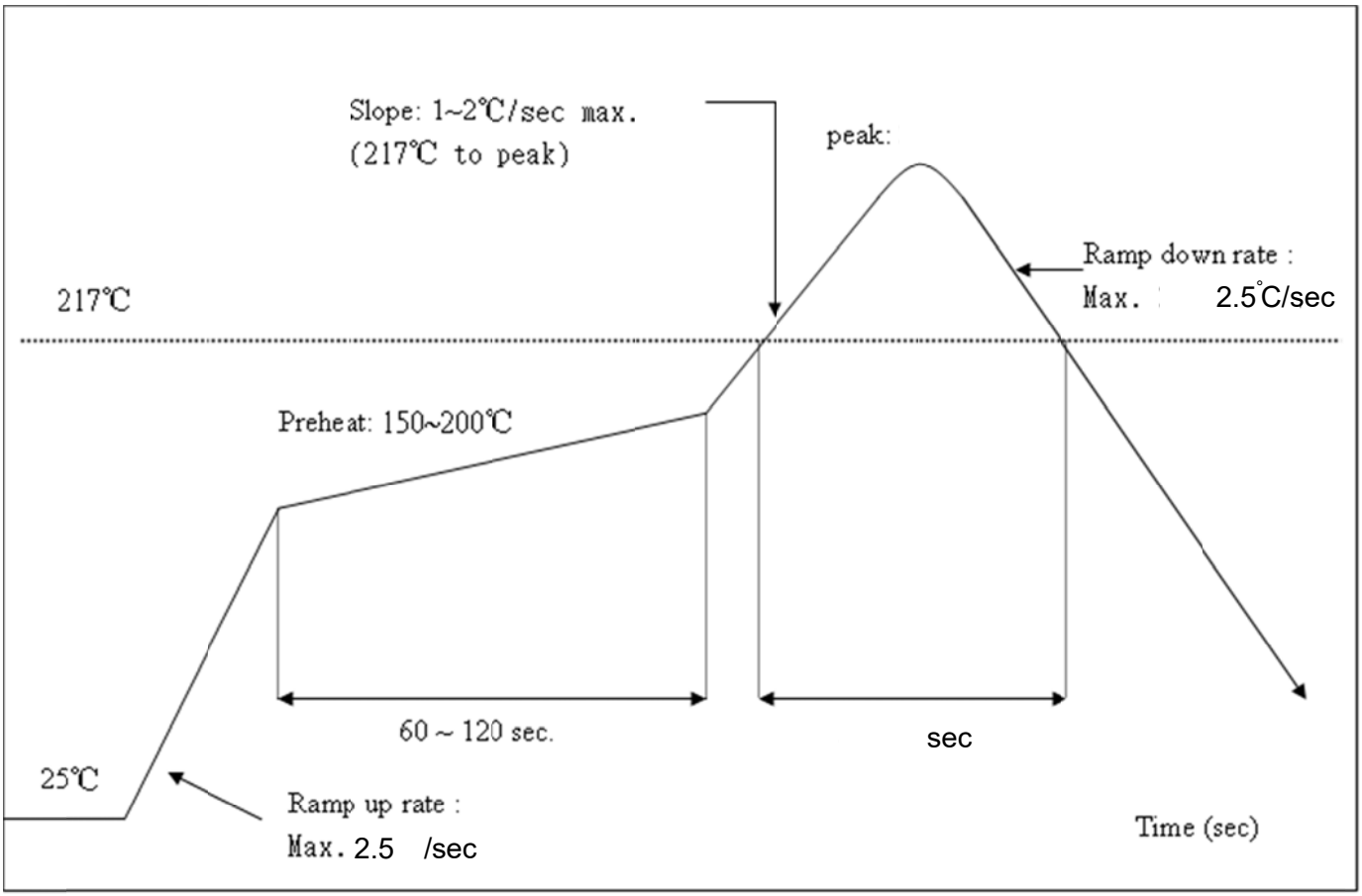


UART Timing Specifications

Ref	Characteristics	Min.	Typ.	Max.	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	Bit periods

9. Recommended Reflow Profile

Referred to IPC/JEDEC standard. Peak Temperature : <250℃ Number of Times : ≤2 times



A. Appendix A
A.1. Requirement of FCC KDB 996369 D03 for module certification:

1.1 List of applicable FCC rules:
The module complies with FCC Part 15.247,15.407

1.2 Summarize the specific operational use conditions:
The module has been certified for Fix, Mobile applications. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

1.3 Limited module procedures:
Not applicable.

1.4 Trace antenna designs:
Not applicable.

1.5 RF exposure considerations:
This equipment complies with FCC's RF radiation exposure limits set forth for an uncontrolled environment. The antenna(s) used for this transmitter must not be collocated or operating in conjunction with any other antenna or transmitter.

Note: the host product manuals must include a statement in order to alert the users of FCC RF exposure compliance.

1.6 Antennas

Type	Gain	Frequency Bands
PCB	2.0dBi	2.4G/5GHz

1.7 Label and compliance information
This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:

(1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Warning: Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radiofrequency energy and, if not installed andused in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
-Consult the dealer or an experienced radio/TV technician for help.

The system integrator must place an exterior label on the outside of the final product housing the **2A9G7AI00400** Modules. Below is the content that must be included on this label.

The host product Labeling Requirements:
NOTICE: The host product must make sure that FCC labeling requirements are met. This includes clearly visible exterior label on the outside of the final product housing that
displays the contents shown in below:

Contains **FCC ID: 2A9G7AI00400**

1.8 Information on test modes and additional testing requirements:
When testing host product, the host manufacture should follow FCC KDB Publication 996369 D04 Module Integration Guide for testing the host products. The host manufacturer may operate their product during the measurements. In setting up the configurations, if the pairing and call box options for testing does not work, then the host product manufacturer should coordinate with the module manufacturer for access to test mode software

1.9 Additional testing, Part 15 Subpart B disclaimer:
The modular transmitter is only FCC authorized for the specific rule parts (FCC Part 15.247) list on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed when contains digital circuity.

1.10 Information on test modes and additional testing requirements:
When testing host product, the host manufacture should follow FCC KDB Publication 996369 D04 Module Integration Guide for testing the host products. The host manufacturer may operate their product during the measurements.

IC Statement

RSS-GEN

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device.
" or "

présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

1) l'appareil ne doit pas produire de brouillage;
2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement." Déclaration sur l'exposition aux rayonnements RF

The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.

L'autre utilisé pour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur

The host product shall be properly labelled to identify the modules within the host product.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word “Contains” or similar wording expressing the same meaning, as follows: “Contains IC: 29756-AI00400” or “where: 29756-AI00400is the module’s certification number.

Le produit hôte doit être correctement étiqueté pour identifier les modules dans le produit hôte. L'étiquette de certification d'Innovation, Sciences et Développement économique Canada d'un module doit être clairement visible en tout temps lorsqu'il est installédans le produit hôte; sinon, le produit hôte doit porter une étiquette indiquant le numéro de certification d'Innovation, Sciences et Développement économique Canada pour le module, précédé du mot «Contient» ou d'un libellé semblable exprimant la même signification, comme suit:"Contient IC: 29756-AI00400" ou "où: 29756-AI00400 est le numéro de certification du module.