FCC STATEMENT:

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-Reorient or relocate the receiving antenna.

-Increase the separation between the equipment and receiver.

-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-Consult the dealer or an experienced radio/TV technician for help.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body

INDUSTEY CANADA STATEMENT:

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation of the device. In additional, this device complies with ICES-003 of the Industry Canada (IC) Rules.

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Industry Canada licence-exempt RSS standard(s). These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-Reorient or relocate the receiving antenna.

-Increase the separation between the equipment and receiver.

-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-Consult the dealer or an experienced radio/TV technician for help.

This equipment complies with RSS-102 radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between

the radiator & your body.

INDUSTEY CANADA STATEMENT(French):

Cet appareil est conforme aux normes RSS exemptes de licence d'Industrie Canada. Son fonctionnement est soumis aux deux conditions suivantes : (1) Cet appareil ne doit pas causer d'interférences nuisibles et (2) cet appareil doit accepter toute interférence reçue, y compris les interférences susceptibles de provoquer un fonctionnement indésirable de l'appareil. De plus, cet appareil est conforme à la norme ICES-003 des règles d'Industrie Canada (IC). Tout changement ou modification non expressément approuvé par la partie responsable de la conformité pourrait annuler l'autorité de l'utilisateur à faire fonctionner l'équipement. Remarque : cet équipement a été testé et déclaré conforme aux limites d'un appareil numérique de classe B, conformément aux normes RSS exemptes de licence d'Industrie Canada. Ces limites sont conçues pour fournir une protection raisonnable contre les interférences nuisibles dans une installation résidentielle. Cet équipement génère des utilisations et peut émettre de l'énergie de radiofréquence et, s'il n'est pas installé et utilisé conformément aux instructions, peut causer des interférences nuisibles aux communications radio. Cependant, il n'y a aucune garantie que des interférences ne se produiront pas dans une installation particulière. Si cet équipement cause des interférences nuisibles à la réception radio ou télévision, ce qui peut être déterminé en éteignant et en rallumant l'équipement, l'utilisateur est encouragé à essayer de corriger l'interférence par une ou plusieurs des mesures suivantes : -Réorientez ou déplacez l'antenne de réception. -Augmenter la distance entre l'équipement et le récepteur. -Connectez l'équipement à une prise sur un circuit différent de celui auquel le récepteur est connecté. -Consultez le revendeur ou un technicien radio/TV expérimenté pour obtenir de l'aide. Cet équipement est conforme aux limites d'exposition aux rayonnements RSS-102 établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec une distance minimale de 2. Cet appareil est conforme aux normes RSS exemptes de licence d'Industrie Canada. Son fonctionnement est soumis aux deux conditions suivantes : (1) Cet appareil ne doit pas causer d'interférences nuisibles et (2) cet appareil doit accepter toute interférence reçue, y compris les interférences susceptibles de provoquer un fonctionnement indésirable de l'appareil. De plus, cet appareil est conforme à la norme ICES-003 des règles d'Industrie Canada (IC).

Tout changement ou modification non expressément approuvé par la partie responsable de la conformité pourrait annuler l'autorité de l'utilisateur à faire fonctionner l'équipement.

Remarque : cet équipement a été testé et déclaré conforme aux limites d'un appareil numérique de classe B, conformément aux normes RSS exemptes de licence d'Industrie Canada. Ces limites sont conçues pour fournir une protection raisonnable contre les interférences nuisibles dans une installation résidentielle. Cet équipement génère des utilisations et peut émettre de l'énergie de radiofréquence et, s'il n'est pas installé et utilisé conformément aux instructions, peut causer des interférences nuisibles aux communications radio. Cependant, il n'y a aucune garantie que des interférences ne se produiront pas dans une installation particulière. Si cet équipement cause des interférences nuisibles à la réception radio ou télévision, ce qui peut être déterminé en éteignant et en rallumant l'équipement, l'utilisateur est encouragé à essayer de corriger l'interférence par une ou plusieurs des mesures suivantes : -Réorientez ou déplacez l'antenne de réception. -Augmenter la distance entre l'équipement et le récepteur. -Connectez l'équipement à une prise sur un circuit différent de celui auquel le récepteur est

connecté. -Consultez le revendeur ou un technicien radio/TV expérimenté pour obtenir de l'aide.
Cet équipement est conforme aux limites d'exposition aux rayonnements RSS-102 établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec une distance minimale de 20 cm entre le radiateur et votre corps.

DataSheet

A6G2C Series Core Board

MiniARM Core Board

DS01010101 V1.05 Date: 2019/06/17 Product Data Manual

Overview

The A6G2C series wireless core board is an embedded industrial control core board that adds WiFi, Bluetooth, Zigbee and other functions on the basis of the M6G2C series core board. The core board adopts Cortex-A7 core processor, which provides fast data processing and smooth interface switching. The product provides eight UART interfaces, two USB OTG interfaces, a maximum of two CAN-bus interfaces, two Ethernet interfaces, and other interfaces. It has powerful industrial control communication interfaces, provides industrial-grade performance guarantee, and meets most industrial applications, portable consumer electronics, automotive electronics and other industries.

Guangzhou ZLG Electronics Co., Ltd. provides various sophisticated hardware solutions, as well as rich software resources including Linux and AWorks. The complete software and hardware architecture allows you to focus only on product application. It has the characteristics of short development cycle, humanized system and complete software supporting.

Product characteristics

- 32-bit Cortex-A7 processor; operating frequency: 528MHz;
- Memory: 128/256MByte DDR3;
- Flash: 128/256MByte NAND Flash (the read and write life is about 100,000 times);
- Support up to eight serial ports;
- Support up to two CAN-bus;
- Support two10/100M Ethernet interfaces;
- Integrate two USB2.0 OTG interfaces;
- Support one SD/MMC card;
- Support CAN, UART, I2C and other standard communication interfaces;
- Onboard WIFI, Bluetooth, Zigbee, NFC;
- Embedded Linux/AWorks operating system;
- Support a variety of upgrade methods.
- Dimensions: 30 mm x 48 mm

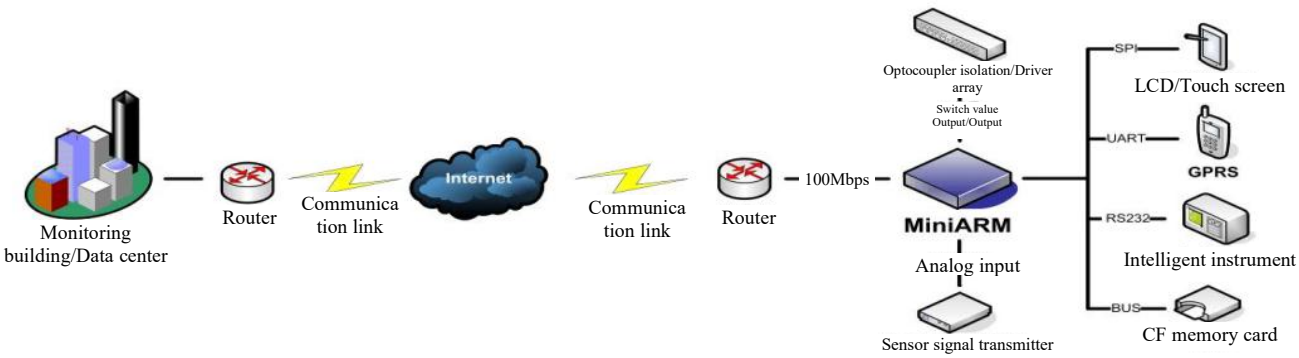
Applications

Portable Medical Equipment Electronic Point of Sale for traffic command automation home and industrial automation human machine interface (HMI)

Ordering information

Model	Range of temperature	System
A6G2C-W128LI	-30°C to +85°C	Pre-installed Linux, AWorks supported
A6G2C-W256LI	-30°C to +85°C	Pre-installed Linux, AWorks supported
A6G2A-W256F256LI-T	-30°C to +85°C	Pre-installed Linux, AWorks supported
A6G2C-WB128LI	-30°C to +85°C	Pre-installed Linux, AWorks supported
A6G2C-WB256LI	-30°C to +85°C	Pre-installed Linux, AWorks supported
A6G2C-5WB128LI-T	-20°C to +75°C	Pre-installed Linux, AWorks supported
A6G2C-Z128F128LI-T	-40°C to +85°C	Pre-installed Linux, AWorks supported
A6G2C-M128F128LI-T	-40°C to +85°C	Pre-installed Linux, AWorks supported

Typical application



Revision History

Version	Date	Reason
V0.90	2015/02/11	Created
V1.00	2015/05/20	Official release
V1.01	2015/06/21	Modified product pictures and mechanical dimension drawings
V1.02	2017/08/08	1. Modified the description of "Overview" 2. Modified the description of "Function Introduction" 3. Modified the picture of "Product Model Naming Rules" 4. Added "Table 1.1 Use of special pins" 5. Added the "3.5 Common Interface Multiplexing on the A6G2C Core Board" section
V1.03	2018/09/05	1. Deleted the model number of A6G1C series 2. Added product models A6G2C-5WB128LI-T and A6G2C-Z128F128LI-T 3. Deleted the content about SAI1 4. Deleted the content about SD2 5. Added 4.12 PCB design precautions; added Flash read/write life indicator to product features 6. Added the introduction to the AWorks system; 7. Added A6G2C-M128F128LI-T 8. Added A6G2A-W256F256LI-T 9. Added the antenna selection chapter 10. Added the description of ambient temperature 11. Modified the boot configuration, and moved it to chapter 4.1.1
V1.04	2019/03/08	1. Updated document headers and footers and the "Sales and Service Network" content, and added "Disclaimer" 2. Added the JTAG description chapter. 3. Added the ESD protection content
V1.05	2019/06/17	1. Modified "1.4 Type Selection Comparison Table"

Contents

1. Function Introduction

A6G2C series core boards are a series of embedded industrial control wireless core boards with NXPi.MX6UL processor as the core developed by Guangzhou ZLG Electronics Co., Ltd. The core board adopts the Cortex-A7 core processor with superior performance, which provides fast data processing and smooth interface switching. The product provides eight UART interfaces, two USB OTG interfaces, a maximum of two CAN-bus interfaces, two Ethernet interfaces, and other communication interfaces, and implements the on-board WiFi, Bluetooth, Zigbee, NFC functions. The product provides powerful industrial control communication interfaces, and meets the needs of most industrial applications, portable consumer electronics, automotive electronics and other industries.

The A6G2C series core board integrates the i.MX6UL processor, standard 128/256MB DDR3 and 128/256MBNAND Flash, hardware watchdog.Different types of core boards are equipped with WiFi, Bluetooth, Zigbee and other modules, with complete minimum system functions, which greatly shortens the product development cycle. The core board has passed strict EMC and high and low temperature tests to ensure that it can work stably in harsh environments.

Guangzhou ZLG Electronics Co., Ltd. provides various mature hardware solutions and rich software resources including Linux and AWorks operating systems. The complete software and hardware architecture allows you to focus on product application. It has the characteristics of short development cycle, humanized system and complete software supporting.

The A6G2C series core board is a 30 mmx48 mm core module with pins routed out through board-to-board connectors. Figure 1.1 shows the product appearance.

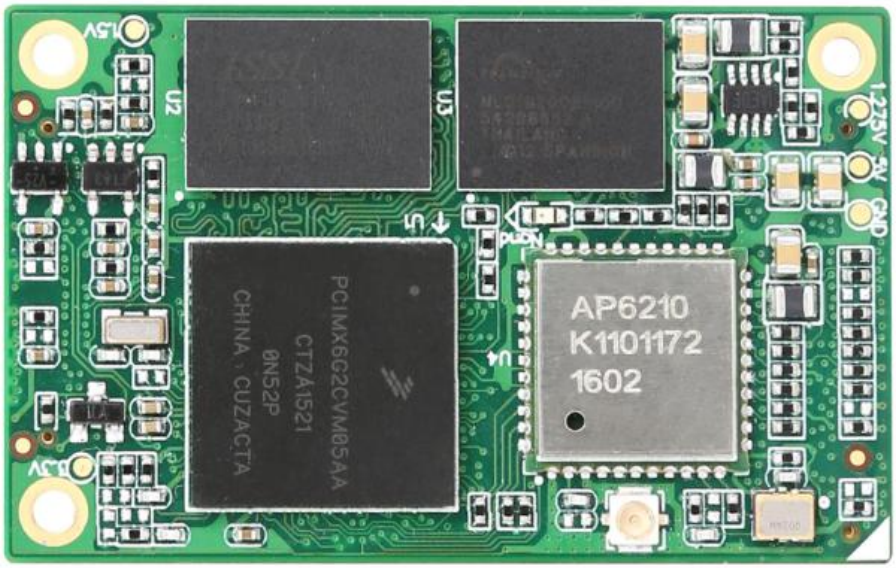


Figure 1.1 Product appearance

The A6G2C series core boards include seven product models: A6G2C-W128LI, A6G2C-W256LI, A6G2C-WB128LI, A6G2C-WB256LI, A6G2C-5WB128LI-T, A6G2C-Z128F128LI-T, and A6G2C-M128F128LI-T. For the convenience of description, the "A6G2C and A6G2A series core board" is abbreviated as "A6G2C core board" below.

1.1 Hardware Parameters

Processor

- 528MHz ARM Cortex-A7 32-bit microcontroller i.MX6UL;
- NEON MPE coprocessor;
- 32KB instruction, 32KB L1 data cache with single error detection (parity);
- 256KBL2 cache with error correcting code (ECC).

System memory

- Standard 128MByte DDR3 SDRAM
- （A6G2C-W128LI、A6G2C-WB128LI、A6G2C-5WB128LI-T、A6G2C-Z128F128LI-T、A6G2C-M128F128LI-T）；
- Standard 256MByte DDR3 SDRAM;
- （A6G2C-W256LI、A6G2C-WB256LI）。

Electronic hard disk

- Standard 128MByte NAND Flash
- （A6G2C-W128LI、A6G2C-WB128LI、A6G2C-5WB128LI-T、A6G2C-Z128F128LI-T、A6G2C-M128F128LI-T）；
- Standard 256MByte NAND Flash;
- （A6G2C-W256LI、A6G2C-WB256LI）。

1.2 Software Parameters

1.2.1 Linux Driver Library

The product provides the driver library under Linux for all the functional components of the A6G2C series core board. The specific driver resources are as follows:

- NAND Flash driver;
- The NAND Flash format is the TFAT file system (The file system will not be damaged if the system is suddenly powered off);
- Display driver (16-bit TFT LCD);
- Touch screen driver;
- LCD screen backlight driver;
- Audio interface driver;
- USB Host driver, support USB keyboard, USB mouse and U disk;
- USB OTG driver, support HOST and Device function driver switching;
- Ethernet driver;
- CAN-bus fieldbus driver;
- RS-232/RS-485 interface driver;
- SD card driver, support hot-swappable SD cards;
- WIFI, Bluetooth, Zigbee, NFC drivers, apps;
- General I/O driver;
- Buzzer driver;
- I2C driver;
- Watchdog driver.

1.2.2 AWorks Driver Library

Provides the driver library under AWorks for all the functional components of the A6G2C series core board, including the specific drivers

The resources are as follows:

- NAND Flash driver;
- Display driver (16-bit TFT LCD);

- Touch screen driver;
- LCD screen backlight driver;
- Audio interface driver;
- USB Host driver, support USB keyboard, USB mouse and U disk;
- USB OTG driver, support HOST and Device function driver switching;
- Ethernet driver;
- CAN-bus fieldbus driver;
- RS-232/RS-485 interface driver;
- SD card driver, support hot-swappable SD cards;
- WIFI, Bluetooth, Zigbee, NFC drivers, apps;
- General I/O driver;
- Buzzer driver;
- I2C driver;
- Watchdog driver.

The software and hardware can be customized. For product customization, please feel free to contact Guangzhou ZLG Electronics Co., Ltd.

1.3 Product Model Naming Rules

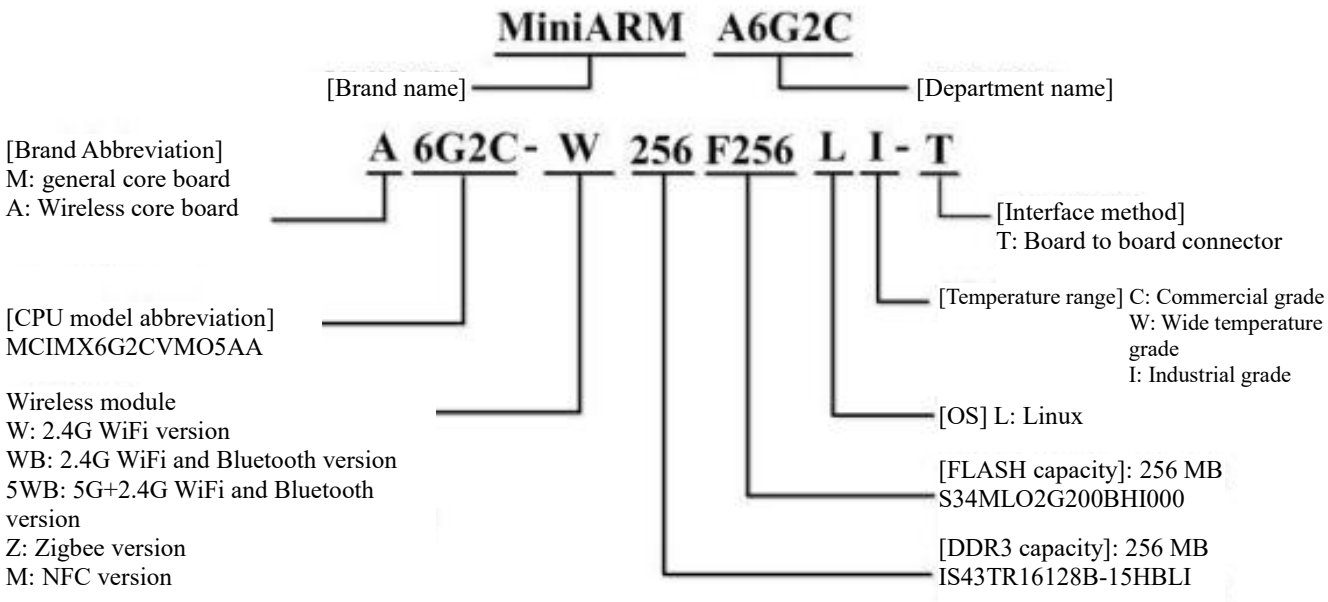


Figure 1.2 Product naming rules

1.4 Type Selection Comparison Table

Table 1.1 A6G2C series core board selection comparison table 1

Model / Resources	A6G2C-5WB128LI-T	A6G2C-Z128F128LI-T	A6G2C-W128LI
			A6G2C-W256LI
CPU model	MCIMX6G2CVM05AA	MCIMX6G2CVM05AA	MCIMX6G2CVM05AA
NandFlash	128MB	128MB	128MB
			256MB
Memory（DDR3）	128MB	128MB	128MB
			256MB
Ethernet	Two	Two	Two
USB OTG	Two	Two	Two
CAN	One way	Two	Two
LCD	Support (RGB565)	Support (RGB565)	Support (RGB565)
SD	One way	One way	One way
UART	7	7	8
I2C	One analog I2C (a maximum of four hardware I2C)	One analog I2C (a maximum of four hardware I2C)	One analog I2C (a maximum of four hardware I2C)
SPI	1 (a maximum of 4)	1 (a maximum of 4)	1 (a maximum of 4)
I^2S/SAI	1 (multiplexed)	1 (multiplexed)	1 (multiplexed)
PWM	2 (a maximum of 8)	2 (a maximum of 8)	2 (a maximum of 8)
ADC	1 x 2 channels (a maximum of 2 x 10 channels)	1 x 2 channels (a maximum of 2 x 10 channels)	1 x 2 channels (a maximum of 2 x 10 channels)
Touch screen	Support (4-wire resistive)	Support (4-wire resistive)	Support (4-wire resistive)
JTAG	Support	Support	Support
Analog audio	Supports medium quality PWM-like audio output	Supports medium quality PWM-like audio output	Supports medium quality PWM-like audio output
GPIO	2 (a maximum of 91)	2 (a maximum of 91)	2 (a maximum of 91)
Watchdog	Support independent hardware watchdog	Support independent hardware watchdog	Support independent hardware watchdog

Table 1.2 A6G2C series core board selection comparison table 2

Model / Resources	A6G2C-WB128LI / A6G2C-WB256LI	A6G2C-M128F128LI-T	A6G2A-W256F256LI-T
CPU model	MCIMX6G2CVM05AA	MCIMX6G2CVM05AA	MCIMX6G2AVM05AA
NandFlash	128MB / 256MB	128MB	256MB
Memory（DDR3）	128MB / 256MB	128MB	256MB
Ethernet	Two	Two	Two
USB OTG	Two	Two	Two
CAN	One way	Two	Two
LCD	Support (RGB565)	Support (RGB565)	Support (RGB565)
SD	One way	One way	One way
UART	7	8	8
I2C	One analog I2C (a maximum of four hardware I2C)	One analog I2C (a maximum of four hardware I2C)	One analog I2C (a maximum of four hardware I2C)
SPI	1 (a maximum of 4)	1 (a maximum of 4)	1 (a maximum of 4)
I^2S/SAI	1 (multiplexed)	1 (multiplexed)	1 (multiplexed)
PWM	2 (a maximum of 8)	2 (a maximum of 8)	2 (a maximum of 8)
ADC	1 x 2 channels (a maximum of 2 x 10 channels)	1 x 2 channels (a maximum of 2 x 10 channels)	1 x 2 channels (a maximum of 2 x 10 channels)
Touch screen	Support (4-wire resistive)	Support (4-wire resistive)	Support (4-wire resistive)
JTAG	Support	Support	Support
Analog audio	Supports medium quality PWM-like audio output	Supports medium quality PWM-like audio output	Supports medium quality PWM-like audio output
GPIO	2 (a maximum of 91)	2 (a maximum of 91)	2 (a maximum of 91)
Watchdog	Support independent hardware watchdog	Support independent hardware watchdog	Support independent hardware watchdog

2. Performance Parameters

2.1 Main Performance Configuration of A6G2C Core Board System

Table 2.1 System main frequency list

Name	Parameter	Specification				Description
		Minimum	Typical	Maximum	Unit	
System frequency	Fclk1	--	--	528	MHz	--
System RTC clock	Fclk2	--	32.768	--	KHz	--

The configuration in this table is the optimal configuration of the system, and it is recommended not to modify the configuration.

2.2 Operating Temperature of the Core Board

Table 2.2 A6G2C core board operating environment temperature

Core board model	Operating ambient temperature				Operating environment humidity (without condensation)			
	Minimum	Typical	Maximum	Unit	Minimum	Typical	Maximum	Unit
A6G2C-W128LI A6G2C-W256LI A6G2C-WB128LI A6G2C-WB256LI	-30	+25	+85	°C	5	--	95	% RH
A6G2A-W256F256LI-T	-30	+25	+85	°C	5	--	95	% RH
A6G2C-5WB128LI-T	-20	+25	+75	°C	5	--	95	% RH
A6G2C-Z128F128LI-T	-40	+25	+85	°C	5	--	95	% RH
A6G2C-M128F128LI-T	-40	+25	+85	°C	5	--	95	% RH

The official recommendation of the CPU manufacturer NXP for the CPU chip (MCIMX6G2CVM05AA):

If the junction temperature of the CPU chip in use exceeds 105°C, the CPU will enter the over-temperature protection state and will not be able to start and run properly. Take thermal measures to ensure that the junction temperature of the CPU is below 105°C so that the CPU can boot and operate properly. If the core board is used when the ambient temperature exceeds 70°C, or the junction temperature of the CPU chip exceeds 105°C, it is recommended that you use a temperature collector to collect the surface temperature of the CPU. If the surface temperature of the CPU exceeds 90°C, take heat dissipation measures, such as adding radiators and fans.

To protect the CPU, takes the following measures for the factory firmware by default:

1) When the board core board attempts to start, it is not allowed to start if the CPU junction temperature exceeds 100°C;

2) After the core board is started, if the CPU junction temperature exceeds 100°C, the system will start the frequency reduction function to reduce the junction temperature;

3) When the core board starts, the system will automatically shut down if the CPU junction temperature exceeds 105°C.

2.3 Storage capacity of the core board

Table 2.3 Storage capacity parameters

Type	Specification				Description
	Minimum	Typical	Maximum	Unit	
DDR3	--	128/256	--	MB	Memory
Nand Flash	--	128/256	--	MB	Program, data storage

2.4 A6G2C Core Board Communication Performance

Table 2.4 Serial communication interface speed of the A6G2C core board

Core board model	Parameter	Specification				Description
		Minimum	Typical	Maximum	Unit	
A6G2C core board	Serial communication speed	--	115200	--	bps	--
A6G2C core board	SPI communication speed	--	--	52	MHz	
A6G2C core board	I2C communication speed	--	100	400	Kbps	--
A6G2C core board	CAN communication speed	--	--	1	Mbps	--

2.5 Other Performance of A6G2C Core Board

Table 2.5 Watchdog parameters

Function	Parameter	Specification				Description
		Minimum	Typical	Maximum	Unit	
Hardware watchdog	Overflow period	1.12	1.4	1.6	s	--
	Reset pulse width	--	200	--	ms	--

Table 2.6 A6G2C core board I/O ports

Parameter	No.	Specification				Description
		Minimum	Typical	Maximum	Unit	
High-level input voltage	VI_H	2.3	--	3.3	V	--
Low-level input voltage	VI_L	0	--	0.69	V	--
High-level output voltage	V_{OH}	3.15	--	--	V	--
Low-level output voltage	V_{OL}	--	--	0.15	V	--
ESD protection	V_{ESD_HBM}	--	--	2000	V	Protection level of human body live contact

level						discharge
	V_{ESD_CDM}	--	--	500	V	Material contact discharge protection level during processing, handling, transportation, etc.

2.6 Power Supply Static Parameters

Table 2.7 Power supply static electrical parameters

Parameter	No.	Specification				Description
		Minimum	Typical	Maximum	Unit	
5.0V system voltage	VDD_5.0	4.75	5.0	5.25	V	--
5.0V system current	$IV_{DD\_5.0}$	--	110	130	mA	Boot current

Continued

parameter	No.	Specification				Description
		Minimum	Typical	Maximum	Unit	
RTC voltage	VDD_RTC	2.5	3.0	3.3	V	--
RTC current	IVDD_RTC	--	--	40	μA	--

3. Pin Function

3.1 Pin Information

The A6G2C series core board maintains the original definition of some pin multiplexing functions of the i.MX6UL processor, and redefines the extension or conversion functions. Users can refer to the design to cooperate with product standard-driven development. To ensure good compatibility and stability of product design, the pin resources not used by the user must be suspended. Figure 3.1 shows the interface pinout sequence.

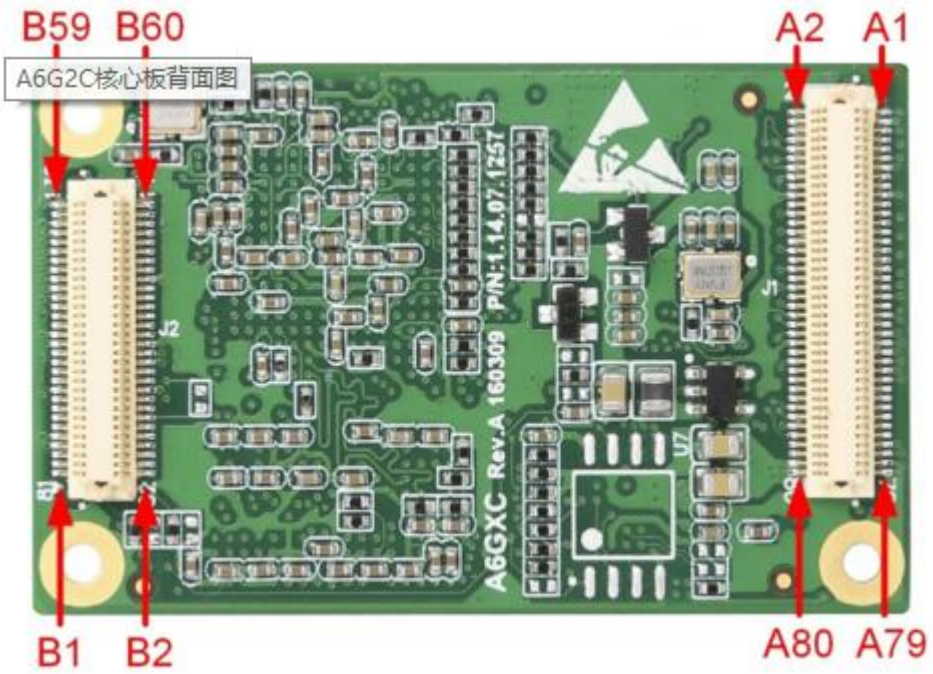


Figure 3.1 Interface pinout sequence

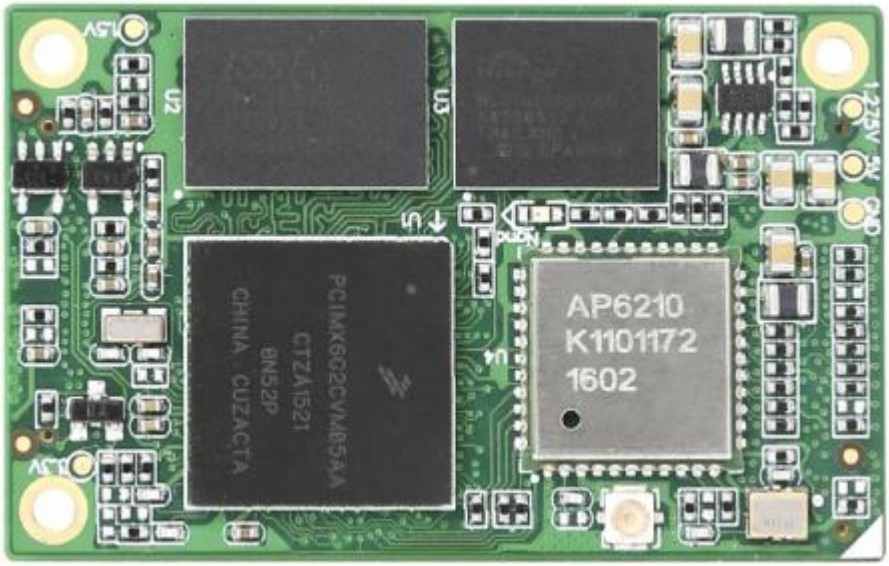


Figure 3.2 Front side of the product

3.2 A6G2C Core Board Pin Definitions

The following table lists the interface pin definitions of the A6G2C core board. All the pin functions of the A6G2C core board are specified in the "default function" of the following table. Do not modify them; otherwise, it may conflict with the factory driver. For any questions, please feel free to contact our sales or technical support.

Table 3.1 Interface pin definitions of the A6G2C series core board A

Pin No.	Name	Default function	Reference level	Input/Output	Processor pins
A1	ENET_MDIO	ENET1& ENET2	3.3V	Input/Output	K17
A2	ENET_MDC		3.3V	Output	L16
A3	ENET1_RXD1		3.3V	Input	E17
A4	ENET2_RXD1		3.3V	Input	C16
A5	ENET1_RXD0		3.3V	Input	F16
A6	ENET2_RXD0		3.3V	Input	C17
A7	ENET1_RXEN		3.3V	Output	E16
A8	ENET2_RXEN		3.3V	Output	B17
A9	ENET1_RXER		3.3V	Input	D15
A10	ENET2_RXER		3.3V	Input	D16
A11	ENET1_TXD1		3.3V	Output	E14
A12	ENET2_TXD1		3.3V	Output	A16
A13	ENET1_TXD0		3.3V	Output	E15
A14	ENET2_TXD0		3.3V	Output	A15
A15	ENET1_TXEN		3.3V	Output	F15
A16	ENET2_TXEN		3.3V	Output	B15
A17	ENET1_TX_CLK		3.3V	Output	F14
A18	ENET2_TX_CLK		3.3V	Output	D17
A19	GND	GND	--	--	--
A20	GND		--	--	--
A21	MQS_LEFT	Audio	--	Output	B16
A22	MOS_RIGHT		--	Output	A14
A23	UART7_RX	UART	3.3V	Input	B13
A24	UART7_TX		3.3V	Output	C13
A25	UART8_RX		3.3V	Input	B14
A26	UART8_TX		3.3V	Output	C14
A27	PWM_OUT6	PWM	3.3V	Output	D14
A28	PWM_OUT5		3.3V	Output	A13
A29	LCD_R4	LCD	3.3V	Output	D13
A30	LCD_R3		3.3V	Output	A12
A31	LCD_R2		3.3V	Output	B12
A32	LCD_R1		3.3V	Output	C12
A33	LCD_R0		3.3V	Output	D12
A34	LCD_G5		3.3V	Output	E12
A35	LCD_G4		3.3V	Output	A11
A36	LCD_G3		3.3V	Output	B11

Continued

Pin No.	Name	Default function	Reference level	Input/Output	Processor pins
A37	LCD_G2	LCD	3.3V	Output	D11
A38	LCD_G1		3.3V	Output	A10
A39	LCD_G0		3.3V	Output	B10
A40	LCD_B4		3.3V	Output	C10
A41	LCD_B3		3.3V	Output	D10
A42	LCD_B2		3.3V	Output	E10
A43	LCD_B1		3.3V	Output	A9
A44	LCD_B0		3.3V	Output	B9
A45	GND	GND	--	--	--
A46			--	--	--
A47	LCD_PCLK	LCD	3.3V	Output	A8
A48	LCD_HSYNC		3.3V	Output	D9
A49	LCD_DE		3.3V	Output	B8
A50	LCD_VSYNC		3.3V	Output	C9
A51	GPIO3_4	For usage details, see Table 3.3	3.3V	Input/Output	E9
A52	GND	GND	--	--	--
A53	BT_CFG1_6	BOOT	3.3V	Input	--
A54	BT_CFG1_7		3.3V	Input	--
A55	GPIO4_14(ERR)	GPIO	3.3V	Input/Output	B5
A56	GPIO4_16(RUN)		3.3V	Input/Output	E6
A57	UART6_TX	UART	3.3V	Output	F5
A58	SD1_CD	SD1	3.3V	Input	J14
A59	UART6_RX	UART	3.3V	Input	E5
A60	SD1_WP	SD1&SD2	3.3V	Input	K15
A61	SD2_CLK		--	--	--
A62	SD1_CLK		3.3V	Output	C1
A63	SD2_CMD		--	--	--
A64	SD1_CMD		3.3V	Output	C2
A65	SD2_DATA0		--	--	--
A66	SD1_DATA0		3.3V	Input/Output	B3
A67	SD2_DATA1		--	--	--
A68	SD1_DATA1		3.3V	Input/Output	B2
A69	SD2_DATA2		--	--	--
A70	SD1_DATA2		3.3V	Input/Output	B1
A71	SD2_DATA3		--	--	--
A72	SD1_DATA3		3.3V	Input/Output	A2
A73	SPI1_SCK	SPI1	3.3V	Output	D4
A74	SPI1_SS0		3.3V	Output	D3
A75	SPI1_MOSI		3.3V	Output	D2

Continued

Pin No.	Name	Default function	Reference level	Input/Output	Processor pins
A76	SPI1_MISO	SPI1	3.3V	Input	D1
A77	GND	GND	--	--	--
A78	5V_IN	POWER	--	Input	--
A79	GND		--	--	--
A80	5V_IN		--	Input	--

Table 3.2 Interface pin definitions of the A6G2C series core board B

Pin No.	Name	Default function	Reference level	Input/Output	Processor pins
B1	BOOT_MODE0	BOOT	3.3V	Input	T10
B2	BOOT_MODE1		3.3V	Input	U10
B3	nRST_OUT	RESET	3.3V	Output	--
B4	nRST_IN		3.3V	Input	--
B5	WDO_EN	Watchdog control pin	3.3V	Input	--
B6	MX6_ONOFF	System startup/shutdown	3.3V	Input	R8
B7	CAN1_TX	CAN1&CAN2 Table 3.3 lists the use of B9/B10	3.3V	Output	H15
B8	CAN1_RX		3.3V	Input	G14
B9	CAN2_TX		3.3V	Output	J15
B10	CAN2_RX		3.3V	Input	H14
B11	GPIO5_9	GPIO Table 3.3 describes the use of B11/B14/B15/B19	3.3V	Input/Output	R6
B12	GPIO5_1(Factory)		3.3V	Input/Output	R9
B13	I2C_SDA		3.3V	Input/Output	N9
B14	GPIO5_2(CLR)		3.3V	Input/Output	P11
B15	GPIO5_5		3.3V	Input/Output	N8
B16	GPIO5_4		3.3V	Input/Output	P9
B17	I2C_SCL		3.3V	Output	N10
B18	GPIO5_3		3.3V	Input/Output	P10
B19	GPIO5_6		3.3V	Input/Output	N11
B20	GND	GND	--	--	--
B21	USB_OTG1_VBUS	USB1&USB2	5V	Input	T12
B22	USB_OTG2_VBUS		5V	Input	U12
B23	USB_OTG1_ID		3.3V	Input	K13
B24	USB_OTG2_ID		3.3V	Input	M17
B25	USB_OTG1_D_N		3.3V	Input/Output	T15
B26	USB_OTG2_D_N		3.3V	Input/Output	T13
B27	USB_OTG1_D_P		3.3V	Input/Output	U15
B28	USB_OTG2_D_P		3.3V	Input/Output	U13
B29	nUSB_OTG_CHD		3.3V	Input	U16
B30	GND	GND	--	--	--
B31	GND	--	--	--	
B32	JTAG_TCK	JTAG	3.3V	Output	M14

Continued

Pin No.	Name	Default function	Reference level	Input/Output	Processor pins
B33	PMIC_ON_REQ	Power management	3.3V	Output	T9
B34	JTAG_nTRST	JTAG	3.3V	Input	N14
B35	CCM_CLK1_N	CPU clock differential negative	3.3V	Output	P16
B36	JTAG_TMS	JTAG	3.3V	Input	P14
B37	CCM_CLK1_P	CPU clock differential positive	3.3V	Output	P17
B38	JTAG_TDI	JTAG	3.3V	Input	N16
B39	ADC_CH9	ADC	--	Input	M15
B40	JTAG_TDO	JTAG	3.3V	Output	N15
B41	ADC_CH8	ADC	--	Input	N17
B42	JTAG_MOD	JTAG	3.3V	Input	P15
B43	VREF_ADC	ADC	--	Input	M13
B44	GND	GND	--	--	--
B45	UART1_TX	UART Table 3.3 describes the use of B47/B48	3.3V	Output	K14
B46	UART1_RX		3.3V	Input	K16
B47	UART2_TX		3.3V	Output	J17
B48	UART2_RX		5.0V	Input	J16
B49	UART3_TX		3.3V	Output	H17
B50	UART3_RX		3.3V	Input	H16
B51	UART4_TX		3.3V	Output	G17
B52	UART4_RX		3.3V	Input	G16
B53	UART5_TX		3.3V	Output	F17
B54	UART5_RX		3.3V	Input	G13
B55	TS_XN	TOUCH	3.3V	Input	L17
B56	TS_XP		3.3V	Input	M16
B57	TS_YN		3.3V	Input	L15
B58	TS_YP		3.3V	Input	L14
B59	GND	GND	--	--	--
B60	3V_BAT	RTC battery	--	Input	--

Table 3.3 Use of special pins

Pin No.	Name	Instructions
A51	GPIO3_4	1) A6G2C-W128LI, A6G2C-W256LI, A6G2A-W256F256LI-T support all except GPIO5_5 and GPIO5_9 2) A6G2C-Z128F128LI-T supports all except UART2_TX, UART2_RX, GPIO5_5, GPIO5_9 3) A6G2C-WB128LI, A6G2C-WB256LI, A6G2C-5WB128LI-T do not support these pins because this signal has been used for BT 4) A6G2C-M128F128LI-T support all the pins
B9	CAN2_TX	
B10	CAN2_RX	
B11	GPIO5_9	
B14	GPIO5_2	
B15	GPIO5_5	
B19	GPIO5_6	
B47	UART2_TX	
B48	UART2_RX	

3.3 Pin Function Description of the A6G2C Core Board

All pin functions of the A6G2C core board are specified in the "default function" in the following table. Do not modify them; otherwise, it may conflict with the factory driver. For any questions, please feel free to contact our sales or technical support.

Table 3.4 A6G2C core board pin function definition 1

Pin No.	Signal Name	Default function	Function description
A1	ENET_MDIO	ENET1&ENET2	Ethernet management data interface
A2	ENET_MDC		Ethernet management clock interface
A3	ENET1_RXD1		ENET1 data receive signal 1
A4	ENET2_RXD1		ENET2 data receive signal 1
A5	ENET1_RXD0		ENET1 data receive signal 0
A6	ENET2_RXD0		ENET2 data receive signal 0
A7	ENET1_RXEN		ENET1 data reception enable
A8	ENET2_RXEN		ENET2 data reception enable
A9	ENET1_RXER		ENET1 data reception error
A10	ENET2_RXER		ENET2 data reception error
A11	ENET1_TXD1		ENET1 data transmit signal 1
A12	ENET2_TXD1		ENET2 data transmit signal 1
A13	ENET1_TXD0		ENET1 data transmission signal 0
A14	ENET2_TXD0		ENET2 data transmission signal 0
A15	ENET1_TXEN		ENET1 data transmission enable
A16	ENET2_TXEN		ENET2 data transmission enable
A17	ENET1_TX_CLK		50MHz reference clock in RMII mode
A18	ENET2_TX_CLK		50MHz reference clock in RMII mode
A19	GND	GND	Power ground
A20	GND		
A21	MQS_LEFT	Analog audio output	Multimedia analog audio output left channel
A22	MQS_RIGHE		Multimedia analog audio output right channel
A23	UART7_RX	UART7&UART8	UART7 data reception
A24	UART7_TX		UART7 data transmission
A25	UART8_RX		UART8 data reception
A26	UART8_TX		UART8 data transmission
A27	PWM_OUT6	PWM	PWM channel 6 output (dedicated to buzzer drive)
A28	PWM_OUT5		PWM channel 5 output (dedicated to LCD backlight control)
A29	LCD_R4	LCD	LCD red component data bit 4
A30	LCD_R3		LCD red component data bit 3
A31	LCD_R2		LCD red component data bit 2
A32	LCD_R1		LCD red component data bit 1
A33	LCD_R0		LCD red component data bit 0
A34	LCD_G5		LCD green component data bit 5
A35	LCD_G4		LCD green component data bit 4
A36	LCD_G3		LCD green component data bit 3

Continued

Pin No.	Signal Name	Default Function	Function Description	
A37	LCD_G2		LCD green component data bit 2	
A38	LCD_G1	LCD	LCD green component data bit 1	
A39	LCD_G0		LCD green component data bit 0	
A40	LCD_B4		LCD blue component data bit 4	
A41	LCD_B3		LCD blue component data bit 3	
A42	LCD_B2		LCD blue component data bit 2	
A43	LCD_B1		LCD blue component data bit 1	
A44	LCD_B0		LCD blue component data bit 0	
A45	GND	GND	Power ground	
A46	GND			
A47	LCD_PCLK	LCD	LCD pixel clock	
A48	LCD_HSYNC		LCD horizontal synchronization signal	
A49	LCD_DE		LCD data output enable	
A50	LCD_VSYNC		LCD vertical synchronization signal	
A51	GPIO3_4	GPIO	General-purpose GPIO	
A52	GND	GND	Power ground	
A53	BT_CFG1_6	BOOT	00: Start from QSPI_Flash	01: Start from Nand (default)
A54	BT_CFG1_7		10: Start from SD card	11： --
A55	GPIO4_14	GPIO	Dedicated to ERR indicator control	
A56	GPIO4_16		System heartbeat RUN indicator control port, dedicated to the RUN indicator	
A57	UART6_TX	UART	UART6 data transmission	
A58	SD1_CD	SD1	SD1 card insertion detection	
A59	UART6_RX	UART	UART6 data reception	
A60	SD1_WP	SD1 SD2 has been used for the wireless module of the core board, so the A6G2C series wireless core board does not support the CSI camera interface	SD card write protection	
A61	SD2_CLK		SD2 card clock	
A62	SD1_CLK		SD1 card clock	
A63	SD2_CMD		SD2 card commands	
A64	SD1_CMD		SD1 card commands	
A65	SD2_DATA0		SD2 card data bit 0	
A66	SD1_DATA0		SD1 card data bit 0	
A67	SD2_DATA1		SD2 card data bit 1	
A68	SD1_DATA1		SD1 card data bit 1	
A69	SD2_DATA2		SD2 card data bit 2	
A70	SD1_DATA2		SD1 card data bit 2	
A71	SD2_DATA3		SD2 card data bit 3	
A72	SD1_DATA3		SD1 card data bit 3	
A73	SPI1_SCK	SPI1	SPI1 clock	
A74	SPI1_SS0		SPI1 chip selection	
A75	SPI1_MOSI		SPI1 master output and slave input	
A76	SPI1_MISO		SPI1 master input and slave output	

Continued

Pin No.	Signal Name	Default function	Function description
A77	GND	POWER	Power ground
A78	5V_IN		5V power supply
A79	GND		Power ground
A80	5V_IN		5V power supply

Table 3.5 A6G2C core board pin function definition 2

Pin No.	Signal Name	Default function	Function description	
B1	BOOT_MODE0	BOOT	00: Start from CPU fuse bit	01: Internal boot (default)
B2	BOOT_MODE1		10: Serial boot	11: Reserved
B3	nRST_OUT	RST	Core board reset output	
B4	nRST_IN		External reset input	
B5	WDO_EN	Function pin	Watchdog disable/enable pin	
B6	MX6_ONOFF		CPU wake/sleep hard control pin	
B7	CAN1_TX	CAN1 &CAN2 The use of B9/B10 is described in Table 3.3	CAN1 data transmission	
B8	CAN1_RX		CAN1 data reception	
B9	CAN2_TX		CAN2 data transmission	
B10	CAN2_RX		CAN2 data reception	
B11	GPIO5_9	GPIO Table 3.3 describes the use of B11/B14/B15/B19	General-purpose GPIO5_9	
B12	Factory		GPIO5_1, used in ZLG factory mode, used in ZLG internal configuration, the user can be suspended	
B13	I2C_SDA		General-purpose GPIO5_8 analog I2C data pin	
B14	CLR（GPIO5_2）		GPIO5_2, the WCE7 system is used to reset the registry. If it is low at startup, clear the registry. Linux systems can be used for normal GPIO.	
B15	GPIO5_5		General-purpose GPIO5_5	
B16	GPIO5_4		General-purpose GPIO5_4	
B17	I2C _SCL		General purpose GPIO5_7 analog I2C clock pin	
B18	GPIO5_3		General-purpose GPIO5_3	
B19	GPIO5_6		General-purpose GPIO5_6	
B20	GND	GND	Power ground	
B21	USB_OTG1_VBUS	USB1&USB2	USB VBUS power input	
B22	USB_OTG2_VBUS			
B23	USB_OTG1_ID		USB ID signal	
B24	USB_OTG2_ID			
B25	USB_OTG1_D_N		USB data signal negative	
B26	USB_OTG2_D_N			
B27	USB_OTG1_D_P		USB data signal positive	
B28	USB_OTG2_D_P			
B29	nUSB_OTG_CHD		USB charging detection	
B30	GND	GND	Power ground	

Continued

Pin No.	Signal Name	Default Function	Function Description
B31	GND	GND	Power ground
B32	JTAG_TCK	JTAG	JTAG controller clock
B33	PMIC_ON_REQ	Function pin	CPU power management enable IO
B34	JTAG_nTRST	JTAG	JTAG controller reset
B35	CCM_CLK1_N	CPU clock	CPU output clock negative
B36	JTAG_TMS	JTAG	JTAG controller mode selection
B37	CCM_CLK1_P	CPU clock	CPU output clock positive
B38	JTAG_TDI	JTAG	JTAG controller data input
B39	ADC_CH9	ADC	ADC channel 9
B40	JTAG_TDO	JTAG	JTAG controller data output
B41	ADC_CH8	ADC	ADC channel 8
B42	JTAG_MOD	JTAG	JTAG mode control
B43	VREF_ADC	ADC	ADC reference voltage pin. This pin has no function
B44	GND	GND	Power ground
B45	UART1_TX	UART The use of B47/B48 is shown in Table 3.3	UART1 data transmission
B46	UART1_RX		UART1 data reception
B47	UART2_TX		UART2 data transmission
B48	UART2_RX		UART2 data reception
B49	UART3_TX		UART3 data transmission
B50	UART3_RX		UART3 data reception
B51	UART4_TX		UART4 data transmission
B52	UART4_RX		UART4 data reception
B53	UART5_TX		UART5 data transmission
B54	UART5_RX		UART5 data reception
B55	TS_XN	TOUCH	Touch screen XPUL signal
B56	TS_XP		Touch screen XNUR signal
B57	TS_YN		Touch screen YPLL signal
B58	TS_YP		Touch screen YNLR signal
B59	GND	GND	Power ground
B60	3V_BAT	3V power supply	CPU internal RTC battery interface

3.4 A6G2C Core Board Pin Description (By Function)

Table 3.6 A6G2C core board function pin definition

Function	Signal Name	Function description	Pin No.
Startup configuration	BT_CFG1_7	Boot mode configuration. You can configure the system to boot from NAND Flash, QSPI Flash or SD Card through jumpers (BOOT_MODE needs to be configured as internal boot)	A53
	BT_CFG1_6		A54
	BOOT_MODE1	Boot mode configuration. You can boot from CPU fuse configuration, serial download or internal boot via jumper configuration.	B2
	BOOT_MODE0		B1

Continued

Function	Signal Name	Function description	Pin No.
Reset control	nRST_OUT	Watchdog reset output. This signal is the same signal as the signal that resets the CPU. If not in use, suspend it	B3
	nRST_IN	Cold reset input, active low level	B4
	WDO_EN	Disable watchdog in the case of high level; enable watchdog in the case of low level or suspension	B5
Function control	MX6_ONOFF	CPU hard sleep, wake-up pin, can be suspended if not used	B6
	CLR	Table 3.3 describes the use of B14	B14
	Factory	ZLG factory mode	B12
	GPIO4_14(ERR)	System error ERR indicator. When not in use, it can be configured as a GPIO	A55
	GPIO4_16(RUN)	System heartbeat RUN indicator	A56
ENET1	ENET1_RXD1	Ethernet 1 data receive 1	A3
	ENET1_RXD0	Ethernet 1 data receive 0	A5
	ENET1_RXEN	Ethernet 1 data reception enable	A7
	ENET1_RXER	Ethernet 1 data receive error	A9
	ENET1_TXD1	Ethernet 1 data send 1	A11
	ENET1_TXD0	Ethernet 1 data send 0	A13
	ENET1_TXEN	Ethernet 1 data transmission enable	A15
	ENET1_TX_CLK	Ethernet 1 50MHz reference clock	A17
Configure the interface	ENET_MDIO	Ethernet management data interface	A1
	ENET_MDC	Ethernet management clock interface	A2
ENET2	ENET2_RXD1	Ethernet 2 data receive 1	A4
	ENET2_RXD0	Ethernet 2 data receive 0	A6
	ENET2_RXEN	Ethernet 2 data reception enable	A8
	ENET2_RXER	Ethernet 2 data receive error	A10
	ENET2_TXD1	Ethernet 2 data send 1	A12
	ENET2_TXD0	Ethernet 2 data send 0	A14
	ENET2_TXEN	Ethernet 2 data transmission enable	A16
	ENET2_TX_CLK	Ethernet 2 50MHz reference clock	A18
LCD	LCD_R4~ LCD_R0	LCD red component	A29~A33
	LCD_G5~ LCD_G0	LCD green component	A34~A39
	LCD_B4~ LCD_B0	LCD blue component	A40~A44
	LCD_PCLK	LCD pixel clock	A47
	LCD_HSYNC	LCD horizontal synchronization signal	A48
	LCD_DE	LCD data output enable	A49
	LCD_VSYNC	LCD vertical synchronization signal	A50
TOUCH	TS_XN	Touch screen XPUL signal	B55
	TS_XP	Touch screen XNUR signal	B56
	TS_YN	Touch screen YPLL signal	B57
	TS_YP	Touch screen YNLR signal	B58
MQS audio	MQS_LEFT	Multimedia audio left channel	A21
	MQS_RIGTH	Multimedia audio right channel	A22

Continued

Function	Signal Name	Function description	Pin No.
PWM	PWM5_OUT	PWM channel 6 output	A27
	PWM6_OUT	PWM channel 5 output	A28
SD1	SD1_CD	SD1 card detection	A58
	SD1_WP	SD1 card write protection	A60
	SD1_CLK	SD1 card clock	A62
SD1	SD1_CMD	SD1 card commands	A64
	SD1_DATA0	SD1 card data 0	A66
	SD1_DATA1	SD1 card data 1	A68
	SD1_DATA2	SD1 card data 2	A70
	SD1_DATA3	SD1 card data 3	A72
SPI1	SPI1_SCK	SPI1 clock	A73
	SPI1_SS0	SPI1 chip selection	A74
	SPI1_MOSI	SPI1 master output and slave input	A75
	SPI1_MISO	SPI1 master input and slave output	A76
CAN	CAN1_RXD	CAN1 data reception	B8
	CAN1_TXD	CAN1 data transmission	B7
	CAN2_RXD	CAN2 data reception	B10
	CAN2_TXD	CAN2 data transmission	B9
GPIO	GPIO5_9	General-purpose GPIO5_9	B11
	GPIO5_6	General-purpose GPIO5_6	B19
	GPIO5_5	General-purpose GPIO5_5	B15
	GPIO5_4	General-purpose GPIO5_4	B16
	GPIO5_3	General-purpose GPIO5_3	B18
I2C	I2C_SCL	I2C_SCL	B17
	I2C_SDA	I2C_SDA	B13
USB_OTG1	USB_OTG1_VBUS	USB1 VBUS power supply	B21
	USB_OTG1_ID	USB1 ID signal	B23
	USB_OTG1_D_N	USB1 D-signal	B25
	USB_OTG1_D_P	USB1 D+ signal	B27
	nUSB_OTG_CHD	USB charging detection	B29
USB_OTG2	USB_OTG2_VBUS	USB2 VBUS power supply	B22
	USB_OTG2_ID	USB2 ID signal	B24
	USB_OTG2_D_N	USB2 D-signal	B26
	USB0_OTG2_D_P	USB2 D+ signal	B28
ADC	ADC_CH9	Analog input	B39
	ADC_CH8	Analog input	B41
JTAG	JTAG_nTRST	JTAG controller reset	B34
	JTAG_TDO	JTAG controller data output	B40
	JTAG_TDI	JTAG controller data input	B38
	JTAG_TMS	JTAG controller mode selection	B36

Continued

Function	Signal Name	Function description	Pin No.
JTAG	JTAG_TCK	JTAG controller clock	B32
UART	UART1_RXD	UART1 data reception (debug serial port)	B46
	UART1_TXD	UART1 data transmission (debug serial port)	B45
	UART2_RXD	UART2 data reception	B48
	UART2_TXD	UART2 data transmission	B47
	UART3_RXD	UART3 data reception	B50
UART	UART3_TXD	UART3 data transmission	B49
	UART4_RXD	UART4 data reception	B52
	UART4_TXD	UART4 data transmission	B51
	UART5_RXD	UART5 data reception	B54
	UART5_TXD	UART5 data transmission	B53
	UART6_RXD	UART6 data reception	A57
	UART6_TXD	UART6 data transmission	A59
	UART7_RXD	UART7 data reception	A23
	UART7_TXD	UART7 data transmission	A24
	UART8_RXD	UART8 data reception	A25
	UART8_TXD	UART8 data transmission	A26
Power supply	GND	Power ground	A19
	GND	Power ground	A20
	GND	Power ground	A45
	GND	Power ground	A46
	GND	Power ground	A52
	GND	Power ground	A77
	GND	Power ground	A79
	5V_IN	Main power supply pin of the core board	A78
	5V_IN	Main power supply pin of the core board	A80
	GND	Power ground	B20
	GND	Power ground	B21
	GND	Power ground	B44
	GND	Power ground	B59
	3V_BAT	CPU internal RTC battery interface	B60

The BOOT_MODE boot configuration in the preceding table has priority over the BT_CFG1 boot configuration.

The VREF_ADC pin in the preceding table is the external reference voltage adjustment pin of the ADC. The internal configuration is 3.3 V, which cannot be modified. This pin has no adjustment function.

3.5 Common Interface Multiplexing of the A6G2C Series Core Board

Here, the maximum number that each interface can achieve is divided. Pay attention to its multiplexing relationship with other interfaces during use to avoid functional conflicts.

3.5.1 SPI

The i.MX6UL manual supports a maximum of four SPIs. The A6G2C series core board uses some SPI interface pins due to the occupation of other interface resources.In the process of using multiple SPIs, you can refer to the following table for reconfiguration.

Table 3.7 SPI1

Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
A73	CSI_DATA04	SPI1_SCK	SPI1_SCK	SPI1 Supports a maximum of four chip selections.
A26	LCD_DATA20	UART8_TX		
A75	CSI_DATA06	SPI1_MOSI	SPI1_MOSI	
A22	LCD_DATA22	MQS_RIGHT		
A76	CSI_DATA07	SPI1_MISO	SPI1_MISO	
A21	LCD_DATA23	MQS_LEFT		
A74	CSI_DATA05	SPI1_SS0	SPI1_SS0	
A25	LCD_DATA21	UART8_RX		
A39	LCD_DATA05	LCD_G0	SPI1_SS1	
A38	LCD_DATA06	LCD_G1	SPI1_SS2	
A37	LCD_DATA07	LCD_G2	SPI1_SS3	

Note 1: All A6G2C core boards support this SPI1 interface;

Note 2: The factory firmware default configuration of SPI1 and CSI_DATA04/05/06/07 is a multiplexing relationship. Make a reasonable allocation before use.

Note 3: If the chip selection SS1/SS2/SS3 is used, the LCD_G0/1/2 signal cannot be used. Make a reasonable allocation before use.

Table 3.8 SPI^2

Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
B51	UART4_TX_DATA	UART4_TX	SPI^2_SCK	SPI^2 Supports a maximum of four chip selections.
B53	UART5_TX_DATA	UART5_TX	SPI^2_MOSI	
B54	UART5_RX_DATA	UART5_RX	SPI^2_MISO	
B52	UART4_RX_DATA	UART4_RX	SPI^2_SS0	
A48	LCD_HSYNC	LCD_HSYNC	SPI^2_SS1	
A50	LCD_VSYNC	LCD_VSYNC	SPI^2_SS2	
A51	LCD_RESET	GPIO3_4	SPI^2_SS3	

Note 1: All A6G2C core boards support the SPI^2 interface;

Note 2: The SPI^2 is not the default function of the firmware, and is in a multiplexing relationship with the CSI and LCD interfaces. Make a reasonable allocation before use.

Note 3: If the chip selection SS1/SS2/SS3 is used, the corresponding LCD signal cannot be used. Make a reasonable allocation before use.

Table 3.9 SPI3

Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
B48	UART2_RX_DATA	UART2_RX	SPI3_SCK	The SPI3 supports a maximum of one chip selection. The SPI3_SS1/2/3 has been used by the Nand Flash signal cable.
B9	UART2_CTS_B	CAN2_TX	SPI3_MOSI	
B10	UART2_RTS_B	CAN2_RX	SPI3_MISO	
B47	UART2_TX_DATA	UART2_TX	SPI3_SS0	

Note 1: The WB wireless core board and A6G2C-Z128F128LI-T do not support the SPI3 interface;

Note 2: The yellow CAN2_TX/RX signal cannot be multiplexed on the A6G2C core board, but can be multiplexed as SPI3_MOSI/MISO signal.

Note 3: This SPI3 is not the default function of the firmware, and is multiplexed with the UART2 and CAN2 interfaces. Make a reasonable allocation before use.

Table 3.10 SPI4

Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
A12	ENET2_TX_DATA1	ENET2_TXD1	SPI4_SCK	The SPI4 supports a maximum of one chip select. The SPI4_SS1/2/3 have been used by Nand Flash signal cables
A16	ENET2_TX_EN	ENET2_TXEN	SPI4_MOSI	
A18	ENET2_TX_CLK	ENET2_TX_CLK	SPI4_MISO	
A10	ENET2_RX_ER	ENET2_RXER	SPI4_SS0	

Note 1: All A6G2C core boards support this SPI4 interface.

Note 2: The A6G2C core board cannot multiplex the yellow ENET signal, but can be multiplexed into the SPI4 signal.

Note 3: The SPI4 is not the default function of the firmware, and it is in a multiplexing relationship with the ENET2 interface. It should be allocated reasonably before use.

3.5.2 uSDHC

The A6G2C series core board supports one Ultra Secured Digital Host Controller (uSDHC), which provides a corresponding interface for the communication between the system and SD/SDIO/MMC card. The uSDHC has the following features:

- Compatible with SD specification V3.0;
- Compatible with SDIO specification V3.0;
- Compatible with MMC specification V4.2 / 4.3 / 4.4 / 4.41;
- Card bus clock frequency up to 208 MHz;
- Support the write operation of the write protection switch;
- Support 1-bit and 4-bit SD/SDIO mode, and 1-bit and 4-bit MMC mode.

The A6G2C series core board firmware has one SD interface by default, as shown in the following figure.

Table 3.11 SD1

Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
A58	UART1_RTS_B	SD1_CD	SD1_CD	SD1_CD is the card inserted Detection signal, valid at low level; SD1_WP is card write protection detection, high Active level, low level Indicates no write protection
A60	UART1_CTS_B	SD1_WP	SD1_WP	
A62	SD1_CLK	SD1_CLK	SD1_CLK	
A64	SD1_CMD	SD1_CMD	SD1_CMD	
A66	SD1_DATA0	SD1_DATA0	SD1_DATA0	
A68	SD1_DATA1	SD1_DATA1	SD1_DATA1	
A70	SD1_DATA2	SD1_DATA2	SD1_DATA2	
A72	SD1_DATA3	SD1_DATA3	SD1_DATA3	

Note 1: This SD interface is the default configuration of the system factory firmware.

3.5.3 UART

The universal asynchronous receiver/transmitter (UART) can use the RS-232 communication cable to realize serial communication with external equipment by using the level converter; or by using an external circuit that converts infrared signals into electrical signals (for reception), or low-speed IrDA communication is achieved by an external circuit that converts the signal to drive the infrared LED (for transmission). The UART supports NRZ

encoding format, compatible with 9-bit RS-485 data format and IrDA infrared low-rate format. The A6G2C series core board provides eight UART interfaces. Its main features are as follows:

- Compatible with high-speed TIA / EIA-232-F specifications, up to 5.0 Mbit/s;
- Support the low-speed serial infrared interface, compatible with IrDA (rate up to 115.2 kbit/s);
- Support 9-bit or multi-point mode (RS-485), and support automatic slave address detection;
- Support 7-bit or 8-bit data bits (RS-232 characters), or 9-bit RS-485 format;
- Support 1 or 2 stop bits;
- Programmable parity check (even check, odd check, no check);
- Support RTS/CTS hardware flow control.

Table 3.12 UART1

Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
B45	UART1_TX_DATA	UART1_TX	UART1_TX	UART1 is the serial port for system debugging
B46	UART1_RX_DATA	UART1_RX	UART1_RX	

Note 1: Default configuration: baud rate 115，200 bps, without flow control, data bit 8bit, stop bit 1bit, no parity check.

Table 3.13 UART2

Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
B47	UART2_TX_DATA	UART2_TX	UART2_TX	Firmware default Hardware flow control B9/B10/B47/B48 is not configured. See Table 3.3 for pin usage
B48	UART2_RX_DATA	UART2_RX	UART2_RX	
B9	UART2_CTS_B	CAN2_TX	UART2_CTS_B	
B49	UART3_TX_DATA	UART3_TX		
B10	UART1_RTS_B	CAN2_RX	UART1_RTS_B	
B50	UART3_RX_DATA	UART3_RX		

Note 1: The default factory configuration does not include hardware flow control. The flow control pin and CAN2/UART3 signal are multiplexed. Make reasonable allocation before use.

Table 3.14 UART3

Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
B49	UART3_TX_DATA	UART3_TX	UART3_TX	Firmware default Do not configure hardware flow control
B50	UART3_RX_DATA	UART3_RX	UART3_RX	
B7	UART3_CTS_B	CAN1_TX	UART3_CTS_B	
B8	UART3_RTS_B	CAN1_RX	UART3_RTS_B	

Note 1: The default factory configuration does not include hardware flow control. The flow control pin and CAN1 signal are multiplexed. Make reasonable allocation before use.

Table 3.15 UART4

Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
B51	UAR4_TX_DATA	UART4_TX	UART4_TX	Firmware default Do not configure hardware flow control
B52	UART4_RX_DATA	UART4_RX	UART4_RX	
A3	ENET1_RX_DATA1	ENET1_RXD1	UART4_CTS_B	
A48	LCD_HSYNC	LCD_HSYNC		
A5	ENET1_RX_DATA0	ENET1_RXD0	UART4_RTS_B	
A50	LCD_VSYNC	LCD_VSYNC		

Note 1: It is the factory default configuration serial port 4. The flow control pin and ENET1/LCD signal are multiplexed. Make a reasonable allocation before use.

Table 3.16 UART5

Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
B53	UART5_TX_DATA	UART5_TX	UART5_TX	Firmware default Do not configure hardware flow control
B54	UART5_RX_DATA	UART5_RX	UART5_RX	
A7	ENET1_TX_DATA0	ENET1_TXD0	UART5_CTS_B	
A13	ENET1_RX_EN	ENET1_RXEN	UART5_RTS_B	

Note 1: It is the default factory configuration serial port 4. The flow control pin and NET1 control signal are multiplexed. Make a reasonable allocation before use.

Table 3.17 UART6

Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
A57	CSI_MCLK	UART6_TX	UART6_TX	Firmware default Do not configure hardware flow control
A59	CSI_PIXCLK	UART6_RX	UART6_RX	
A11	ENET1_TX_DATA1	ENET1_TXD1	UART6_CTS_B	
A15	ENET1_TX_EN	ENET1_TXEN	UART6_RTS_B	

Note 1: It is the default factory configuration serial port 6. The flow control pin and NET1 control signal are multiplexed. Make a reasonable allocation before use.

Table 3.18 UART7

Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
A24	LCD_DATA16	UART7_TX	UART7_TX	Firmware default Do not configure hardware flow control
A23	LCD_DATA17	UART7_RX	UART7_RX	
A17	ENET1_TX_CLK	ENET1_TX_CLK	UART7_CTS_B	
A38	LCD_DATA06	LCD_G1		
A9	ENET1_RX_ER	ENET1_RXER	UART7_RTS_B	
A37	LCD_DATA07	LCD_G2		

Note 1: It is the default factory configuration serial port 7. The flow control pin and NET1/LCD control signal are multiplexed. Make a reasonable allocation before use.

Table 3.19 UART8

Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
A26	LCD_DATA20	UART8_TX	UART8_TX	Firmware default Do not configure hardware flow control
A25	LCD_DATA21	UART8_RX	UART8_RX	
A18	ENET2_TX_CLK	ENET2_TX_CLK	UART8_CTS_B	
A40	LCD_DATA04	LCD_B4		
A37	ENET2_RX_ER	ENET2_RXER	UART8_RTS_B	
A39	LCD_DATA05	LCD_G0		

Note 1: It is the default factory configuration serial port 8. The flow control pin and NET2/LCD control signal are multiplexed. Make a reasonable allocation before use.

3.5.4 I²C

The MX6UL supports a maximum of four I2Cs. It mainly works in two functional modes: In standard mode, the data transfer rate can reach a maximum of 100 kbits/s. In fast mode, the data transfer rate can reach a maximum of 400 kbits/s.

The A6G2C series core board has multiplexed four hardware I2C pins into other functions for common interface considerations, such as UART1/4/5/6, touch screen signal, and LCD signal, as shown in Table 3.20. Therefore, the configured firmware I2C is analog I2C.

Table 3.20 I2C1

Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
A59	CSI_PIXCLK	UART6_RX	I2C1_SCL	Firmware default I2C1 is not configured
B51	UART4_TX_DATA	UART4_TX		
B58	GPIO1_IO02	TS_YP	I2C1_SCL	
A57	CSI_MCLK	UART6_TX	I2C1_SDA	
B52	UART4_RX_DATA	UART4_RX		
B55	GPIO1_IO03	TS_XN		

Note 1: Because the default configuration of the firmware uses the UART4/UART6/TS_YP/XN function, the I2C1 firmware is not configured and used by default.

Table 3.21 I2C2

Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
B23	GPIO1_IO00	USB_OTG1_ID	I2C2_SCL	Firmware default The I2C2 is not configured
B53	UART5_TX_DATA	UART5_TX		
B54	UART5_RX_DATA	UART5_RX	I2C2_SDA	
B57	GPIO1_IO01	TS_YN		

Note 1: Because the firmware uses the UART5/TS_YN/USB_OTG1_ID function by default, the I2C2 firmware is not configured and used by default.

Table 3.22 I2C3

Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
A6	ENET2_RX_DATA0	ENET2_RXD0	I2C3_SCL	Firmware default The I2C3 is not configured
A43	LCD_DATA01	LCD_B1		
B45	UART1_TX_DATA	UART1_TX		
A4	ENET2_RX_DATA1	ENET2_RXD1	I2C3_SDA	
A44	LCD_DATA00	LCD_B0		
B46	UART1_RX_DATA	UART1_RX		

Note 1: Because the firmware uses the UART1/NET2/LCD signal function by default, the I2C3 firmware is not configured and used by default.

Table 3.23 I2C4

Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
A8	ENET2_RX_EN	ENET2_RXEN	I2C4_SCL	Firmware default The I2C4 is not configured
A41	LCD_DATA03	LCD_B3		
B47	UART2_TX_DATA	UART2_TX		
A14	ENET2_TX_DATA0	ENET2_TXD0	I2C4_SDA	
A42	LCD_DATA02	LCD_B2		
B48	UART2_RX_DATA	UART2_RX		

Note 1: Because the firmware uses the UART2/NET2/LCD signal function by default, the I2C4 firmware is not configured and used by default.

Note 2: Table 3.3 lists the use of B47/B48

3.5.5 SAI

The i.MX6UL supports a maximum of three simultaneous audio interfaces (SAI). The interface supports full-duplex serial interfaces with frame synchronization, such as I^2S, AC97, TDM and codec/DSP interfaces. Due

to resource reallocation, the A6G2C supports a maximum of two SAI interfaces. The SAI interface has the following features:

- The transmitter/receiver has independent bit clock and frame synchronization and supports one data line;
- The maximum frame size is 32 characters;
- The character size is between 8 bits and 32 bits;
- Each transmit and receive channel supports asynchronous 32x32-bit FIFO;
- Support normal restart after FIFO error;

Table 3.24 SAI3 pin allocation

Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
A35	LCD_DATA09	LCD_G4	SAI3_MCLK	Firmware default The SAI3 is not configured
A47	LCD_CLK	LCD_PCLK		
A33	LCD_DATA11	LCD_R0	SAI3_RX_BCLK	
A30	LCD_DATA14	LCD_R3	SAI3_RX_DATA	
A50	LCD_VSYNC	LCD_VSYNC		
A34	LCD_DATA10	LCD_G5	SAI3_RX_SYNC	
A31	LCD_DATA13	LCD_B2	SAI3_TX_BCLK	
A48	LCD_HSYNC	LCD_HSYNC	SAI3_TX_BCLK	
A29	LCD_DATA15	LCD_R4	SAI3_TX_DATA	
A51	LCD_RESET	GPIO3_4		
A32	LCD_DATA12	LCD_R1	SAI3_TX_SYNC	
A49	LCD_ENABLE	LCD_DE		

3.5.6 PWM

The i.MX6UL supports a maximum of eight PWMs. The PWM has one 16-bit counter. It is optimized to generate sounds and tones from stored sample audio images. It uses 16-bit resolution and 4x16-bit data FIFO to generate sound, and its main features are as follows:

- 16-bit up-counter with clock source selection;
- 4 x 16-bit FIFO to minimize interrupt overhead;
- Support 12-bit prescaler for frequency division;
- Generate sounds and tones;
- Configurable High level or low level active output;
- Programmable to be active in low power mode;
- Programmable to be active in debug mode.

Table 3.25 A6G2C series core board PWM allocation

Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
A5	ENET1_RX_DATA0	ENET1_RXD0	PWM1	The firmware is not configured with the PWM1 function by default
A44	LCD_DATA00	LCD_B0		
B41	GPIO1_IO08	ADC_CH8		
A3	ENET1_RX_DATA1	ENET1_RXD1	PWM2	The firmware is not configured with the PWM2 function by default
A43	LCD_DATA01	LCD_B1		
B39	GPIO1_IO09	ADC_CH9		

Continued

Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
A42	LCD_DATA02	LCD_B2	PWM3	The firmware is not configured with the PWM3 function by default
B56	GPIO1_IO04	TS_XP		
A41	LCD_DATA03	LCD_B3	PWM4	The PWM4 function is not configured by default
B24	GPIO1_IO05	USB_OTG2_ID		
A11	ENET1_TX_DATA1	ENET1_TXD1	PWM5	The PWM5 firmware is configured by default; the PWM5 function is configured by default
A28	LCD_DATA18	PWM_OUT5		
A56	NAND_DQS	GPIO4_16(RUN)		
A15	ENET1_TX_EN	ENET1_TXEN	PWM6	The firmware is configured with the PWM6 function by default
A27	LCD_DATA19	PWM_OUT6		
B38	JTAG_TDI	JTAG_TDI		
A17	ENET1_TX_CLK	ENET1_TX_CLK	PWM7	The firmware is not configured with the PWM7 function by default
B32	JTAG_TCK	JTAG_TCK		
A9	ENET1_RX_ER	ENET1_RXER	PWM8	The firmware is not configured with the PWM8 function by default
B34	JTAG_TRST_B	JTAG_nTRST		

Note 1: The i.MX6UL supports a maximum of eight PWMs, but the A6G2C is configured only with PWM5/6 by default, as shown in green font.

3.5.7 ADC

The i.MX6UL integrates two successive approximation ADCs with a resolution of up to 12 bits. Each channel supports a maximum of 10 input channels. Its main features are as follows:

Linear successive approximation ADC, 12-bit resolution, supports 10/11-bit precision;

- Support up to 10 dedicated single-ended input channels;
- A maximum of 1 MS/s sampling rate;
- A maximum of 16 single-ended external analog inputs;
- Support 8-bit, 10-bit, 12-bit output modes.

Table 3.26 ADC channels supported by i.MX6UL

Signal	Description	Chip corresponding pin	Direction
ADC1_IN0	A/D converter 1 input channel 0	GPIO1_IO00	Input
ADC1_IN1	A/D converter 1 input channel 1	GPIO1_IO01	Input
ADC1_IN2	A/D converter 1 input channel 2	GPIO1_IO02	Input
ADC1_IN3	A/D converter 1 input channel 3	GPIO1_IO03	Input
ADC1_IN4	A/D converter 1 input channel 4	GPIO1_IO04	Input
ADC1_IN5	A/D converter 1 input channel 5	GPIO1_IO05	Input
ADC1_IN6	A/D converter 1 input channel 6	GPIO1_IO06	Input
ADC1_IN7	A/D converter 1 input channel 7	GPIO1_IO07	Input
ADC1_IN8	A/D converter 1 input channel 8	GPIO1_IO08	Input
ADC1_IN9	A/D converter 1 input channel 9	GPIO1_IO09	Input
ADC2_IN0	A/D converter 2 input channel 0	GPIO1_IO00	Input
ADC2_IN1	A/D converter 2 input channel 1	GPIO1_IO01	Input
ADC2_IN2	A/D converter 2 input channel 2	GPIO1_IO02	Input

Continued

Signal	Description	Chip corresponding pin	Direction
ADC2_IN3	A/D converter 2 input channel 3	GPIO1_IO03	Input
ADC2_IN4	A/D converter 2 input channel 4	GPIO1_IO04	Input
ADC2_IN5	A/D converter 2 input channel 5	GPIO1_IO05	Input
ADC2_IN6	A/D converter 2 input channel 6	GPIO1_IO06	Input
ADC2_IN7	A/D converter 2 input channel 7	GPIO1_IO07	Input
ADC2_IN8	A/D converter 2 input channel 8	GPIO1_IO08	Input
ADC2_IN9	A/D converter 2 input channel	GPIO1_IO09	Input

Note 1: The 10 channels of ADC1 share GPIO1_IO00 - GPIO1_IO09 with the 10 channels of ADC2.

The A6G2C series core board has re-allocated resources to GPIO1_IO00~GPIO1_IO09. The default configuration of the system firmware is as follows. If you need multiple ADCs, you can configure them after careful check.

Table 3.27 Default configuration of GPIO1_IO00 - GPIO1_09 pins of A6G2C series core boards

Chip corresponding pin	Default firmware function	Pin number	Description	Direction
GPIO1_IO00	USB_OTG1_ID	B23	USB_OTG1_ID signal	Input
GPIO1_IO01	TS_YN	B57	Touch screen YPLL signal	Input
GPIO1_IO02	TS_YP	B58	Touch screen YNLR signal	Input
GPIO1_IO03	TS_XN	B55	Touch screen XPUL signal	Input
GPIO1_IO04	TS_XP	B56	Touch screen XNUR signal	Input
GPIO1_IO05	USB_OTG2_ID	B24	USB_OTG2_ID signal	Input
GPIO1_IO06	ENET_MDIO	A1	Ethernet management data signals	Input/Output
GPIO1_IO07	ENET_MDC	A2	Ethernet management clock signal	Output
GPIO1_IO08	ADC1_IN8	B41	ADC1 channel 8	Input
GPIO1_IO09	ADC1_IN9	B39	ADC1 channel 9	Input

Note 1: The A6G2C series core boards do not support ADC2;

Note 2: The firmware of A6G2C series core board is configured with ADC1 channel 8 and channel 9 by default, and the other channels have been reused by other functions.

3.5.8 JTAG

The A6G2C series core board supports one JTAG debug interface, which can be used as debug function and GPIO function. When it is used as a GPIO function, adding a 0.1μF filter capacitor to the signal pins in Table 3.28 can effectively protect against EMC. When it is used as a debugging function, a filter capacitor cannot be added; otherwise, the kernel cannot be connected and thus debugging is disabled. Design the circuit according to your actual application.

Table 3.28 A6G2C series core board JTAG default configuration

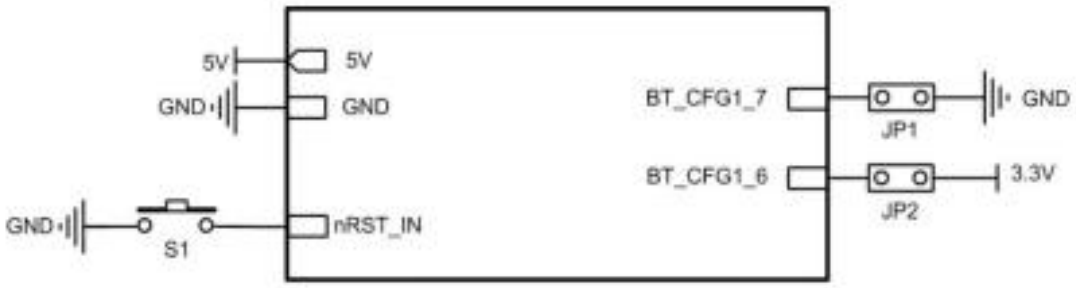
Pin number	Chip corresponding pin	Default firmware function	Reusable function	Remarks
B32	JTAG_TCK	TAP controller clock	GPIO	Firmware default JTAG functionality
B34	JTAG_nRST	TAP controller reset		
B36	JTAG_TMS	TAP controller mode selection		
B38	JTAG_TDI	TAP controller data input		
B40	JTAG_TDO	TAP controller data output		

4. System Hardware Design

The A6G2C core board contains a lot of interface resources, and reliable peripheral circuits must be designed for cooperation. This document provides the reference design method of some peripheral circuits. All circuits have experienced strict functional verification. When designing the circuit, you can refer to the *A6G2C Core Board Reference Design Schematic Diagram*.

4.1 A6G2C Core Board Interface

The A6G2C core board has integrated the power supply, reset monitoring circuit, and storage circuit into a compact module. The required external circuits are very simple. As shown in Figure 4.1, a minimal system only needs 5V power supply, reset button, and startup and configuration.

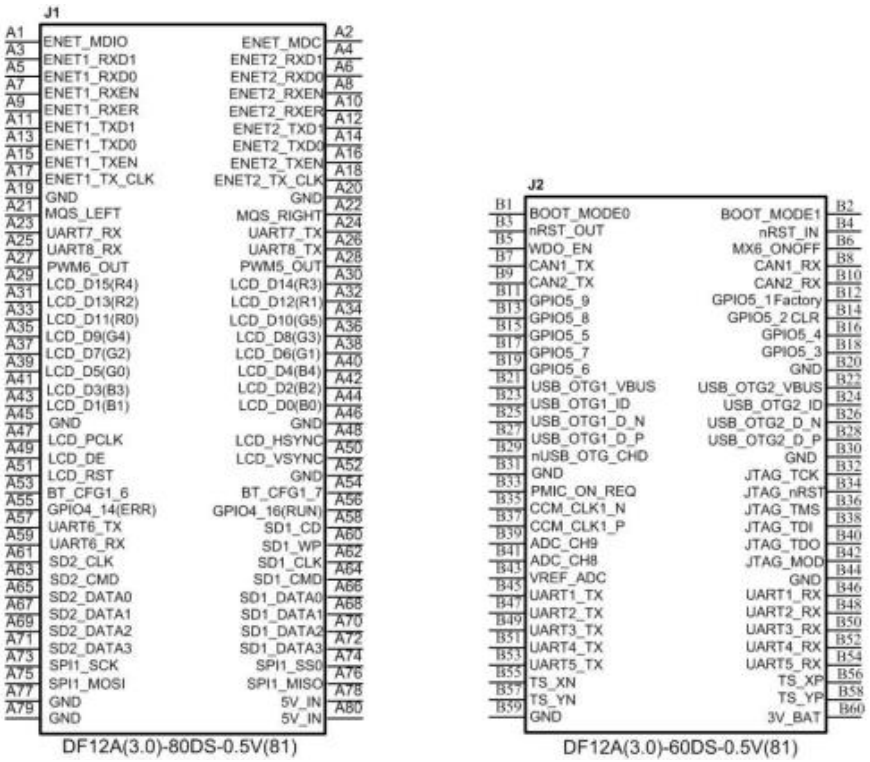


Minimum system block diagram of the M6G2C core board

Figure 4.1 Minimum system block diagram of the A6G2C core board

The A6G2C core board has a reliable independent reset circuit. You do not need to process the reset circuit. To use manual reset, just use a button connected to the ground on the nRST_IN pin. Note that the reset signal is a sensitive signal.Therefore, the cable routed from the nRST_IN pin to the button should be as short as possible, and the cable should be grounded to avoid interference and system stability.

Two pins, BT_CFG1_7 and BT_CFG1_6, are used as boot configuration pins. Two-pin suspension indicates that the core board boots from NAND Flash by default. If you need to configure SD Card to boot, just connect the jumpers JP1 and JP2, as shown in the preceding figure.



Board-to-board interface connector A port (80Pin)

Board-to-board interface connector B port (60Pin)

Figure 4.2 A6G2C core board interface

4.1.1 Startup Configuration Circuit

The A6G2C series core board reserves four pins, BOOT_MODE0, BOOT_MODE1, BT_CFG1_6, and BT_CFG1_7, as boot configuration pins. The A6G2C core board boots from NAND Flash by default.

Table 4.1 describes the boot mode configuration of the A6G2C series core board. Figure 4.3 shows the boot mode configuration reference circuit.

Table 4.1 A6G2C core board boot mode configuration

Startup method	Configuration
NAND	Disconnect JP1, JP2, JP3 (default)
USB	Short JP1, disconnect JP2, JP3
QSPI	Short JP2, disconnect JP1, JP3
SD	Short JP2, JP3, disconnect JP1

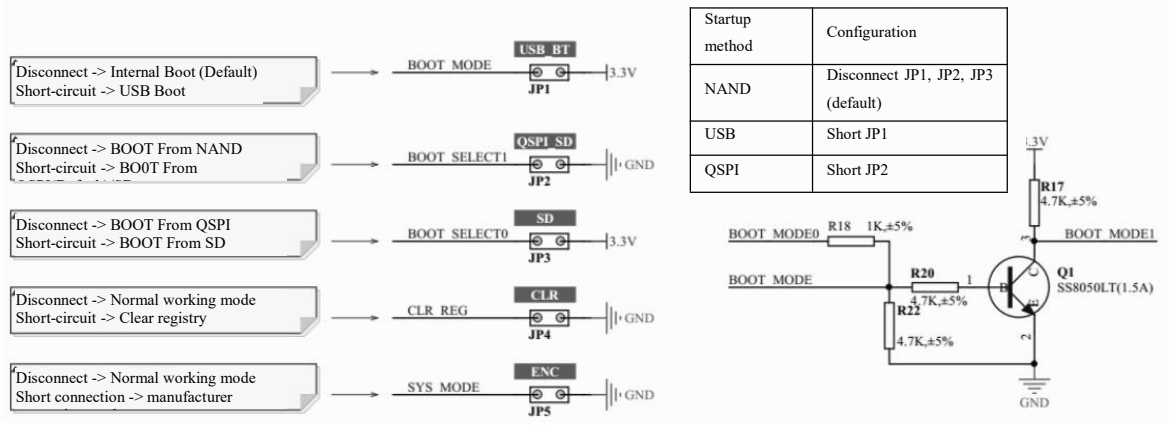


Figure 4.3 Startup configuration circuit

4.2 Power Design

The design of the power supply system is crucial in the design of embedded products. Engineers not only need to consider the basic electrical parameters of the power supply itself, but also the stability design of the power supply, such as electromagnetic compatibility, temperature range, safety design, three-proof design and other factors. Any negligent factor may cause system breakdown. Before designing a power supply system for a new product, engineers should thoroughly understand the actual needs of the entire system, and select an appropriate power supply method for the system based on a feasible design solution that has been fully demonstrated in terms of cost and efficiency.

The simple switching regulated power supply features simple use, high efficiency, large conversion pressure difference, strong current output capability and low heat generation, which make it widely used in the field of embedded systems. However, there are certain differences in the price and characteristics of various types of power chips. For example, LM2575 features wide power input range and high output power. The SP7656EN2-L and TPS5430DDA feature low price and ultra-small size.You can choose a suitable switching power supply chip based on the actual situation. The solution chosen for the evaluation board is MP1482. The chip has the advantages of large output current, low power dissipation and low price. This section uses this as an example.

The A6G2C core board needs to provide 5 V voltage. Figure 4.4 shows the reference circuit.

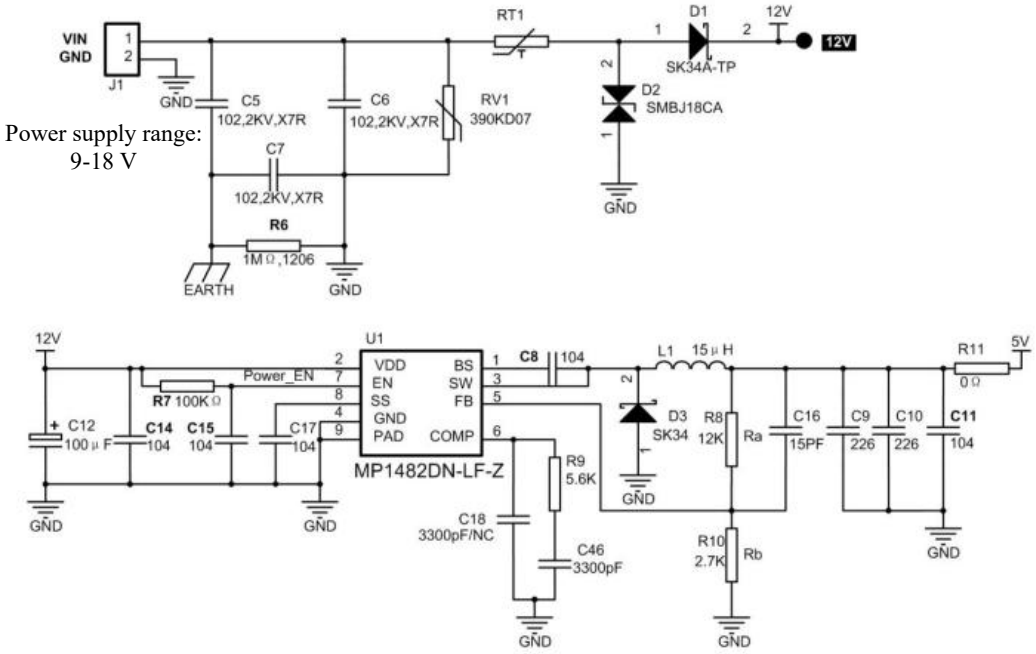


Figure 4.4 Core board 5V power supply circuit

The average current of the A6G2C core board during normal operation is about 110 mA. However, the peak current at the moment of startup may reach 130 mA, in order to leave a certain margin and ensure the stable and reliable operation of the system. In addition, the power consumption at the moment of power-on after long-time storage at a low temperature is large. Insufficient power will result in the system boot failure. Therefore, it is recommended to use a power supply of more than 1 A, instead of linear power chips such as LM1117.

The function of the rectifier bridge D1 is to prevent the power supply circuit from being reversely inserted, so as to prevent the product from being damaged. If you use a power input connector with a foolproof function, consider removing this design.

In the entire power supply system, ensure that you power on the 5 V power supply of the core board first, and then enable the 3.3 V power supply.

To ensure the accuracy of the output voltage, R8 and R10 are recommended to use an accuracy of more than 1%.

Ensure that you power on the 5 V power supply for the core board first, and then power on the other power supplies on the backplane.

4.3 Fast Ethernet Circuit

The A6G2C core board supports two 10M/100M Ethernet controllers. You need an external PHY circuit and a network port socket to achieve network communication. Figure 4.5 shows the overall block diagram.

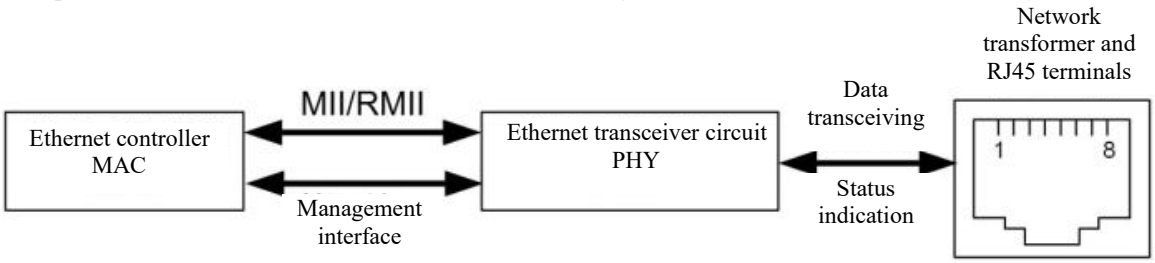


Figure 4.5 Ethernet communication

The i.MX6UL Ethernet controller supports RMII and MII interfaces at 10/100 Mbps. The signal cables of the RMII interface for sending and receiving data are reduced by half compared with the MII interface. The interface is simple. To save I/O resources, the A6G2C core board adopts RMII interface to connect with Ethernet PHY.

4.3.1 Single Ethernet Transceiver Circuit

The DP83848 used in the reference circuit shown in Figure 4.6 is a Fast Ethernet PHY. The chip uses a 3.3V power supply. You can choose the LDO scheme. There are some configuration resistors on the right side of the chip. The "NC" sign means no soldering. Follow the default configuration in the picture.

To ensure stable Ethernet communication, the PCB cables connecting the signals between the DP83848 and the A6G2C core board need to be equal in length.

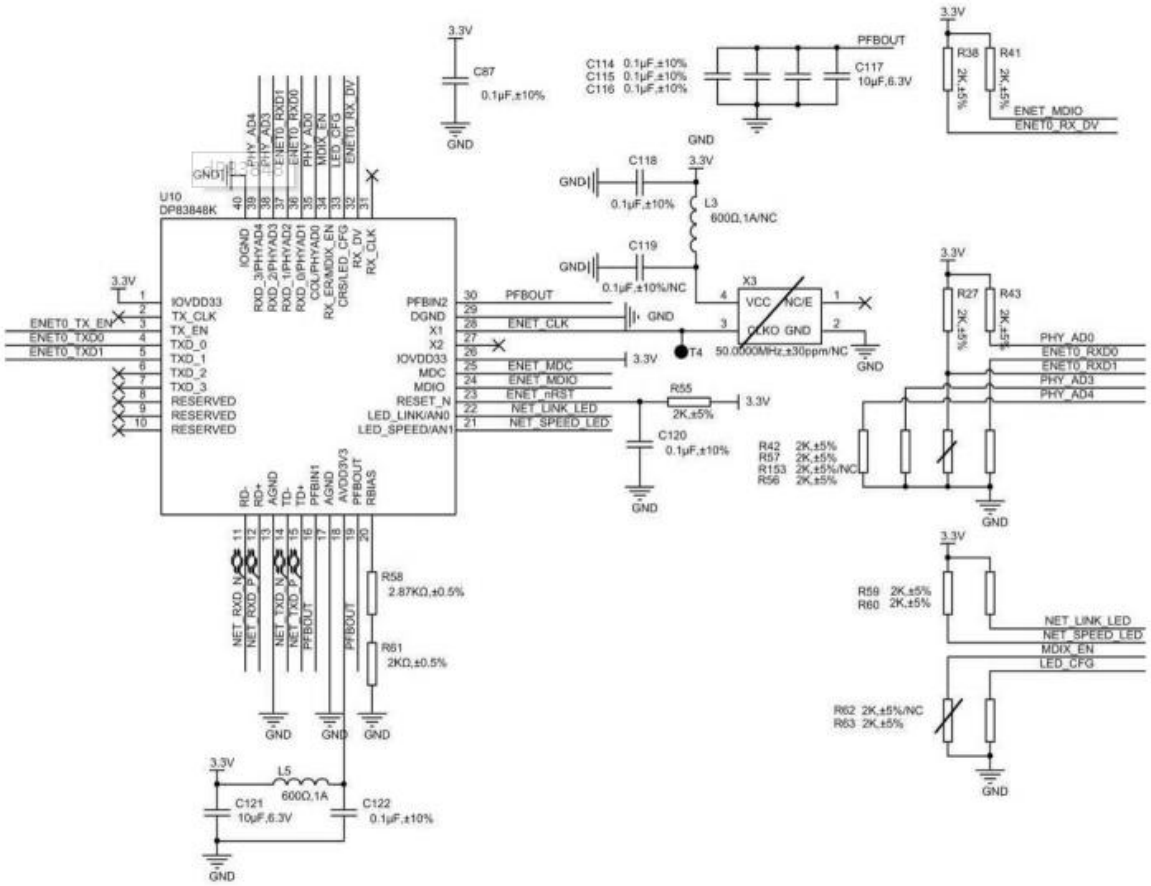


Figure 4.6 Single Ethernet reference circuit

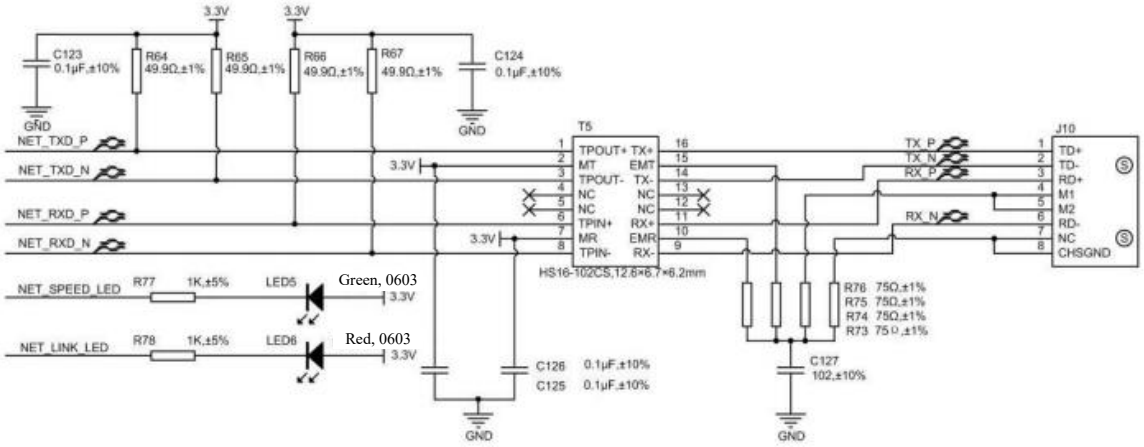


Figure 4.7 Single Ethernet port

Due to limited space, the reference circuit here is a single Ethernet. The model used by the network interface J10 is the RJ45 interface without indicators. If you use dual Ethernet ports, just copy one reference circuit. The network port interface can use the two-in-one HLJ5622S-8P8C-1×2, dual-port model. For details, see the *A6G2C Core Board Reference Circuit Diagram*.

4.4 USB Circuit Design

The A6G2C core board supports two USB OTG interfaces. Users only need to connect a simple OTG interface circuit to realize the OTG function.Figure 4.8 shows the reference circuit. The switching of USB OTG interface from Device to Host adopts manual switching of ID lines. Due to the circuit structure, this circuit performs Device processing when the ID line is suspended.When the jumper cap is inserted and the ID line is pulled down, it is used as Host, and J8 is the MicroUSB interface.

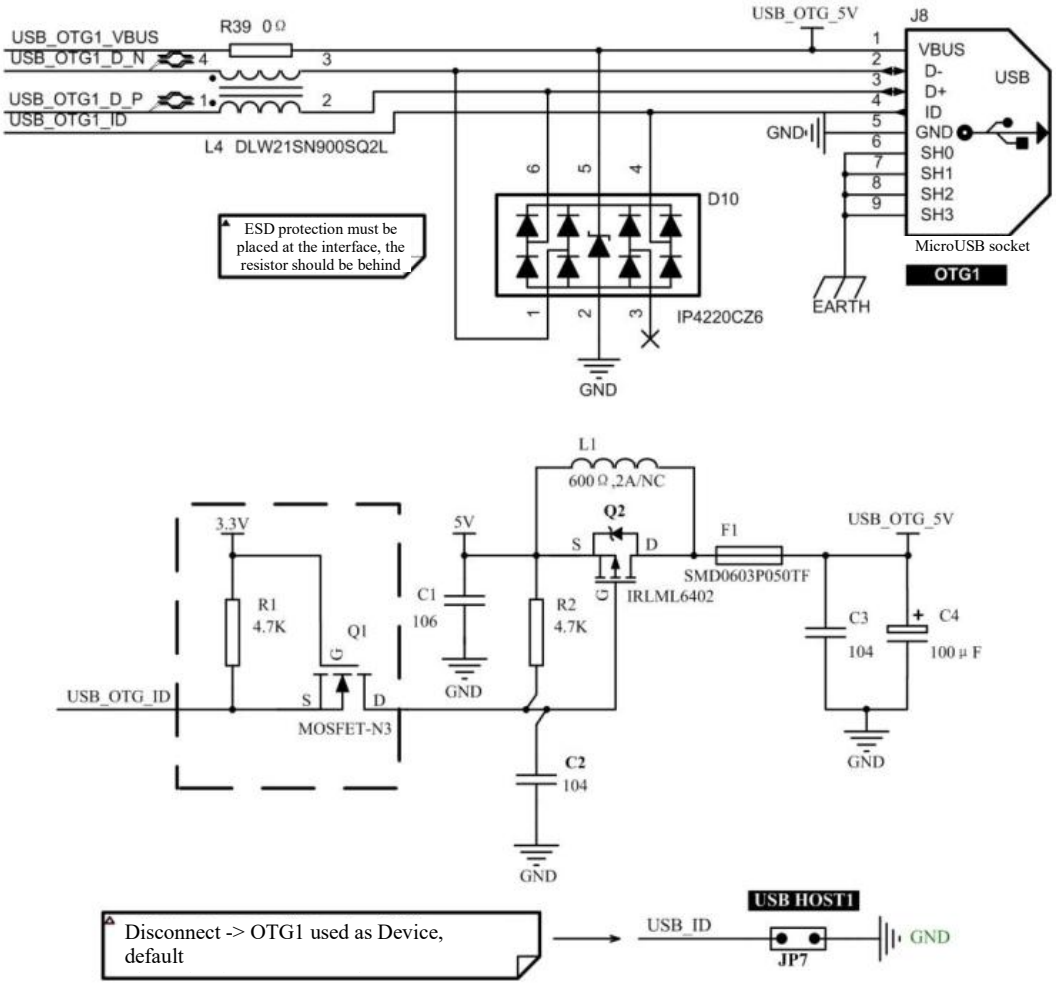


Figure 4.8 USB power switching circuit for discrete devices

The advantage of the circuit in Figure 4.8 is that it is composed of discrete MOS transistors and can pass a larger current. It can be used in the occasions where the USB port is connected to an external GPS, 3G or 4G module with high current startup. In addition, discrete devices are cheaper than integrated USB power management chips. The disadvantage is that you need to manually switch between Device and Host.

The USB detection of the i.MX6UL needs to identify two signals, ID and VBUS. The power of VBUS and Host are on the same circuit. In the case of detection USB device identification, VBUS needs to have a changing state. Therefore, it is not advisable to connect capacitors with large capacity in parallel on the VBUS to prevent the discharge of the capacitors from being completed and the failure of next identification.

The USB power management chip SP2526A-1EN-L can be used for switching when the USB port is used in the occasions where the current is not high and the price requirements are not strict. Figure 4.9 shows the reference circuit.

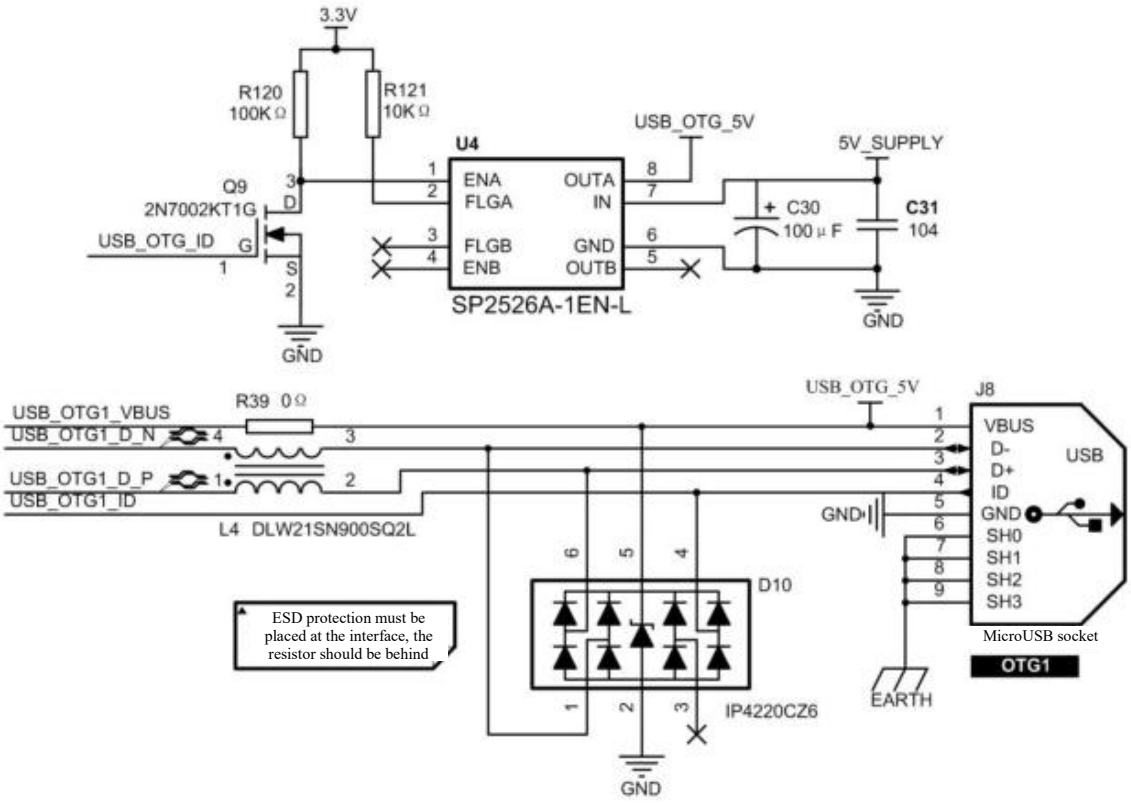


Figure 4.9 SP2526A USB_OTG circuit

4.5 SD/MMC Circuit

The SD/MMC card is a memory card with large capacity, high cost performance, small size and simple access interface. SD cards are widely used in digital cameras, MP3, mobile phones, and mass storage devices. As a storage carrier for these portable devices, it features low power consumption, non-volatile memory, and data saving without consuming energy. The SD card interface is backward compatible with the MMC card. The SPI protocol and some commands for accessing the SD card are also applicable to the MMC card. The SD/MMC card can be accessed in SD bus mode or in SPI bus mode.

The CPU of the A6G2C core board contains an SD/MMC card controller. Therefore, when designing the SD/MMC card interface circuit, you only need to connect these interfaces to the SD/MMC card socket accordingly. Figure 4.10 shows the reference circuit.

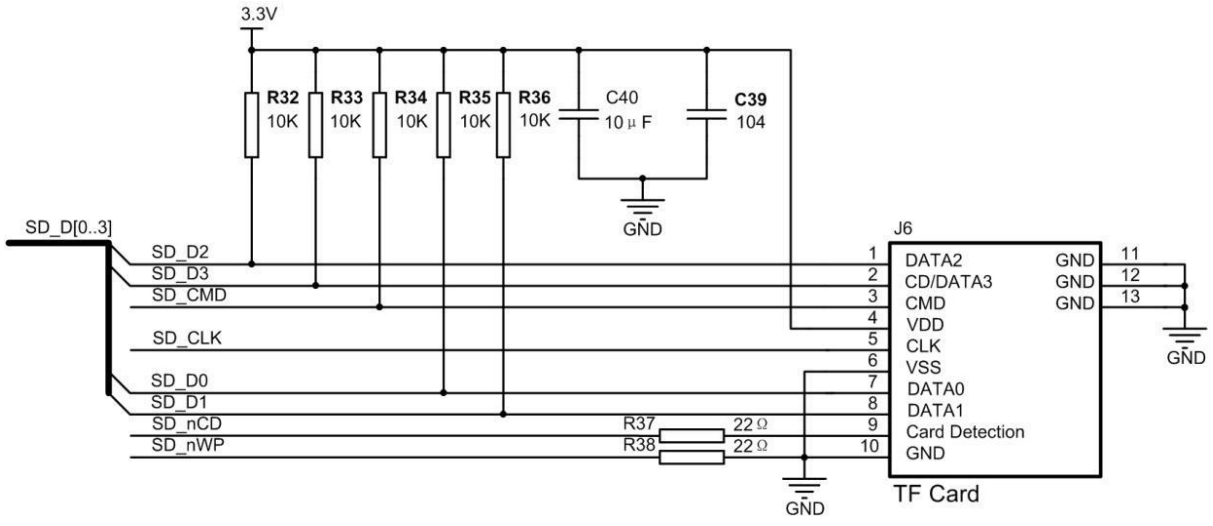


Figure 4.10 SD/MMC circuit

4.6 Buzzer Circuit

Figure 4.11 shows the buzzer reference circuit. The buzzer used in the figure is a passive buzzer. The buzzer is controlled by PWM_OUT5 by default.

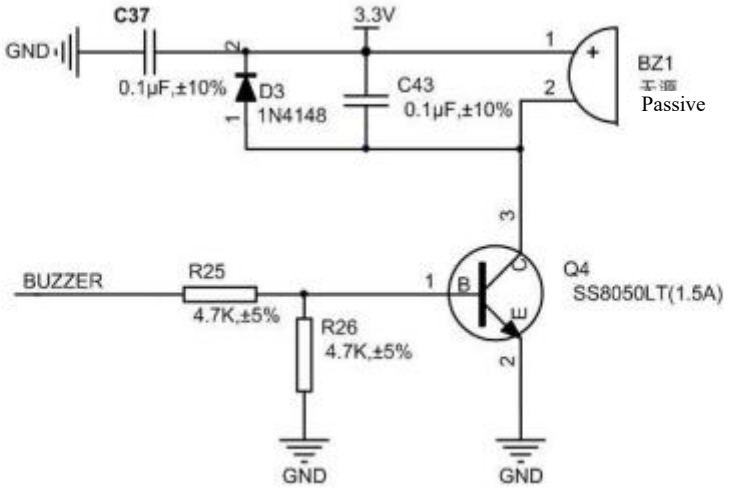


Figure 4.11 Buzzer circuit

4.7 RTC circuit

To ensure accuracy, you are advised to use an external RTC. Figure 4.12 shows the reference circuit. The RTC chip is PCF85063A. This chip communicates data addresses through I2C, which verifies the analog I2C bus function of the A6G2C core board.

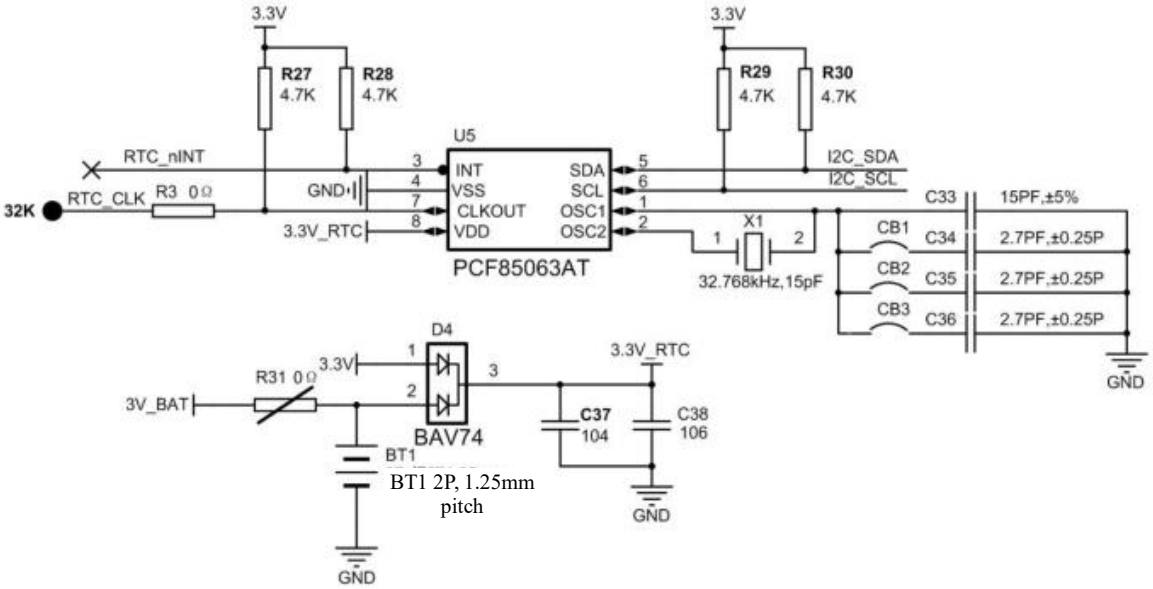


Figure 4.12 RTC circuit

4.8 LCD Circuit

The A6G2C core board has an LCD controller, which supports a variety of LCD displays such as color TFT displays. Figure 4.13 shows the reference circuit. J14 is a general-purpose 16-bit LCD interface 0.5mm FFC connector for industrial control boards of Guangzhou ZLG Electronics Co., Ltd. It contains four-wire resistive touch screen and other interfaces. This interface is compatible with LCD_TM070RDH12_24B 7-inch LCD kit; compatible with PC104_VGA conversion board for VGA display; compatible with PC104_LCD conversion board for LVDS signal LCD screen.

Note: The TFT-4.3A LCD kit supports 24-bit color display. If 16-bit TFT liquid crystal display is used, TFT_B2 - TFT_B0, TFT_G1 - TFT_G0, TFT_R2 - TFT_R0 are connected to GND.

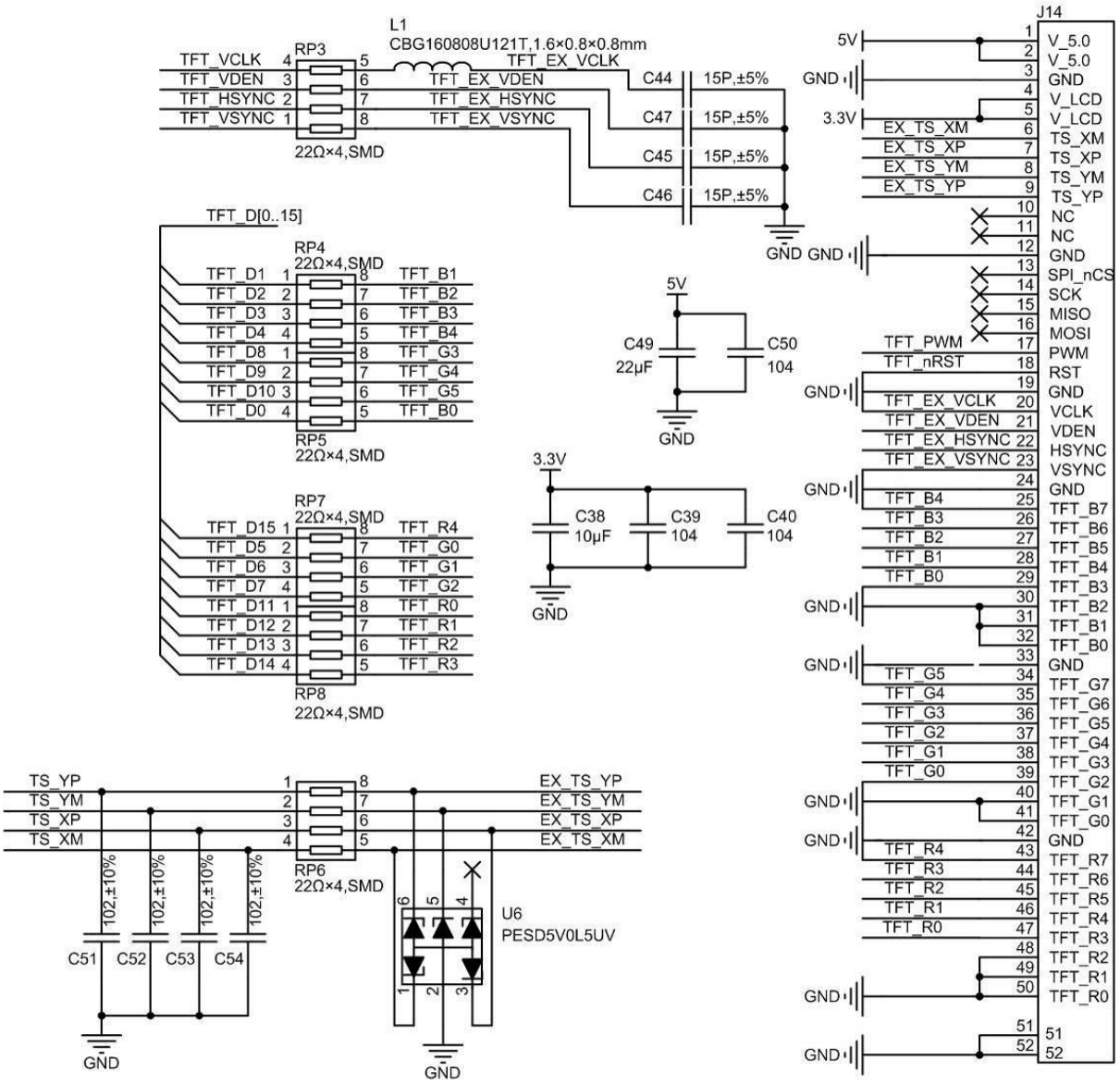


Figure 4.13 LCD circuit

4.9 RS232 Debugging Serial Port Circuit

The A6G2C core board provides eight UART interfaces, all of which have interrupt mode and DMA mode, among which UART1 is an important communication port for downloading and debugging programs. It is recommended to ensure that UART1_TXD and UART1_RXD are dedicated to UART1 function during design.

Figure 4.14 shows the RS-232 interface reference circuit. The SP3232 has an efficient charge pump. When the operating voltage is 3.3 V, the 0.1μF capacitor is enough for operation. The charge pump allows the SP3232 to send RS-232C compliant signals at a voltage within +3.3 V to +5.0 V. The ESD protection inside the SP3232 device allows the pins of the driver and receiver to withstand ±15kV human body discharge and IEC61000-4-2 air gap discharge. The SP3232 device includes a low-power shutdown mode. The device's driver outputs and charge pump are disabled in this mode. In shutdown, the supply current is less than 1 μA.

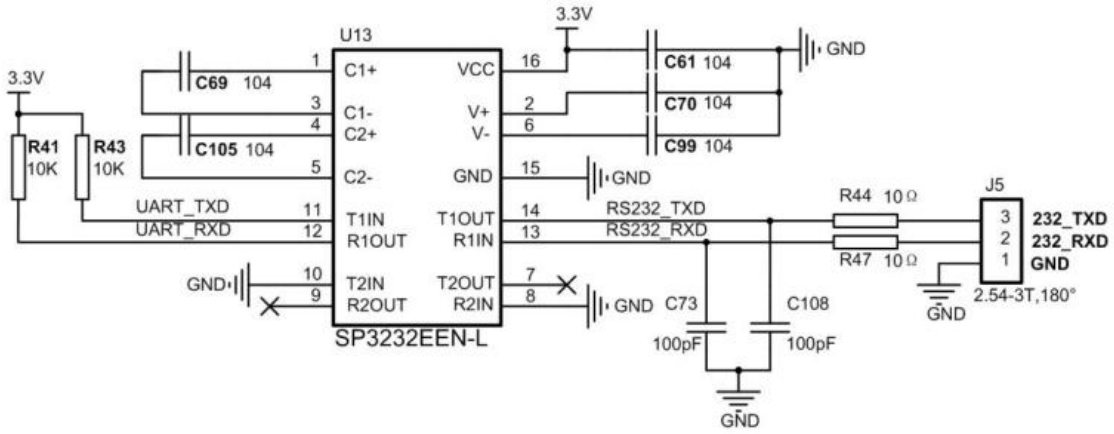


Figure 4.14 RS232 circuit

4.10 Reset Circuit

The watchdog reset function has been integrated on the A6G2C core board. If the feeding is not performed within 1.6 seconds, the hardware watchdog will forcibly reset the processor, which ensures that the system can recover by itself when the system crashes unexpectedly. As shown in Figure 4.15, when JP6 is suspended, the watchdog is enabled; when JP6 is shorted, the watchdog is invalid. The reset input pin of the core board is connected to the watchdog chip. When the button is pressed, the watchdog resets directly.

In addition, the A6G2C core board also leads a nRST_OUT pin for reset output. This signal and the reset signal of the processor are the same signal, which can be used to reset the external device, and can reset the external device and the processor at the same time. If not in use, it can be suspended.

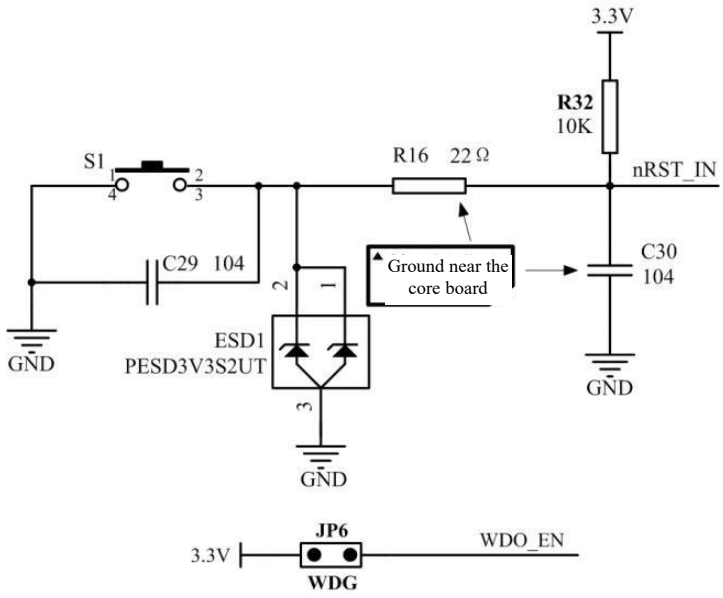


Figure 4.15 External reset circuit

4.11 Indicators

When designing the backplane of the A6G2C core board, it is recommended to add some indicators, such as power indicator and running indicator. See Figure 4.16. In addition, when GPIO is abundant, error indicators, user indicators, etc. can be added.

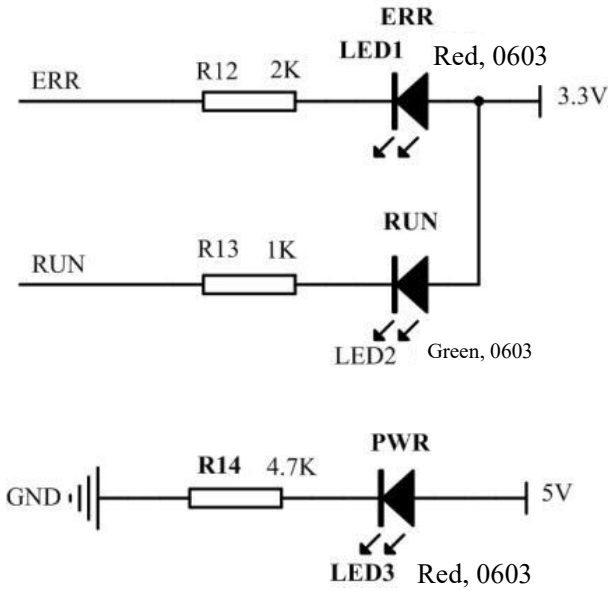


Figure 4.16 Indicator circuit

Due to the limited space, the preceding chapters only briefly introduce the peripheral design of the A6G2C core board. For detailed application, see the *A6G2C Industrial Control Core Board Reference Circuit Diagram*.

4.12 PCB Design Precautions

The integrated industrial communication and multimedia functions of the A6G2C series core boards involve many high-frequency and high-speed signals. While ensuring the functional design of the schematic diagram, a good PCB design will greatly improve the stability and reliability of peripheral functions.

For high-frequency and high-speed signals, the characteristic impedance is a key parameter on the PCB. The A6G2C series core board is recommended to use no less than four layers for the bottom PCB stack-up, which usually consists of two signal layers, top and bottom, one power layer, one ground layer, and other insulating materials. Traces and layers constitute impedance control, and the impedance value is determined by their physical structure and the electrical properties of the insulating material: the width and thickness of the signal traces, the height of the core or pre-fill material on both sides of the trace, the configuration of the trace and the board, the insulation constant of the core and pre-fill material, etc.

Table 4.2 describes the common signal cable impedance control of the A6G2C core board.

Table 4.2 Main signal impedance control description of the core board

Signal type	Differential trace or not	Impedance control size	Description
RMII fast Ethernet	No	Single ended 50 ohms	The PHY chip should be as close as possible to the RMII signal pins of the core board
NET cable	Yes	Differential 100 ohms	——
EMMC/SD/TF card	No	Single ended 50 ohms	Parallel signal traces of equal length and 10K resistors increased on the signal cables
USB HOST/OTG	Yes	Differential 90 ohm	——
CSI camera	No	Single ended 50 ohms	Parallel signal cables routed in equal length
Onboard antenna	No	Single ended 50 ohms	It needs to be calculated based on the actual RF signal frequency, usually 50 ohms
LCD	No	No	Equal length processing of parallel signal cables

5. Antenna Selection

The role of the antenna is to radiate radio frequency signals into free space. Choosing the appropriate antenna is crucial for the transmission distance. The communication quality or communication distance of the wireless module largely depends on whether the design and selection of the antenna are reasonable. Antennas are very sensitive to the surrounding environment. If the antenna is not properly selected, it will not only fail to play its due role, but it will waste a lot of time and cost; in many cases, the expected effect cannot be achieved even if a suitable antenna is selected. This section introduces commonly used antennas and important parameters that affect the performance of the antenna, and provides suggestions for antenna selection and precautions for antenna placement or installation.

5.1 Antenna Types

1. On-board PCB antenna

The on-board PCB antenna is made of PCB etching, which is low in cost, but has limited performance and good adjustability. They can be used in large quantities for Bluetooth and Wi-Fi wireless communication.

2. SMT patch antenna

The commonly used antennas include ceramic antennas, which have the advantages of small footprint, high integration, and easy replacement.They are suitable for products with high space requirements, but are slightly more expensive and have smaller bandwidths.

3. External rod antenna

The external rod antenna has good performance, can be installed directly without debugging, and is easy to replace. It has high gain and can be used in various terminal equipment.

4. FPC Antenna

The FPC antenna is connected by the feeder and features free installation and high gain. It can usually be pasted on the non-metallic casing of the machine using self-adhesive. It is suitable for products with high performance requirements and sufficient housing space.

Table 5.1 Common antennas and features

Category	Product picture	Features	Application
Onboard PCB antenna		Low cost, but limited performance and good adjustability	Integrated RF modules, such as WiFi, Bluetooth modules
SMT ceramic antenna		Small footprint, high integration and easy replacement	Suitable for high-volume embedded wireless modules
External rod antenna		Good performance, no need to debug, easy to replace, high gain	Customer terminal equipment
FPC antenna		Free installation and high gain	Customer terminal equipment

The preceding table is the commonly used antennas and their characteristics. Due to the diversity of wireless communication and the miniaturization of products, the A6G2C series hardware core board does not have an onboard PCB antenna designed on the board, nor does it reserve a station for an SMT ceramic antenna. Therefore, the optional antenna types are external rod antenna and FPC antenna.

5.2 Antenna Parameters

The primary parameter that affects the wireless communication distance is the transmit power. Generally, the transmit power of the wireless core board and the corresponding ideal transmission distance can be found in the manual. On the premise that the transmit power meets the requirements, other parameters of the antenna are considered. The main indicators of the antenna include: frequency range, standing wave ratio VSWR, antenna gain, polarization and impedance.

5.2.1 Frequency Range

The frequency range is generally selected according to the corresponding wireless communication method. For example, select 2.4 GHz antennas for WiFi and zigbee wireless core boards, 470 MHz antennas for LoRa core boards, and 13.56 MHz coil antennas for Mifare core boards.

5.2.2 Standing Wave Ratio VSWR

The VSWR indicates the reflected power of the RF signal. The larger the VSWR, the more signals are reflected, and the less power is transmitted. According to Table 5.2, when VSWR=1.5, the theoretical transmission power is 96%; when VSWR=2, the transmission power is only 88.9%.Therefore, you are advised to choose an antenna with the VSWR of less than 1.5, so that a relatively high transmission power can be obtained. The VSWR is a very critical parameter. After purchasing the antenna, you are advised to measure the VSWR with a network analyzer.

Table 5.2 Comparison table of standing wave ratio, return loss and transmission power

THE EFFECT OF VSWR ON TRANSMITTED POWER						
VSWR	**VSWR (dB)**	**Return Loss (dB)**	**Trans.Loss (dB)**	**Volt.Refl. Coeff**	**Power Trans. (%)**	**Power Refl. (%)**
1.0	.0	∞	.000	.00	100	.0
1.1	.8	26.4	.010	.05	99.8	.2
1.2	1.6	20.8	.036	.09	99.2	.8
1.3	2.3	17.7	.075	.13	98.3	1.7
1.4	2.9	15.6	.122	.17	97.2	2.8
1.5	3.5	14	.177	.2	96	4
1.6	4.1	12.7	.238	.23	94.7	5.3
1.7	4.6	11.7	.302	.26	93.3	6.7
1.8	5.1	10.9	.37	.29	91.8	8.2
1.9	5.6	10.2	.440	.31	90.4	9.6
2	6	9.5	.512	.33	88.9	11.1
2.5	8	7.4	.881	.43	81.6	18.4
3	9.5	6	1.249	.5	75	25

5.2.3 Impedance

The impedance of the antenna needs to match the output impedance of the wireless module. Typically, it is 50 ohms. The M105x series cross-border hardware core boards have been output matched at 50 ohms, and the transmission cables are also designed as 50 ohms. You just need to choose a 50 ohm antenna. Figure 5.1 shows the output transmission cable and output matching of the A6G2C series Wi-Fi wireless core board.

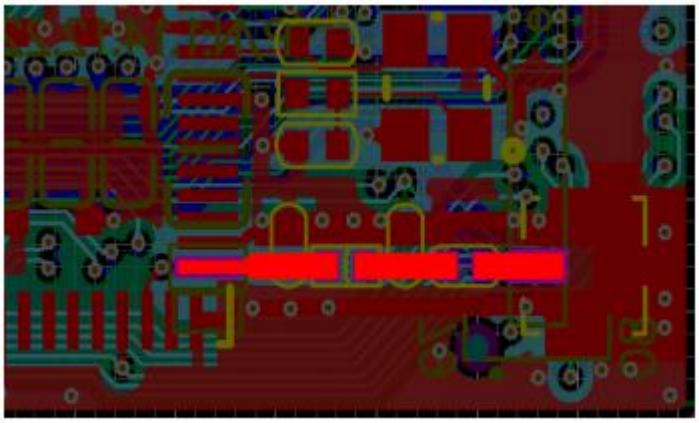


Figure 5.1 Wireless module output transmission cable and output matching

5.2.4 Directivity of the Antenna

All antennas have directivity, which means that the antenna has different radiation or reception capabilities for different directions in space. The directivity of an antenna is usually measured using a pattern. Figure 5.2 shows the pattern of an antenna in the frequency range from 2.4 GHz to 2.5 GHz.

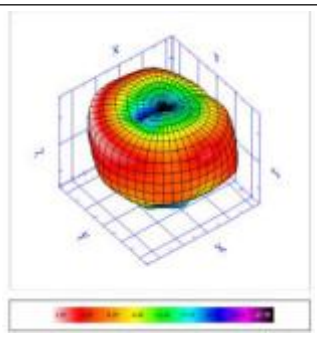
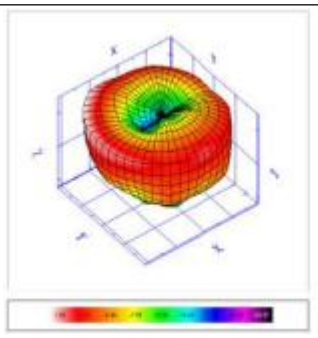
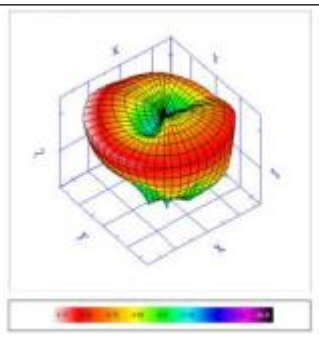
2400 MHz	2450 MHz	2500 MHz
		

Figure 5.2 Three-dimensional pattern of an antenna

The antenna patterns given in some antenna manuals are represented by two-dimensional diagrams, which are divided into H-Plane and E-Plane, that is, the magnetic field plane and the electric field plane, as shown in Figure 5.3.

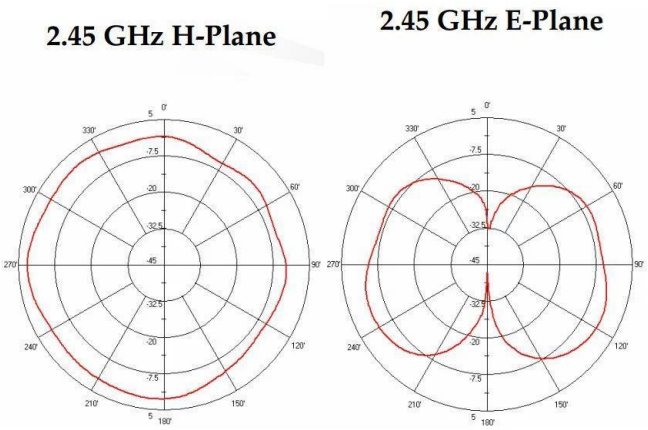


Figure 5.3 Two-dimensional pattern of an antenna

5.3 Antenna Installation and Precautions

When installing the antenna, you must consider the directivity of the antenna. When the antenna is placed vertically, the direction with the deepest red color is the direction with the strongest radiation or reception ability of the antenna, as shown in Figure 5.2. Therefore, when installing the antenna, install the antenna in the direction of the red point if possible, so as to ensure good enough signal quality. When the communication space is not blocked and the direction of the antenna corresponds to the strongest radiation direction, the communication distance can be maximized. Improper installation of the antenna will shorten the communication distance or even the communication will fail.

Metal materials can also have an effect on the antenna, because metals reflect electromagnetic waves. If there is an object of metal material near the antenna, it will not only affect the actual use space of the antenna, increase the loss resistance of the antenna, reduce the radiation efficiency, but also lead to the deterioration of the radiation performance of the antenna. When installing the antenna, pay attention to:

(1) The antenna should be at least 5 mm away from the battery;

(2) The antenna should be at least 4 mm away from the shielding case;

(3) When the case needs to be installed, do not use paint or plating with metal components on the surface of the case.

5.4 Mifare Coil Antenna

Mifare coil antennas are slightly different from the Wi-Fi, zigbee, and LoRa antennas mentioned above. Antennas such as Wi-Fi realize wireless communication by radiating and receiving electromagnetic waves into space, while Mifare coil antennas realize data transmission through electromagnetic induction by generating a magnetic field around the coil.

The Mifare coil antenna also needs to consider impedance matching and the influence of surrounding metals. ZLG Electronics recommends to use its self-developed RFID-ANT-L54 coil antenna directly, as shown in Figure 5.4. This coil antenna can be directly adapted to the Mifare wireless core board of the M105x series.

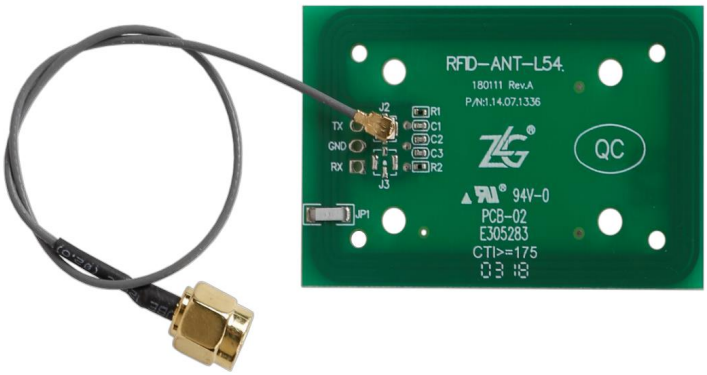


Figure 5.4 RFID-ANT-L54 coil antenna

6. Mechanical Dimensions

Figure 6.1 and Figure 6.2 show the actual A6G2C core board.

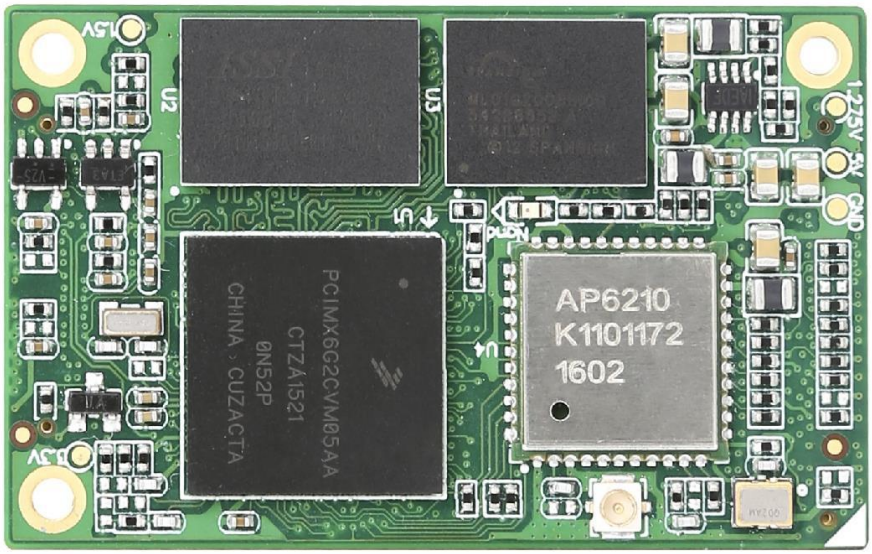


Figure 6.1 Top view of A6G2C core board

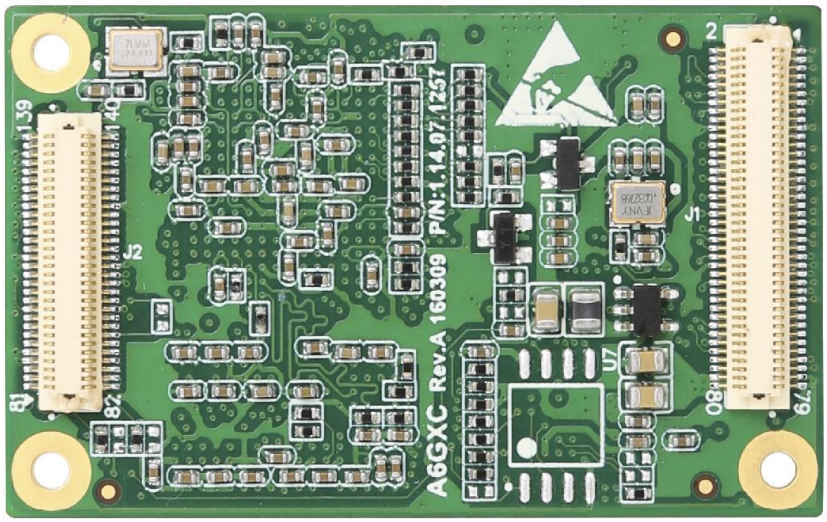
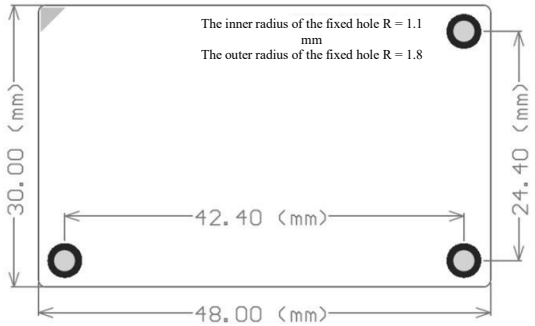


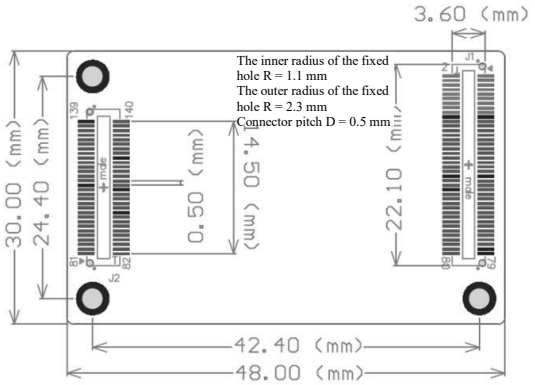
Figure 6.2 Bottom view of A6G2C core board

The pictures are for reference only, and the actual pictures shall prevail.

Figure 6.3 shows the dimensions of the A6G2C core board. Unit (mm)

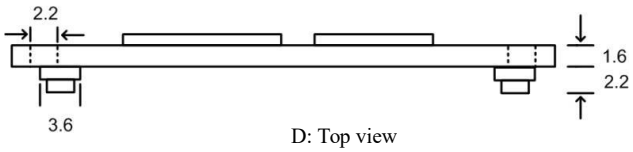


A: Front dimension drawing



B: Back dimension drawing

C: Side view



D: Top view

Figure 6.3 A6G2C core board dimensions

Note: In Figure 6.3, the tolerance of hole diameter dimensions is +/-0.1 mm, and the tolerance of the external dimensions of the board is +/-0.15 mm.

Pay attention when choosing the fixing column of the four positioning holes of the core board. You must choose a fixed column with a height that is exactly the height between the base plate and the core plate. If the fixed column is too high, it will lead to poor contact of the core board; if the fixing column is too low, the core board will be deformed after the screws are tightened, which will cause poor contact and affect the use. It is recommended to use copper pillars of Φ 2 x 3 + 3.5 mm

Due to the large number of BGA components on the core board, it is recommended not to remove and insert the board frequently. When you need to remove and insert the board, you must be careful to avoid PCB deformation; otherwise, the component may be falsely welded.

7. Disclaimer

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