Bluetooth® Low Energy Module

Introduce

The module base on Renesas RA4W1 MCU which in included a BLE v5.0 RF modem and other rich peripheral. It support BLE stack and Software and relative IO for user development .

Features

- Arm Cortex-M4 Core with Floating Point Unit (FPU)
  - Armv7E-M architecture with DSP instruction set
  - Maximum operating frequency: 48 MHz
  - Support for 4-GB address space
  - Arm Memory Protection Unit (Arm MPU) with 8 regions
  - Debug and Trace: ITM, DWT, FPB, TPIU, and ETB
- Memory
  - 512-KB code flash memory
  - 8-KB data flash memory (100,000 erase/write cycles)
  - 96-KB SRAM
  - Flash Cache (FCACHE)
  - Memory Protection Units
  - Memory Mirror Function (MMF)
  - 128-bit unique ID
- Connectivity
  - Bluetooth Low Energy
    - - Bluetooth 5.0 core specification compliant BLE transceiver and link layer
    - - Supporting LE 1M and Coded PHY, and LE Advertising extension
    - - Dedicated AES-CCM (128-bit blocks) encryption circuit
  - USB 2.0 Full-Speed (USBFS) module
    - - On-chip transceiver
    - - Compliant with USB Battery Charging Specification 1.2
  - Serial Communications Interface (SCI) × 4
    - UART
    - Simple IIC
    - Simple SPI
  - Serial Peripheral Interface (SPI) × 2
  - I2C bus interface (IIC) × 2
  - Controller Area Network (CAN) module
- Analog
  - 14-bit A/D Converter (ADC14)
  - 12-bit D/A Converter (DAC12)
  - 8-bit D/A Converter (DAC8) ×2 (for ACMPLP)
  - Low Power Analog Comparator (ACMPLP) × 2
  - Operational Amplifier (OPAMP) × 1
  - Temperature Sensor (TSN)
- Timers
  - General PWM Timer 32-bit (GPT32) × 4

General PWM Timer 16-bit (GPT16) × 3

Asynchronous General-Purpose Timer (AGT) × 2

Watchdog Timer (WDT)

- Safety

  Error Correction Code (ECC) in SRAM

  SRAM parity error check

  Flash area protection

  ADC self-diagnosis function

  Clock Frequency Accuracy Measurement Circuit (CAC)

  Cyclic Redundancy Check (CRC) calculator

  Data Operation Circuit (DOC)

  Port Output Enable for GPT (POEG)

  Independent Watchdog Timer (IWDT)

  GPIO readback level detection

  Register write protection

  Main oscillator stop detection

  Illegal memory access

- System and Power Management

  Low power modes

  Realtime Clock (RTC) with calendar and Battery Backup support

  Event Link Controller (ELC)

  DMA Controller (DMAC) × 4

  Data Transfer Controller (DTC)

  Key Interrupt Function (KINT)

  Power-on reset

  Low Voltage Detection (LVD) with voltage settings

- Security and Encryption

  AES128/256

  GHASH

  True Random Number Generator (TRNG)

- Human Machine Interface (HMI)

  Segment LCD Controller (SLCDC)
  - Up to 9 segments × 4 commons
  - Capacitive Touch Sensing Unit (CTSU)

- Multiple Clock Sources

  Main clock oscillator (MOSC)
  - (1 to 20 MHz when VCC = 2.4 to 3.6 V)
  - (1 to 8 MHz when VCC = 1.8 to 2.4 V)

  Sub-clock oscillator (SOSC) (32.768 kHz)

  High-speed on-chip oscillator (HOCO)
  - (24, 32, 48, 64 MHz when VCC = 2.4 to 3.6 V)
  - (24, 32, 48 MHz when VCC = 1.8 to 3.6 V)

  Middle-speed on-chip oscillator (MOCO) (8 MHz)

  Low-speed on-chip oscillator (LOCO) (32.768 kHz)

  IWDT-dedicated on-chip oscillator (15 kHz)

  Clock trim function for HOCO/MOCO/LOCO

  Clock out support

- General Purpose I/O Ports

  Up to 35 input/output pins
  - Up to 3 CMOS input
  - Up to 32 CMOS input/output
  - Up to 4 input/output 5 V tolerant

- Up to 1 high current (20 mA)

- Operating Voltage

  VCC: 1.8 to 3.6 V

- Module

  Certified to FCC, ISED, CE, KCC, NCC and SRRC

  On-Board Bluetooth Low Energy (BLE) Stack

  ASCII Command Interface API Over UART

  Scripting Engine for Hostless Operation

  Compact Form Factor – 20 * 16 mm

  Ta = –40°C to +85°C

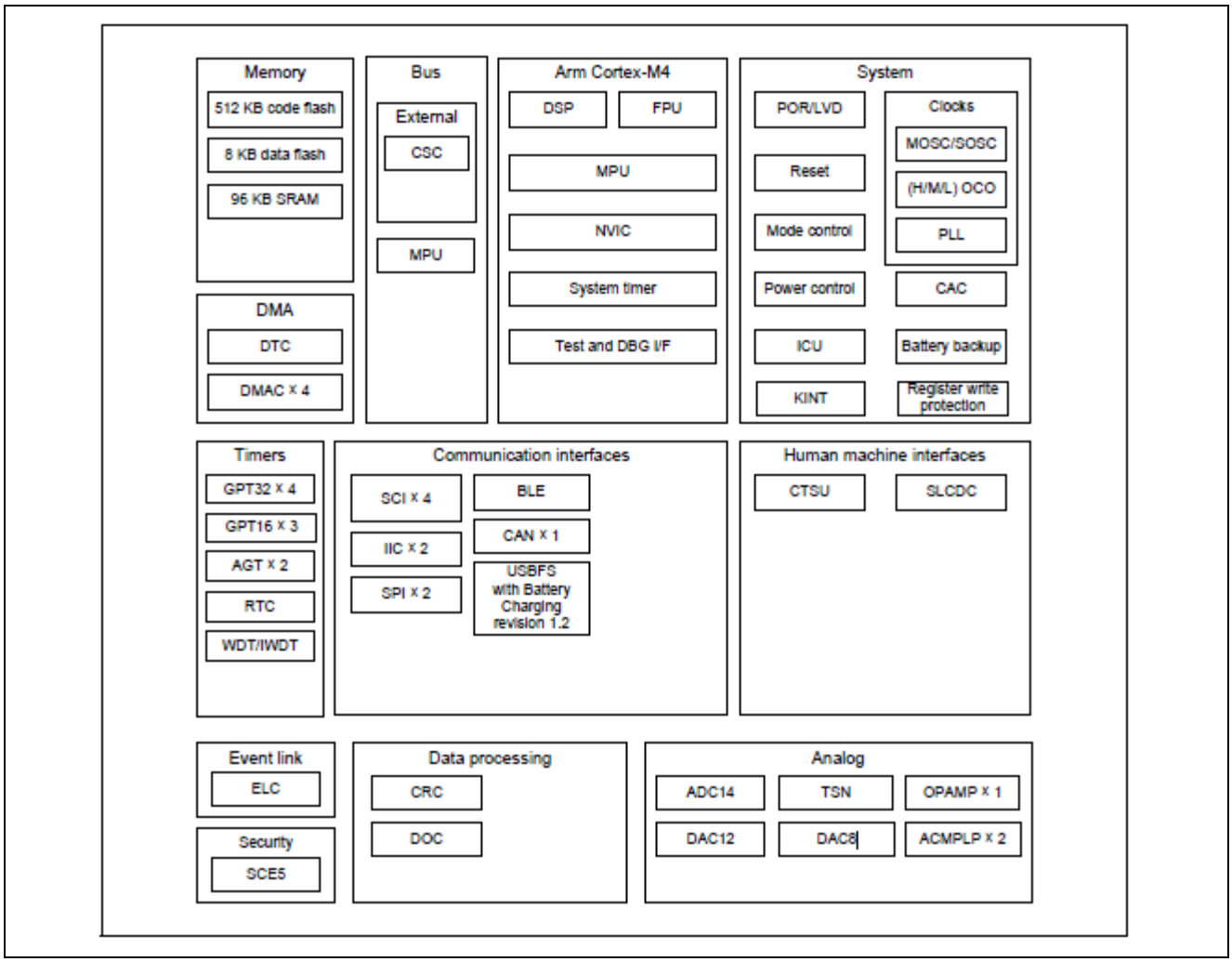
Contents

1. Module Overview

1.1 Overview

The module integrated ARM Cortex M4 and Bluetooth5.0 baseband controller , on -board Bluetooth stack, Digital and Analog I/Os in to one solution .

Block diagram of MCU



1.2 Bluetooth Low Energy (BLE)

This MCU has a Bluetooth Low Energy (BLE), which consists of an RF transceiver compliant with Bluetooth 5.0 Low
Energy (single mode), a link layer, and an RF transceiver power-supply.
The BLE is controlled by a Bluetooth middleware available from Renesas Electronics Corporation.

Specifications of the BLE

Item	Description		
Features	• RF transceiver compliant with the Bluetooth 5.0 Low Energy specification and a link layer • An on-chip matching circuit allows reducing the number of external parts • On-chip BLE-dedicated high-precision low-speed oscillator (32.768 kHz) • Transmission power is selectable as 0 dBm or +4 dBm. • The minimum receiving sensitivity is selectable from among –105 dBm (125 kbps), –100 dBm (500 kbps), –95 dBm (1 Mbps), or –92 dBm (2 Mbps).		
Bluetooth 5.0 functions	Classification	Function	Remark
	Device Address	Public or random address	The address can be set as a desired address.
	Advertising	Extended or periodic	
		Multiple advertising	Maximum number of sets: 4
		Advertising or Scan Response Data	Maximum data length=1650 bytes
	Scanning	Passive, active, or periodic	Number of units for concurrent synchronization with periodic advertising=2
		Whitelist or periodic advertiser list	Number of units registered in the whitelist: 4 Number of units registered in the periodic advertiser list: 4
	Master or slave	Data transmission or reception	Maximum payload length=251 bytes MoreData function is supported. Master/slave multi-role function is supported.
	Other	Bit rates	125 kbps, 500 kbps, 1 Mbps, 2 Mbps Bit-rate combinations for transmission and reception can be set as desired.
		Frequency hopping	Channel Selection Algorithm #2
		Encryption circuit for Bluetooth	On-chip Bluetooth-dedicated AES-CCM (128 bits) circuit
Other functions	RF transceiver power-supply (DC-to-DC converter, and linear regulator)		

Application board top view

2. Specification

Pins Description

Pin	Description	Remark
1	P501/USB_OVRCURA/ AN017	General purpose Input/Output pins
2	P015/TS28/ AN010	General purpose Input/Output pins Capacitive Touch detection pin
3	AVCC0	Analog block power supply pin
4	AVSS0	Analog block power supply ground pin
5	P011/TS31/ AN006/ AMP2+	General purpose Input/Output pins Capacitive Touch detection pin
6	P010/TS30/ AN005/ AMP2-	General purpose Input/Output pins Capacitive Touch detection pin
7	P014/ AN009/ DA0	General purpose Input/Output pins
8	P004/ AN004/ AMP2O	General purpose Input/Output pins
9	P402/TS18/RXD1/ MISO1/SCL1/ CRX0	General purpose Input/Output pins Capacitive Touch detection pin
10	X	N/C
11	X	N/C
12	P404	General purpose Input/Output pins
13	MCU-VCC	Power supply pin
14	P213/TXD1/MOSI1/SDA1	General purpose Input/Output pins
15	P212/RXD1/MISO1 /SCL1	General purpose Input/Output pins
16	GND	Ground pin
17	P414/SSLA1	General purpose Input/Output pins
18	P409/ USB_EXICEN	General purpose Input/Output pins
19	P407/TS03/CTS4_RTS4 /SS4/SDA0/USB_VBUS/ADTRG0	General purpose Input/Output pins Capacitive Touch detection pin
20	P915/USB_DM	General purpose Input/Output pins
21	P914/USB_DP	General purpose Input/Output pins
22	P206/TS01/RXD4/MISO4/SCL4 /SDA1/SSLB1/USB_VBUSEN	General purpose Input/Output pins Capacitive Touch detection pin
23	P205/TSCAP/TXD4/MOSI4 /SDA4/CTS9_RTS9/SS9 /SCL1/SSLB0/USB_OVRCURA	General purpose Input/Output pins Secondary power supply pin for the touch driver
24	P204/TS00/SCK4/SCK9/SCL0 /RSPCKBUSB_OVRCURB	General purpose Input/Output pins Capacitive Touch detection pin
25	RES	Reset pin
26	P201/MD	General purpose Input/Output pins Chip Operation mode

27	GND	Ground pin
28	P200	General purpose input pin
29	P300/SWCLK/SSLB1	General purpose Input/Output pins Serial wire clock pin
30	P108/CTS9_RTS9 /SS9/SSLB0	General purpose Input/Output pins Serial wire debug data input/output pin
31	P107	General purpose Input/Output pins
32	P106/SSLA3	General purpose Input/Output pins
33	P103/CTS0_RTS0/SS0/ CTX0/ AN019	General purpose Input/Output pins
34	X	N/C
35	P109/TS10/SCK1/TXD9/MOSI9 /SDA9/MOSIB/CTX0	General purpose Input/Output pins Capacitive Touch detection pin
36	P110/RXD9/MISO9 /SCL9 /MISOB/ CRX0	General purpose Input/Output pins Capacitive Touch detection pin
37	P111/TS12/SCK9/RSPCKB	General purpose Input/Output pins Capacitive Touch detection pin
38	P105/TS34/SSLA2	General purpose Input/Output pins Capacitive Touch detection pin
39	P104/TS13/SSLA1	General purpose Input/Output pins Capacitive Touch detection pin
40	P102/SCK0/RSPCKA/ CRX0/ AN020/ADTRG0	General purpose Input/Output pins
41	P101/TXD0/MOSI0/SDA0 /CTS1_RTS1/SS1/SDA1 /MOSIA	General purpose Input/Output pins
42	P100/RXD0/MISO0/SCL0 /SCK1/SCL1/MISOA	General purpose Input/Output pins

Note:

MCU support SCI 4 channels, SPI 2channles and IIC 2 channles, CAN 1 channel, USB FS 1channel, communication interface. 14bit ADC 8channels, 12bit DAC 1 channel.

- **Serial Communication Interface:**

The Serial Communications Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces:

Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA))

8-bit clock synchronous interface

Simple IIC (master-only)

Simple SPI

Smart card interface.

Channel	Pin name	Input/Output	Function
SCI0	SCK0	Input/Output	SCI0 clock input/output
	RXD0/SCL0/ MISO0	Input/Output	SCI0 receive data input SCI0 I2C clock input/output SCI0 slave transmit data input/output
	TXD0/SDA0/ MOSI0	Input/Output	SCI0 transmit data output SCI0 I2C data input/output SCI0 master transmit data input/output
	SS0/CTS0_RTS0	Input/Output	SCI0 chip select input, active-low SCI0 transfer start control input/output, active-low

Channel	Pin name	Input/Output	Function
SCI1	SCK1	Input/Output	SCI1 clock input/output
	RXD1/SCL1/ MISO1	Input/Output	SCI1 receive data input SCI1 I2C clock input/output SCI1 slave transmit data input/output
	TXD1/SDA1/ MOSI1	Input/Output	SCI1 transmit data output SCI1 I2C data input/output SCI1 master transmit data input/output
	SS1/CTS1_RTS1	Input/Output	SCI1 chip select input, active-low SCI1 transfer start control input/output, active-low
SCI4	SCK4	Input/Output	SCI4 clock input/output
	RXD4/SCL4/ MISO4	Input/Output	SCI4 receive data input SCI4 I2C clock input/output SCI4 slave transmit data input/output
	TXD4/SDA4/ MOSI4	Input/Output	SCI4 transmit data output SCI4 I2C data input/output SCI4 master transmit data input/output
	SS4/CTS4_RTS4	Input/Output	SCI4 chip select input, active-low SCI4 transfer start control input/output, active-low
SCI9	SCK9	Input/Output	SCI9 clock input/output
	RXD9/SCL9/ MISO9	Input/Output	SCI9 receive data input SCI9 I2C clock input/output SCI9 slave transmit data input/output
	TXD9/SDA9/ MOSI9	Input/Output	SCI9 transmit data output SCI9 I2C data input/output SCI9 master transmit data input/output
	SS9/CTS9_RTS9	Input/Output	SCI9 chip select input, active-low SCI9 transfer start control input/output, active-low

- **Serial Peripheral Interface (SPI)**

The MCU provides two independent channels of the Serial Peripheral Interface (SPI). The SPI channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices.

Channel	Pin name	I/O	Function
SPI0	RSPCKA	I/O	Clock I/O
	MOSIA	I/O	Master transmit data I/O
	MISOA	I/O	Slave transmit data I/O
	SSLA0	I/O	Slave selection I/O
	SSLA1	Output	Slave selection output
	SSLA2	Output	Slave selection output
	SSLA3	Output	Slave selection output
SPI1	RSPCKB	I/O	Clock I/O
	MOSIB	I/O	Master transmit data I/O
	MISOB	I/O	Slave transmit data I/O
	SSLB0	I/O	Slave selection I/O
	SSLB1	Output	Slave selection output
	SSLB3	Output	Slave selection output

- **I2C Bus Interface (IIC)**

The MCU has a 2-channel I2C Bus Interface (IIC). The IIC module conforms with and provides a subset of the NXP I2C (Inter-Integrated Circuit) bus interface functions.

Channel	Pin name	I/O	Function
IIC0	SCL0	I/O	IIC0 serial clock I/O pin
	SDA0	I/O	IIC0 serial data I/O pin
IIC1	SCL1	I/O	IIC1 serial clock I/O pin
	SDA1	I/O	IIC1 serial data I/O pin

- **Controller Area Network (CAN) Module**

The CAN module uses a message-based protocol to receive and transmit data between multiple slaves and masters in electromagnetically noisy applications. The module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. The CAN module requires an additional external CAN transceiver.

Pin name	I/O	Function
CRX0	Input	Data receive pin
CTX0	Output	Data transmit pin

- **USB 2.0 Full-Speed Module (USBFS)**

The MCU provides a USB 2.0 Full-Speed module (USBFS) that operates as a host or device controller compliant with the Universal Serial Bus (USB) specification revision 2.0. The host controller supports USB 2.0 full-speed and low speed transfers, and the device controller supports USB 2.0 full-speed transfers. The USBFS has an internal USB transceiver and supports all of the transfer types defined in the USB 2.0 specification.

Port	Pin name	I/O	Function
USBFS	USB_DP	I/O	D+ I/O pin for the on-chip USB transceiver. Must be connected to the D+ pin of the USB bus.
	USB_DM	I/O	D– I/O pin for the on-chip USB transceiver. Must be connected to the D- pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. Must be connected to VBUS signal on the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USBFS is a device controller.*1
	USB_VBUSEN	Output	VBUS (5 V) enable signal for the external power supply IC
	USB_OVRCURA USB_OVRCURB	Input	Overcurrent pins for USBFS. Must be connected to external overcurrent detection signals.
Common	VCC_USB	Input	Power supply for USB transceiver.
	VCC_USB_LDO	Input	Power supply pin for USB transceiver. Apply the same voltage as VCC_USB
	VSS_USB	Input	USB ground pin

- **14-Bit A/D Converter (ADC14)**

The MCU provides a 14-bit successive approximation A/D converter (ADC14) unit. Up to 8 analog input channels are selectable. Temperature sensor output and internal reference voltage can be selected for conversion. The A/D conversion accuracy is 14-bit conversion, making it possible to optimize the trade-off between speed and resolution in generating a digital value.

Unit	Pin name	I/O	Function
Unit 0	AVCC0	Input	Analog block power supply pin
	AVSS0	Input	Analog block power supply ground pin
	VREFH0	Input	Reference power supply pin
	VREFL0	Input	Reference power supply ground pin
	AN004 to AN006, AN009, AN010, AN017, AN019, and AN020	Input	Analog input pins 4 to 6, 9, 10, 17, 19, and 20
	ADTRG0	Input	External trigger input pin for starting A/D conversion

- **12-Bit D/A Converter (DAC12)**

The MCU provides a 12-bit D/A Converter (DAC12).

Pin name	I/O	Function
DA0	Output	Channel 0 analog output pin

Inside MCU pin list of Module

Pin number				Timers				Communication Interfaces					Analogs			HMI	
QFN56	Power, System, Clock, Debug, CAC, VBATT	Interrupt	I/O Ports	AGT	GPT_OPS, POEG	GPT	RTC	USBFS, CAN	SCI	IIC	SPI	RF	ADC14	DAC12, OPAMP	ACMPLP	SLCDC	CTSU
1			P407	AGTIO0			RTCOUT	USB_VBUS	CTS4_RTS4 /SS4	SDA0	SSLB3		ADTRG0			SEG11	TS3
2	VSS_USB																
3			P915					USB_DM									
4			P914					USB_DP									
5	VCC_USB																
6	VCC_USB _LDO																
7		IRQ0	P206		GTIU			USB_VBUS EN	RXD4/ MISO4/SCL4	SDA1	SSLB1					SEG12	TS1
8	CLKOUT	IRQ1	P205	AGTO1	GTIV	GTIOC4A		USB_OVRC URA	TXD4/ MOSI4/ SDA4/ CTS9_RTS9 /SS9	SCL1	SSLB0					SEG20	TSCAP
9	CACREF		P204	AGTOI	GTIW	GTIOC4B		USB_OVRC URB	SCK4/SCK9	SCL0	RSPCKB					SEG23	TS0
10	RES																
11	MD		P201														
12		NMI	P200														
13	TCK/ SWCLK		P300		GTOUUP	GTIOC0A					SSLB1						
14	TMS/ SWDIO		P108		GTOULO	GTIOC0B			CTS9_RTS9 /SS9		SSLB0						
15	TDO/ SWO/ CLKOUT		P109		GTOVUP	GTIOC1A		CTX0	SCK1/ TXD9/ MOSI9/ SDA9		MOSIB					SEG52	TS10
16	TDI	IRQ3	P110		GTOVLO	GTIOC1B		CRX0	RXD9/ MISO9/SCL9		MISOB				VCOUT	SEG53	
17		IRQ4	P111			GTIOC3A			SCK9		RSPCKB						TS12
18	VCC																
19	VSS																
20		KR07	P107			GTIOC6A										COM3	
21		KR06	P106			GTIOC6B					SSLA3					COM2	
22		KR05/ IRQ0	P105		GTETRGA	GTIOC1A					SSLA2					COM1	TS34
23		KR04/ IRQ1	P104		GTETRGB	GTIOC1B			RXD0/ MISO0/SCL0		SSLA1					COM0	TS13
24		KR03	P103		GTOWUP	GTIOC2A		CTX0	CTS0_RTS0 /SS0		SSLA0		AN019		CMPREF1	VL4	
25		KR02	P102	AGTO0	GTOWLO	GTIOC2B		CRX0	SCK0		RSPCKA		AN020/ ADTRG0		CMPIN1		
26		KR01/ IRQ1	P101	AGTEE0	GTETRGB	GTIOC5A			TXD0/ MOSI0/ SDA0/ CTS1_RTS1 /SS1	SDA1	MOSIA				CMPREF0	VL3	

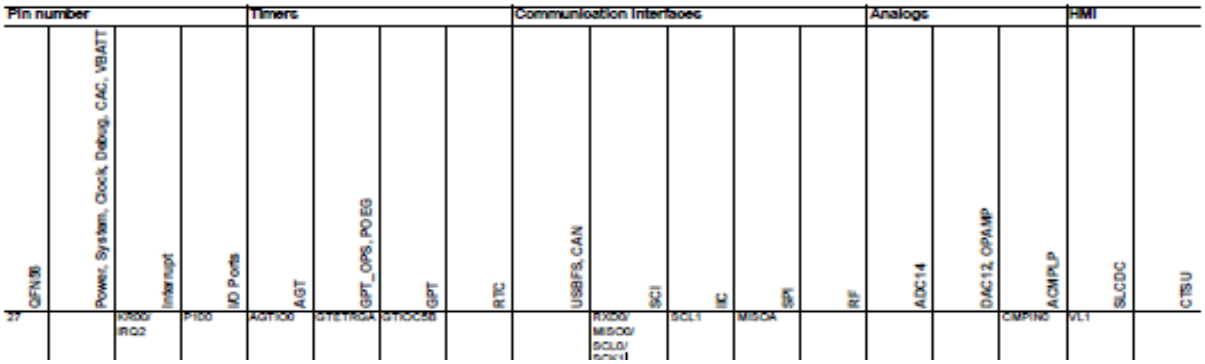


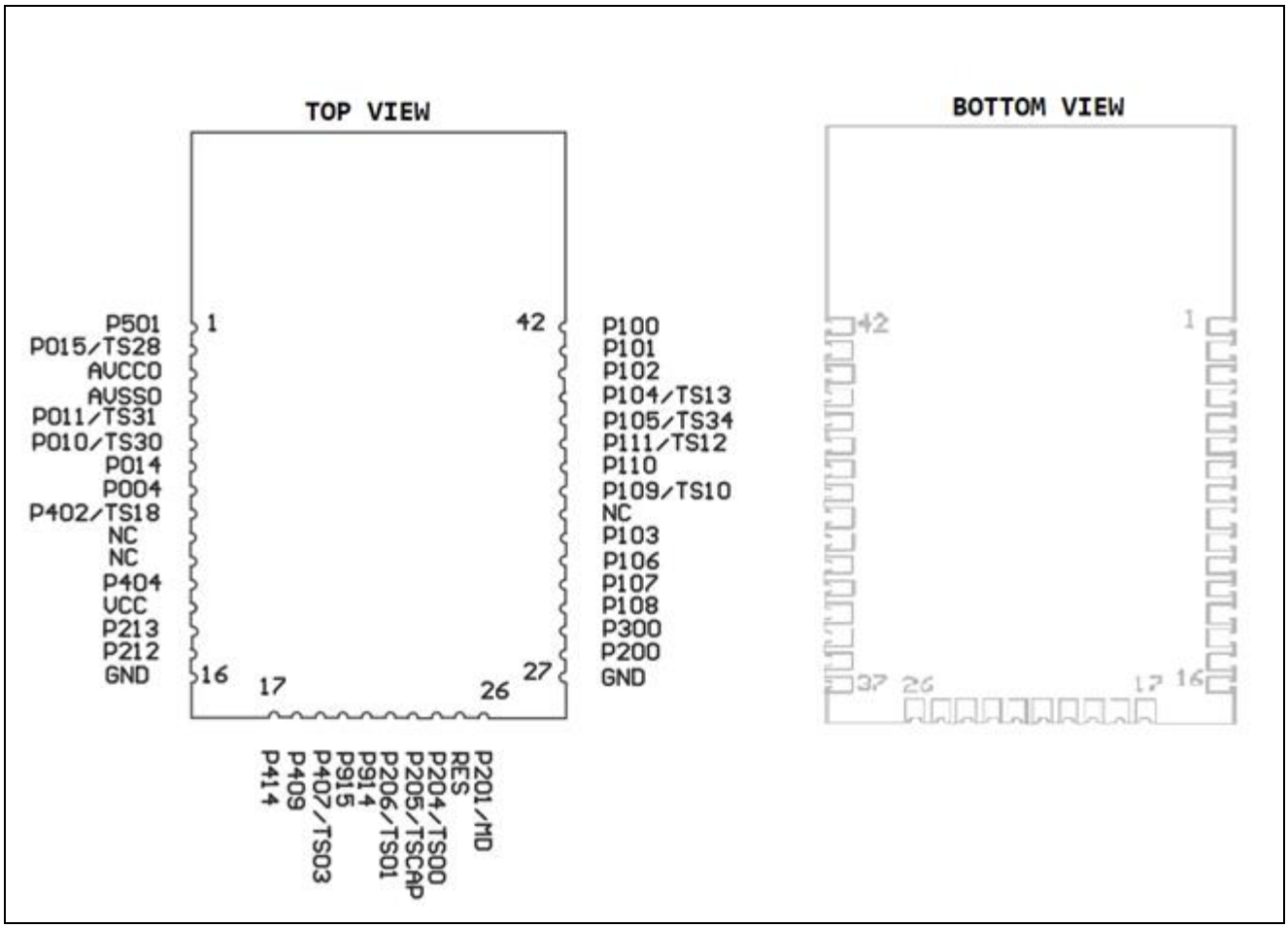
Table 3.1 Hardware specifications (1/2)

Item	Description	Remarks
Board size	• MCU Board 40.0 × 45.5[mm] • Emulator Board 40.0 × 13.5[mm]	MCU Board + Emulator Board 40 × 60[mm] (Include slit)
Power supply	USB bus power (VBUS) 5V	
MCU	RENESAS R7FA4M2AD3CFL	• Max. operating frequency: 100MHz Arm Cortex-M33 core • Code flash: 512KB • Data flash: 8KB • SRAM: 128KB • 48pin LQFP package (0.5mm pitch) • Operating temperature: -40°C to 105°C
Internal power supply	Circuit voltage: 3.3V LDO IC: RENESAS ISL9003A	Output current : 150mA max
Clock	• MCU main clock High-speed on-chip oscillator • MCU sub clock 32.768kHz crystal	
MIC	CUI DEVICES CMEJ-0415-42-LP	• Electret condenser microphone • Omni-directional • Sensitivity: -42dBV/Pa • MIC2 is optional.
MIC AMP	• Amp Gain: • 46dB(201 times), Default value • OPAMP IC: RENESAS READ2303G	Amplifier gain can be changed by replacing the external resistor.
LED	Power LED: orange color × 1 pc	
	Function display: 3-color (RGB) LED × 1 pc	MCU port control
Switch	System reset switch	Push switch × 1 pc
	Mode switch	DIP switch × 1 bit
USB connector	USB Micro B × 1 pc	USB2.0 full speed
Emulator connector	J-Link 9-pin Cortex-M adopter × 1 pc	
PMOD connector	2.54mm pitch,12 pin (6pin × 2) × 1 pc	Optional

Pin number				Timers				Communication Interfaces					Analogs			HMI	
QFN36	Power, System, Clock, Debug, CAC, VBATT	Interrupt	I/O Ports	AGT	GPT_OPS, POEG	GPT	RTC	USBFS, CAN	SCI	IIC	SPI	RF	ADC14	DAC12, OPAMP	ACMPLP	SLCDC	CTSU
49	XCIN		P215														
50	XCOUT		P214														
51	VSS																
52	XTAL	IRQ2	P213		GTETRGA	GTIOC0A			TXD1/ MOSI1/ SDA1								
53	EXTAL	IRQ3	P212	AGTEE1	GTETRGB	GTIOC0B			RXD1/ MISO1/SCL1								
54	VCC																
55		IRQ9	P414			GTIOC0B					SSLA1	CLKOUT_ RF					
56		IRQ8	P409		GTOWUP	GTIOC0A		USB_EXCE N								SEG9	

Noted:

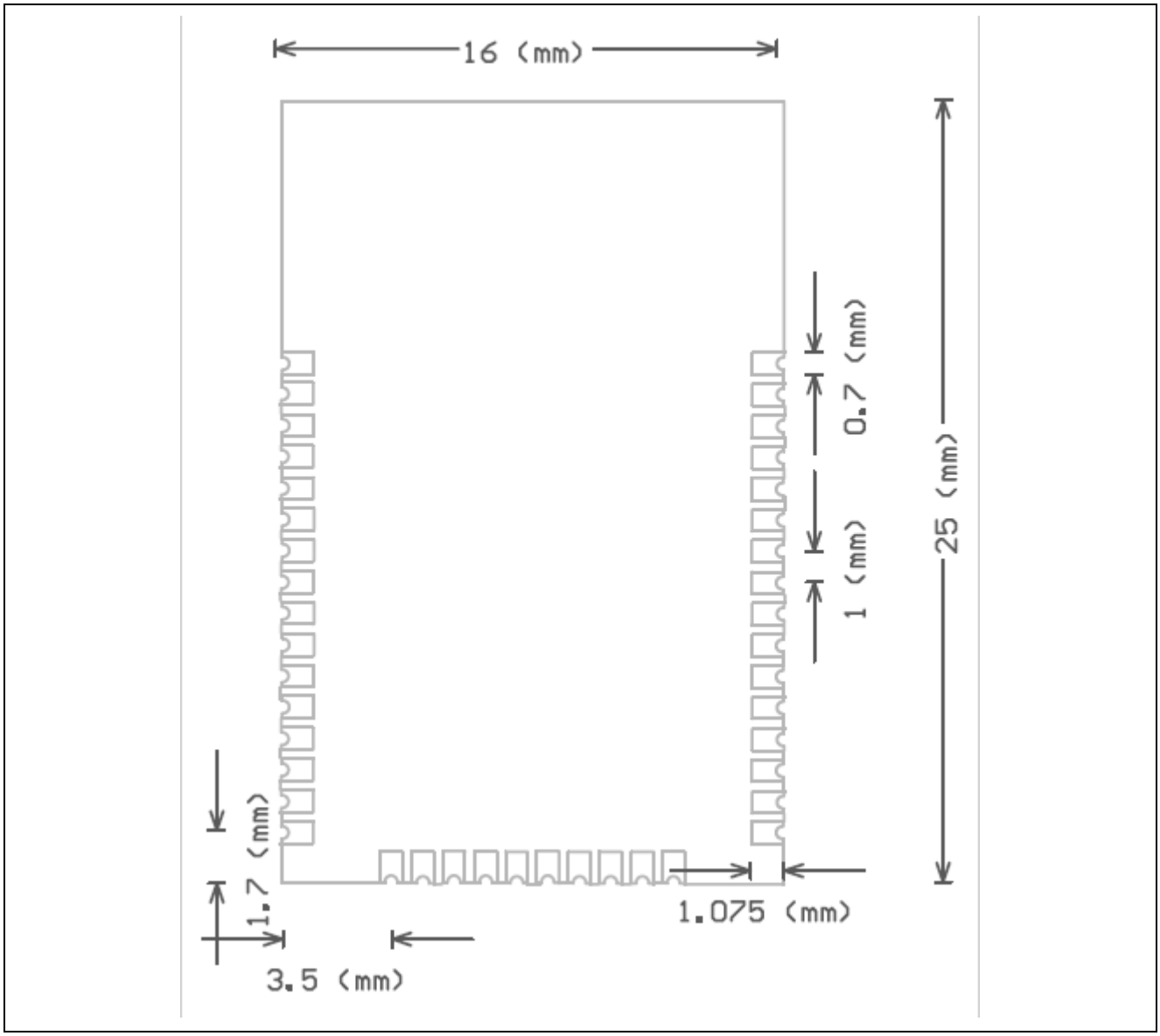
Not all of MCU pin be connected for Module use . User have to check output pin of module and check pin function which corresponding.



To be available

Module Picture

Dimension :



3. Characteristics:

3.1 BLE Characteristics:

Transmission Characteristics:

Conditions: VCC=VCC_RF=AVCC_RF=3,3V, VSS=VSS_RF=0V , Ta=25℃

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Range of frequency	RF_{CF}	2402	-	2480	MHz	
Data rate	RF_{DATA_2M}	-	2	-	Mbps	
	RF_{DATA_1M}	-	1	-	Mbps	
	RF_{DATA_500k}	-	500	-	kbps	
	RF_{DATA_125k}	-	125	-	kbps	
Maximum transmitted output power	RF_{POWER}	-	0	2	dBm	0 dBm output mode
		-	4	6	dBm	4 dBm output mode
Output frequency error	RF_{TXFERR}	–10	-	10	ppm	*1

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.
Note 1. This does not take frequency errors due to manufacturing irregularities, drift with temperature, or deterioration of the crystal over time into account.

Reception Characteristics(1Mbps)

Conditions: VCC=VCC_RF=AVCC_RF=3,3V, VSS=VSS_RF=0V , Ta=25℃

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Input frequency	RF_{RXFIN_1M}	2402	—	2480	MHz		
Maximum input level	RF_{LEVL_1M}	–10	4	—	dBm	*1	
Receiver sensitivity	RF_{STY_1M}	—	–95	—	dBm	*1	
Secondary emission strength	RF_{RXSP_1M}	—	–72	–57	dBm	30MHz to 1GHz	
		—	–54	–47	dBm	1GHz to 12GHz	
Co-channel rejection ratio	RF_{CCR_1M}	—	–7	—	dB	Prf = –67dBm*1	
Adjacent channel rejection ratio	RF_{ADCR_1M}	—	–1	—	dB	Prf = –67dBm*1	±1MHz
		—	34	—	dB		±2MHz
		—	35	—	dB		±3MHz
Blocking	RF_{BLK_1M}	—	0	—	dBm	Prf = –67dBm*1	30MHz to 2000MHz
		—	–24	—	dBm		2000MHz to 2399MHz
		—	–20	—	dBm		2484MHz to 3000MHz
		—	–4	—	dBm		> 3000MHz
Allowable frequency deviation*2	RF_{RXFER_1M}	–120	—	120	ppm	*1	
RSSI accuracy	RF_{RSSIS_1M}	—	±4	—	dB	–70dBm ≤ Prf ≤ –10dBm	

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.
Note 1. PER ≤ 30.8%, and a 37-byte payload
Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip

Reception Characteristics(500 Kbps)

Conditions: VCC=VCC_RF=AVCC_RF=3,3V, VSS=VSS_RF=0V , Ta=25℃

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Input frequency	RF_{RXFIN_500k}	2402	—	2480	MHz		
Maximum input level	RF_{LEVL_500k}	–10	4	—	dBm	*1	
Receiver sensitivity	RF_{STY_500k}	—	–100	—	dBm	*1	
Secondary emission strength	RF_{RXSP_500k}	—	–72	–57	dBm	30MHz to 1GHz	
		—	–54	–47	dBm	1GHz to 12GHz	
Co-channel rejection ratio	RF_{CCR_500k}	—	–4	—	dB	Prf = –72dBm*1	
Adjacent channel rejection ratio	RF_{ADCR_500k}	—	6	—	dB	Prf = –72dBm*1	±1MHz
		—	36	—	dB		±2MHz
		—	42	—	dB		±3MHz
Blocking	RF_{BLK_500k}	—	0	—	dBm	Prf = –72dBm*1	30MHz to 2000MHz
		—	–23	—	dBm		2000MHz to 2399MHz
		—	–20	—	dBm		2484MHz to 3000MHz
		—	–7	—	dBm		> 3000MHz
Allowable frequency deviation*2	RF_{RXFER_500k}	–120	—	120	ppm	*1	
RSSI accuracy	RF_{RSSIS_500k}	—	±4	—	dB	–70dBm ≤ Prf ≤ –10dBm	

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.
Note 1. PER ≤ 30.8%, and a 37-byte payload
Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip

Reception Characteristics (125 Kbps)

Conditions: VCC=VCC_RF=AVCC_RF=3,3V, VSS=VSS_RF=0V , Ta=25℃

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Input frequency	RF_{RXFIN_125k}	2402	—	2480	MHz		
Maximum input level	RF_{LEVL_125k}	–10	4	—	dBm	*1	
Receiver sensitivity	RF_{STY_125k}	—	–105	—	dBm	*1	
Secondary emission strength	RF_{RXSP_125k}	—	–72	–57	dBm	30 MHz to 1 GHz	
		—	–54	–47	dBm	1 GHz to 12 GHz	
Co-channel rejection ratio	RF_{CCR_125k}	—	–2	—	dB	Prf = –79 dBm*1	
Adjacent channel rejection ratio	RF_{ADCR_125k}	—	12	—	dB	Prf = –79 dBm*1	±1 MHz
		—	39	—	dB		±2 MHz
		—	45	—	dB		±3 MHz
Blocking	RF_{BLK_125k}	—	0	—	dBm	Prf = –79 dBm*1	30 MHz to 2000 MHz
		—	–23	—	dBm		2000 MHz to 2399 MHz
		—	–20	—	dBm		2484 MHz to 3000 MHz
		—	–1	—	dBm		> 3000MHz
Allowable frequency deviation*2	RF_{RXFER_125k}	–120	—	120	ppm	*1	
RSSI accuracy	RF_{RSSIS_125k}	—	±4	—	dB	T_a = +25°C, –70 dBm ≤ Prf ≤ –10 dBm	

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.
Note 1. PER ≤ 30.8%, and a 37-byte payload
Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip

Bluetooth low Energy operating and stanby current

Conditions: VCC=VCC_RF=AVCC_RF=3,3V, VSS=VSS_RF=0V , Ta=25℃

Parameter		Symbol	Min	Typ		Max	Unit	Test conditions
				Transmit output power				
				0 dBm	4 dBm			
BLE operating current (When DC-DC converter is selected)	Transmit mode, 2 Mbps	Idd_tx	-	4.5	8.7	-	mA	-
	Transmit mode, 1 Mbps		-			-	mA	-
	Transmit mode, 500 kbps		-			-	mA	-
	Transmit mode, 125 kbps		-			-	mA	-
	Receive mode, 2 Mbps Prf = -67 dBm	Idd_rx	-	3.3	3.5	-	mA	-
	Receive mode, 1 Mbps Prf = -67 dBm		-			-	mA	-
	Receive mode, 500 kbps Prf = -72 dBm		-			-	mA	-
	Receive mode, 125 kbps Prf = -79 dBm		-			-	mA	-
	Idle mode	Idd_idle	-	0.5		-	mA	-
	Deep sleep mode	Idd_slp	-	1.5		-	µA	-
	Power down mode	Idd_down	-	0.1		-	µA	-
BLE operating current (When linear regulator is selected)	Transmit mode, 2 Mbps	Idd_tx	-	10.2	18.1	-	mA	-
	Transmit mode, 1 Mbps		-			-	mA	-
	Transmit mode, 500 kbps		-			-	mA	-
	Transmit mode, 125 kbps		-			-	mA	-
	Receive mode, 2M bps Prf = -67 dBm	Idd_rx	-	6.9		-	mA	-
	Receive mode, 1 Mbps Prf = -67 dBm		-	6.9		-	mA	-
	Receive mode, 500 kbps Prf = -72 dBm		-	6.9		-	mA	-
	Receive mode, 125 kbps Prf = -79 dBm		-	7.1		-	mA	-
	Idd_idle	Idd_idle	-	0.7		-	mA	-
	Idd_slp	Idd_slp	-	1.5		-	µA	-
	Idd_down	Idd_down	-	0.1		-	µA	-

3.2 MCU Characteristics:

MCU operating and standby current

Conditions: VCC=AVCC0=1.8 to 3.6V

Parameter					Symbol	Typ*10	Max	Unit	Test conditions
Supply current*1	High-speed mode*2	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 48 MHz	I_{CC}	8.4	-	mA	*7
				ICLK = 32 MHz		5.9	-		
				ICLK = 16 MHz		3.5	-		
				ICLK = 8 MHz		2.3	-		
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 48 MHz		17.9	-		
				ICLK = 32 MHz		12.4	-		
				ICLK = 16 MHz		7.0	-		
				ICLK = 8 MHz		4.3	-		
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 48 MHz		21.2	-		*9
				ICLK = 32 MHz		16.0	-		*8
				ICLK = 16 MHz		8.8	-		
				ICLK = 8 MHz		5.1	-		
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 48 MHz		-	56.0		*9
		Sleep mode	All peripheral clock disabled*5	ICLK = 48 MHz		3.7	-		*7
				ICLK = 32 MHz		2.7	-		
				ICLK = 16 MHz		2.0	-		
				ICLK = 8 MHz		1.5	-		
			All peripheral clock enabled*5	ICLK = 48 MHz		16.4	-		*9
				ICLK = 32 MHz		12.7	-		*8
				ICLK = 16 MHz		7.2	-		
				ICLK = 8 MHz		4.3	-		
		Increase during BGO operation*6				2.5	-		-

	Middle-speed mode*2	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 12 MHz	I_{CC}	2.5	-	mA	*7
				ICLK = 8 MHz		2.1	-		
				ICLK = 1 MHz		1.0	-		
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 12 MHz		5.2	-		
				ICLK = 8 MHz		4.0	-		
				ICLK = 1 MHz		1.3	-		
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 12 MHz		6.5	-		*8
				ICLK = 8 MHz		4.8	-		
				ICLK = 1 MHz		1.6	-		
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 12 MHz		-	23.0		
		Sleep mode	All peripheral clock disabled*5	ICLK = 12 MHz		1.4	-		*7
				ICLK = 8 MHz		1.3	-		
				ICLK = 1 MHz		0.9	-		
			All peripheral clock enabled*5	ICLK = 12 MHz		5.3	-		*8
				ICLK = 8 MHz		4.0	-		
				ICLK = 1 MHz		1.5	-		
		Increase during BGO operation*6				2.5	-		-

Parameter					Symbol	Typ*10	Max	Unit	Test conditions
Supply current*1	Low-speed mode*3	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 1 MHz	I_{CC}	0.4	-	mA	*7
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 1 MHz		0.6	-		
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 1 MHz		1.1	-		*8
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 1 MHz		-	2.5		
		Sleep mode	All peripheral clock disabled*5	ICLK = 1 MHz		0.3	-		*7
			All peripheral clock enabled*5	ICLK = 1 MHz		1.0	-		*8
	Low-voltage mode*3	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 4 MHz	I_{CC}	1.8	-	mA	*7
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 4 MHz		3.0	-		
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 4 MHz		3.3	-		*8
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 4 MHz		-	9.0		
		Sleep mode	All peripheral clock disabled*5	ICLK = 4 MHz		1.4	-		*7
			All peripheral clock enabled*5	ICLK = 4 MHz		2.9	-		*8

	Subosc-speed mode*4	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 32.768 kHz	I_{CC}	9.3	-	µA	*8
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 32.768 kHz		17.2	-		
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 32.768 kHz		-	106.0		
		Sleep mode	All peripheral clock disabled*5	ICLK = 32.768 kHz		6.0	-		
			All peripheral clock enabled*5	ICLK = 32.768 kHz		14.0	-		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. The clock source is HOCO.
Note 3. The clock source is MOCO.
Note 4. The clock source is the sub-clock oscillator.
Note 5. This does not include BGO operation.
Note 6. This is the increase for programming or erasure of the flash memory for data storage during program execution.
Note 7. FCLK, PCLKA, PCLKB, PCLKC and PCLKD are set to divided by 64.
Note 8. FCLK, PCLKA, PCLKB, PCLKC and PCLKD are the same frequency as that of ICLK.
Note 9. FCLK and PCLKB are set to divided by 2 and PCLKA, PCLKC and PCLKD are the same frequency as that of ICLK.
Note 10. VCC = 3.3 V.

Parameter			Symbol	Typ*4	Max	Unit	Test conditions
Supply current*1	Software Standby mode*2	T_a = 25°C	I_{CC}	0.9	5.0	µA	PSMCR.PSMC[1:0] = 01b (48-KB SRAM on)
		T_a = 55°C		1.5	8.1		
		T_a = 85°C		3.6	22.1		
		T_a = 25°C		1.0	5.6		PSMCR.PSMC[1:0] = 00b (All SRAM on)
		T_a = 55°C		1.6	8.4		
		T_a = 85°C		4.3	26.7		
	Increment for RTC operation with low-speed on-chip oscillator*3			0.5	-		-
	Increment for RTC operation with sub-clock oscillator*3			0.4	-		SOMCR.SODRV[1:0] are 11b (Low power mode 3)
				1.2	-		SOMCR.SODRV[1:0] are 00b (Normal mode)

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. The IWDT and LVD are not operating.
Note 3. Includes the current of sub-oscillation circuit or low-speed on-chip oscillator.
Note 4. VCC = 3.3 V.

Parameter			Symbol	Typ	Max	Unit	Test conditions
Supply current*1	RTC operation when VCC is off	T_a = 25°C	I_{CC}	0.8	-	µA	VBATT = 2.0 V SOMCR.SORDRV[1:0] = 11b (Low power mode 3)
		T_a = 55°C		0.9	-		
		T_a = 85°C		1.1	-		
		T_a = 25°C		0.9	-		VBATT = 3.3 V SOMCR.SORDRV[1:0] = 11b (Low power mode 3)
		T_a = 55°C		1.0	-		
		T_a = 85°C		1.2	-		
		T_a = 25°C		1.6	-		VBATT = 2.0 V SOMCR.SORDRV[1:0] = 00b (Normal mode)
		T_a = 55°C		1.8	-		
		T_a = 85°C		2.1	-		
		T_a = 25°C		1.7	-		VBATT = 3.3 V SOMCR.SORDRV[1:0] = 00b (Normal mode)
		T_a = 55°C		1.9	-		
		T_a = 85°C		2.2	-		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

. Reorient or relocate the receiving antenna.

. Increase the separation between the equipment and receiver.

. Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

. Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: To assure continued compliance, any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. (Example - use only shielded interface cables when connecting to computer or peripheral devices).

End Product Labeling

This transmitter module is authorized only for use in devices where the antenna may be installed such that 0.5 cm may be maintained between the antenna and users. The final end product must be labeled in visible area with the following: “Contains FCC ID: 2A4AP0001”

End Product Manual Information

The user manual for end users must include the following information in a prominent location “IMPORTANT NOTE: To comply with FCC RF exposure compliance requirements, the antenna used for this transmitter must be installed to provide a separation distance of at least 0.5 cm from all persons and must not be colocated or operating in conjunction with any other antenna or transmitter. “This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT NOTE: In the event that these conditions cannot be met (for example certain laptop configurations or colocation with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for reevaluating the end product (including the transmitter) and obtaining a separate FCC authorization. This device is intended only for OEM integrators under the following conditions: The antenna must be installed such that 0.5 cm is maintained between the antenna and users. As long as a condition above is met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

NCC警語

取得審驗證明之低功率射頻器材，非經核准，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。

低功率射頻器材之使用不得影響飛航安全及干擾合法通信；經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。

前述合法通信，指依電信管理法規定作業之無線電通信。低功率射頻器材須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。

本模組於取得認證後將依規定於模組本體標示審驗合格標籤，並要求最終產品平台廠商(OEM Integrator)於最終產品平台(End Product)上標示"本產品內含射頻模組，其NCC型式認證號碼為:"CCXXxxYYyyyZzW"

Revision Record

Rev.	Date	Description	
		Page	Summary
0.01	Oct.08.2021	—	First edition issued
0.02	Oct.24.2021		Update Pin description
0.03	Feb.17,2022		Federal Communication Commission Interference Statement
0.04	Mar.01.2022		Corrected FCC ID.
0.05	Mar.07.2022		NCC 警語