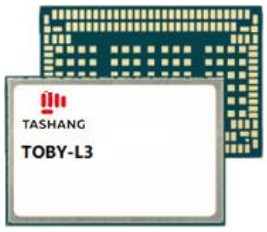
TOBY-L3 series

Multi-mode LTE (Cat 4) modules with 3G and 2G fallback

System Integration Manual



35.6 x 24.8 x 2.6 mm

Abstract

This document describes the features and the system integration of TOBY-L3 series multi-mode cellular modules. The modules are a complete and cost efficient LTE-FDD, LTE-TDD, DC-HSPA+, (E)GPRS multi-mode and multi-band solution with open CPU embedded Linux programming capability. The modules offer up to 150 Mb/s download and up to 50 Mb/s upload data rates with Category 4 LTE technology in the compact TOBY form factor.

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Document Information

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Product status	Corresponding content status	
Functional Sample	Draft	For functional testing. Revised and supplementary data will be published later.
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Initial Production	Early Production Information	Data from product verification. Revised and supplementary data may be published later.
Mass Production / End of Life	Production Information	Document contains the final product specification.

This document applies to the following products:

Product name	Type number	Modem version	Application version	PCN reference	Product status
TOBY-L3104	TOBY-L3104-50A-00-00	M31.01.01.03.11	A31.50.20.11		Mass Production
	TOBY-L3104-50A-00-01	M31.01.01.03.12	A31.50.20.12	TSD-21121301	Mass Production
	TOBY-L3104-50B-00-00	M30.01.01.02.11	A30.50.20.11		Mass Production
	TOBY-L3104-50B-00-01	M30.01.01.02.14	A30.50.20.14	TSD-21121302	Mass Production
TOBY-L3204	TOBY-L3204-50A-00-00	M31.02.01.03.12	A31.50.20.12		Mass Production
	TOBY-L3204-50B-00-00	M30.02.01.03.12	A30.50.20.12		Mass Production
TOBY-L3404	TOBY-L3404-50A-00-00	M31.04.01.03.12	A31.50.20.12		Mass Production
	TOBY-L3404-50B-00-00	M30.04.01.03.12	A30.50.20.12		Mass Production
TOBY-L3904	TOBY-L3904-50A-00-00	M31.09.00.03.14	A31.50.20.14		Mass Production
	TOBY-L3904-50B-00-00	M30.09.00.05.08	A30.50.20.08		Mass Production
	TOBY-L3904-50A-01-00	M31.09.01.01.10	A31.50.20.10		Mass Production
	TOBY-L3904-50A-01-01	M31.09.01.03.13	A31.50.20.13	TSD-21090101	Mass Production
	TOBY-L3904-50A-01-02	M31.09.01.03.14	A31.50.20.14	TSD-21101501	Mass Production
	TOBY-L3904-50B-01-00	M30.09.01.02.13	A30.50.20.13		Mass Production
	TOBY-L3904-50A-11-00	M31.09.01.03.01	A31.00.12.01		Mass Production

Contents

1 System description

1.1 Overview

The TOBY-L3 series modules support multi-band LTE-FDD, LTE-TDD, DC-HSPA+, and (E)GPRS radio access technologies in the very small TOBY 248-pin LGA form-factor (35.6 x 24.8 x 2.6 mm), which is easy to integrate in compact designs.

TOBY-L3 series modules are form-factor compatible with the other u-blox cellular module families (including SARA, LISA, LARA, and TOBY form factors): this allows customers to take maximum advantage of their hardware and software investments, and provides very short time-to-market.

With LTE category 4 data rates up to 150 Mb/s (downlink) / 50 Mb/s (uplink), the modules are ideal for applications requiring the highest data-rates and high-speed internet access.

TOBY-L3 series modules include the following product versions:

- The "1x" product feature versions, or "SMART modem" product feature versions, which allow customers to run their own dedicated applications on an embedded Linux distribution with libTS library APIs in the open CPU on-chip processor
- The "0x" product feature versions, or "SLIM modem" product feature versions, which can be controlled by an external application processor through standard TOBY-L3 series AT commands User Manual [2].

TOBY-L3 series modules are the ideal product for the development of all kinds of automotive or industrial devices, such as smart antennas and in-dash telematics / infotainment devices. This module supports a comprehensive set of HW interfaces (including SGMII for Ethernet and digital audio) over an extended temperature range that allows the establishment of an emergency call up to +85 °C, and complemented by a set of state-of-the art security features.

TOBY-L3 series modules are also the perfect choice for consumer fixed-wireless terminals, mobile routers and gateways, applications requiring video streaming and many other industrial (M2M) applications.

TOBY-L3 series modules are manufactured in ISO/TS 16949 certified sites, with the highest production standards and the highest quality and reliability. Each module is fully tested and inspected during production. The modules are qualified according to the automotive requirements as for systems installed in vehicles.

Table 1summarizes the main features and interfaces of the TOBY-L3 series modules.

Order Code	Region	Bands			Interfaces													Features																				Grade		
		LTE	UMTS	GSM	UART(2 settable as SPI)	USB 2.0 device/host	SPI(settable as UART)	SGMII	eMMC	SDIO	DDC (I2C)	SIM	GPIO	ADC	Antenna supervisor	MIMO / Rx Diversity	Digital Audio	Host Select	Open CPU for customer applications	GNSS via modem	Wi-Fi via modem	Bluetooth via modem	Network indication	Jamming detection	Embedded TCP/IP, UDP/IP stack	Embedded HTTP, FTP, SSL, TLS	FOTA	FOAT	Dual stack IPv4/IPv6	VoLTE[1]	SMS	eCall	SMTP	Telematics	Standard	Professional	Automotive
TOBY-L3104-50A-00	EMEA	1,3,7,8,20,28,38	1,8	900,1800	4	1		1			2	1	8		•	•	•		•			•	•	•	•	•	•	•	•	•	•		•						•
TOBY-L3204-50A-00	APAC / South. American	1,3,5,7,8,9,19,28	1,5,6,8,19	850,900,1800,1900	4	1		1			2	1	8		•	•	•		•			•	•	•	•	•	•	•	•	•	•		•						•
TOBY-L3404-50A-00	North. American	2,4,5,7,12,13,66	2,4,5	850,1900	4	1		1			2	1	8		•	•	•		•			•	•	•	•	•	•	•	•	•	•		•						•
TOBY-L3904-50A-00	China / India / Japan	1,3,5,8,18,19,26,38,39,40,41	1,6,8,19	900,1800	4	1		1			2	1	8		•	•	•		•			•	•	•	•	•	•	•	•	•	•		•						•
TOBY-L3904-50A-01	China	1,3,5,8,38,39,40,41	1,8	900,1800	4	1		1			2	1	8		•	•	•		•			•	•	•	•	•	•	•	•	•	•		•						•
TOBY-L3904-50A-11	China	1,3,5,8,38,39,40,41	1,8	900,1800	4	1	1	1	1	1	2	1	8	2	•	•	•	2	•	•	•	•	•	•	•	•	•	•	•	•	•		•						•
TOBY-L3104-50B-00	EMEA	1,3,7,8,20,28,38	1,8	900,1800	4	1		1			2	1	8		•	•	•		•			•	•	•	•	•	•	•	•	•	•		•						•
TOBY-L3204-50B-00	APAC / South. American	1,3,5,7,8,9,19,28	1,5,6,8,19	850,900,1800,1900	4	1		1			2	1	8		•	•	•		•			•	•	•	•	•	•	•	•	•	•		•						•
TOBY-L3404-50B-00	North. American	2,4,5,7,12,13,66	2,4,5	850,1900	4	1		1			2	1	8		•	•	•		•			•	•	•	•	•	•	•	•	•	•		•						•

[1] Available in future releases

TOBY-L3904-50B-00	China / India / Japan	1,3,5,8,18,19,26,38,39,40,41	1,6,8,19	900,1800	4 1 1 2 1 8 • • •	• • • • • • • • • • •	•
TOBY-L3904-50B-01	China	1,3,5,8,38,39,40,41	1,8	900,1800	4 1 1 2 1 8 • • •	• • • • • • • • • • •	•

Table 1: TOBY-L3 series main features summary

TOBY-L3 series modules provide multi-band 4G / 3G / 2G multi-mode radio access technologies, based on the 3GPP Release 10 protocol stack, with main characteristics summarized in Table 2 and Table 3.

LTE	3G	2G
Frequency Division Duplex (LTE FDD) Time Division Duplex (LTE TDD) Down-Link / MIMO / Rx diversity	Dual-Cell High Speed Packet Access Frequency Division Duplex (UMTS FDD) Down-Link Rx diversity	Enhanced Data rate GSM Evolution (EDGE) Time Division Multiple Access (TDMA) DL Advanced Rx Performance Phase 1
LTE FDD Power Class Class 3 (23±2dBm) LTE TDD Power Class Class 3 (23±2dBm)	UMTS FDD Power Class Class 3 (23±2dBm)	GMSK Power Class Class 4 (32.5±2dBm) for GSM/E-GSM/GSM850 bands Class 1 (30±2dBm) for DCS/PCS bands 8-PSK Power Class Class E2 (26±2dBm) for GSM/E-GSM/GSM850 bands Class E2 (26±2dBm) for DCS/PCS bands
LTE category 4: up to 150 Mb/s DL up to 50 Mb/s UL LTE category 1: up to 10 Mb/s DL up to 5 Mb/s UL	FDD UE categories: DL cat.24, up to 42.2 Mb/s UL cat.6, up to 5.76 Mb/s	GPRS multi-slot class 12, CS1-CS4: up to 85.6 kbit/s DL/UL EDGE multi-slot class 12, MCS1-MCS9 up to 236.8 kbit/s DL/UL

Table 2: TOBY-L3 series LTE, 3G and 2G characteristics summary

Module	Region	LTE FDD bands	LTE TDD bands	UMTS FDD bands	GSM bands
TOBY-L3104-50A-00 **TOBY-L3104-50B-00**	EMEA	1 (2100 MHz) 3 (1800 MHz) 7 (2600 MHz) 8 (900 MHz) 20 (800 MHz) 28 (700 MHz)	38 (2600 MHz)	1 (2100 MHz) 8 (900 MHz)	E-GSM 900 DCS 1800
TOBY-L3204-50A-00 **TOBY-L3204-50B-00**	APAC / South America	1 (2100 MHz) 3 (1800 MHz) 5 (850 MHz) 7 (2600 MHz) 8 (900 MHz) 9 (1800 MHz) 19 (850 MHz) 28 (700 MHz)		1 (2100 MHz) 5 (850 MHz) 6 (800 MHz) 8 (900 MHz) 19 (850 MHz)	GSM 850 E-GSM 900 DCS 1800 PCS 1900
TOBY-L3404-50A-00 **TOBY-L3904-50B-00**	North America	2 (1900 MHz) 4 (1700 MHz) 5 (850 MHz) 7 (2600 MHz) 12 (700 MHz) 13 (700 MHz) 66 (1700 MHz)		2 (1900 MHz) 4 (1700 MHz) 5 (850 MHz)	GSM 850 PCS 1900

TOBY-L3904-50A-00 **TOBY-L3904-50B-00**	China / India / Japan	1 (2100 MHz) 3 (1800 MHz) 5 (850 MHz) 8 (900 MHz) 18 (850 MHz) 19 (850 MHz) 26 (850 MHz)	38 (2600 MHz) 39 (1900 MHz) 40 (2300 MHz) 41 (2500 MHz)	1 (2100 MHz) 6 (800 MHz) 8 (900 MHz) 19 (850 MHz)	E-GSM 900 DCS 1800
TOBY-L3904-50A-01 **TOBY-L3904-50A-11** **TOBY-L3904-50B-01**	China	1 (2100 MHz) 3 (1800 MHz) 5 (850 MHz) 8 (900 MHz)	38 (2600 MHz) 39 (1900 MHz) 40 (2300 MHz) 41 (2500 MHz)	1 (2100 MHz) 8 (900 MHz)	E-GSM 900 DCS 1800

Table 3: TOBY-L3 series supported bands[2] summary

[2] TOBY-L3 series modules support all E-UTRA channel bandwidths for each operating band according to 3GPP TS 36.521-1.

1.2 Architecture

Figure 1 summarizes the internal architecture of the TOBY-L3 series modules.

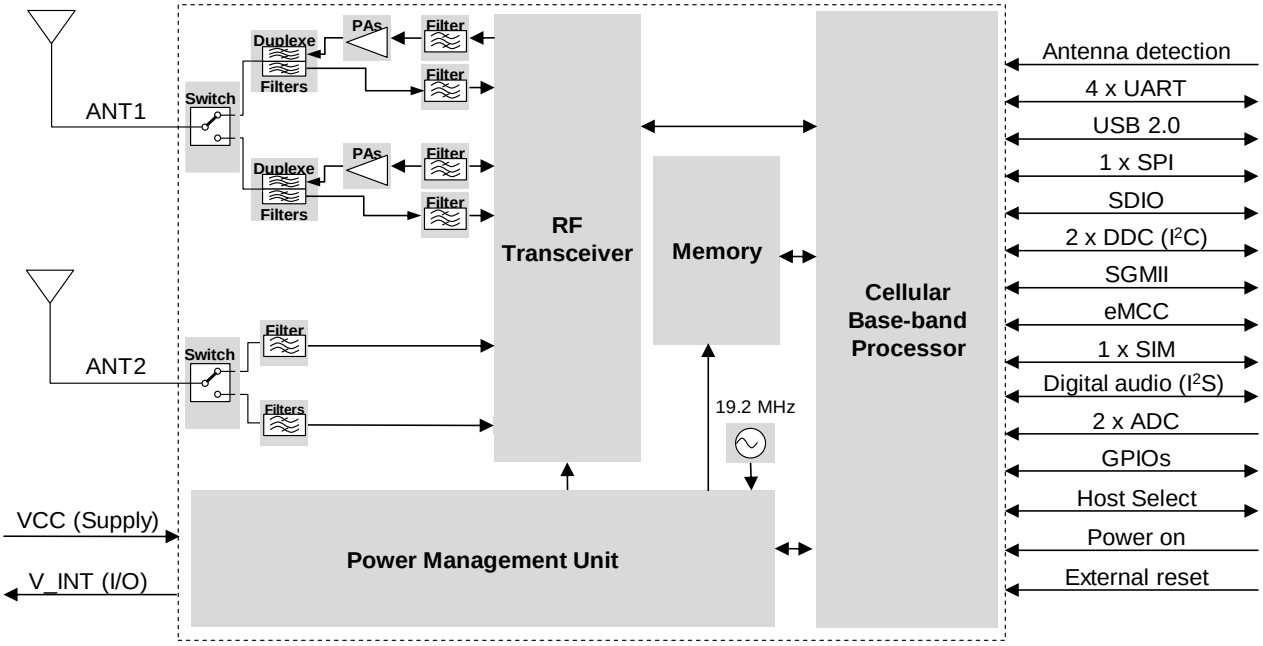

Figure 1: TOBY-L3 series modules simplified block diagram

TOBY-L3 series modules internally consist of the RF, Baseband and Power Management sections described herein with more details than the simplified block diagrams of Figure 1.

RF section

The RF section is composed of an RF transceiver, PAs, crystal oscillator, filters, duplexers and RF switches.

The Tx signal is pre-amplified by the RF transceiver, then output to the primary antenna input/output port (**ANT1**) of the module via power amplifier (PA), SAW band pass filters band, specific duplexer and antenna switch.

Dual receiving paths are implemented according to MIMO, and Receiver Diversity radio technologies supported by the modules as LTE category 4 and HSDPA category 24 User Equipment: incoming signals are received through the primary (**ANT1**) and the secondary (**ANT2**) antenna input ports which are connected to the RF transceiver via specific antenna switch, diplexer, duplexer, SAW band pass filters.

- RF transceiver performs modulation, up-conversion of the baseband I/O signals for Tx, down-conversion and demodulation of the dual RF signals for Rx. The RF transceiver contains:
  Single chain high linearity receivers with integrated LNAs for multi-mode operation,
  Highly linear RF demodulator / modulator capable GMSK, 8-PSK, QPSK, 16-QAM, 64-QAM
  RF synthesizer,
  VCO.

- Power Amplifiers (PA) amplify the Tx signal modulated by the RF transceiver
- RF switches connect the primary (ANT1) and secondary (ANT2) antenna ports to the suitable Tx / Rx path
- SAW duplexers and band pass filters separate the Tx and Rx signal paths and provide RF filtering
- 19.2 MHz temperature-controlled crystal oscillator (TCXO) generates the clock reference in active mode or connected mode.

Baseband and power management section

The Baseband and Power Management section is composed of the following main elements:

- A mixed signal ASIC, which integrates
  - Microprocessor for control functions
  - DSP core for cellular Layer 1 and digital processing of Rx and Tx signal paths
  - Memory interface controller
  - Dedicated peripheral blocks for control of the USB, SIM and generic digital interfaces
  - Interfaces to the RF transceiver ASIC
- Memory system, which includes NAND flash and LPDDR2 RAM
- Voltage regulators to derive all the subsystem supply voltages from the module supply input **VCC**
- Voltage sources for external use: **V_INT**, **V_SIM**, **V_ETH**, **V_MMC**
- Hardware power on
- Hardware reset
- Low power idle mode support

1.3 Pin-out

Table 4 lists the pin-out of the TOBY-L3 series modules, with pins grouped by function.

Function	Pin Name	Pin No	I/O	Description	Remarks
Power	**VCC**	70,71,72	I	Module supply input	**VCC** supply circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.5.1 for functional description / requirements. See section 2.2.1 for external circuit design-in.
	GND	2, 30, 32, 44, 46, 69, 73, 74, 76, 78, 79, 80, 82, 83, 85, 86, 88-90, 92-152, 209, 219, 226, 229, 232, 235, 238, 241	N/A	Ground	**GND** pins are internally connected each other. External ground connection affects the RF and thermal performance of the device. See section 1.5.1for functional description. See section 2.2.1 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
	V_INT	5	O	Generic digital interfaces supply output	**V_INT** = 1.8 V (typical) generated by internal DC/DC regulator when the module is switched on. Test-Point for diagnostic access is recommended. See section 1.5.2 for functional description. See section 2.2.2 for external circuit design-in.
System	**PWR_ON**	20	I	Power-on input	The **PWR_ON** input is pulled up to an internal voltage (dVdd) minus a diode drop. As per the design, this causes the PWR_ON pin's VIL(max) to vary from 0.35 V up to 0.67 V based on the diode drop offered. Active-low module power-on/off input. Test-Point for diagnostic access is recommended. See section 1.6.1 for functional description. See section 2.3.1 for external circuit design-in.
	RESET_N	23	I	External reset input	Active-low module reset input. Internal pull-up to V_INT. Test-Point for diagnostic access is recommended. See section 1.6.3 for functional description. See section 2.3.2 for external circuit design-in.
	HOST_SELECT0	26	I / I/O / I	Host select / GPIO / External Interrupt	1.8 V GPIO or External Interrupt configurable by open CPU API. See sections 1.6.4, 1.13 for functional description. See sections 2.3.3, 2.10 for external circuit design-in.
	HOST_SELECT1	62	I/O / I	GPIO / External Interrupt	1.8 V GPIO or External Interrupt configurable by open CPU API. See sections 1.6.4, 1.13 for functional description. See sections 2.3.3, 2.10 for external circuit design-in.
Antennas	**ANT1**	81	I/O	Primary antenna	Main Tx / Rx antenna interface. 50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and application device compliance with required certification schemes. See section 1.7.1 for functional description / requirements. See section 2.4 for external circuit design-in.
	ANT2	87	I	Secondary antenna	Rx only for Down-Link, MIMO and Rx diversity. 50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and application device compliance with required certification schemes. See section 1.7.1 for functional description / requirements. See section 2.4 for external circuit design-in.
	ANT_DET	75	I	Antenna detection	ADC for antenna presence detection function. See section 1.7.2 for functional description. See section 2.4.2 for external circuit design-in.
SIM	**VSIM**	59	O	SIM supply output	**VSIM** = 1.8 V / 3 V output as per the connected SIM type. See section 1.8 for functional description. See section 2.5 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
	SIM_IO	57	I/O	SIM data	Data input/output for 1.8 V / 3 V SIM. Internal 4.7 kΩ pull-up to **VSIM**. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_CLK	56	O	SIM clock	3.9 MHz clock output for 1.8 V / 3 V SIM. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_RST	58	O	SIM reset	Reset output for 1.8 V / 3 V SIM. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
USB	**VUSB_DET**	4	I	USB detect input	VBUS (5 V typical) must be connected to this pin to enable the module USB device interface. Test-Point for diagnostic / FW update access is recommended. See section 1.8.1 for functional description. See section 2.6.1 for external circuit design-in.
	USB_D–	27	I/O	USB High-Speed 2.0 diff. transceiver (–)	90 Ω nominal differential impedance (Z_0). 30 Ω nominal common mode impedance (Z_{CM}). Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 specs [4] are part of the USB pin driver and need not be provided externally. Test-Point for diagnostic / FW update access is recommended. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	USB_D+	28	I/O	USB High-Speed 2.0 diff. transceiver (+)	90 Ω nominal differential impedance (Z_0). 30 Ω nominal common mode impedance (Z_{CM}). Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 specs [4] are part of the USB pin driver and need not be provided externally. Test-Point for diagnostic / FW update access is recommended. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	USB_ID	168	I	USB device identification	Pin for ID resistance measurement. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
UART0	**RXD**	17	O / O	UART0 data output / SPI1 Master Output Slave Input	1.8 V output, Circuit 104 (RXD) in ITU-T V.24. Alternatively configurable as SPI1 Master Output Slave Input. Test-Point for diagnostic access recommended. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
	TXD	16	I / I	UART0 data input / SPI1 Master Input Slave Output	1.8 V input, Circuit 103 (TXD) in ITU-T V.24. Alternatively configurable as SPI1 Master Input Slave Out. Internal active pull-up to **V_INT**. Test-Point for diagnostic access recommended. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
	CTS	15	O / O	UART0 clear to send output / SPI1 Shift Clock	1.8 V output, Circuit 106 (CTS) in ITU-T V.24. Alternatively configurable as SPI1 Shift Clock. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
	RTS	14	I / O	UART0 ready to send input / SPI1 Chip Select	1.8 V input, Circuit 105 (RTS) in ITU-T V.24. Internal active pull-up to **V_INT**. Alternatively configurable as SPI1 Chip Select. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
	RI	11	O / I/O / I	UART0 ring indicator / GPIO / External Interrupt	1.8 V output, Circuit 125 (RI) in ITU-T V.24. Configurable as GPIO or External Interrupt. See sections 1.9.2 for functional description. See sections 2.6.2 for external circuit design-in.
UART1	**RXD1**	160	O / O / O / O	UART1 data output / SPI2 MOSI / I2S1 Word Alignment / PCM1 Frame Sync	1.8 V output, Circuit 104 (RXD) in ITU-T V.24, alternatively configurable as SPI2 MOSI, I2S1 Word Alignment or PCM1 Frame Sync by open CPU API or AT command. See section 1.9.2 for functional description. See section 2.6.2 / 2.6.3 for external circuit design-in.
	TXD1	159	I / I / I / I	UART1 data input / SPI2 MISO / I2S1 Receive Data In / PCM1 Data In	1.8 V input, Circuit 103 (TXD) in ITU-T V.24, alternatively configurable as SPI2 MISO, I2S1 Receive Data In or PCM1 Data In by open CPU API or AT command. Internal pull-up to **V_INT** enabled when UART1 data input. See section 1.9.2 / 1.9.2.3 for functional description. See section 2.6.2 / 2.6.3 for external circuit design-in.
	CTS1	195	O / O / O / O	UART1 CTS output / SPI2 Chip Select / I2S1 Serial Clock / PCM1 Clock	1.8 V output, Circuit 106 (CTS) in ITU-T V.24, alternatively configurable as SPI2 Chip Select, I2S1 Serial Clock or PCM1 Clock by open CPU API or AT Command. See section 1.9.2 for functional description. See section 2.6.2 / 2.6.3 for external circuit design-in.
	RTS1	193	I / O / O / O	UART1 RTS input / SPI2 Shift Clock / I2S1 Chip Select / PCM1 Data Out	1.8 V input, Circuit 105 (RTS) in ITU-T V.24, alternatively configurable as SPI2 Shift Clock, I2S1 Chip Select or PCM1 Data Out by open CPU API or AT Command. Internal pull-up to **V_INT** enabled when UART1 RTS input. See section 1.9.2 for functional description. See section 2.6.2 / 2.6.3 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
UART2	**RXD2**	162	O	UART2 data output,	1.8 V output, Circuit 104 (RXD) in ITU-T V.24. Used only for coexistence between LTE and WIFI. See section 1.9.2.3 for functional description. See section 2.6.2 for external circuit design-in.
	TXD2	161	I	UART2 data input	1.8 V input, Circuit 103 (TXD) in ITU-T V.24. Internal active pull-up to **V_INT**. Used only for coexistence between LTE and WIFI See section 1.9.2.3 for functional description. See section 2.6.2 for external circuit design-in.
UART3	**RXD3**	19	O	UART3 data output	1.8 V output, Circuit 104 (RXD) in ITU-T V.24. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
	TXD3	18	I	UART3 data input	1.8 V input, Circuit 103 (TXD) in ITU-T V.24. Internal active pull-up to **V_INT**. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
SPI0	**SPI_MOSI**	174	O / O	SPI0 Master Output Slave Input / UART4 Receive Data	1.8 V, SPI0 data output. Alternatively configurable as UART4 Receive Data by Open CPU or AT Command. See section 1.9.3.1 for functional description. See section 2.6.3 for external circuit design-in.
	SPI_MISO	169	I / I	SPI0 Master Input Slave Output / UART4 Transmit Data	1.8 V, SPI0 data input. Alternatively configurable as UART4 Transmit Data by Open CPU or AT Command. See section 1.9.3.1 for functional description. See section 2.6.3 for external circuit design-in.
	SPI_SCLK	179	O / O	SPI0 Shift Clock / UART4 Clear To Send	1.8 V, SPI0 clock. Alternatively configurable as UART4 Clear To Send by Open CPU or AT Command. See section 1.9.3.1 for functional description. See section 2.6.3 for external circuit design-in.
	SPI_CS	173	O / I	SPI0 Chip Select 0 / UART4 Ready To Send	1.8 V, SPI0 chip select 0. Alternatively configurable as UART4 Ready To Send by Open CPU or AT Command. See section 1.9.3.1 for functional description. See section 2.6.3 for external circuit design-in.
I2C0	**SCL**	54	O	I2C0 clock	1.8 V open drain. External pull-up required. See section 1.9.4 for functional description. See section 2.6.4 for external circuit design-in.
	SDA	55	I/O	I2C0 data	1.8 V open drain. External pull-up required. See section 1.9.4 for functional description. See section 2.6.4 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
I2C1	**SCL1**	203	O	I2C1 clock	1.8 V open drain. External pull-up required. See section 1.9.4 for functional description. See section 2.6.4 for external circuit design-in.
	SDA1	204	I/O	I2C1 data	1.8 V open drain. External pull-up required. See section 1.9.4 for functional description. See section 2.6.4 for external circuit design-in.
SDIO	**SDIO_D0**	66	I/O	SDIO serial data [0]	SDIO interface for communication with Wi-Fi / Bluetooth. See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
	SDIO_D1	68	I/O	SDIO serial data [1]	SDIO interface for communication with Wi-Fi / Bluetooth. See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
	SDIO_D2	63	I/O	SDIO serial data [2]	SDIO interface for communication with Wi-Fi / Bluetooth. See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
	SDIO_D3	67	I/O	SDIO serial data [3]	SDIO interface for communication with Wi-Fi / Bluetooth. See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
	SDIO_CLK	64	O	SDIO serial clock	SDIO interface for communication with Wi-Fi / Bluetooth. See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
	SDIO_CMD	65	I/O	SDIO command	SDIO interface for communication with Wi-Fi / Bluetooth. See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
Ethernet	**V_ETH**	221	O	Ethernet Interface supply output	Ethernet SGMII interface supply output. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	ETH_RST_N	33	O	Ethernet PHY reset signal	SGMII: Ethernet PHY reset signal. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	SGMII_TX_N	36	O	Ethernet Transmit Minus	SGMII: Transmit minus signal See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	SGMII_TX_P	35	O	Ethernet Transmit Plus	SGMII: Transmit plus signal See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	SGMII_RX_P	39	I	Ethernet Receive Plus	SGMII: Receive plus signal. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	SGMII_RX_N	40	I	Ethernet Receive Minus	SGMII: Receive minus signal. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
	ETH_INTR	220	I	Ethernet Interrupt Input	Input for the detection of an interrupt event in the PHY. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	ETH_MDIO	222	I/O	Ethernet Management Data Input Output	Ethernet management data input / output. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
	ETH_MDC	223	O	Ethernet Management Data Clock	Ethernet management data clock output. See section 1.9.6 for functional description. See section 2.6.6 for external circuit design-in.
eMMC	**V_MMC**	210	O	Multi-Media Card Interface supply output	Embedded Multi-Media / SD Card memory supply. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	MMC_D0	214	I/O	Multi-Media Card Data [0]	Embedded Multi-Media / SD Card memory data [0]. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	MMC_D1	212	I/O	Multi-Media Card Data [1]	Embedded Multi-Media / SD Card memory data [1]. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	MMC_D2	217	I/O	Multi-Media Card Data [2]	Embedded Multi-Media / SD Card memory data [2]. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	MMC_D3	213	I/O	Multi-Media Card Data [3]	Embedded Multi-Media / SD Card memory data [3]. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	MMC_CMD	215	I/O	Multi-Media Card Command	Embedded Multi-Media / SD Card memory command. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	MMC_CLK	216	O	Multi-Media Card Clock	Embedded Multi-Media / SD Card memory clock. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	MMC_RST_N	211	O	Multi-Media Card Reset	Embedded Multi-Media / SD Card memory reset. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	MMC_CD_N	218	I	Multi-Media Card Detect	Embedded Multi-Media / SD Card detect. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
I2S0	**I2S_TXD**	51	O / O	I2S0 transmit data / PCM0 data out	I^2S (I2S0) transmit data output. Alternatively configurable as PCM0 data out by Open CPU or AT Command. See sections 1.11 for functional description. See sections 2.8 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
	I2S_RXD	53	I / I	I2S0 receive data / PCM0 data in	I²S (I2S0) receive data input. Alternatively configurable as PCM0 data in by Open CPU or AT Command. See sections 1.11 for functional description. See sections 2.8 for external circuit design-in.
	I2S_CLK	52	I/O / I/O	I2S0 clock / PCM0 clock	I²S (I2S0) serial clock. Alternatively configurable as PCM0 clock by Open CPU or AT Command. See sections 1.11 for functional description. See sections 2.8 for external circuit design-in.
	I2S_WA	50	I/O / I/O	I2S0 word alignment / PCM0 frame sync	I²S (I2S0) word alignment. Alternatively configurable as PCM0 frame sync by Open CPU or AT Command. See sections 1.11 for functional description. See sections 2.8 for external circuit design-in.
ADC	**ADC1**	240	I	ADC input	See section 1.12 for functional description. See section 2.9 for external circuit design-in.
	ADC2	239	I	ADC input	See section 1.12 for functional description. See section 2.9 for external circuit design-in.
GPIO	**GPIO1**	21	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.13 for functional description. See section 2.10 for external circuit design-in.
	GPIO2	22	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.13 for functional description. See section 2.10 for external circuit design-in.
	GPIO3	24	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. Configurable as External Interrupt by open CPU API. See section 1.13 for functional description. See section 2.10 for external circuit design-in.
	GPIO4	25	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. Configurable as SPI0 Chip Select 1 by open CPU API. See sections 1.13, 1.9.2.3 for functional description. See sections 2.10, 2.6.3 for external circuit design-in.
	GPIO5	60	I/O	GPIO	Used as the SIM card detection by default. Alternately settable as normal GPIO by open CPU API or AT commands. 1.8 V GPIO with alternatively configurable functions. See section 1.13 for functional description. See section 2.10 for external circuit design-in.
	GPIO6	61	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.13 for functional description. See section 2.10 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
	GPIO7	248	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.13 for functional description. See section 2.10 for external circuit design-in.
	GPIO8	247	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.13 for functional description. See section 2.10 for external circuit design-in.
Reserved	**RSVD**	1, 3, 6-10, 11-13, 29, 31,34, 37, 38, 41,42, 43, 45, 47-48, 77, 84, 91, 153-158, 163-167, 170-172, 175-178, 180-192, 194, 196-202, 205, 206-208, 224, 225, 227, 228, 230, 231, 233, 234, 236, 237, 242-246	N/A	Reserved pin	Leave unconnected. See sections 1.14 and 2.11

Table 4: TOBY-L3 series module pin definition, grouped by function

1.4 Operating modes

TOBY-L3 series modules have several operating modes. The operating modes are defined in Table 5 and described in detail in Table 6, provding general guidelines for operation.

General Status	Operating Mode	Definition
Power-down	Not-Powered Mode	**VCC** supply not present and the module is switched off.
	Power-Off mode	**VCC** supply within operating range and modules is switched off.
Booting Up	Booting-Mode	The module automatically enters booting-mode from power-off mode when it switched on
Download	Download-Mode	The modules in the download mode are ready to download the firmware and recovery the system.
Normal Operation	Sleep-Mode	The interfaces of the module are temporarily disabled or suspended in this mode, the system current consumption is reduced to save power.
	Active-Mode	The interfaces of the modules are enabled or not suspended in this mode.
	Connected-Mode	The module have registered the wireless network, the 4G/3G/2G data connection or incoming/outgoing voice call is in progress.

Table 5: TOBY-L3 series modules operating modes definition

Operating Mode	Description	Transition between operating modes
Not-Powered Mode	Module is switched off. Application interfaces are not accessible.	When **VCC** supply is removed, the module enters **not-powered** mode. When in **not-powered** mode, TOBY-L3 series modules enter **Power-Off mode** after applying **VCC** supply.
Power-Off Mode	Module is switched off: normal shutdown by an appropriate power-off event. Application interfaces are not accessible.	When the module is switched off by an appropriate power-off event, the module enters power-off mode from active-mode. When in power-off mode, TOBY-L3 series modules can be switched on by **PWR_ON** and enter the booting mode. If the pin **TX2** is pull up to high level when before switch on, the module enter the download mode. When in power-off mode, TOBY-L3 series enter the not-powered mode after removing **VCC** supply.
Booting-Mode	Module is booting up with application interfaces temporarily disabled or not used as the system is loading and not ready.	The modules automatically switch from **booting-mode** to **active-mode** when the system booting up finished and successful. If the booting procedure failed, the modules enter the **download mode** to recovery the system.
Download-Mode	Module is ready for download	The module automatically enters the emergency download mode when the pin **TX2** is pull up to the high level before switching on or the booting procedure is failed or in recovery situation.

		The modules switch from **active mode** to **download mode** before starting the firmware downloading procedure, once the firmware downloading is finished, the system reboot and enter **booting mode**.
Sleep-Mode	Module is switched on with application interfaces temporarily disabled or suspended: the module is temporarily not ready to communicate with an external device by means of the application interfaces as configured to reduce the current consumption. The module enters the low power idle-mode whenever possible if power saving is enabled by AT+UPSV command. Power saving configuration is not enabled by default: it can be enabled by the AT+UPSV command (see TOBY-L3 series AT commands manual [2]).	The modules automatically switch from active-mode to low power sleep-mode whenever possible if power saving is enabled. The module wakes up from low power idle-mode to active-mode in the following events: • Automatic periodic monitoring of the paging channel for the reception of the paging block sent by the base station according to network conditions • The connected USB host forces a remote wakeup of the module as USB device. • Automatic periodic enable of the UART interface to receive / send data, with AT+UPSV=1 • Data received on UART interface, with HW flow control disabled and power saving enabled • The module pin that configured as Wake-up function is triggered by the external device • The SIM card hot insertion or removal function is enabled and the SIM hot plug event is triggered • The GNSS data ready pin trigger the interruption
Active-Mode	Modules is switched on with application interfaces enabled or not suspended: the module is ready to communicate with an external device by means of the application interfaces unless power saving configuration is enabled by AT+UPSV command (see TOBY-L3 series AT commands manual [2]).	If power saving configuration is enabled by the AT+UPSV command, the module automatically switches from active to sleep-mode whenever possible and the module wakes up from sleep-mode to active-mode in the events listed above (see sleep-mode to active-mode transition description above). When a LTE/3G/2G data connection is initiated and connected, the module switches from active to connected-mode.
Connected-Mode	LTE/3G/2G data connection or incoming/ outgoing voice call is in progress. The module is prepared to accept data signals from an external device unless power saving configuration is enabled by AT+UPSV command (see TOBY-L3 series AT commands manual [2]).	When a data connection is initiated, the module enters connected-mode from active-mode. Connected-mode is suspended if LTE/3G/2G data connection and the voice call are not in progress, due to connected discontinuous reception and fast dormancy capabilities of the module and according to network environment settings and scenario. In such case, the module automatically switches from connected to active mode and then, if power saving configuration is enabled by the AT+UPSV command, the module automatically switches to idle-mode whenever possible. Vice-versa, the module wakes up from idle to active mode and then connected mode if LTE/3G/2G data connection is necessary. When a data connection is terminated, the module returns to the active-mode.

Table 6: TOBY-L3 series modules operating modes description

Figure 2 Describes the transition between the different operating modes.

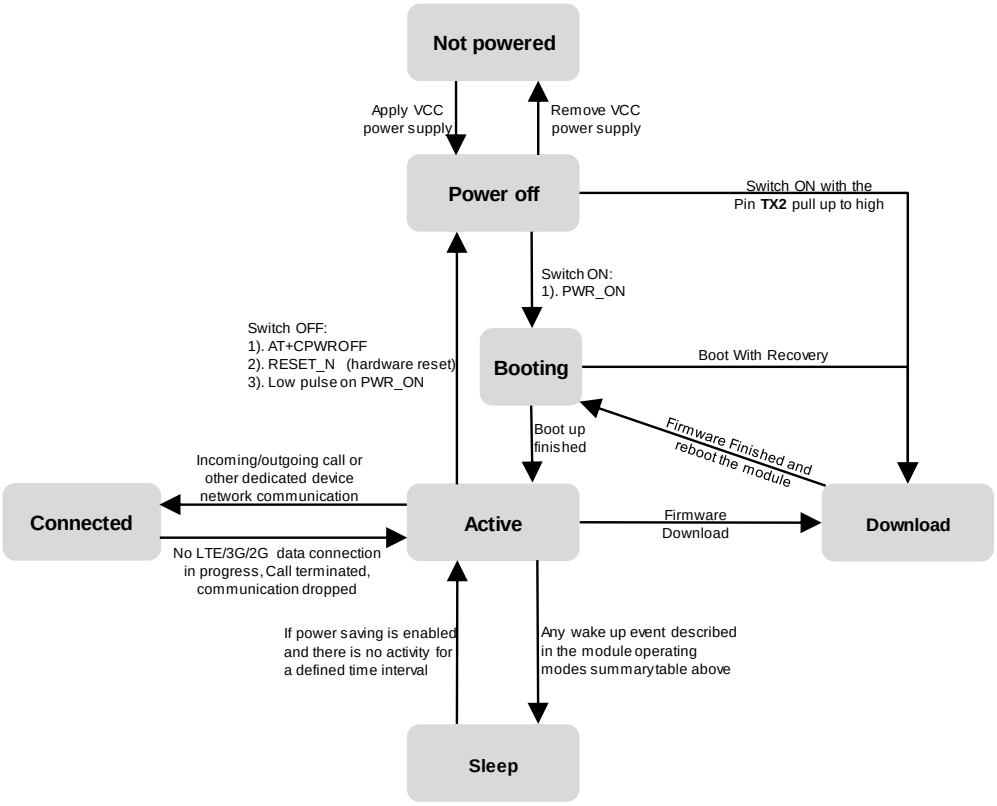

Figure 2: TOBY-L3 series operating modes transition

1.5 Supply interfaces

1.5.1 Module supply input (VCC)

The modules must be supplied via the three **VCC** pins that represent the module power supply input.

The **VCC** pins are internally connected to the RF power amplifier and to the integrated Power Management Unit: all supply voltages needed by the module are generated from the **VCC** supply by integrated voltage regulators, **V_INT** generic digital interfaces supply, **VSIM** SIM card supply, **V_ETH** SGMII interface supply, **V_MMC** eMMC interface supply, and any other internal rail.

During operation, the current drawn by the TOBY-L3 series modules through the **VCC** pins can vary by several orders of magnitude. This ranges from the pulse of current consumption during GSM transmitting bursts at maximum power level in connected mode (as described in section 1.5.1.2) to the low current consumption during low power idle mode with power saving enabled (as described in section 1.5.1.5).

Figure 3 provides a simplified block diagram of the TOBY-L3 series modules' internal VCC supply routing.

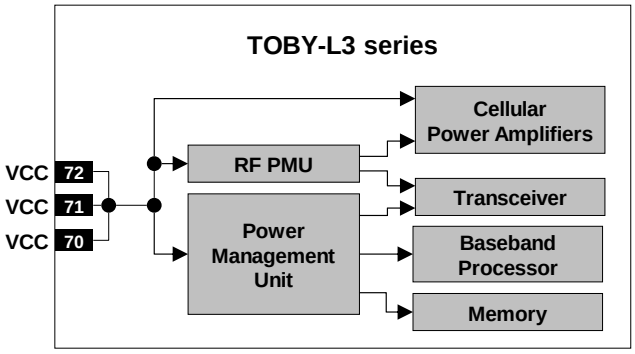

Figure 3: TOBY-L3 series modules' internal VCC supply routing simplified block diagram

1.5.1.1 VCC supply requirements

Table 7 summarizes the requirements for the **VCC** modules supply. See section 2.2.1 for suggestions on how to properly design a **VCC** supply circuit compliant with the requirements listed in Table 7.

⚠ The supply circuit affects the RF compliance of the device integrating TOBY-L3 series modules with applicable required certification schemes as well as antenna circuit design. Compliance is guaranteed if the requirements summarized in Table 7 are fulfilled.

Item	Requirement	Remark
VCC nominal voltage	Within **VCC** normal operating range: 3.30 V min. / 4.20 V max.	RF performance is guaranteed when **VCC** PA voltage is inside the normal operating range limits. RF performance may be affected when **VCC** PA voltage is outside the normal operating range limits, though the module is still fully

		functional until the **VCC** voltage is inside the extended operating range limits.
VCC average current	Support with adequate margin the highest averaged **VCC** current consumption value in connected mode conditions	The maximum average current consumption can be greater than the specified value according to the actual antenna mismatching, temperature and supply voltage. Sections 1.5.1.2, 1.5.1.3 and 1.5.1.4 describe the current consumption profiles in 2G, 3G and LTE connected modes.
VCC peak current	Support with margin the highest peak **VCC** current consumption value in connected mode conditions	The specified maximum peak of current consumption occurs during the GSM single transmit slot in 850/900 MHz connected mode, in case of a mismatched antenna. Section 1.5.1.2 describes 2G Tx peak/pulse current.
VCC voltage drop during 2G Tx slots	Lower than 400 mV	Supply voltage drop values greater than recommended during 2G TDMA transmission slots directly affect the RF compliance with the applicable certification schemes. Figure 5 describes supply voltage drop during 2G Tx slots.
VCC voltage ripple during 2G/3G/LTE Tx	Noise in the supply must be minimized	High supply voltage ripple values during LTE/3G/2G RF transmissions in connected mode directly affect the RF compliance with applicable certification schemes. Figure 5 describes supply voltage ripple during RF Tx.
VCC under/over-shoot at start/end of Tx slots	Absent or at least minimized	Supply voltage under-shoot or over-shoot at the start or the end of 2G TDMA transmission slots directly affect the RF compliance with the applicable certification schemes. Figure 5 describes supply voltage under/over-shoot

Table 7: Summary of VCC modules supply requirements

1.5.1.2 VCC current consumption in 2G connected mode

When a GSM call is established, the **VCC** module current consumption is determined by the current consumption profile typical of the GSM transmitting and receiving bursts.

The peak of current consumption during a transmission slot is strictly dependent on the RF transmitted power, which is regulated by the network (the current base station). The transmitted power in the transmit slot is also the more relevant factor for determining the average current consumption.

If the module is transmitting in 2G single-slot mode in the 850 or 900 MHz bands, at the maximum RF power level (approximately 2 W or 33 dBm in the allocated transmit slot/burst) the current consumption can reach an upper peak for 576.9 µs (width of the transmit slot/burst) with a periodicity of 4.615 ms (width of 1 frame = 8 slots/burst), so with a 1/8 duty cycle according to GSM TDMA (Time Division Multiple Access).

If the module is transmitting in 2G single-slot mode in the 1800 or 1900 MHz bands, the current consumption figures are considerably lower than the one in the low bands, due to the 3GPP transmitter output power specifications.

During a GSM call, current consumption is not so significantly high in receiving or in monitor bursts and is low in the inactive unused bursts.

Figure 4 shows an example of the module current consumption profile versus time in 2G single-slot mode.

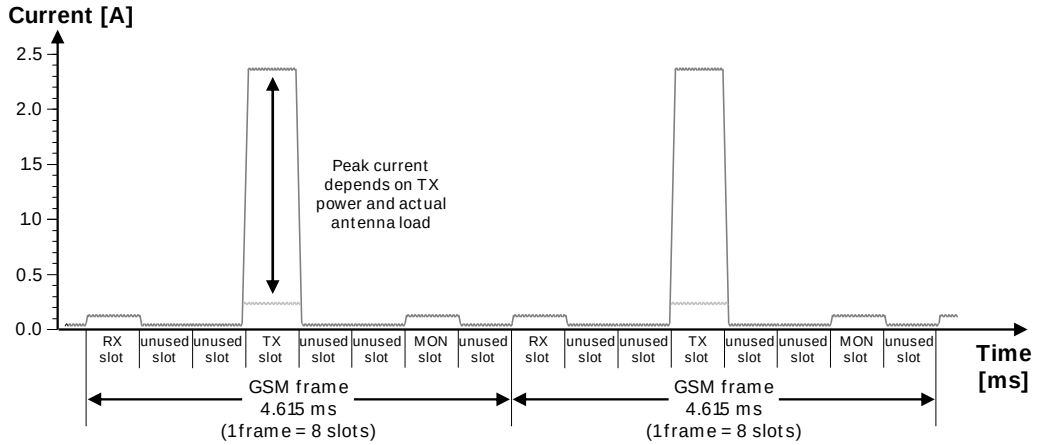

Figure 4: VCC current consumption profile versus time during a 2G single-slot call (1 TX slot, 1 RX slot)

Figure 5 illustrates **VCC** voltage profile versus time during a 2G single-slot call, according to the relative **VCC** current consumption profile illustrated in Figure 4.

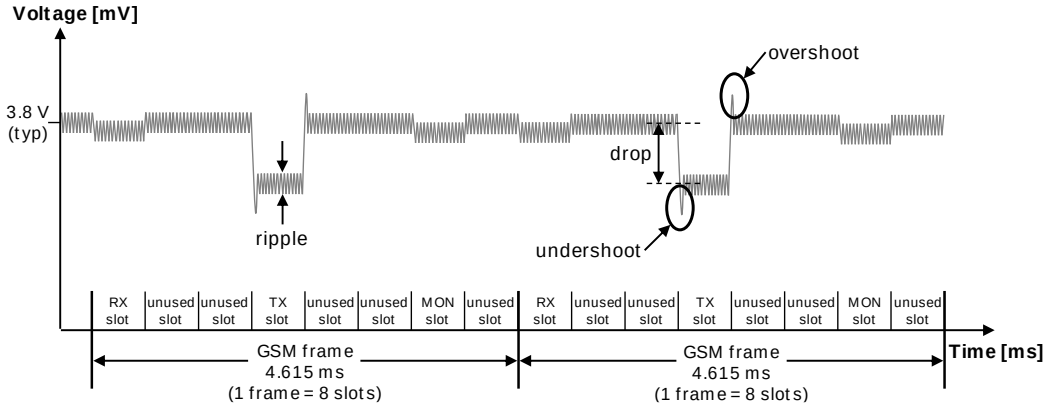

Figure 5: VCC voltage profile versus time during a 2G single-slot call (1 TX slot, 1 RX slot)

When a GPRS connection is established, more than one slot can be used to transmit and/or more than one slot can be used to receive. The transmitted power depends on the network conditions, which set the peak current consumption, but following the 3GPP specifications, the maximum Tx RF power is reduced if more than one slot is used to transmit, so the maximum peak of current is not as high as can be the case with a 2G single-slot call.

If the module transmits in GPRS class 12 in the 850 or 900 MHz bands, at the maximum RF power control level, the current consumption can reach a quite high peak but lower than the one achievable in 2G single-slot mode. This happens for 2.307 ms (width of the 4 transmit slots/bursts) with a periodicity of 4.615 ms (width of 1 frame = 8 slots/bursts), so with a 1/2 duty cycle, according to 2G TDMA.

If the module is in GPRS connected mode in the 1800 or 1900 MHz bands, the current consumption figures are quite less high than the one in the low bands, due to 3GPP transmitter output power specifications.

Figure 6 reports the current consumption profiles in GPRS class 12 connected mode, in the 850 or 900 MHz bands, with 4 slots used to transmit and 1 slot used to receive.

It must be noted that the actual current consumption of the module in 2G connected mode depends also on the specific concurrent activities performed by the integrated CPU, beside the actual Tx power and antenna load.

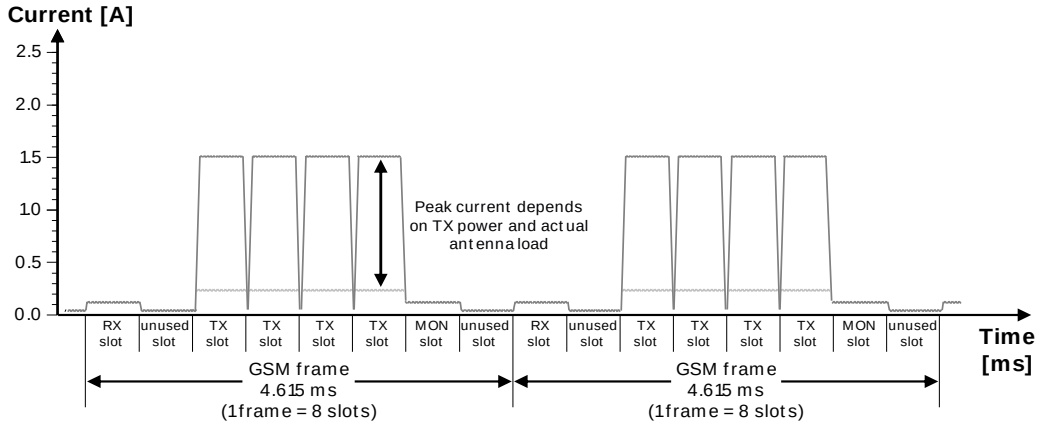

Figure 6: VCC current consumption profile during a 2G GPRS/EDGE multi-slot connection (4 TX slots, 1 RX slot)

For EDGE connections, the VCC current consumption profile is very similar to the GPRS current profile, so the image shown in Figure 6, representing the current consumption profile in GPRS class 12 connected mode, is valid for the EDGE class 12 connected mode as well.

1.5.1.3 VCC current consumption in 3G connected mode

During a 3G connection, the module can transmit and receive continuously due to the Frequency Division Duplex (FDD) mode of operation with the Wideband Code Division Multiple Access (WCDMA).

The current consumption depends on output RF power, which is always regulated by the network (the current base station) sending power control commands to the module. These power control commands are logically divided into a slot of 666 µs, so the rate of power change can reach a maximum rate of 1.5 kHz.

There are no high current peaks as in the 2G connection, since transmission and reception are continuously enabled due to FDD WCDMA implemented in the 3G that differs from the TDMA implemented in the 2G case.

In the worst case scenario, corresponding to a continuous transmission and reception at maximum output power (approximately 250 mW or 24 dBm), the average current drawn by the module at the VCC pins is considerable. At the lowest output RF power (approximately 0.01 µW or –50 dBm), the current drawn by the internal power amplifier is strongly reduced. The total current drawn by the module at the VCC pins is due to baseband processing and transceiver activity.

Figure 7 shows an example of the current consumption profile of the module in 3G WCDMA/DC-HSPA+ continuous transmission mode.

It must be noted that the actual current consumption of the module in 3G connected mode depends also on the specific concurrent activities performed by the integrated CPU, beside the actual Tx power and antenna load.

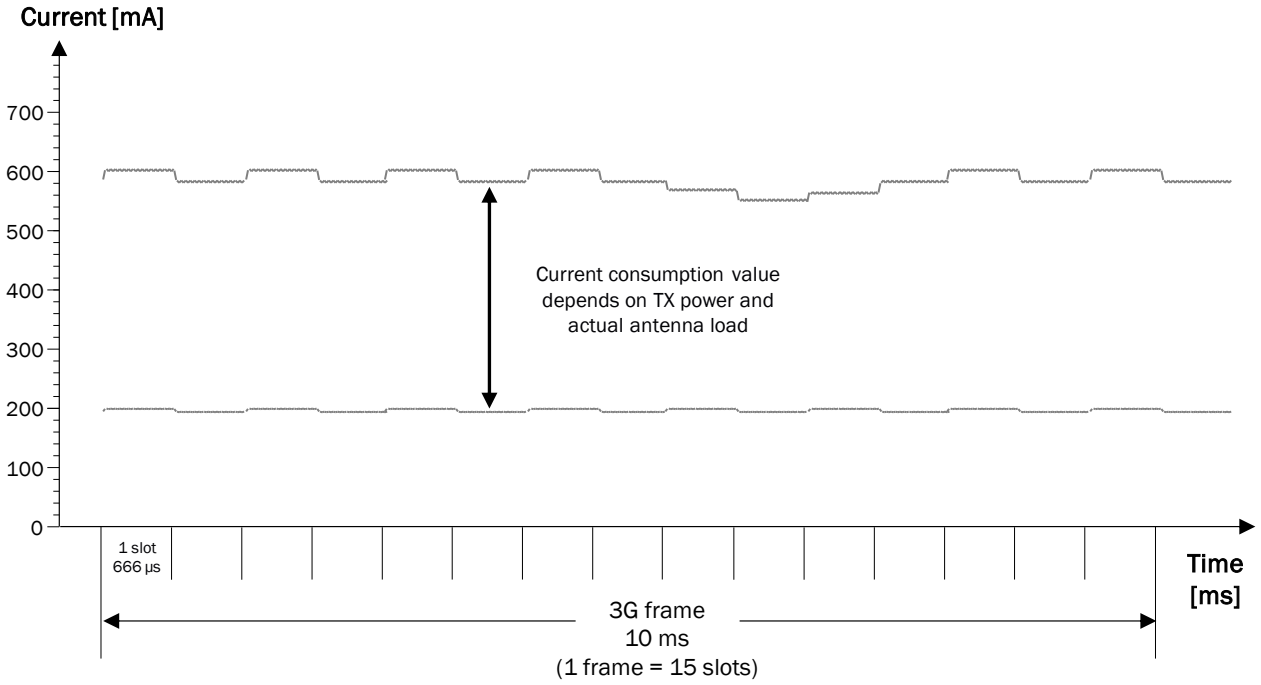

Figure 7: VCC current consumption profile versus time during a 3G connection (TX and RX continuously enabled)

1.5.1.4 VCC current consumption in LTE connected mode

During an LTE connection, the module can transmit and receive continuously due to the Frequency Division Duplex (FDD) mode of operation used in LTE radio access technology.

The current consumption depends on output RF power, which is always regulated by the network (the current base station) sending power control commands to the module. These power control commands are logically divided into a slot of 0.5 ms (time length of one Resource Block), thus the rate of power change can reach a maximum rate of 2 kHz.

The current consumption profile is similar to that in 3G radio access technology. Unlike the 2G connection mode, which uses the TDMA mode of operation, there are no high current peaks since transmission and reception are continuously enabled in FDD.

In the worst case scenario, corresponding to a continuous transmission and reception at maximum output power (approximately 250 mW or 24 dBm), the average current drawn by the module at the VCC pins is considerable. At the lowest output RF power (approximately 0.1 µW or –40 dBm), the current drawn by the internal power amplifier is greatly reduced and the total current drawn by the module at the VCC pins is due to baseband processing and transceiver activity.

Figure 8 shows an example of the module current consumption profile versus time in LTE connected mode.

It must be noted that the actual current consumption of the module in LTE connected mode depends also on the specific concurrent activities performed by the integrated CPU, beside the actual Tx power and antenna load.

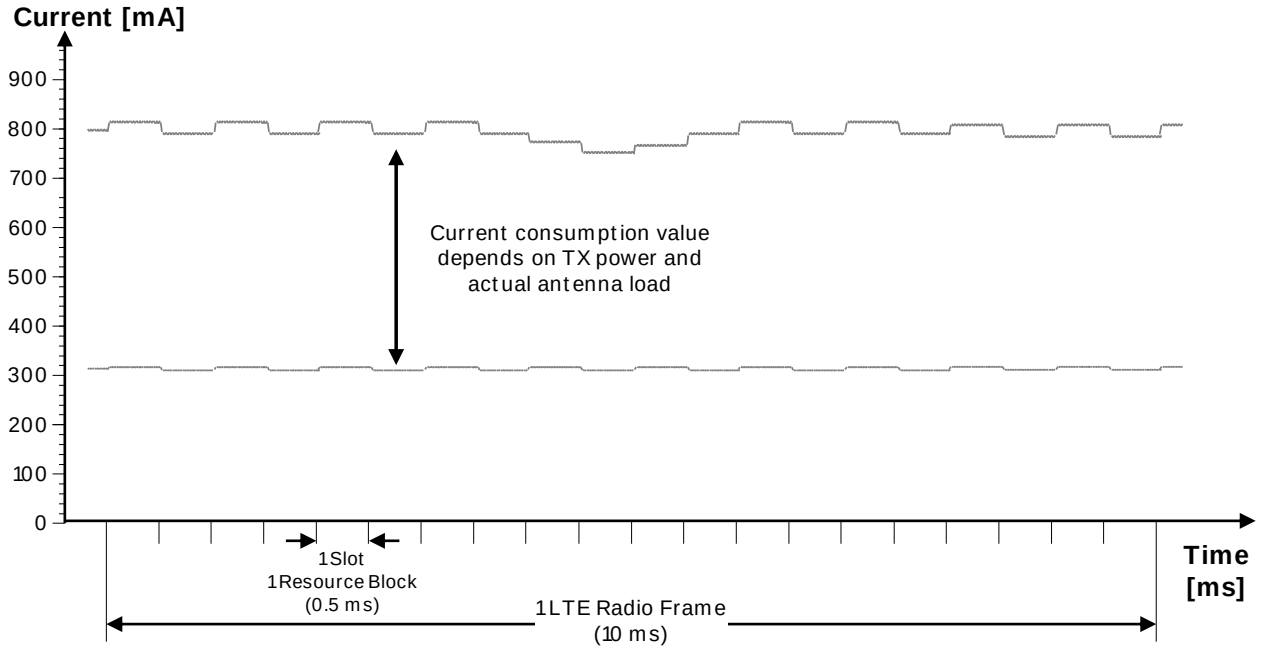

Figure 8: VCC current consumption profile versus time during LTE connection (TX and RX continuously enabled)

1.5.1.5 VCC current consumption in cyclic low power idle mode / active mode

When both the USB and the Ethernet SGMII interfaces are either suspended or unconnected, the module enters low power idle mode whenever possible by default on the "50" product version, or if the power saving configuration is enabled by the AT+UPSV command on the "50" product version (see the TOBY-L3 series AT Commands Manual [2]), or if power state manager is enabled on the "00" product version.

When the module is registered or attached to a network, the module must periodically monitor the paging channel of the current base station (paging block reception), in accordance with the 2G/3G/LTE system requirements, even if connected mode is not enabled by the application. When the module monitors the paging channel, it wakes up to the active mode to then enable the reception of the paging block. In between, the module switches to low power idle mode. This is known as discontinuous reception (DRX).

The time period between two paging block receptions is defined by the network. This is the paging period parameter, fixed by the base station through the broadcast channel sent to all users on the same serving cell:

- In 2G, the paging period can vary from 470.8 ms (DRX = 2, length of 2 x 51 2G frames = 2 x 51 x 4.615 ms) up to 2118.4 ms (DRX = 9, length of 9 x 51 2G frames = 9 x 51 x 4.615 ms)
- In 3G, the paging period can vary from 640 ms (DRX = 6, i.e. length of 2^6 3G frames = 64 x 10 ms) up to 5120 ms (DRX = 9, length of 2^9 3G frames = 512 x 10 ms).

- In LTE, the paging period can vary from 320 ms (DRX = 5, i.e. length of 2^5 LTE frames = 32 x 10 ms) up to 2560 ms (DRX = 8, length of 2^8 LTE frames = 256 x 10 ms).

Figure 9 illustrates a typical example of the module current consumption profile when power saving is enabled. The module is registered with the network, automatically enters the low power idle mode and periodically wakes up to active mode to monitor the paging channel for the paging block reception.

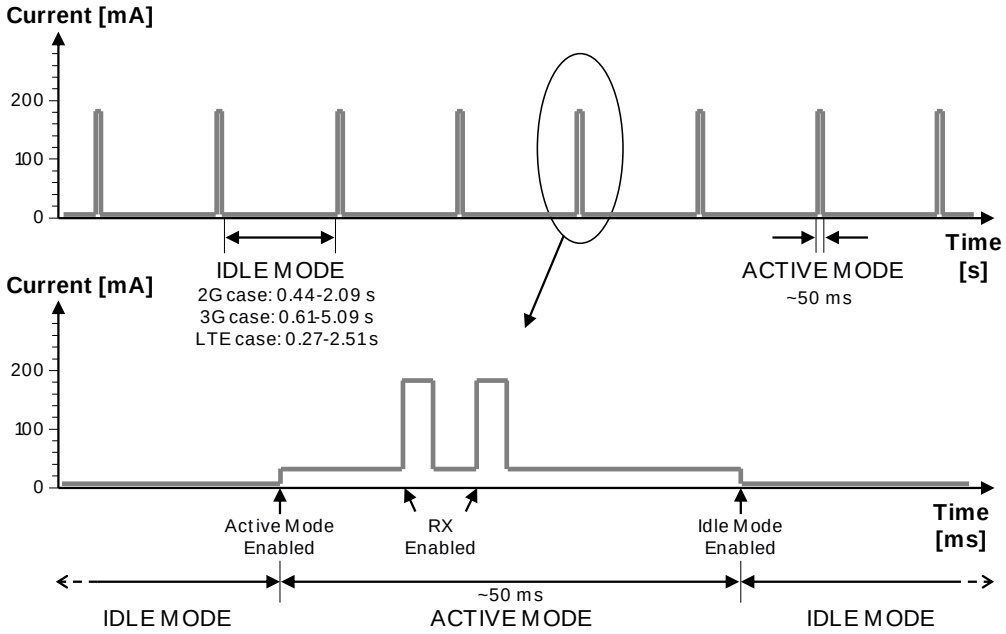

Figure 9: VCC current consumption profile with low power mode enabled and module registered with the network: the module is in low-power idle mode and periodically wakes up to active mode to monitor the paging channel for paging block reception

1.5.1.6 VCC current consumption in fixed active mode

When the USB or the Ethernet SGMII interface is not suspended, the module stays in active mode, ready to perform its designed operations.

The module processor core is activated during idle mode, and the 19.2 MHz system clock frequency is used. It would draw more current during the paging period than that in the power saving mode.

Figure 10 illustrates a typical example of the module current consumption profile when power saving is disabled. In such a case, the module is registered with the network and while active mode is maintained, the receiver is periodically activated to monitor the paging channel for paging block reception.

It must be noted that the actual current consumption of the module in active mode depends on the specific concurrent activities performed by the integrated CPU.

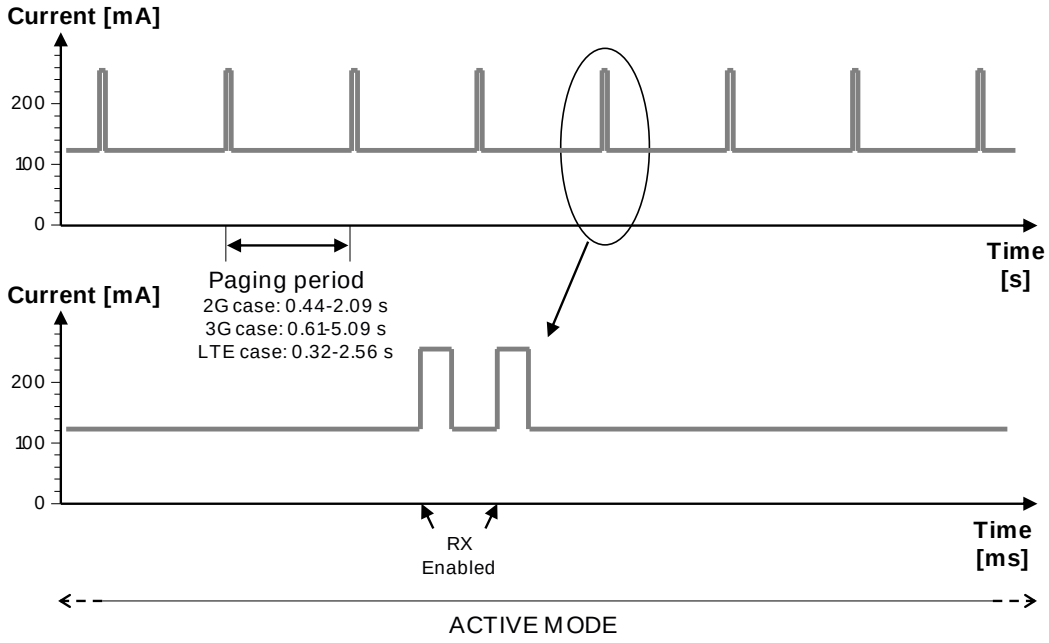

Figure 10: VCC current consumption profile with low power mode disabled and module registered with the network: active mode is always held and the receiver is periodically activated to monitor the paging channel for paging block reception

1.5.2 Generic digital interfaces supply output (V_INT)

The **V_INT** output pin of the TOBY-L3 series modules is connected to an internal 1.8 V supply. This supply is internally generated by a switching step-down regulator integrated in the Power Management Unit and it is internally used to source the generic digital I/O interfaces of the cellular module, as shown in Figure 11. The output of this regulator is enabled when the module is switched on and it is disabled when the module is switched off.

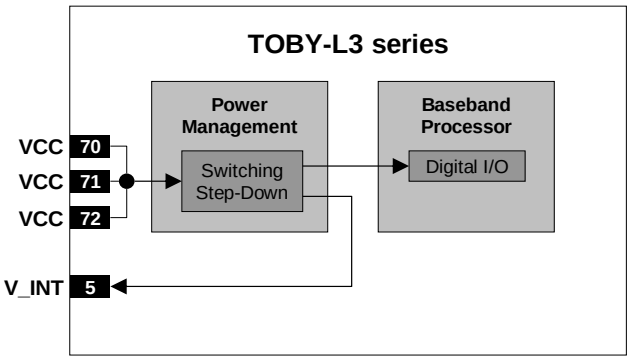

Figure 11: TOBY-L3 series generic digital interfaces supply output (V_INT) simplified block diagram

1.6 System function interfaces

1.6.1 Module power-on

TOBY-L3 series modules can be switched on in the following way:

- Low pulse on the **PWR_ON** pin, which is normally set high by an internal pull-up, for a valid time period, when the applied **VCC** voltage is stable at its nominal value within normal operating range.

As shown in Figure 12, the TOBY-L3 series **PWR_ON** input is equipped with an internal active pull-up resistor to an internal 1.3 V supply rail: the **PWR_ON** input voltage thresholds are different from the other generic digital interfaces, and the line should be driven by an open drain, by an open collector or by a contact switch, without an external pull-up resistor.

Detailed electrical characteristics and specifications are described in TOBY-L3 series Data Sheet [1].

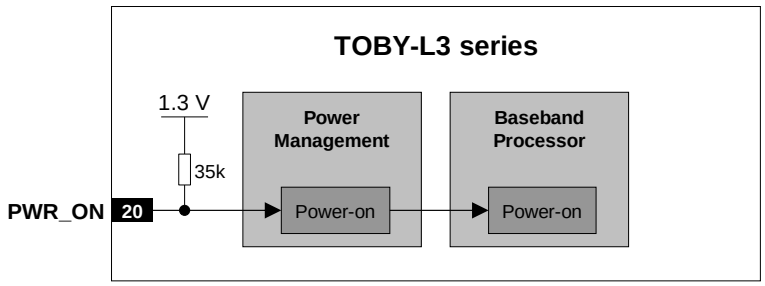

Figure 12: TOBY-L3 series PWR_ON input description

☞ TOBY-L3 series modules do not switch on by applying the **VCC** supply only: a low pulse must be forced on the **PWR_ON** pin when the **VCC** voltage is stable at its nominal value within the valid operating range.

Figure 13 shows the module power-on sequence, describing the following phases:

- The **VCC** module supply is stable at its nominal value within the normal operating range
- The **PWR_ON** input pin is set low for a valid time period, representing the switch-on event.
- All the generic digital pins of the modules are tri-stated until the switch-on of their supply source (**V_INT**): any external signal connected to the generic digital pins must be tri-stated or set low at least until the activation of the **V_INT** supply output to avoid latch-up of circuits and allow a clean boot of the module.
- The **V_INT** generic digital interfaces supply output is enabled by the integrated power management unit.
- The **RESET_N** line rises suddenly to the high logic level due to internal pull-up to **V_INT**.
- The internal reset signal is held low by the integrated power management unit: the baseband processor core and all the digital pins of the modules are held in reset state.
- When the internal reset signal is released, any digital pin is set in the correct sequence from the reset state to the default operational configured state. The duration of this pins' configuration phase differs within the generic digital interfaces and the USB interface due to host / device enumeration timings (see section 1.9.1).
- The module sends the "+AT: READY" URC notification over the AT communication interface (USB) when it is ready to receive AT commands
- The module is fully ready to operate after all interfaces are configured.

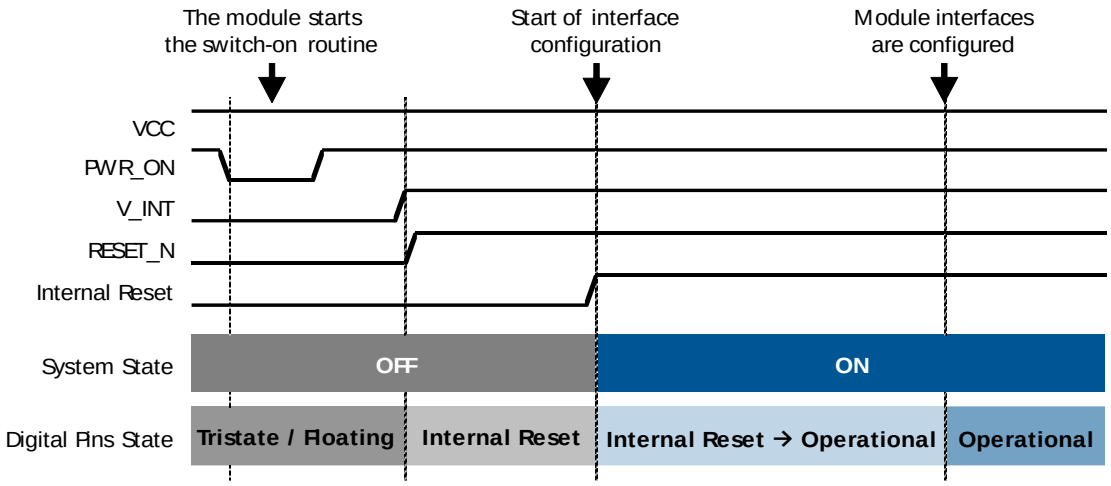

Figure 13: TOBY-L3 series power-on sequence description

☞ The Internal Reset signal is not available on a module pin, but it is recommended to monitor:

- the **V_INT** pin, to sense the start of the module switch-on sequence
- the "+AT: READY" URC notification, to sense when the module is ready to operate

☞ Before the switch-on of the generic digital interface supply (**V_INT**) of the module, no voltage driven by an external application should be applied to any generic digital interface of the module.

☞ Before the TOBY-L3 series module is fully ready to operate, the host application processor should not send any AT command over the AT communication interface (USB) of the module.

☞ The duration of the TOBY-L3 series modules' switch-on routine can largely vary depending on the application / network settings and any concurrent module activities.

⚠ It is highly recommended to avoid an abrupt removal of the **VCC** supply and/or performing an abrupt emergency shutdown procedure during TOBY-L3 series modules' switch-on routine.

1.6.2 Module power-off

TOBY-L3 series can be properly switched off by:

- +CPWROFF AT command (see the TOBY-L3 series AT Commands Manual [2])
- Power off command on the Linux shell[3]
- Low pulse on the **PWR_ON** pin, which is normally set high by an internal pull-up, for a valid time period (see the TOBY-L3 series Data Sheet [1], module normal graceful switch-off: the internal switch-off sequence of the module starts when the external application releases the **PWR_ON** line from the low logic level, after that it has been set low for an appropriate time period.

The methods listed above represent the appropriate normal switch-off events, triggering an appropriate normal switch-off procedure of the module: the current parameter settings are saved in the module's non-volatile memory and a clean network detach is performed.

An abrupt under-voltage shutdown occurs on TOBY-L3 series modules when the **VCC** module supply is removed. If this occurs, it is not possible to perform the storing of the current parameter settings in the module's non-volatile memory or to perform a clean network detach.

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply during TOBY-L3 series modules normal operations: the switch-off routine must be started by an appropriate switch-off event (see above), and then a suitable **VCC** supply must be held at least until the end of the modules' internal switch-off sequence, which occurs when the generic digital interfaces supply output (**V_INT**) is switched off by the module.

☞ If the module does not provide a reply to a specific AT command after a time period longer than the one defined in the TOBY-L3 series AT Commands Manual [2], than the reset procedure by toggling the **RESET_N** line (see section 1.6.3) is preferred.

An over-temperature shutdown occurs on TOBY-L3 series modules when the temperature measured within the cellular module reaches a critical range.

[3] Not supported by "0x" product feature versions

Figure 14 describes the TOBY-L3 series modules' proper normal switch-off sequence started by means of the +CPWROFF AT command, allowing storage of current parameter settings in module's non-volatile memory and a clean network detach, with the following phases

- The +CPWROFF AT command is sent to the module by the external application: the module starts the switch-off routine
- Then, the module replies OK on the AT interface: the switch-off routine is in progress
- At the end of the switch-off routine, all the digital pins are tri-stated and all the internal voltage regulators are turned off, including the generic digital interfaces supply (**V_INT**).
- Then, the module remains in power-off mode as long as a switch-on event does not occur (i.e. applying a suitable low level pulse to the **PWR_ON** input pin), and enters not-powered mode if the supply is removed from the **VCC** pins.

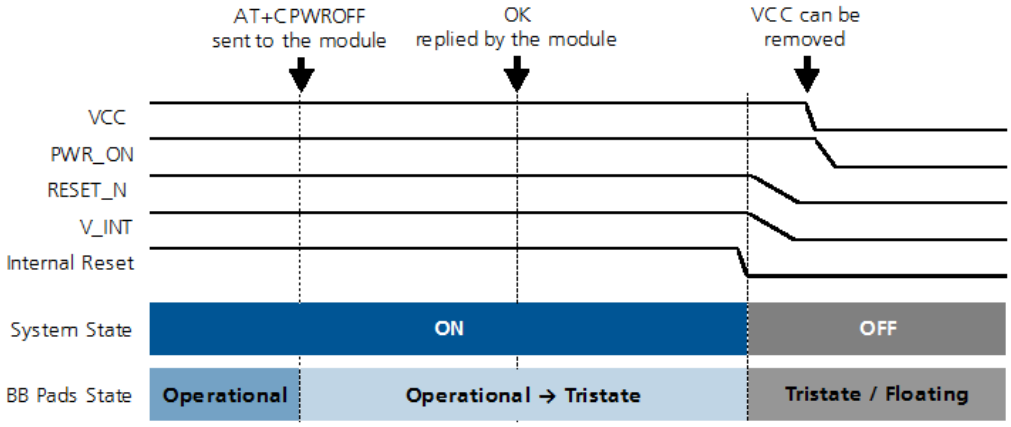

Figure 14: Description of TOBY-L3 series power-off sequence, as triggered by +CPWROFF AT command

☞ The Internal Reset signal is not available on a module pin, but it is highly recommended to monitor the **V_INT** pin to sense the end of the switch-off sequence.

⚠ **VCC** supply can be removed only after **V_INT** goes low: an abrupt removal of the **VCC** supply during TOBY-L3 series modules normal operations may lead to an unrecoverable faulty state!

☞ The duration of each phase in the TOBY-L3 series modules' switch-off routines can largely vary depending on the application / network settings and the concurrent module activities.

Figure 15 describes the TOBY-L3 series modules' proper normal switch-off sequence started by means of the **PWR_ON** input pin, allowing storage of current parameter settings in the module's non-volatile memory and a clean network detach, with the following phases

- A low pulse with the appropriate time duration is applied at the **PWR_ON** input (see TOBY-L3 series Data Sheet [1], normal graceful switch-off), which is normally set high by an internal pull-up: the module starts the switch-off routine when the **PWR_ON** signal is released from the low logical level.
- At the end of the switch-off routine, all the digital pins are tri-stated and all the internal voltage regulators are turned off, including the generic digital interfaces supply (**V_INT**).
- Then, the module remains in power-off mode as long as a switch-on event does not occur (i.e. applying a suitable low level pulse to the **PWR_ON** input pin), and enters not-powered mode if the supply is removed from the **VCC** pins.

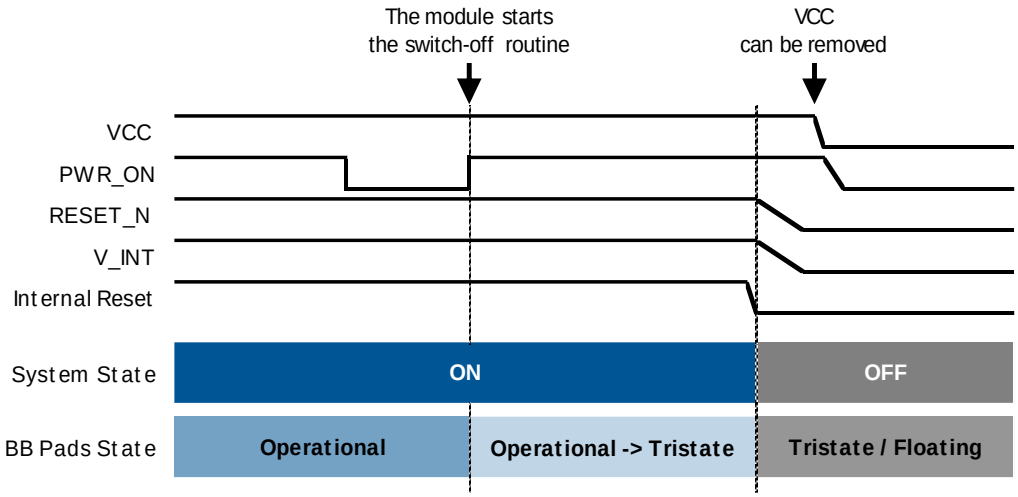

Figure 15: Description of TOBY-L3 series power-off sequence, as triggered by PWR_ON input pin

☞ The Internal Reset signal is not available on a module pin, but it is highly recommended to monitor the **V_INT** pin to sense the end of the switch-off sequence.

⚠ **VCC** supply can be removed only after **V_INT** goes low: an abrupt removal of the **VCC** supply during TOBY-L3 series modules normal operations may lead to an unrecoverable faulty state!

☞ The duration of each phase in the TOBY-L3 series modules' switch-off routines can largely vary depending on the application / network settings and the concurrent module activities.

1.6.3 Module reset

TOBY-L3 series modules can be properly reset (rebooted) by:

- +CFUN AT command (see the TOBY-L3 series AT Commands Manual [2])
- reboot command on the Linux shell[4]

The methods listed above represent appropriate reset (reboot) events, triggering an appropriate "internal" or "software" reset of the module: the current parameter settings are saved in the module's non-volatile memory and a clean network detach is performed.

An abrupt hardware reset occurs on TOBY-L3 series modules when a low level is applied on the **RESET_N** input pin. In this case, the current parameter settings are not saved in the module's non-volatile memory and a clean network detach is not performed.

☞ It is recommended to avoid an abrupt hardware reset of the module by forcing a low level on the **RESET_N** input during modules normal operation: the **RESET_N** line should be set low only if reset via AT command or Linux shell fails, or if the module does not provide a reply to a specific AT command after a time period longer than the one defined in the TOBY-L3 series AT Commands Manual [2].

As shown in Figure 16, the **RESET_N** input pins are equipped with an internal pull-up to the internally generated voltage supply. For more electrical characteristics details see the TOBY-L3 series Data Sheet [1].

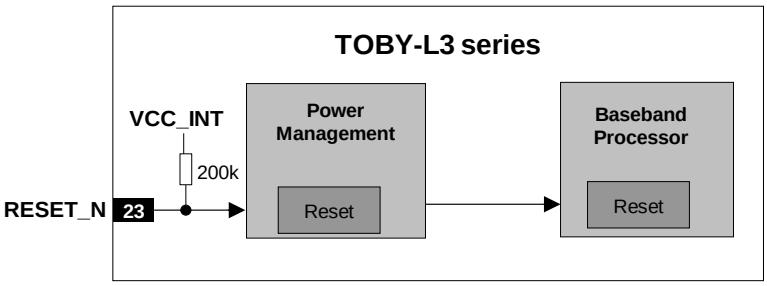

Figure 16: TOBY-L3 series RESET_N input equivalent circuit description

1.6.4 Module / host configuration selection

☞ Host Select pins are not supported by the "0x" product feature version.

TOBY-L3 series modules include two 1.8 V digital pins (**HOST_SELECT0**, **HOST_SELECT1**), which can be configured for External Interrupt detection or as GPIO by means of the open CPU API.

[4] Not supported by "0x" product feature version

1.7 Antenna interfaces

1.7.1 Antenna RF interfaces (ANT1 / ANT2)

TOBY-L3 series modules provide two RF interfaces for connecting the external antennas for 4G/3G/2G network:

- **ANT1** represents the primary RF input/output for transmission and reception of RF signals.
  ANT1 pin has a nominal characteristic impedance of 50 Ω and must be connected to the primary Tx / Rx antenna through a 50 Ω transmission line to allow clean RF transmission and reception.
- **ANT2** represents the secondary RF input for reception of RF signals in MIMO and Rx diversity configurations supported by TOBY-L3 series modules as a required feature for LTE category 4 UEs.
  ANT2 pin has a nominal characteristic impedance of 50 Ω and must be connected to the secondary Rx antenna through a 50 Ω transmission line to allow clean RF reception.

1.7.1.1 Antenna RF interfaces (ANT1 / ANT2) requirements

Table 8, Table 9 and Table 10 summarize the RF interfaces' requirements. See section 2.4.1 for suggestions on how to correctly design antennas circuits compliant with these requirements.

⚠ The antenna circuits affect the RF compliance of the device integrating TOBY-L3 series modules with the applicable required certification schemes (see section 4). Compliance is guaranteed if the antenna RF interfaces requirements summarized in Table 8, Table 9 and Table 10 are fulfilled.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the **ANT1** port.
Frequency Range	See the TOBY-L3 series Data Sheet [1]	The required frequency range of the antenna connected to the **ANT1** port depends on the operating bands of the used cellular module and the used mobile network.
Return Loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The Return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the antenna RF connection matches the 50 Ω characteristic impedance of the **ANT1** port. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of the **ANT1** port over the operating frequency range, reducing as much as possible the amount of reflected power.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to antenna input: the efficiency is a measure of how well an antenna receives or transmits. The radiation efficiency of the antenna connected to the **ANT1** port needs to be enough high over the operating frequency range to comply with the Over-The-Air radiated performance requirements, as Total

Item	Requirements	Remarks
		Radiated Power (TRP) and the Total Isotropic Sensitivity (TIS), specified by applicable related certification schemes.
Maximum Gain	According to radiation exposure limits	The power gain of an antenna is the radiation efficiency multiplied by the directivity: the gain describes how much power is transmitted in the direction of peak radiation to that of an isotropic source. The maximum gain of the antenna connected to **ANT1** port must not exceed the herein stated value to comply with regulatory agencies' radiation exposure limits.
Input Power	> 33 dBm (> 2 W)	The antenna connected to the **ANT1** port must support with adequate margin the maximum power transmitted by the modules.

Table 8: Summary of primary Tx/Rx antenna RF interface (ANT1) requirements

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the **ANT2** port.
Frequency Range	See the TOBY-L3 series Data Sheet [1]	The required frequency range of the antennas connected to **ANT2** port depends on the operating bands of the used cellular module and the used mobile network.
Return Loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The Return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the antenna RF connection matches the 50 Ω characteristic impedance of the **ANT2** port. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of the **ANT2** port over the operating frequency range, reducing as much as possible the amount of reflected power.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to antenna input: the efficiency is a measure of how well an antenna receives or transmits. The radiation efficiency of the antenna connected to the **ANT2** port needs to be enough high over the operating frequency range to comply with the Over-The-Air radiated performance requirements, as the TIS, specified by applicable related certification schemes.

Table 9: Summary of secondary Rx antenna RF interface (ANT2) requirements

Item	Requirements	Remarks
Efficiency imbalance	< 0.5 dB recommended < 1.0 dB acceptable	The radiation efficiency imbalance is the ratio of the primary (**ANT1**) antenna efficiency to the secondary (**ANT2**) antenna efficiency: the efficiency imbalance is a measure of how much better an antenna receives or transmits compared to the other antenna.

		The radiation efficiency of the secondary antenna needs to be roughly the same as the radiation efficiency of the primary antenna for good RF performance.
Envelope Correlation Coefficient	< 0.4 recommended < 0.5 acceptable	The Envelope Correlation Coefficient (ECC) between the primary (**ANT1**) and the secondary (**ANT2**) antenna is an indicator of 3D radiation pattern similarity between the two antennas: low ECC results from antenna patterns with radiation lobes in different directions. The ECC between the primary and secondary antennas needs to be low enough to comply with the radiated performance requirements specified by related certification schemes.
Isolation	> 15 dB recommended > 10 dB acceptable	The antenna to antenna isolation is the loss between the primary (**ANT1**) and the secondary (**ANT2**) antenna: high isolation results from low coupled antennas. The isolation between primary and secondary antenna needs to be high for good RF performance.

Table 10: Summary of primary (ANT1) and secondary (ANT2) antennas relationship requirements

1.7.2 Antenna detection interface (ANT_DET)

The antenna detection is based on ADC measurement. The **ANT_DET** pin is an Analog to Digital Converter (ADC) provided to sense the antennas(**ANT1**/**ANT2**) presence.

The antenna detection function provided by **ANT_DET** pin is an optional feature that can be implemented if the application requires it. The **ANT_DET** pin generates a DC current and measures the resulting DC voltage, thus determining the resistance from the antenna connector provided on the application board to GND. So the requirements to achieve antenna detection functionality are the following:

- an RF antenna assembly with a built-in resistor (diagnostic circuit) must be used
- an antenna detection circuit must be implemented on the application board

See section 2.4.2 for the antenna detection circuit on the application board and the diagnostic circuit in the antenna assembly design-in guidelines.

1.8 SIM interfaces

1.8.1 SIM interfaces

TOBY-L3 series modules provide one SIM interfaces for the direct connection of external SIM cards/chips:

- SIM0 interface (**VSIM**, **SIM_IO**, **SIM_CLK**, **SIM_RST** pins)

Both 1.8 V and 3 V SIM types are supported by the SIM interfaces. Activation and deactivation with an automatic voltage switch from 1.8 V to 3 V is implemented, according to ISO-IEC 7816-3 specifications.

High-speed SIM/ME interface and the PPS procedure for baud-rate selection is implemented according to the values proposed by the SIM card/chip.

The **VSIM** supply output provide internal short circuit protection to limit the start-up current and protect the SIM from short circuits.

1.8.2 SIM detection interface

The **GPIO5** pin of TOBY-L3 series modules can be configured to detect the mechanical / physical presence of an external SIM card connected to the SIM interface. The pin can sense SIM card presence as intended to be properly connected to the mechanical switch of a SIM card holder as described in section 2.5:

- Low logic level at **GPIO5** input pin is recognized as SIM card present
- High logic level at **GPIO5** input pin is recognized as SIM card not present

☞ Only the **GPIO5** can be used as the SIM card detection on TOBY-L3 series modules.

☞ The logic level of the SIM detection GPIO for SIM detection can be configured through the AT command (See the TOBY-L3 series AT Commands Manual [2], +UGPIOC).

The SIM card detection function provided by **GPIO5** pin is an optional feature that can be implemented / used or not according to the application requirements: an Unsolicited Result Code (URC) is generated each time that there is a change of status (for more details, see the TOBY-L3 series AT Commands Manual [2], +UGPIOC, +CIND, +CMER).

The optional function "SIM card hot insertion/removal" can be additionally configured on the **GPIO5** pin by specific AT command (see the TOBY-L3 series AT Commands Manual [2], +UDCONF=50), in order to enable / disable the SIM interface upon detection of external SIM card physical insertion / removal.

1.9 Data communication interfaces

TOBY-L3 series modules provide the following serial communication interfaces:

- USB interface (see section 1.9.1):
  - USB High-Speed 2.0 interface, with the module acting as a USB device or host, providing:
    - ADB interface (Linux console for open CPU applications development and debug)
    - Modem interface (Dialing up the Network with PPP protocol or Sending AT commands)
    - AT Interface (Sending AT commands)
    - GNSS interface (Transport NMEA data information)
    - NDIS network interface over USB (Ethernet over USB data connection)
    - Diagnostic interface (Trace log capture, diagnostic purpose)
    - FW upgrades by means of the +UDWNFILE and +UFWINSTALL AT commands
    - FW upgrades by means of the Download Tool

- UART interfaces (see section 1.9.2):
  - UART0 interface, providing:
    - Can be configured as SPI (**SPI1**) interface by open CPU API or AT commands alternatively.
    - Communication with external serial devices by means of open CPU API or AT commands.
  - UART1 interface, providing:
    - Can be configured as I2S (**I2S1**), PCM (**PCM1**) or SPI (**SPI2**) interface by open CPU API or AT commands alternatively.
    - Communication with external serial devices by means of open CPU API or AT commands.
    - Communication with external slave SPI devices when configured as SPI1 by means of open CPU API
    - PPP data connection and AT command function.
  - UART2 interface, providing:
    - Only used to communicate with external WI-FI/Bluetooth devices to avoid RF interference between LTE and Wi-Fi/Bluetooth
  - UART3 interface, providing:
    - Communication with external serial devices by means of open CPU API
    - Trace log capture (diagnostic purposes)
- SPI interfaces[5] (see section 1.9.3):
  - Can be configured as UART (**UART4**) interface by open CPU API or AT commands.
  - **SPI0** interface, with the module acting as SPI master, providing:
    - Communication with external SPI slave devices by means of open CPU API
- Two DDC I^2C bus compatible interfaces (see section 1.9.4):
  - I2C0 interface, with the module acting as I^2C master, providing:
    - Communication with u-blox GNSS positioning chips / modules
    - Communication with external I^2C slave devices by means of open CPU API
  - I2C1 interface, with the module acting as I^2C master, providing:
    - Communication with external I^2C slave devices by means of open CPU API
- SDIO interface[5], with the module acting as SDIO host, providing (see section 1.9.5):
  - Communication with compatible u-blox short range radio modules by means of open CPU API
  - Communication with external SDIO devices by means of open CPU API
- SGMII interface, with the module acting as Ethernet MAC, providing (see section 1.9.6):

  Ethernet connection enabled through the external compatible Ethernet PHY SIM interfaces

1.9.1 USB interface

TOBY-L3 series modules include a USB High-Speed 2.0 interface, supporting up to 480 Mbit/s data rate.

[5] Not supported by "0x" product feature version

The USB High-Speed 2.0 compliant interface consists of the following pins:

- **USB_D+/USB_D–**, USB High-Speed differential data lines as per USB 2.0 specification [4]
- **VUSB_DET** input pin, which senses the VBUS rail presence (nominally 5 V at the source) to detect the host connection and enable the USB 2.0 interface with the module acting as a USB device.
  Neither the USB interface, nor the whole module is supplied by the **VUSB_DET** input pin, which senses the VBUS USB supply voltage presence and absorbs few microamperes.
- **USB_ID** pin, available for USB ID resistance measurement:
  - if the **USB_ID** pin is externally connected to GND, then the module acts as a USB host
  - if the **USB_ID** pin is externally left unconnected (floating), then the module acts as a USB device

The USB High-Speed 2.0 compliant interface, with the module acting as a USB device, provides:

- ADB interface[6] (Linux console for open CPU applications development and debug)
- Modem interface (Dialing up the Network with PPP protocol or Sending AT commands)
- AT interface (Sending AT commands)
- GNSS interface (Transport GNSS NMEA data information)
- NDIS network interface over USB (Ethernet over USB data connection)
- FW upgrades by means of the +UDWNFILE and +UFWINSTALL AT commands
- FW upgrades by means of the Download Tool

The module, acting as a USB device, identifies itself by its VID (Vendor ID) and PID (Product ID) combination, included in the USB device descriptor according to the USB 2.0 specifications [4].

The USB High-Speed 2.0 compliant interface, with the module acting as USB host (OTG), provides:

- Communication with external device by means of the open CPU application

1.9.2 UART interfaces

1.9.2.1 UART0 interface

The UART0 Universal Asynchronous Receiver/Transmitter serial interface has CMOS compatible signal levels (0 V for ON / active state and 1.8 V for OFF / idle state), providing:

- Can be configured as SPI (**SPI1**) interface by open CPU API or AT commands alternatively.
- Communication with external devices by means of the open CPU API, over the following pins:
  - **RXD** module output and **TXD** module input data lines
  - **CTS** module output and **RTS** module input hardware flow control lines
- Trace logging (diagnostic purpose), over the following pins:
  - **RXD** module output and **TXD** module input data lines

[6] Not supported by "0x" product feature versions

- Ring Indicator functionality, over the following pin:
  - **RI** module output line

The UART0 interface can operate at 4.8kbit/s, 9.6kbit/s, 19.2kbit/s, 38.4kbit/s, 57.6kbit/s, 115.2kbit/s, 230.4kbit/s, 1Mbit/s, 3Mbit/s, 4Mbit/s baud rates, with 8N1 frame format (illustrated in Figure 17), and with hardware flow control output (**CTS** line) driven to the OFF state when the module is not prepared to accept data by the UART0 interface.

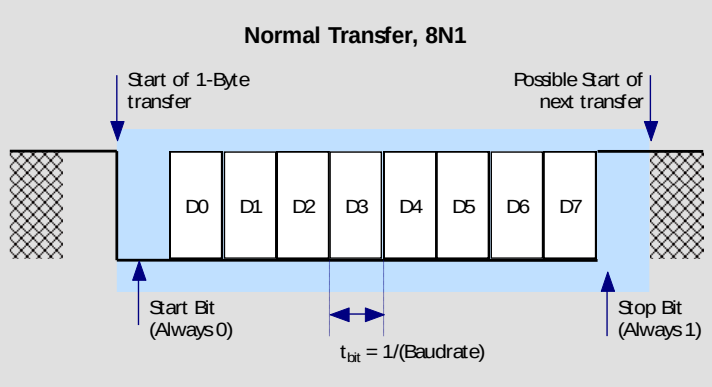

Figure 17: Description of UART 8N1 frame format (8 data bits, no parity, 1 stop bit)

RI can be used to notify an incoming call or SMS arrival and wake up the host. This PIN can be configured as two mode (see Table 11) through AT command (see the TOBY-L3 series AT Commands Manual [2]).

Mode	Output	Remarks
Mode 1 (Default mode)	Switch from on to off cyclically, (High-Level for 1s, Low-level for 4s)	Voice call incoming, see Figure 18. For more details, see the TOBY-L3 series AT Commands Manual.
	Switch from off to on for 1s, (Low-level for 1s)	SMS arrival, see Figure 19. For more details, See the TOBY-L3 series AT Commands Manual.
Mode 2	Switch from off to on for 120ms	Wakeup the host, see Figure 20. For more details, See the TOBY-L3 series AT Commands Manual.

Table 11: RI pin configuration mode

The **RI** line can notify an incoming call: the line is switched from the OFF state to the ON state with a 4:1 duty cycle and a 5 s period (ON for 1 s, OFF for 4 s, see Figure 18), until the DTE attached to the module sends the ATA string and the module accepts the incoming data call. The RING string sent by the module (DCE) to the serial port at constant time intervals is not correlated with the switch of the **Ring Indicator** line to the ON state.

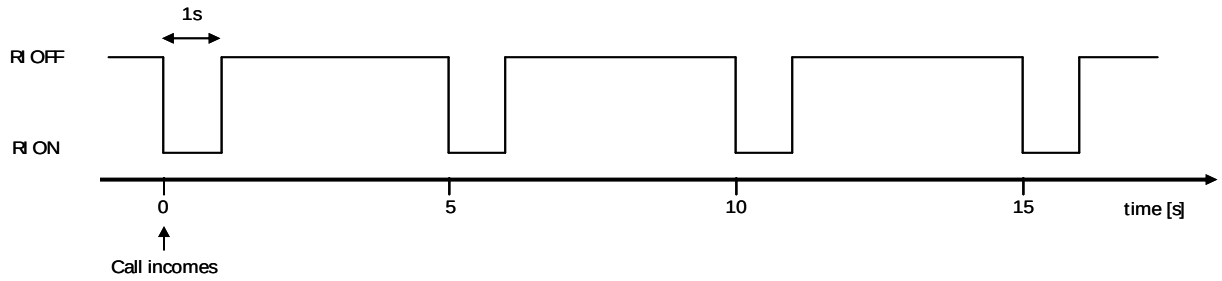

Figure 18: RI behavior during an incoming call

The **RI** output line can notify an SMS arrival. When the SMS arrives, the line switches from OFF to ON for 1 s (see Figure 19), if the feature is enabled by the AT+CNMI command (see the TOBY-L3 series AT Commands Manual [2]).

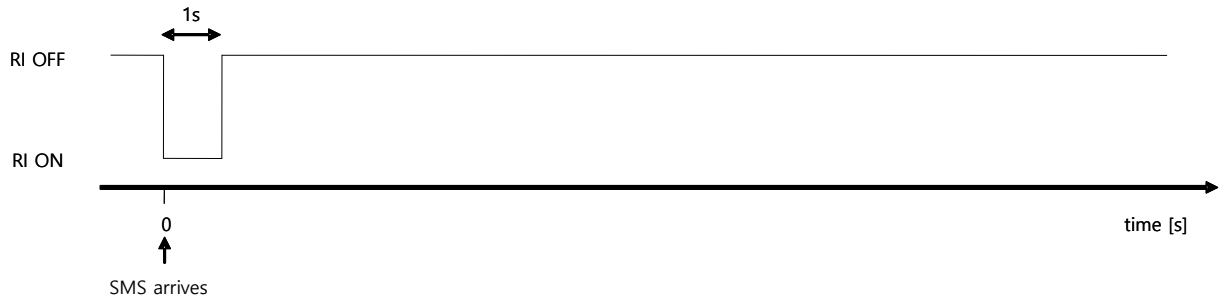

Figure 19: RI behavior at SMS arrival

This behavior allows the DTE to stay in power saving mode until the DCE related event requests service.
For SMS arrival, if several events coincidently occur or in quick succession, each event independently triggers the **RI** line, although the line will not be deactivated between each event. As a result, the **RI** line may stay to ON for more than 1 s, if an incoming call is answered within less than 1 s (with ATA or if auto-answering is set to ATS0=1) then the **RI** line is set to OFF earlier, so that:

- **RI** line monitoring cannot be used by the DTE to determine the number of received SMSs.
- For multiple events (incoming call plus SMS received), the **RI** line cannot be used to discriminate the two events, but the DTE must rely on subsequent URCs and interrogate the DCE with the suitable commands.

The **RI** line can additionally notify all the URCs and responses, if the feature is enabled by the specific AT+URING command (for more details, see the TOBY-L3 series AT Commands Manual [2]): the **RI** line is

asserted when one of the configured events occur and it remains asserted for 1 s unless another configured event will happen, with the same behavior illustrated in Figure 19.

The **RI** function can be alternatively configured by GPIO by an AT command.

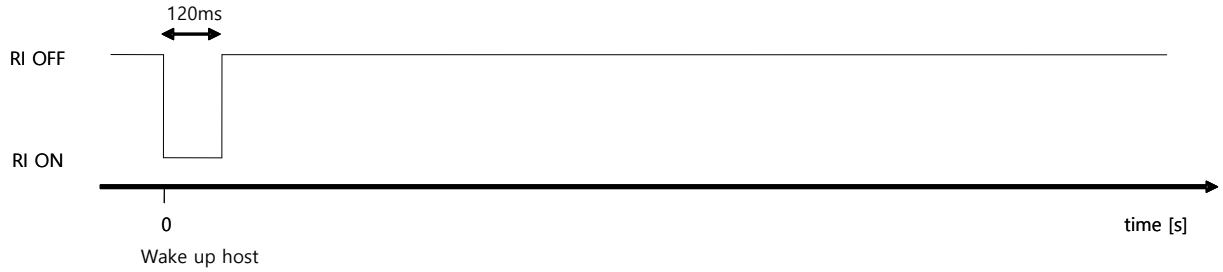

Figure 20: RI behavior at wake up host in mode 2

As described in Figure 20, the **RI** line can wake up the external host after configured the pin as mode 2 by AT command.

The UART0 interface can be alternatively, in mutually exclusive way, configured as SPI **(SPI1)** interface by means of open CPU API or AT command (see the TOBY-L3 series AT Commands Manual [2]), for communication with external devices with the following configuration Table 13:

4-wire UART Mode (UART0)	SPI Mode (SPI1)
RXD (Module output); UART0 Receive Data	**SPI1_MOSI**; SPI1 MOSI Pin (Module Output)
TXD (Module Input); UART0 Transmit Data	**SPI1_MISO**; SPI1 MISO Pin (Module Input)
CTS (Module Output); UART0 Clear To Send	**SPI1_SCLK**; SPI1 Clock Pin (Module Output)
RTS (Module Input); UART0 Ready To Send	**SPI1_CS**; SPI1 Chip Select Pin (Module Output)

Table 12: TOBY-L3 series modules UART0 PINs configuration

1.9.2.2 UART1 interface

The UART1 Universal Asynchronous Receiver/Transmitter serial interface, with CMOS compatible signal levels (0 V for ON / active state and 1.8 V for OFF / idle state), can operate as a serial interface for communication with external devices by means of the open CPU API, with the following pins:

- RXD1 module output and TXD1 module input data lines
- CTS1 module output and RTS1 module input hardware flow control lines

The UART1 interface can operate at 300bit/s, 600bit/s, 1.2kbit/s, 2.4kbit/s, 4.8kbit/s, 9.6kbit/s, 19.2kbit/s, 38.4kbit/s, 57.6kbit/s, 115.2kbit/s, 230.4kbit/s, 1Mbit/s, 3Mbit/s, 4Mbit/s baud rates, with 8N1 frame format (illustrated in Figure 17), and with hardware flow control output (**CTS1** line) driven to the OFF state when the module is not prepared to accept data by the UART1 interface.

The UART1 interface can be alternatively, in mutually exclusive way, configured as SPI **(SPI2)**, I2S **(I2S1)** or PCM (**PCM1**) interface by means of open CPU API or AT command (see the TOBY-L3 series AT Commands Manual [2]), for communication with external devices with the following configuration Table 13:

4-wire UART Mode (UART1)	SPI Mode (SPI2)	I2S Mode (I2S1)	PCM Mode (PCM1)
RXD1 (Module output); UART1 Receive Data	**SPI2_MOSI**; SPI2 MOSI Pin (Module Output)	**I2S1_WA**; I2S1 Word alignment	**PCM1_SYNC**; PCM1 Frame Sync
TXD1 (Module Input); UART1 Transmit Data	**SPI2_MISO**; SPI2 MISO Pin (Module Input)	**I2S1_RXD**; I2S1 Receive Data In	**PCM1_DIN**; PCM1 Data In
CTS1 (Module Output); UART1 Clear To Send	**SPI2_CLK**; SPI2 Clock Pin (Module Output)	**I2S1_CLK**; I2S Serial Clock	**PCM1_CLK**; PCM1 Clock
RTS1 (Module Input); UART1 Ready To Send	**SPI2_CS**; SPI2 Chip Select Pin (Module Output)	**I2S1_TXD**; I2S1 Transmit Data Out	**PCM1_DOUT**; PCM1 Data Out

Table 13: TOBY-L3 series modules UART1 PINs configuration

1.9.2.3 UART2 interface

☞ The UART2 interface is used for LTE-ISM concurrency only.

The UART2 two wire Universal Asynchronous Receiver/Transmitter serial interface (**TXD2** and **RXD2** pin) is only used for the LTE and ISM concurrency procedure. The UART2 has CMOS compatible signal levels (0 V for ON / active state and 1.8 V for OFF / idle state). As some LTE band and Wi-Fi band or BT band is overlapped, to avoid the RF interference, the module provide the UART2 interface to exchange the wireless information message and the control commands.

The UART2 interface is only used for LTE-ISM concurrency, over the following pins:

- **RXD2** module output and **TXD2** module input data lines

UART2 interface can operate at 300bit/s, 600bit/s, 1.2kbit/s, 2.4kbit/s, 4.8kbit/s, 9.6kbit/s, 19.2kbit/s, 38.4 kbit/s, 57.6kbit/s, 115.2kbit/s, 230.4kbit/s, 1Mbit/s, 3Mbit/s, 4Mbit/s baud rates, with 8N1 frame format.

1.9.2.4 UART3 interface

The UART3 Universal Asynchronous Receiver/Transmitter serial interface has CMOS compatible signal levels (0 V for ON / active state and 1.8 V for OFF / idle state), providing:

- Linux console for open CPU API development and debug, over the following pins:
  - **RXD3** module output and **TXD3** module input data lines

UART3 interface can operate at 300bit/s, 600bit/s, 1.2kbit/s, 2.4kbit/s, 4.8kbit/s, 9.6kbit/s, 19.2kbit/s, 38.4 kbit/s, 57.6kbit/s, 115.2kbit/s, 230.4kbit/s, 1Mbit/s, 3Mbit/s, 4Mbit/s baud rates, with 8N1 frame format.

1.9.3 SPI interfaces

1.9.3.1 SPI0 interface

The SPI0 1.8 V Serial Peripheral Interface supports communication with an external SPI slave devices, with the module acting as SPI master, by means of the open CPU API, with the following pins:

- **SPI_MOSI** pin, SPI0 Master Output Slave Input (module output)
- **SPI_MISO** pin, SPI0 Master Input Slave Output (module input)
- **SPI_SCLK** pin, SPI0 Serial Clock (module output)
- **SPI_CS** pin, SPI0 Chip Select 0 (module output)

The SPI Serial Clock signal work on the frequency at 960KHz, 4.8MHz, 9.6MHz, 16MHz, 19.2MHz, 25MHz and 50MHz, the default frequency is 50MHz.

The **SPI0** interface can be configured as UART (**UART4**) interface by means of open CPU API or AT command (see the TOBY-L3 series AT Commands Manual [2]), for communication with external devices with the following configuration Table 13:

SPI Mode (SPI0)	4-wire UART Mode (UART4)
SPI_MOSI; SPI0 MOSI Pin (Module Output)	**RXD4** (Module output); UART4 Receive Data
SPI_MISO; SPI0 MISO Pin (Module Input)	**TXD4** (Module Input); UART4 Transmit Data
SPI_SCLK; SPI0 Clock Pin (Module Output)	**CTS4** (Module Output); UART4 Clear To Send
SPI_CS; SPI0 Chip Select Pin (Module Output)	**RTS4** (Module Input); UART4 Ready To Send

Table 14: TOBY-L3 series modules SPI0 PINs configuration

1.9.4 DDC (I2C) interfaces

1.9.4.1 I2C0 interface

The **SDA** and **SCL** pins represent the I2C0 1.8 V I^2C bus compatible Display Data Channel (DDC) interface, with the module acting as I^2C master, available for

- communication with u-blox GNSS chips / modules
- communication with other external I^2C devices by means of the open CPU API or AT commands

I2C0 interface pins of the module are open drain outputs conforming to the I^2C bus specifications [7], supporting up to 100 kbit/s data rate in Standard-mode, and up to 400 kbit/s data rate in Fast-mode.

Tashang has implemented special features to ease the design effort required for the integration of the TOBY-L3 cellular module with a u-blox GNSS device.

Combining the TOBY-L3 cellular module with a u-blox GNSS device allows designers to have full access to the positioning device directly via the cellular module: it relays control messages to the GNSS device via a

dedicated DDC (I²C) interface. An interface connected to the positioning device is not necessary: the cellular module allows full control of the GNSS device.

The modules provide embedded GNSS aiding that is a set of specific features developed by u-blox to improve the cellular / GNSS system power consumption and the GNSS performance, decreasing the Time-To-First-Fix (TTFF), thus allowing to calculate the position in shorter time with higher accuracy.

The cellular modules provide additional custom functions over GPIO pins to improve the integration with u-blox positioning chips and modules (see section 1.13). GPIO pins can handle:

- "GNSS supply enable" function provided by **GPIO2**, improving the power consumption of the positioning device: when the GNSS functionality is not required, the external positioning device can be completely switched off by the cellular module
- "GNSS Tx data ready" function provided by **GPIO3**, improving the power consumption of the cellular module: when low power idle mode is enabled in the cellular module, the GNSS device can wake up the cellular module notifying that it is ready to send data by the DDC (I²C) interface, so the cellular module does not lose the data sent by the GNSS device even if low power idle mode is enabled

1.9.4.2 I2C1 interface

The **SDA1** and **SCL1** pins represent the I2C1 I²C bus compatible Display Data Channel (DDC) interface, with the module acting as the I²C master, available for

- communication with other external I²C devices by means of open CPU API

I2C1 interface pins of the module are open drain outputs conforming to the I²C bus specifications [7], supporting up to 100 kbit/s data rate in Standard-mode, and up to 400 kbit/s data rate in Fast-mode. External pull-up resistors to a suitable 1.8 V supply (e.g. **V_INT**) are required for operations.

1.9.5 SDIO interface

TOBY-L3 series modules include a 4-bit Secure Digital Input Output interface (**SDIO_D0**, **SDIO_D1**, **SDIO_D2**, **SDIO_D3**, **SDIO_CLK**, **SDIO_CMD**), where the module acts as an SDIO host controller designed to

- communicate with compatible u-blox short range radio communication modules by means of the open CPU API
- communicate with external SDIO devices by means of the open CPU API

The SDIO interface supports up to SD 3.0 SDR104 bus speed mode.

Combining the TOBY-L3 cellular module with a u-blox short range communication module gives designers full access to the Wi-Fi module directly via the cellular module, so that a second interface connected to the Wi-Fi module is not necessary. The cellular module allows a full control of the Wi-Fi module, because Wi-Fi control messages are relayed to the Wi-Fi module via the dedicated SDIO interface.

Tashang has implemented special features in the cellular modules to ease the design effort for the integration of the TOBY-L3 cellular module with a u-blox short range radio communication module, to provide Router functionality.

The cellular modules provide additional custom functions over GPIO pins to improve the integration with u-blox short range radio communication modules (see section 1.13). GPIO pins can handle:

- "Wi-Fi enable" function provided by **GPIO6**, improving the power consumption of the short range radio communication module: when the Wi-Fi functionality is not required, the external short range radio communication module can be switched off by the cellular module

1.9.6 SGMII interface

TOBY-L3 series modules include an Ethernet Media Access Control (MAC) block supporting up to 1Gbit/s data rate via a Serial Gigabit Media-Independent Interface compliant with the SGMII Version 1.8 specification [8].

The module represents an Ethernet MAC controller, which can be connected to an external Ethernet physical transceiver (PHY) chip for communication with a remote processor over Ethernet.

The following signals are provided for communication and management of an external Ethernet PHY:

- **V_ETH** Interface supply output
- **SGMII_TX_P** SGMII transmit-plus
- **SGMII_TX_N** SGMII transmit-minus
- **SGMII_RX_P** SGMII receive-plus
- **SGMII_RX_N** SGMII receive-minus
- **ETH_INTR** Ethernet Interrupt Input, from PHY to MAC (module input)
  When this signal is high, it indicates an interrupt event in the PHY
- **ETH_MDIO** Management Data Input Output, bidirectional signal (module input/output)
- **ETH_MDC** Management Data Clock, from MAC to PHY (module output)

1.10 eMMC interface

TOBY-L3 series modules include a 4-bit embedded Multi-Media Card interface compliant with the JESD84-B451 Embedded Multimedia Card (eMMC) Electrical Standard 4.51 [9]. The following signals are provided for connection and management of an external eMMC / SD memory by means of the open CPU API:

- **V_MMC** Interface supply output (module output)
- **MMC_D0** Multi-Media Card Data [0], bidirectional signal (module input/output)
- **MMC_D1** Multi-Media Card Data [1], bidirectional signal (module input/output)
- **MMC_D2** Multi-Media Card Data [2], bidirectional signal (module input/output)
- **MMC_D3** Multi-Media Card Data [3], bidirectional signal (module input/output)
- **MMC_CMD** Multi-Media Card Command, bidirectional signal (module input/output)
- **MMC_CLK** Multi-Media Card Clock (module output)
- **MMC_RST_N** Multi-Media Card Reset (module output)
- **MMC_CD_N** Multi-Media Card Detect (module input)

Supported Bus Speed Modes:

- SD2.0 Default Speed mode: 2.85V signaling, up to 25 MHz, up to 12.5 MB/s
- SD2.0 High Speed Mode: 2.85V signaling, up to 50 MHz, up to 25 MB/s
- SD3.0 SDR12: 1.8V signaling, up to 25 MHz, up to 12.5 MB/s
- SD3.0 SDR25: 1.8V signaling, up to 50 MHz, up to 25 MB/s
- SD3.0 SDR50: 1.8V signaling, up to 100 MHz, up to 50 MB/s
- SD3.0 SDR104 1.8V signaling, up to 208MHz, up to 104MB/s
- SD3.0 DDR50: 1.8V signaling, up to 50 MHz, sampled on both clock edges, up to 50 MB/s
- eMMC Backward Compatibility Mode: 1.8V / 2.85V signaling, up to 26 MHz, up to 26 MB/s
- eMMC High Speed SDR Mode: 1.8V / 2.85V signaling, up to 52 MHz, up to 52 MB/s
- eMMC High Speed DDR Mode: 1.8V / 2.85V signaling, up to 52 MHz, up to 104 MB/s

1.11 Digital Audio interfaces

TOBY-L3 series modules provide a 4-wire I²S digital audio interface:

- I2S digital audio interface, consisting of the following pins:
  - **I2S_TXD** data output
  - **I2S_RXD** data input
  - **I2S_CLK** bit clock input/output
  - **I2S_WA** world alignment / synchronization signal input/output

The I2S0 digital audio interfaces is suitable to transfer digital audio data with an external compatible digital audio device, as an audio codec or as an audio digital signal processor.

The I²S interfaces can be alternatively set in different modes:

- PCM mode (short synchronization signal): I²S word alignment signal is set high for 1 or 2 clock cycles for the synchronization, and then is set low for 16 clock cycles according to the 17 or 18 clock cycles frame length.
- Normal I²S mode (long synchronization signal): I²S word alignment is set high / low with a 50% duty cycle (high for 16 clock cycles / low for 16 clock cycles, according to the 32 clock cycles frame length).

The Digital Audio interface can be configured as I2S (**I2S0**) or PCM (**PCM0**) interface by means of open CPU API or AT command, for communication with external devices with the following configuration is listed in the Table 15:

I2S Mode (I2S0)	PCM Mode (PCM0)
I2S_TXD; I2S0 Transmit Data Out	**PCM0_DOUT**; PCM0 Data Out
I2S_RXD; I2S0 Receive Data In	**PCM0_DIN**; PCM0 Data In
I2S_CLK; I2S0 Serial Clock	**PCM0_CLK**; PCM0 Clock
I2S_WA; I2S0 Word Alignment	**PCM0_SYNC**; PCM0 Frame Sync

Table 15: TOBY-L3 series modules Digital Audio PINs configuration

The I²S interface can be alternatively set in 2 different roles:

- Master mode
- Slave mode

The sample rate of transmitted/received words, which corresponds to the I²S word alignment / synchronization signal frequency (<I2S_sample_rate>), can be alternatively set to:

- 8 kHz
- 16 kHz
- 48 kHz

The modules support I^2S transmit and I^2S receive data 16-bit words long, linear. Data is transmitted and read in 2's complement notation. The MSB is transmitted and read first.

I^2S clock signal frequency depends on the frame length, the sample rate and the selected mode of operation:

- 17 x <I2S_sample_rate> or 18 x <I2S_sample_rate> in PCM mode (short synchronization signal)
- 16 x 2 x <I2S_sample_rate> in Normal I2S mode (long synchronization signal)

1.12 ADC interfaces

TOBY-L3 series modules include Analog to Digital Converter inputs (**ADC1**, **ADC2**), which can be handled by means of the dedicated open CPU API.

1.13 General Purpose Input/Output

TOBY-L3 series modules include 11 pins (**GPIO1**, **GPIO2**, **GPIO3**, **GPIO4**, **GPIO5**, **GPIO6**, **GPIO7**, **GPIO8**, **HOST_SELECT0**, **HOST_SELECT1**, **RI**) that can be configured through AT command or the open CPU application as general purpose input/output or to provide custom functions as summarized in Table 16.

Function	Description	Default	Configurable GPIOs
Ring Indicator	UART0 Ring Indicator functionality	RI	RI
Wi-Fi enable	Switch-on/off the external u-blox Wi-Fi module connected to the cellular module over the SDIO interface	GPIO6	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, HOST_SELECT0, HOST_SELECT1, RI
GNSS supply enable	Enable/disable the supply of u-blox GNSS device connected to the cellular module over the I2C0 interface	GPIO2	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, HOST_SELECT0, HOST_SELECT1, RI
GNSS data ready	Sense when u-blox GNSS device connected to the module is ready for sending data over the I2C0 interface	GPIO3	GPIO3, GPIO5, HOST_SELECT0, HOST_SELECT1, RI
External Interrupt	External Interrupt detection (module input)	-	GPIO3, GPIO5, HOST_SELECT0, HOST_SELECT1, RI
Wake-up	Pull up the PIN to high level internally. When the input level of the PIN is low, make the module enter active mode from sleep mode.	-	GPIO3, GPIO5, HOST_SELECT0, HOST_SELECT1, RI
Sleep Control	When the input level of the PIN is high, make the module enter active mode(Wake up from sleep mode); When the input level of the PIN is low or the PIN is in floating, the module can enter sleep mode.	-	GPIO3, GPIO5, HOST_SELECT0, HOST_SELECT1, RI
Sleep Status	Indicator the sleep status of the module; When the module is in active mode, the output of the PIN is high level; When the module is in sleep mode, the output of the PIN is low level;	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, HOST_SELECT0, HOST_SELECT1, RI

Function	Description	Default	Configurable GPIOs
Wake-up Wi-Fi	Wake-up the Wi-Fi module from sleep mode	GPIO1	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, HOST_SELECT0, HOST_SELECT1, RI
WWAN Status	Indicator the status of WWAN.	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, HOST_SELECT0, HOST_SELECT1, RI
WWAN RF enable	Enable/disable the RF function of the cellular module; When the input of the PIN is set high level, enable the RF function of the cellular, disable the RF function on the reverse.	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, HOST_SELECT0, HOST_SELECT1, RI
SIM card detection	External SIM card physical presence detection	GPIO5	GPIO5
SIM card hot insertion/removal	Enable / disable SIM interface upon detection of external SIM card physical insertion / removal	GPIO5	GPIO5
Input	Input to sense high or low digital level	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, HOST_SELECT0, HOST_SELECT1, RI
Output	Output to set the high or the low digital level	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, HOST_SELECT0, HOST_SELECT1, RI
Pin disabled	Output tri-stated with an internal active pull-down enabled	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, HOST_SELECT0, HOST_SELECT1, RI

Table 16: TOBY-L3 series modules GPIO custom functions summary

1.14 Reserved pins (RSVD)

TOBY-L3 series modules have pins reserved for future use, marked as **RSVD**. They must all be left unconnected on the application board.

1.15 System features

1.15.1 Network indication

☞ The Network indication feature of TOBY-L3 series modules is disabled by default, it can be configured in different working modes(see Table 17) through AT command. For details, see the TOBY-L3 series AT Commands Manual [2].

TOBY-L3 series modules provide the Wireless Wide Area Network status indication as described below:

- No service (No network coverage or not registered)

- Network searching
- Registered the network
- Data transfer is on going
- Voice call is on going

Mode	Output Status	Remarks
Mode 1		Network indication function is disabled. (Default configuration mode)
Mode 2	Blink slowly (200ms High/1800ms Low)	Network is on searching.
	Blink slowly (1800ms High/200ms Low)	The module has registered on the network and work in idle state.
	Blink quickly (125ms High/125ms Low)	The module has registered on the network with data transfer is ongoing.
	Keep High	The module has registered on the network with voice calling is ongoing.
Mode 3	Low level (light on)	The module has registered on the network.
	High Level (light off)	No network coverage or not registered
Mode 4	Blink quickly (100ms Low, 100ms High, 100ms Low then 1700ms High)	No network coverage or not registered
	Blink slowly (100ms Low, 1900ms High)	The module has registered on the network.

Table 17: The configuration mode of the network indication pin output

1.15.2 Jamming detection

In real network situations modules can experience various kind of out-of-coverage conditions: limited service conditions when roaming to networks not supporting the specific SIM, limited service in cells which are not suitable or barred due to operators' choice, no cell condition when moving to poorly served or highly interfered areas. In the latter case, interference can be artificially injected in the environment by a noise generator covering a given spectrum, thus obscuring the operator's carries entitled to give access to the LTE/3G/2G service.

The congestion (i.e. jamming) detection feature can be enabled and configured by the +UCD AT command: the feature consists of detecting an anomalous sources of interference and signaling the start and stop of such conditions to the host application processor with an unsolicited indication, which can react appropriately by e.g. switching off the radio transceiver of the module (i.e. configuring the module in "airplane mode" by means of the +CFUN AT command) in order to reduce power consumption and monitoring the environment at constant periods (for more details, see the TOBY-L3 series AT command manual [2]).

1.15.3 IP modes of operation

IP modes of operation refer to the TOBY-L3 series modules configuration related to the network IP termination and network interfaces settings in general IP modes of operation are following:

- **Bridge mode**: In bridge mode the module acts as a cellular modem dongle connected to the host over serial interface. The IP termination of the network is placed on the host IP stack. The module is configured as a bridge which means the network IP address is assigned to the host (host IP termination).
- **Router mode**: In router mode the module acts as a cellular modem router which means the IP termination of the network is placed on the Internal IP stack of the module (on-target IP termination). In particular, in this configuration the application processor belongs to a private network and is not aware of the mobile connectivity setup of the module.

For more details about IP modes of operation, see the TOBY-L3 series AT command manual [2].

1.15.4 Dual stack IPv4 and IPv6

TOBY-L3 series modules support both Internet Protocol version 4 and Internet Protocol version 6 in parallel.

For more details about dual stack IPv4 and IPv6 see the TOBY-L3 series AT command manual [2].

1.15.5 Embedded TCP/IP and UDP/IP

TOBY-L3 series modules provide embedded TCP/IP and UDP/IP protocol stack: a PDP context can be configured, established and handled via the data connection management packet switched data commands.

TOBY-L3 series modules provide Direct Link mode to establish a transparent end-to-end communication with an already connected TCP or UDP socket via serial interfaces (USB, UART). In Direct Link mode, data sent to the serial interface from an external application processor is forwarded to the network and vice-versa.

For more details about the embedded TCP/IP and UDP/IP functionalities, see the TOBY-L3 series AT commands manual [2].

1.15.6 Embedded FTP and FTPS

TOBY-L3 series modules provide embedded File Transfer Protocol (FTP) and FTP over SSL (FTPS) services. Files are read and stored in the local file system of the module, it can also be transfered between the file FTP server and the external application processor via serial interfaces (USB, UART) in FTP (or FTPS) Direct link mode:

- **FTP (or FTPS) download**: data coming from the FTP server is forwarded to the host processor via USB / UART serial interfaces (for FTP without Direct Link mode, the data is always stored in the module's Flash File System)
- **FTP (or FTPS) upload**: data coming from the host processor via USB / UART serial interface is forwarded to the FTP server (for FTP without Direct Link mode, the data is read from the module's Flash File System)

When Direct Link is used for a FTP (or FTPS) file transfer, only the file content pass through USB / UART serial interface, whereas all the FTP (or FTPS) commands handling is managed internally by the FTP application.

For more details about the embedded FTP and FTPS functionalities, see the TOBY-L3 series AT commands manual [2].

1.15.7 Embedded HTTP and HTTPS

TOBY-L3 series modules provide the embedded Hyper-Text Transfer Protocol (HTTP) and Hyper-Text Transfer Protocol Secure (HTTPS) services via AT commands for sending requests to a remote HTTP(HTTPS) server, receiving the server response and transparently storing it in the module's Flash File System, it can also be transferred the HTTP or HTTPS data between the remote HTTP or HTTPS server and the external application processor via serial interfaces (USB, UART) in HTTP or HTTPS Direct link mode:

- **HTTP (or HTTPS) download**: data coming from the HTTP or HTTPS server is forwarded to the host processor via USB / UART serial interfaces (for HTTP or HTTPS without Direct Link mode, the data is always stored in the module's Flash File System)
- **HTTP (or HTTPS) upload**: data coming from the host processor via USB / UART serial interface is forwarded to the HTTP or HTTPS server (for HTTP or HTTPS without Direct Link mode, the data is read from the module's Flash File System)

When Direct Link is used for a HTTP or HTTPS file transfer, only the file content pass through USB / UART serial interface, whereas all the HTTP or HTTPS commands handling is managed internally by the embedded HTTP(S) application.

For more details about the embedded HTTP and HTTPS functionalities, see the TOBY-L3 series AT commands manual [2].

1.15.8 SSL and TLS

TOBY-L3 series modules support the Secure Socket Layer (SSL) / Transport Layer Security (TLS) with certificate key sizes up to 4096 bits to provide security over the FTP and HTTP protocols.

The SSL/TLS support provides different connection security aspects:

- **Server authentication:** use of the server certificate verification against a specific trusted certificate or a trusted certificate list
- **Client authentication:** use of the client certificate and the corresponding private key
- **Data security and integrity:** data encryption and Hash Message Authentication Code (HMAC) generation

The security aspects used during a connection depend on the SSL/TLS configuration and features supported. For a complete list of supported SSL/TLS configurations and settings see the TOBY-L3 series AT commands manual [2].

1.15.9 Firmware update Over AT (FOAT)

This feature allows upgrading the module firmware over USB / UART serial interfaces, using AT commands.

- The +UFWUPD AT command triggers a reboot followed by the upgrade procedure at specified a baud rate.
- A special boot loader on the module performs firmware installation, security verifications and module reboot.
- Firmware authenticity verification is performed via a security signature during the download. The firmware is then installed, overwriting the current version. In case of power loss during this phase, the boot loader detects a fault at the next wake-up, and restarts the firmware downloaded. After completing the upgrade, the module is reset again and wakes-up in normal boot.

For more details about Firmware update Over AT procedure, see the Firmware update application not and the TOBY-L3 series AT commands manual [2], +UFWUPD AT command.

1.15.10 Firmware update Over The Air (FOTA)

This feature allows upgrading the module firmware over the LTE/3G/2G air interface.

In order to reduce the amount of data to be transmitted over the air, the implemented FOTA feature requires downloading only a "delta file" instead of the full firmware. The delta file contains only the differences between the two firmware versions (old and new), and is compressed. The firmware update procedure can be triggered using dedicated AT command with the delta file stored in the module file system via over the air FTP.

For more details about Firmware update Over The Air procedure, see the firmware update application note and the TOBY-L3 series AT commands manual [2], +UFWINSTALL AT command.

1.15.11 Power Saving

The power saving configuration is by default disabled, but is can be enabled using the AT+UPSV command (for the detail of the AT+UPSV command, see the TOBY-L3 series AT commands manual [2]).

When power saving is enabled, the module automatically enters the low power idle-mode whenever possible, reducing current consumption (See the TOBY-L3 series data sheet [1]).

During the low power idle-mode, the module is not ready to communicate with an external device, as it is configured to reduce power consumption. The module wakes up from low power idle-mode to active-mode in the following events:

- Automatic periodic monitoring of the paging channel for the reception of the paging block sent by the base station according to network conditions.
- The connected USB host forces a remote wakeup of the module as USB device.
- Automatic periodic enable of the UART interface to receive / send data, with AT+UPSV=1
- Data received on UART interface, with HW flow control disabled and power saving enabled
- The module pin that configured as Wake-up function is triggered by the external device
- The SIM card hot insertion or removal function is enabled and the SIM hot plug event is triggered

- The GNSS data ready pin trigger the interruption
- Other interruption pin have the interrupt input signal

For the definition and the description of TOBY-L3 series modules operating modes, including the events forcing transitions between the different operating modes.

2 Design-in

2.1 Overview

For optimal integration of the modules in the application PCB, follow the design guidelines stated in this section.

Every application circuit must be properly designed to guarantee the correct functionality of the relative interface, but a number of points require greater attention during the design of the application device.

The following list provides a rank of importance in the application design, starting with the most significant:

1. Module antenna connection:
   Antenna circuit directly affects the RF compliance of the device integrating a TOBY-L3 series module with applicable certification schemes. Very carefully follow the suggestions provided in section 2.4 for the schematic and layout design.
2. Module supply:
   The supply circuit affects the RF compliance of the device integrating a TOBY-L3 series module with applicable required certification schemes as well as the antenna circuit design. Very carefully follow the suggestions provided in section 2.2.1 for the schematic and layout design.
3. USB interface:
   Accurate design is required to guarantee USB functionality. Carefully follow the suggestions provided in section 2.6.1 for the schematic and layout design.
4. SIM interface:
   Accurate design is required to guarantee SIM card functionality reducing the risk of RF coupling. Carefully follow the suggestions provided in section 2.5 for the schematic and layout design.
5. System functions:
   Accurate design is required to guarantee well defined voltage level during operation at Reset and Power-on inputs. Carefully follow the suggestions provided in section 2.3 for the schematic and layout design.
6. Digital Audio:
   Accurate design is required to obtain clear and high quality audio reducing the risk of noise from audio lines due to both supply burst noise coupling and RF detection. Carefully follow the suggestions provided in section 2.8 for the schematic and layout design.
7. SDIO, SGMII, eMMC interfaces:
   Accurate design is required to guarantee SDIO, SGMII, eMMC interfaces functionality. Carefully follow the suggestions provided in section 2.6.5, 2.6.6, 2.7 for the schematic and layout design.
8. ADC interfaces:
   Accurate design is required to guarantee ADC interfaces functionality. Carefully follow the suggestions provided in section 2.9 for the schematic and layout design.

9. Other digital interfaces: (UART, SPI, I^2C, I^2S, Host Select, GPIOs, and Reserved pins).
   Accurate design is required to guarantee correct functionality and reduce the risk of digital data frequency harmonics coupling. Follow the suggestions provided in sections 2.6.1, 2.6.3, 2.6.4, 2.3.3, 2.10, 2.11.
10. Other supplies: **V_INT** is generic digital interface supply.
    Correct design is required to guarantee functionality. Follow the suggestions provided in 2.2.2.

☞ It is recommended to also follow the specific design guidelines provided by each manufacturer of any external part selected for the application board that integrates the u-blox cellular modules.

2.2 Supply interfaces

2.2.1 Module supply (VCC)

2.2.1.1 General guidelines for VCC supply circuit selection and design

All the available **VCC** pins must be connected to the external supply minimizing the power loss due to series resistance.

GND pins are internally connected. Application design shall connect all the available pads to solid ground on the application board, since a good (low impedance) connection to external ground can minimize power loss and improve RF and thermal performance.

TOBY-L3 series modules must be sourced through the **VCC** pins with a suitable DC power supply that should meet the following prerequisites to comply with the modules' **VCC** requirements summarized in Table 7.

The suitable DC power supply can be selected according to the application requirements (see Figure 21) between the different possible supply sources types, which most common ones are the following:

- Switching DC/DC regulator
- Low Drop-Out (LDO) linear regulator
- Rechargeable Lithium-ion (Li-Ion) or Lithium-ion polymer (Li-Pol) battery
- Primary (disposable) battery

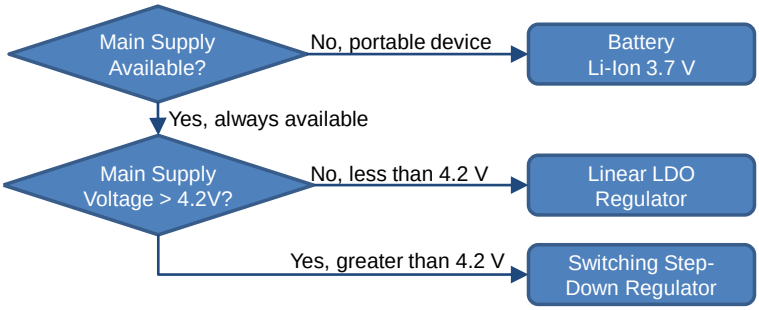

Figure 21: VCC supply concept selection

The switching step-down regulator is the typical choice when the available primary supply source has a nominal voltage much higher (e.g. greater than 4.2 V) than the operating supply voltage of TOBY-L3 series. The use of switching step-down provides the best power efficiency for the overall application and minimizes current drawn from the main supply source. See sections 2.2.1.2, 2.2.1.6, 2.2.1.10, 2.2.1.11 for specific design-in.

The use of an LDO linear regulator becomes convenient for a primary supply with a relatively low voltage (e.g. less or equal than 4.2). In this case the typical 90% efficiency of the switching regulator diminishes the benefit of voltage step-down and no true advantage is gained in input current savings. On the opposite side, linear regulators are not recommended for high voltage step-down as they dissipate a considerable amount of energy in thermal power. See sections 2.2.1.3, 2.2.1.6, 2.2.1.10, 2.2.1.11 for specific design-in.

If TOBY-L3 series modules are deployed in a mobile unit where no permanent primary supply source is available, then a battery will be required to provide **VCC**. A standard 3-cell Li-Ion or Li-Pol battery pack directly connected to **VCC** is the usual choice for battery-powered devices. During charging, batteries with Ni-MH chemistry typically reach a maximum voltage that is above the maximum rating for **VCC**, and should therefore be avoided. See sections 2.2.1.4, 2.2.1.6, 2.2.1.10, 2.2.1.11 for specific design-in.

Keep in mind that the use of rechargeable batteries requires the implementation of a suitable charger circuit which is not included in the modules. The charger circuit must be designed to prevent over-voltage on **VCC** pins, and it should be selected according to the application requirements: a DC/DC switching charger is the typical choice when the charging source has an high nominal voltage (e.g. ~12 V), whereas a linear charger is the typical choice when the charging source has a relatively low nominal voltage (~5 V). If both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as possible supply source, then a suitable charger / regulator with integrated power path management function can be selected to supply the module while simultaneously and independently charging the battery. See sections 2.2.1.7, 2.2.1.8, and 2.2.1.4, 2.2.1.6, 2.2.1.10, 2.2.1.11 for specific design-in.

An appropriate primary (not rechargeable) battery can be selected taking into account the maximum current specified in the TOBY-L3 series Data Sheet [1] during connected mode, considering that primary cells might have weak power capability. See sections 2.2.1.5, and 2.2.1.6, 2.2.1.10, 2.2.1.11 for specific design-in.

The usage of more than one DC supply at the same time should be evaluated carefully: depending on the supply source characteristics, different DC supply systems can result as mutually exclusive.

The usage of a regulator or a battery not able to support the highest peak of **VCC** current consumption specified in the TOBY-L3 series Data Sheet [1] is generally not recommended. However, if the selected regulator or battery is not able to support the highest peak current of the module, it must be able to support with adequate margin at least the highest averaged current consumption value specified in the TOBY-L3 series Data Sheet [1]. The additional energy required by the module during a 2G Tx slot can be provided by an appropriate bypass tank capacitor or a super-capacitor with very large capacitance and very low ESR placed close to the module **VCC** pins. Depending on the actual capability of the selected regulator or battery, the required capacitance can be considerably larger than 1 mF and the required ESR can be in the range of few tens of mΩ. Carefully evaluate the super-capacitor characteristics since aging and temperature may affect the actual characteristics.

The following sections highlight some design aspects for each of the supplies listed above providing application circuit design-in compliant with the module **VCC** requirements summarized in Table 7.

2.2.1.2 Guidelines for VCC supply circuit design using a switching regulator

The use of a switching DC/DC regulator is suggested when the difference from the available supply rail source to the **VCC** value is high, since switching regulators provide good efficiency transforming a 12 V or greater voltage supply to the typical 3.8 V value of the **VCC** supply.

The characteristics of the switching regulator connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 7:

- **Power capability**: the switching regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to **VCC** pins the maximum peak / pulse current consumption during Tx burst at maximum Tx power specified in the TOBY-L3 series Data Sheet [1].
- **Low output ripple**: the switching regulator together with its output circuit must be capable of providing a clean (low noise) **VCC** voltage profile.
- **High switching frequency:** for best performance and for smaller applications it is recommended to select a switching frequency ≥ 600 kHz (since L-C output filter is typically smaller for high switching frequency). The use of a switching regulator with a variable switching frequency or with a switching frequency lower than 600 kHz must be evaluated carefully since this can produce noise in **VCC** voltage profile and thus negatively impact modulation spectrum figure. An additional L-C low-pass filter between the switching regulator output to **VCC** supply pins can mitigate the ripple at the input of the module, but adds extra voltage drop due to resistive losses on series inductors.

Figure 22 and Table 18 show an example of a high reliability power supply circuit, where the module **VCC** input is supplied by a step-down switching regulator capable of delivering maximum current with low output ripple and with fixed switching frequency in PWM mode operation greater than 1 MHz.

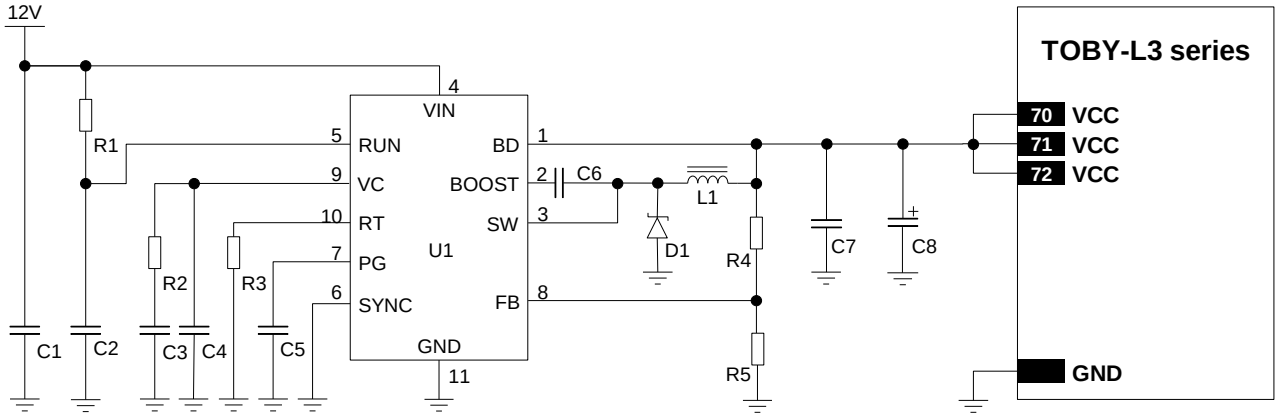

Figure 22: Example of high reliability VCC supply application circuit using a step-down regulator

Reference	Description	Part Number - Manufacturer
C1	10 µF Capacitor Ceramic X7R 5750 15% 50 V	C5750X7R1H106MB - TDK
C2	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	680 pF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71H681KA01 - Murata
C4	22 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H220JZ01 - Murata
C5	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C6	470 nF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E474KA12 - Murata
C7	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C8	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
D1	Schottky Diode 40 V 3 A	MBRA340T3G - ON Semiconductor
L1	10 µH Inductor 744066100 30% 3.6 A	744066100 - Wurth Electronics
R1	470 kΩ Resistor 0402 5% 0.1 W	2322-705-87474-L - Yageo
R2	15 kΩ Resistor 0402 5% 0.1 W	2322-705-87153-L - Yageo
R3	22 kΩ Resistor 0402 5% 0.1 W	2322-705-87223-L - Yageo
R4	390 kΩ Resistor 0402 1% 0.063 W	RC0402FR-07390KL - Yageo
R5	100 kΩ Resistor 0402 5% 0.1 W	2322-705-70104-L - Yageo
U1	Step-Down Regulator MSOP10 3.5 A 2.4 MHz	LT3972IMSE#PBF - Linear Technology

Table 18: Components for high reliability VCC supply application circuit using a step-down regulator

☞ See section 2.2.1.6, in particular Figure 24 / Table 20, for the additional parts recommended for noise-sensitive applications and/or for applications with antenna(s) placed close to the module.

2.2.1.3 Guidelines for VCC supply circuit design using a LDO linear regulator

The use of a linear regulator is suggested when the difference from the available supply rail source and the **VCC** value is low. The linear regulators provide high efficiency when transforming a 5 VDC supply to a voltage value within the module **VCC** normal operating range.

The characteristics of the Low Drop-Out (LDO) linear regulator connected to the **VCC** pins should meet the following prerequisites to comply with module **VCC** requirements summarized in Table 7:

- **Power capabilities**: the LDO linear regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to the **VCC** pins the maximum peak / pulse current consumption during Tx burst at maximum Tx power specified in the TOBY-L3 series Data Sheet [1].
- **Power dissipation**: the power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the maximum rated operating range (i.e. check the voltage drop from the maximum input voltage to the minimum output voltage to evaluate the power dissipation of the regulator).

Figure 23 and the components listed in Table 19 show an example of a power supply circuit where the **VCC** module supply is provided by an LDO linear regulator capable of delivering the required current with a suitable power handling capability.

It is recommended to consider configuring the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module **VCC** normal operating range (e.g. ~4.1 V for the **VCC**, as in the circuits illustrated in Figure 23 and Table 19). This reduces the power on the linear regulator and improves the thermal design of the circuit.

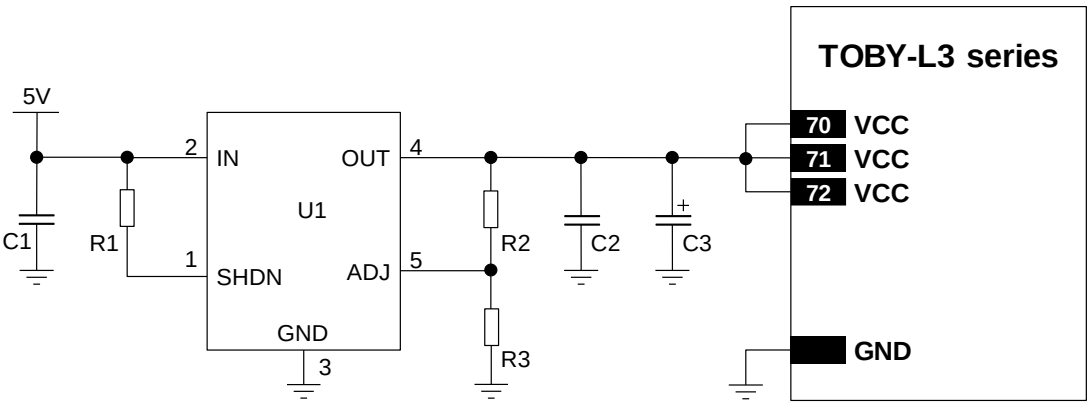

Figure 23: Example of high reliability VCC supply application circuit using an LDO linear regulator

Reference	Description	Part Number - Manufacturer
C1, C2	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
C3	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
R1	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
R2	9.1 kΩ Resistor 0402 5% 0.1 W	RC0402JR-079K1L - Yageo Phycomp

R3	3.9 kΩ Resistor 0402 5% 0.1 W	RC0402JR-073K9L - Yageo Phycomp
U1	LDO Linear Regulator ADJ 3.0 A	LT1764AEQ#PBF - Linear Technology

Table 19: Components for high reliability VCC supply application circuit using an LDO linear regulator

☞ See section 2.2.1.6, in particular Figure 24 / Table 20, for the additional parts recommended for noise-sensitive applications and/or for applications with antenna(s) placed close to the module.

2.2.1.4 Guidelines for VCC supply circuit design using a rechargeable battery

Rechargeable Li-Ion or Li-Pol batteries connected to the **VCC** pins should meet the following prerequisites to comply with the module's **VCC** requirements as summarized in Table 7:

- **Maximum pulse and DC discharge current**: the rechargeable Li-Ion battery with its related output circuit connected to the **VCC** pins must be capable of delivering a pulse current as the maximum peak / pulse current consumption during Tx burst at the maximum Tx power specified in TOBY-L3 series Data Sheet [1] and must be capable of extensively delivering a DC current as the maximum average current consumption as specified in the TOBY-L3 series Data Sheet [1]. The maximum discharge current is not always reported in the data sheets of batteries, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the rechargeable Li-Ion battery with its output circuit must be capable of avoiding a VCC voltage drop as recommended in Table 7 during transmit bursts.

2.2.1.5 Guidelines for VCC supply circuit design using a primary battery

The characteristics of a primary (non-rechargeable) battery connected to the **VCC** pins should meet the following prerequisites to comply with the module's **VCC** requirements as summarized in Table 7:

- **Maximum pulse and DC discharge current**: the non-rechargeable battery with its related output circuit connected to the **VCC** pins must be capable of delivering a pulse current as the maximum peak current consumption during Tx burst at the maximum Tx power specified in the TOBY-L3 series Data Sheet [1] and must be capable of extensively delivering a DC current as the maximum average current consumption as specified in the TOBY-L3 series Data Sheet [1]. The maximum discharge current is not always reported in the data sheets of batteries, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the non-rechargeable battery with its output circuit must be capable of avoiding a VCC voltage drop as recommended in Table 7 during transmit bursts.

2.2.1.6 Additional guidelines for VCC supply circuit design

To reduce voltage drops, use a low impedance power source. The series resistance of the supply lines (connected to modules' **VCC** and **GND** pins) on the application board and battery pack should also be considered and minimized: cabling and routing must be as short as possible to minimize losses.

Three pins are allocated to the **VCC** supply. Several pins are designated for **GND** connection. It is recommended to correctly connect all of them to supply the module to minimize series losses.

For modules supporting 2G radio access technology, to avoid voltage drop undershoot and overshoot at the start and end of a transmit burst during a GSM call (when current consumption on the **VCC** supply can rise up as specified in the TOBY-L3 series Data Sheet [1]), place the following bypass capacitor near the **VCC** pins (see Figure 24 / Table 20):

- a large capacitance (at least 100 µF) and low Equivalent Series Resistance (few mOhm) capacitor

To reduce voltage ripple and noise, improving RF performance especially in case an internal embedded antenna is used, place the following bypass capacitors near the **VCC** pins (see Figure 24 / Table 20):

- 68 pF 0402 capacitor with Self-Resonant Frequency in the 800/900 MHz range
- 15 pF 0402 capacitor with Self-Resonant Frequency in the 1800/1900 MHz range
- 8.2 pF 0402 capacitor with Self-Resonant Frequency in 2500/2600 MHz range
- 10 nF 0402 capacitor to filter digital logic noise from clocks and data sources
- 100 nF 0402 capacitor to filter digital logic noise from clocks and data sources

A suitable series ferrite bead can be correctly placed on the **VCC** line for additional noise filtering if required by the specific application according to the whole application board design.

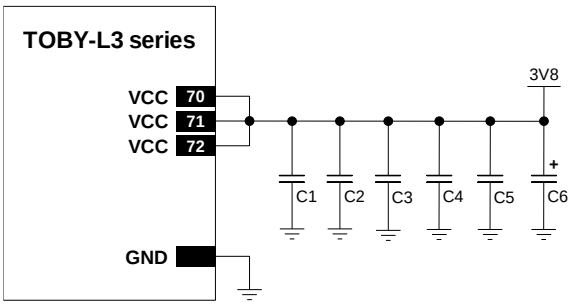

Figure 24: Suggested schematic for the VCC bypass capacitors to reduce ripple / noise on the supply voltage profile

Reference	Description	Part Number - Manufacturer
C1	8.2 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H8R2DZ01 - Murata
C2	15 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H150JA01 - Murata
C3	68 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C4	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
C6	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET

Table 20: Suggested components to reduce ripple / noise on the VCC

☞ The necessity of each part depends on the specific design, but it is recommended to provide all the bypass capacitors illustrated in Figure 24 / Table 20 for noise-sensitive applications and/or if the end-device integrates an internal antenna.

☞ The ESD sensitivity rating of the **VCC** supply pins is 1 kV (HBM as per JESD22-A114). A higher protection level can be required if the line is externally accessible on the application board, e.g. if the accessible battery connector is directly connected to the supply pins. A higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to the accessible point.

2.2.1.7 Guidelines for the external battery charging circuit

TOBY-L3 series modules do not have an on-board charging circuit. Figure 25 provides an example of a battery charger design which is suitable for applications that are battery powered with a Li-Ion (or Li-Polymer) cell.

In the application circuit, a rechargeable Li-Ion (or Li-Polymer) battery cell, that features the correct pulse and DC discharge current capabilities and the correct DC series resistance, is directly connected to the **VCC** supply input of the module. Battery charging is completely managed by the STMicroelectronics L6924U Battery Charger IC that, from a USB power source (5.0 V typ.), charges the battery as a linear charger, in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current.
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for USB power source (~500 mA).
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the L6924U starts to reduce the current until the charge termination is done. The charging process ends when the charging current reaches the value configured by an external resistor to ~15 mA or when the charging timer reaches the value configured by an external capacitor to ~9800 s.

Using a battery pack with an internal NTC resistor, the L6924U can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

The L6924U, as a linear charger, is more suitable for applications where the charging source has a relatively low nominal voltage (~5 V), so that a switching charger is suggested for applications where the charging source has a relatively high nominal voltage (e.g. ~12 V, see the following section 2.2.1.8 for the specific design-in).

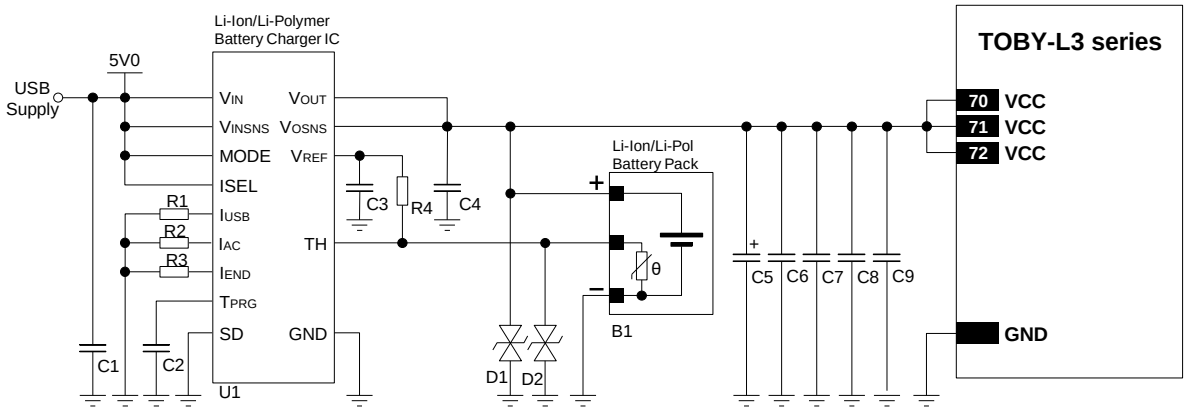

Figure 25: Li-Ion (or Li-Polymer) battery charging application circuit

Reference	Description	Part Number - Manufacturer
B1	Li-Ion (or Li-Polymer) battery pack with 470 Ω NTC	Various manufacturer
C1, C4	1 µF Capacitor Ceramic X7R 0603 10% 16 V	GRM188R71C105KA12 - Murata
C2, C6	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	1 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H102KA01 - Murata
C5	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C7	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C8	68 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C9	15 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H150JA01 - Murata
D1, D2	Low Capacitance ESD Protection	CG0402MLE-18G - Bourns
R1, R2	24 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0724KL - Yageo Phycomp
R3	3.3 kΩ Resistor 0402 5% 0.1 W	RC0402JR-073K3L - Yageo Phycomp
R4	1.0 kΩ Resistor 0402 5% 0.1 W	RC0402JR-071K0L - Yageo Phycomp
U1	Single Cell Li-Ion (or Li-Polymer) Battery Charger IC	L6924U - STMicroelectronics

Table 21: Suggested components for Li-Ion (or Li-Polymer) battery charging application circuit

2.2.1.8 Guidelines for external charging and power path management circuit

Application devices where both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as possible supply source should implement a suitable charger / regulator with integrated power path management function to supply the module and the whole device while simultaneously and independently charging the battery.

Figure 26 reports a simplified block diagram circuit showing the working principle of a charger / regulator with an integrated power path management function. This component allows the system to be powered by a permanent primary supply source (e.g. ~12 V) using the integrated regulator which simultaneously and independently recharges the battery (e.g. 3.7 V Li-Pol) that represents the back-up supply source of the system: the power path management feature permits the battery to supplement the system current requirements when the primary supply source is not available or cannot deliver the peak system current.

A power management IC should meet the following prerequisites to comply with the module's **VCC** requirements as summarized in Table 7:

- High efficiency internal step down converter, compliant with features specified in section 2.2.1.2
- Low internal resistance in the active path Vout – Vbat, typically lower than 50 mΩ
- High efficiency switch mode charger with separate power path control

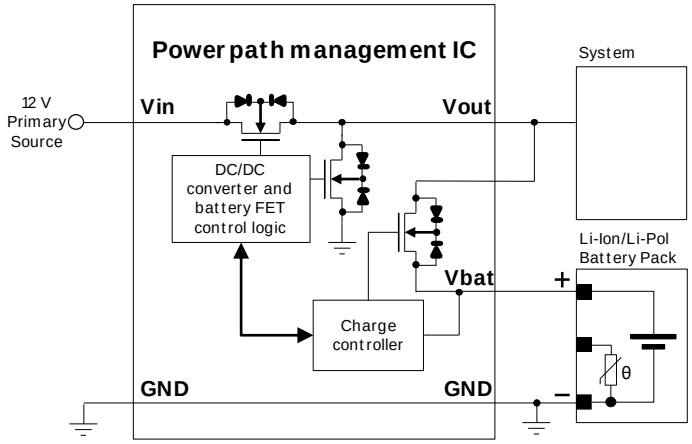

Figure 26: Charger / regulator with integrated power path management circuit block diagram

Figure 27 / Table 22 provide an application circuit example where the MPS MP2617H switching charger and regulator with integrated power path management provides the supply to the cellular module. At the same time it also concurrently and autonomously charges a suitable Li-Ion (or Li-Polymer) battery with the correct pulse and DC discharge current capabilities and the appropriate DC series resistance according to the rechargeable battery recommendations described in section 2.2.1.4.

The MP2617H IC constantly monitors the battery voltage and selects whether to use the external main primary supply / charging source or the battery as the supply source for the module, and starts a charging phase accordingly.

The MP2617H IC normally provides a supply voltage to the module regulated from the external main primary source allowing immediate system operation even under missing or deeply discharged battery: the integrated switching step-down regulator is capable to provide up to 3 A output current with low output ripple and fixed 1.6 MHz switching frequency in PWM mode operation. The module load is satisfied in priority, then the integrated switching charger will take the remaining current to charge the battery.

Additionally, the power path control allows an internal connection from the battery to the module with a low series internal ON resistance (40 mΩ typical), in order to supplement additional power to the module when the current demand increases over the external main primary source or when this external source is removed.

Battery charging is managed in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current.
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for the application.
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the current is progressively reduced until the charge termination is done. The charging process ends when the charging current reaches 10% of the fast-charge current or when the charging timer reaches the value configured by an external capacitor.

Using a battery pack with an internal NTC resistor, the MP2617H can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

Several parameters as the charging current, the charging timings, the input current limit, the input voltage limit, and the system output voltage, can be easily set according to the specific application requirements to the actual electrical characteristics of the battery and the external supply / charging source: suitable resistors or capacitors must be accordingly connected to the related pins of the IC.

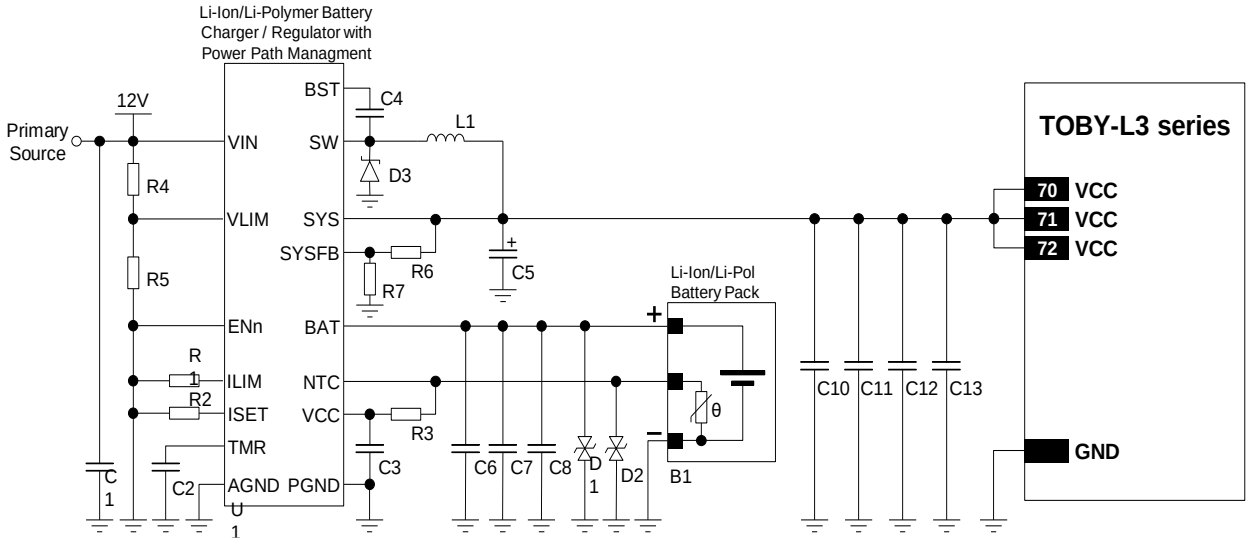

Figure 27: Li-Ion (or Li-Polymer) battery charging and power path management application circuit

Reference	Description	Part Number - Manufacturer
B1	Li-Ion (or Li-Polymer) battery pack with 10 kΩ NTC	Various manufacturer
C1, C6	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C2, C4, C10	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C3	1 µF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E105KA12 - Murata
C5	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C7, C12	68 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C8, C13	15 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata
C11	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata

D1, D2	Low Capacitance ESD Protection	CG0402MLE-18G - Bourns
D3	Schottky Diode 40 V 3 A	MBRA340T3G - ON Semiconductor
R1, R3, R5, R7	10 kΩ Resistor 0402 1% 1/16 W	Generic manufacturer
R2	1.05 kΩ Resistor 0402 1% 0.1 W	Generic manufacturer
R4	22 kΩ Resistor 0402 1% 1/16 W	Generic manufacturer
R6	26.5 kΩ Resistor 0402 1% 1/16 W	Generic manufacturer
L1	2.2 µH Inductor 7.4 A 13 mΩ 20%	SRN8040-2R2Y - Bourns
U1	Li-Ion/Li-Polymer Battery DC/DC Charger / Regulator with integrated Power Path Management function	MP2617H - Monolithic Power Systems (MPS)

Table 22: Suggested components for a Li-Ion (or Li-Pol) battery charging and power path management application circuit

2.2.1.9 Guidelines for removing VCC supply

As described in section 1.6.2, in particular in Figure 14 and Figure 15, the **VCC** supply can be removed after the end of TOBY-L3 series module's internal power-off sequence, which must be properly started as described in section 1.6.2.

Removing **VCC** power can be useful in order to minimize the power consumption when TOBY-L3 series modules are switched off. Then, the modules can be switched on again by re-applying **VCC** supply.

If the **VCC** supply is generated by a switching or an LDO regulator, the application processor may control the input pin of the regulator which is provided to enable / disable the output of the regulator (as for example, the RUN input pin for the regulator illustrated in Figure 22, or the SHDNn input pin for the regulator illustrated in Figure 23), in order to apply / remove the **VCC** supply.

If the regulator that generates the **VCC** supply does not provide an on / off pin, or for other applications such as the battery-powered ones, the **VCC** supply can be switched off using an appropriate external p-channel MOSFET controlled by the application processor by means of a suitable inverting transistor as shown in Figure 28, given that the external p-channel MOSFET has provided:

- Very low $R_{DS(ON)}$ (for example, less than 50 mΩ), to minimize voltage drops
- Adequate maximum Drain current (see TOBY-L3 series Data Sheet [1] for consumption figures)
- Low leakage current, to minimize the current consumption

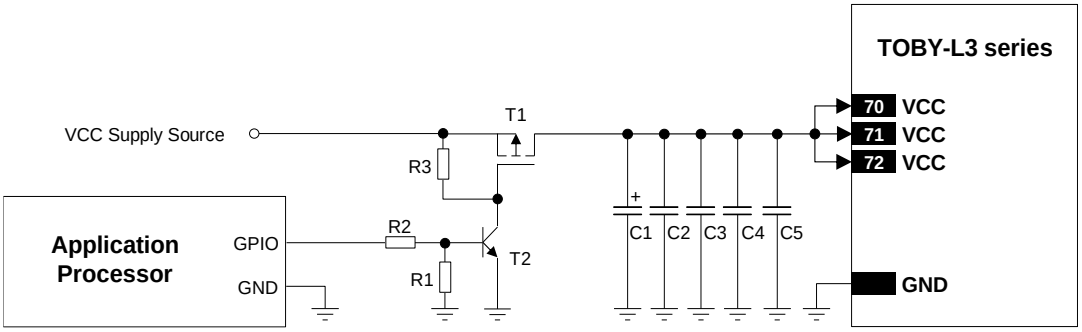

Figure 28: Example of application circuit for VCC supply removal

Reference	Description	Part Number - Manufacturer
R1	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
R2	10 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0710KL - Yageo Phycomp
R3	100 kΩ Resistor 0402 5% 0.1 W	RC0402JR-07100KL - Yageo Phycomp
T1	P-Channel MOSFET Low On-Resistance	AO3415 - Alpha & Omega Semiconductor Inc.
T2	NPN BJT Transistor	BC847 - Infineon
C1	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C2	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C4	56 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E560JA01 - Murata
C5	15 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata

Table 23: Components for VCC supply removal application circuit

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply during the TOBY-L3 series module's normal operations: the power off procedure must be started as described in section 1.6.2, and then a suitable **VCC** supply must be held at least until the end of the modules' internal power off sequence, which occurs when the generic digital interfaces supply output (**V_INT**) is switched off by the module.

2.2.1.10 Guidelines for VCC supply layout design

A clean connection of the module **VCC** pins with a DC supply source is required for correct RF performance. Guidelines are summarized in the following list:

- All the available **VCC** pins must be connected to the DC source.
- **VCC** connection must be as wide as possible and as short as possible.
- Any series component with Equivalent Series Resistance (ESR) greater than few milliohms must be avoided.
- **VCC** connection must be routed through a PCB area separated from RF lines / parts, sensitive analog signals and sensitive functional units: it is good practice to interpose at least one layer of PCB ground between the **VCC** track and other signal routing.
- Coupling between **VCC** and digital lines, especially USB, must be avoided.
- The tank bypass capacitor with low ESR for current spikes smoothing described in section 2.2.1.6 should be placed close to the **VCC** pins. If the main DC source is a switching DC-DC converter, place the large capacitor close to the DC-DC output and minimize the **VCC** track length. Otherwise consider using separate capacitors for the DC-DC converter and module tank capacitor.
- The bypass capacitors in the pF range illustrated in Figure 24 and Table 20 should be placed as close as possible to the **VCC** pins, where the **VCC** line narrows close to the module input pins, improving the RF

noise rejection in the band centered on the Self-Resonant Frequency of the pF capacitors. This is highly recommended if the application device integrates an internal antenna.

- Since **VCC** input provides the supply to the RF Power Amplifiers, any voltage ripple at high frequency may result in unwanted spurious modulation of the transmitter RF signal. This is more likely to happen with switching DC-DC converters, in which case it is better to select the highest operating frequency for the switcher and add a large L-C filter before connecting to the TOBY-L3 series modules in the worst case.
- Shielding of switching DC-DC converter circuit, or at least the use of shielded inductors for the switching DC-DC converter, may be considered since all switching power supplies may potentially generate interfering signals as a result of high-frequency high-power switching.
- If the **VCC** is protected by a transient voltage suppressor to ensure that the voltage maximum ratings are not exceeded, place the protecting device along the path from the DC source toward the module, preferably close to the DC source, otherwise protection functionality may be affected.

2.2.1.11 Guidelines for grounding layout design

A clean connection of the module **GND** pins with the application board solid ground layer is required for correct RF performance. It significantly reduces EMC issues and provides a thermal heat sink for the module.

- Connect each **GND** pin with the application board solid GND layer. It is strongly recommended that each **GND** pad surrounding the **VCC** pins has one or more dedicated via down to the application board solid ground layer.
- The **VCC** supply current flows back to the main DC source through GND as the ground current: provide an adequate return path with suitable uninterrupted ground plane to the main DC source.
- It is recommended to design one layer of the application PCB as a ground plane as wide as possible.
- If the application board is a multilayer PCB, then all the board layers should be filled with GND plane as much as possible and each GND area should be connected together with a complete via stack down to the main ground layer of the board.
- If the whole application device is composed of more than one PCB, then it is required to provide a good and solid ground connection between the GND areas of all the multiple PCBs.
- Good grounding of the **GND** pads also ensures the thermal heat sink. This is critical during connection, when the real network commands the module to transmit at maximum power: correct grounding helps prevent module overheating.

2.2.2 Generic digital interfaces supply output (V_INT)

2.2.2.1 Guidelines for V_INT circuit design

TOBY-L3 series provide the **V_INT** generic digital interfaces 1.8 V supply output, which can be mainly used to:

- Indicate when the module is switched on (as described in sections 1.6.1, 1.6.2)

- Pull-up SIM detection signal (see section 2.5 for more details)
- Supply voltage translators to connect 1.8 V module generic digital interfaces to 3.0 V devices (e.g. see section 2.6.1 for more details)
- Pull-up DDC (I^2C) interface signals (see section 2.6.4 for more details)
- Supply a 1.8 V u-blox GNSS device (see section 2.6.4 for more details)
- Enable external voltage regulators providing supply for external devices, as linear LDO regulators providing the 3.3 V / 1.8 V supply rails for a u-blox EMMY-W1 series module (see section 2.6.5 for more details)
- Supply an external device as an external 1.8 V audio codec (see section 2.8 for more details)

The **V_INT** supply output pin provides internal short circuit protection to limit the start-up current and protect the device in short circuit situations. No additional external short circuit protection is required.

☞ Do not apply loads which might exceed the limit for the maximum available current from **V_INT** supply (see TOBY-L3 series Data Sheet [1]) as this can cause malfunctions in the internal circuitry.

☞ Since the **V_INT** supply is generated by an internal switching step-down regulator (the **V_INT** voltage ripple can range as specified in the TOBY-L3 series Data Sheet [1]), it is not recommended to supply sensitive analog circuitry without adequate filtering for digital noise.

☞ **V_INT** can only be used as an output: do not connect any external supply source on **V_INT**.

☞ The ESD sensitivity rating of the **V_INT** supply pin is 1 kV (Human Body Model according to JESD22-A114). A higher protection level could be required if the line is externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible point.

☞ It is recommended to monitor the **V_INT** pin to sense the end of the internal switch-off sequence of TOBY-L3 series modules: the **VCC** supply can be removed only after **V_INT** goes low

☞ It is recommended to provide direct access to the **V_INT** pin on the application board by means of an accessible test point directly connected to the **V_INT** pin, for diagnostic purposes.

2.3 System functions interfaces

2.3.1 Module power-on (PWR_ON)

2.3.1.1 Guidelines for PWR_ON circuit design

TOBY-L3 series **PWR_ON** input is equipped with an internal active pull-up resistor to an internal 1.3 V supply rail as shown in Figure 29: an external pull-up resistor is not required and should not be provided.

If connecting the **PWR_ON** input to a push button, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection should be provided close to the accessible point, as shown in Figure 29 and Table 24.

☞ The ESD sensitivity rating of the **PWR_ON** pin is 1 kV (HBM according to JESD22-A114). A higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to the **PWR_ON** pin, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to the accessible point.

An open drain or open collector output is suitable to drive the **PWR_ON** input from an application processor, as the pin is equipped with an internal active pull-up resistor, as shown in Figure 29.

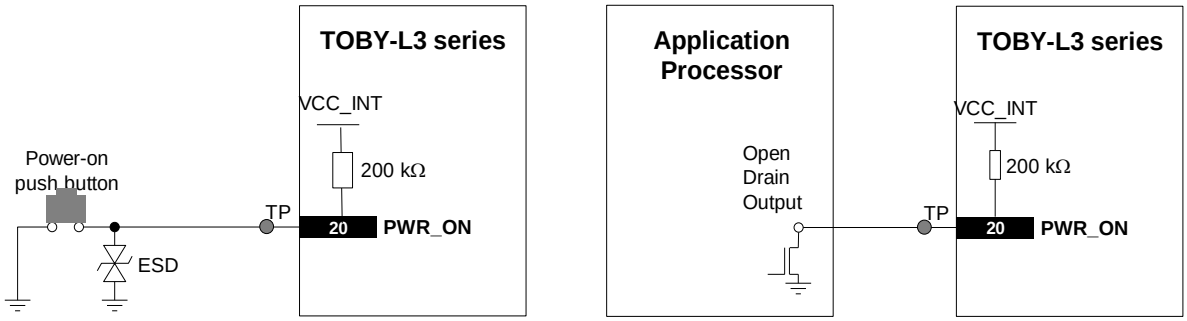

Figure 29: PWR_ON application circuits using a push button and an open drain output of an application processor

Reference	Description	Part Number - Manufacturer
ESD	CT0402S14AHSG - EPCOS	Varistor array for ESD protection

Table 24: Example ESD protection component for the PWR_ON application circuit

☞ It is recommended to provide direct access to the **PWR_ON** pin on the application board by means of an accessible test point directly connected to the **PWR_ON** pin, for diagnostic purposes.

2.3.1.2 Guidelines for PWR_ON layout design

The power-on circuit (**PWR_ON**) requires careful layout since it is the sensitive input available to switch on the TOBY-L3 series modules. It is required to ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious power-on request.

2.3.2 Module reset (RESET_N)

2.3.2.1 Guidelines for RESET_N circuit design

TOBY-L3 series **RESET_N** line is equipped with an internal pull-up to the **V_INT** supply as shown in Figure 30. An external pull-up resistor is not required.

If connecting the **RESET_N** input to a push button, the pin will be externally accessible on the application device. According to the EMC/ESD requirements of the application, an additional ESD protection device (e.g. the EPCOS CA05P4S14THSG varistor) should be provided close to the accessible point on the line connected to this pin, as shown in Figure 30 and Table 25.

☞ The ESD sensitivity rating of the **RESET_N** pin is 1 kV (HBM according to JESD22-A114). A higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to the **RESET_N** pin, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to the accessible point.

An open drain output is suitable to drive the **RESET_N** input from an application processor as it is equipped with an internal pull-up to **V_INT** supply, as shown in Figure 30.

A compatible push-pull output of an application processor can also be used. In any case, take care to set the correct level in all the possible scenarios to avoid an inappropriate module reset.

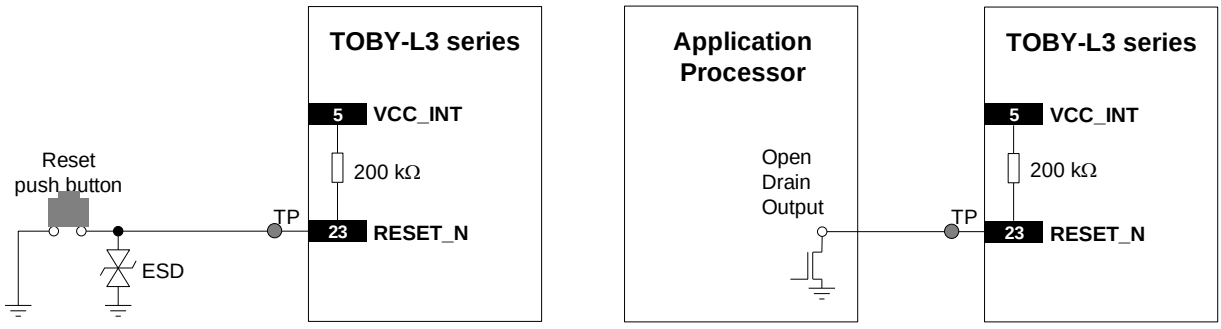

Figure 30: RESET_N application circuits using a push button and an open drain output of an application processor

Reference	Description	Part Number - Manufacturer
ESD	Varistor for ESD protection	CT0402S14AHSG - EPCOS

Table 25: Example of ESD protection component for the RESET_N application circuits

☞ If the external reset function is not required by the customer application, the **RESET_N** pin can be left unconnected to external components, but it is recommended to provide direct access on the application board by means of an accessible test point directly connected to the **RESET_N** pin.

2.3.2.2 Guidelines for RESET_N layout design

The **RESET_N** circuit requires careful layout due to the pin function: ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious reset request. It is recommended to keep the connection line to the **RESET_N** pin as short as possible.

2.3.3 Module / host configuration selection

☞ Host Select pins are not supported by the "0x" product feature version.

2.3.3.1 Guidelines for HOST_SELECTx circuit design

TOBY-L3 series modules include two 1.8 V digital pins (**HOST_SELECT0**, **HOST_SELECT1**), which can be configured for External Interrupt detection or as GPIO by means of the open CPU API: the pins can be connected to external devices following the guidelines provided in section 2.10.

☞ Do not apply voltage to the **HOST_SELECT0** and **HOST_SELECT1** pins before the switch-on of their supply source (**V_INT**), to avoid latch-up of circuits and allow a correct boot of the module.

☞ The ESD sensitivity rating of the **HOST_SELECT0** and **HOST_SELECT1** pins is 1 kV (HBM as per JESD22-A114). A higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible points.

☞ If the functionality of the **HOST_SELECT0** and **HOST_SELECT1** pins is not required, the pins can be left unconnected on the application board.

2.3.3.2 Guidelines for HOST_SELECTx layout design

The design for **HOST_SELECT0** and **HOST_SELECT1** pins functions is generally not critical for layout.

2.4 Antenna interface

TOBY-L3 series modules provide two RF interfaces for connecting the external antennas:

- The **ANT1** pin represents the primary RF input/output for RF signals transmission and reception.
- The **ANT2** pin represents the secondary RF input for MIMO and Rx diversity RF signals reception.

Both the **ANT1** and the **ANT2** pins have a nominal characteristic impedance of 50 Ω and must be connected to the related antenna through a 50 Ω transmission line to allow correct transmission / reception of RF signals.

☞ Two antennas (one connected to **ANT1** pin and one connected to **ANT2** pin) must be used to support the MIMO and Rx diversity configurations. This is a required feature for LTE category 4 User Equipment (up to 150 Mbit/s Down-Link data rate) according to the 3GPP specifications.

2.4.1 Antenna RF interfaces (ANT1 / ANT2)

2.4.1.1 General guidelines for antenna selection and design

The antenna is the most critical component to be evaluated. Designers must take care of the antennas from all perspectives at the very start of the design phase when the physical dimensions of the application board are under analysis/decision, since the RF compliance of the device integrating TOBY-L3 series modules with all the applicable required certification schemes depends on the antenna radiating performance.

LTE/3G/2G antennas are typically available in the types of linear monopole or PCB antennas such as patches or ceramic SMT elements.

- External antennas (e.g. linear monopole)
  - External antennas basically do not imply a physical restriction to the design of the PCB where the TOBY-L3 series module is mounted.
  - The radiation performance mainly depends on the antennas. It is required to select antennas with optimal radiating performance in the operating bands.
  - RF cables should be carefully selected to have minimum insertion losses. Additional insertion loss will be introduced by low quality or long cable. Large insertion loss reduces both transmit and receive radiation performance.
  - A high quality 50 Ω RF connector provides suitable PCB-to-RF-cable transition. It is recommended to strictly follow the layout and cable termination guidelines provided by the connector manufacturer.
- Integrated antennas (e.g. patch-like antennas):
  - Internal integrated antennas imply a physical restriction to the design of the PCB:

    An integrated antenna excites RF currents on its counterpoise, typically the PCB ground plane of the device that becomes part of the antenna: its dimension defines the minimum frequency that

can be radiated. Therefore, the ground plane can be reduced down to a minimum size that should be similar to the quarter of the wavelength of the minimum frequency that must be radiated, given that the orientation of the ground plane relative to the antenna element must be considered.

The isolation between the primary and the secondary antennas must be as high as possible and the correlation between the 3D radiation patterns of the two antennas must be as low as possible. In general, a separation of at least a quarter wavelength between the two antennas is required to achieve a good isolation and low pattern correlation.

As a numerical example, the physical restriction to the PCB design can be considered as following:

Frequency = 750 MHz → Wavelength = 40 cm → Minimum GND plane size = 10 cm

- Radiation performance depends on the whole PCB and antenna system design, including product mechanical design and usage. Antennas should be selected with optimal radiating performance in the operating bands according to the mechanical specifications of the PCB and the whole product.
- It is recommended to select a pair of custom antennas designed by an antennas' manufacturer if the required ground plane dimensions are very small (less than 6.5 cm long and 4 cm wide). The antenna design process should begin at the start of the whole product design process.
- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, antennas may require tuning to obtain the required performance for compliance with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for the design-in guidelines for antenna matching relative to the custom application.

In both cases, selecting external or internal antennas, these recommendations should be observed:

- Select antennas providing optimal return loss (VSWR) figures over all the operating frequencies.
- Select antennas providing optimal efficiency figures over all the operating frequencies.
- Select antennas providing similar efficiency for both the primary (**ANT1**) and the secondary (**ANT2**) antenna.
- Select antennas providing appropriate maximum gain figures (i.e. combined antenna directivity and efficiency figures) so that the in-band radiation intensity does not exceed the regulatory limits specified by local authorities.
- Select antennas capable of providing a low Envelope Correlation Coefficient between the primary (**ANT1**) and the secondary (**ANT2**) antenna: the 3D antenna radiation patterns should have lobes in different directions.

2.4.1.2 Guidelines for antenna RF interface design

Guidelines for ANT1 / ANT2 pins RF connection design

Correct transition between **ANT1** / **ANT2** pads and application board must be provided, implementing the following design-in guidelines for the application PCB layout close to the **ANT1** / **ANT2** pads:

- On a multilayer board, the whole layer stack below the RF connection should be free of digital lines.
- Increase GND keep-out (i.e. clearance, a void area) around the **ANT1** / **ANT2** pads, on the top layer of the application PCB, to at least 250 µm up to the adjacent pads metal definition and up to 400 µm on the area below the module, to reduce parasitic capacitance to ground, as shown in the left example of Figure 31.
- Add GND keep-out (i.e. clearance, a void area) on the buried metal layer below the **ANT1** / **ANT2** pads if the top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground, as shown in the right example of Figure 31.

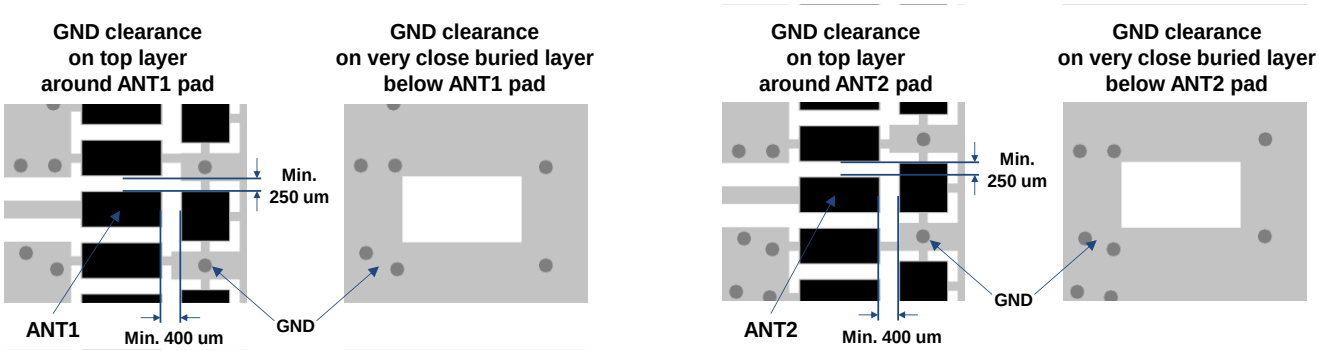

Figure 31: GND keep-out area on top layer around ANT1 / ANT2 pads and on very close buried layer below ANT1 / ANT2 pads

Guidelines for RF transmission line design

Any RF transmission line, such as the ones from the **ANT1** and **ANT2** pads up to the related antenna connector or up to the related internal antenna pad, must be designed so that the characteristic impedance is as close as possible to 50 Ω.

RF transmission lines can be designed as a micro strip (consists of a conducting strip separated from a ground plane by a dielectric material) or a strip line (consists of a flat strip of metal which is sandwiched between two parallel ground planes within a dielectric material). The micro strip, implemented as a coplanar waveguide, is the most common configuration for printed circuit boards.

Figure 32 and Figure 33 provide two examples of suitable 50 Ω coplanar waveguide designs. The first example of an RF transmission line can be implemented for a 4-layer PCB stack-up herein illustrated, and the second example of an RF transmission line can be implemented for a 2-layer PCB stack-up herein illustrated.

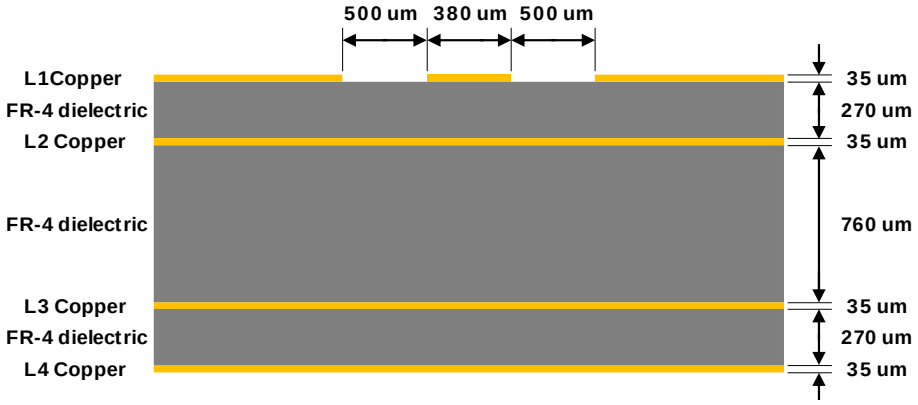

Figure 32: Example of a 50 Ω coplanar waveguide transmission line design for the described 4-layer board layup

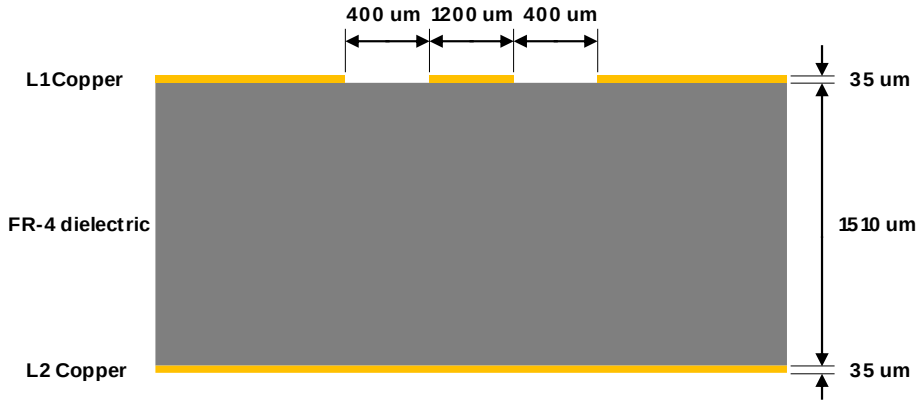

Figure 33: Example of a 50 Ω coplanar waveguide transmission line design for the described 2-layer board layup

If the two examples do not match the application PCB stack-up, the 50 Ω characteristic impedance calculation can be made using the HFSS commercial finite element method solver for electromagnetic structures from Ansys Corporation, or using freeware tools like Avago / Broadcom AppCAD (https://www.broadcom.com/appcad), taking care of the approximation formulas used by the tools for the impedance computation.

To achieve a 50 Ω characteristic impedance, the width of the transmission line must be chosen depending on:

- the thickness of the transmission line itself (e.g. 35 µm in the examples of Figure 32 / Figure 33)
- the thickness of the dielectric material between the top layer (where the transmission line is routed) and the inner closer layer implementing the ground plane (e.g. 270 µm in Figure 32, 1510 µm in Figure 33)
- the dielectric constant of the dielectric material (e.g. dielectric constant of the FR-4 dielectric material in Figure 32 and Figure 33)
- the gap from the transmission line to the adjacent ground plane on the same layer of the transmission line (e.g. 500 µm in Figure 32, 400 µm in Figure 33)

If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the track width of the micro strip, use the "Coplanar Waveguide" model for the 50 Ω calculation.

Additionally to the 50 Ω impedance, the following guidelines are recommended for transmission line design:

- Minimize the transmission line length: the insertion loss should be minimized as much as possible, in the order of a few tenths of a dB.
- Add GND keep-out (i.e. clearance, a void area) on buried metal layers below any pad of a component present on the RF transmission lines, if the top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground.
- The transmission lines width and spacing to GND must be uniform and routed as smoothly as possible: avoid abrupt changes of width and spacing to GND.
- Add GND stitching vias around the transmission lines, as shown in Figure 34.
- Ensure a solid metal connection of the adjacent metal layer on the PCB stack-up to the main ground layer, providing enough vias on the adjacent metal layer, as shown in Figure 34.
- Route RF transmission lines far from any noise source (as switching supplies and digital lines) and from any sensitive circuit (as USB).
- Avoid stubs on the transmission lines.
- Avoid signal routing in parallel to the transmission lines or crossing the transmission lines on a buried metal layer.
- Do not route the microstrip lines below discrete components or other mechanics placed on the top layer.

An example of a suitable RF circuit design is illustrated in Figure 34. In this case, the **ANT1** and **ANT2** pins are directly connected to SMA connectors by means of suitable 50 Ω transmission lines, designed with a suitable layout.

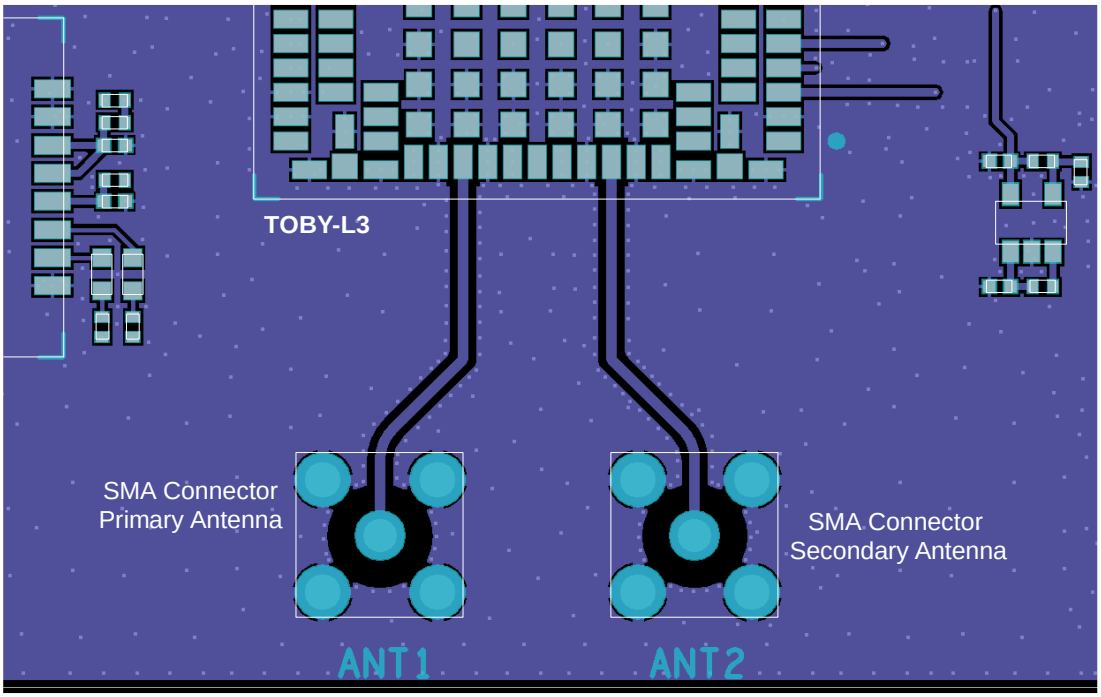

Figure 34: Example of the circuit and layout for antenna RF circuits on the application board

Guidelines for RF termination design

RF terminations must provide a characteristic impedance of 50 Ω as well as the RF transmission lines up to the RF terminations themselves, to match the characteristic impedance of the **ANT1** / **ANT2** ports of the modules.

However, real antennas do not have a perfect 50 Ω load on all the supported frequency bands. Therefore, to reduce as much as possible any performance degradation due to antennas mismatch, the RF terminations must provide optimal return loss (or VSWR) figures over all the operating frequencies, as summarized in Table 8 and Table 9.

If external antennas are used, the antenna connectors represent the RF termination on the PCB:

- Use suitable 50 Ω connectors providing a correct PCB-to-RF-cable transition.
- Strictly follow the connector manufacturer's recommended layout, for example:
  - SMA pin-through-hole connectors require GND keep-out (i.e. clearance, a void area) on all layers around the central pin up to the annular pads of the four GND posts, as shown in Figure 34.
  - U.FL surface-mounted connectors require no conductive traces (i.e. clearance, a void area) in the area below the connector between the GND land pads.
- Cut out the GND layer under RF connectors and close to buried vias, in order to remove stray capacitance and thus keep the RF line 50 Ω, e.g. the active pad of U.FL connectors needs to have a GND keep-out (i.e. clearance, a void area) at least on the first inner layer to reduce parasitic capacitance to ground.

If integrated antennas are used, the RF terminations are represented by the integrated antennas themselves. The following guidelines should be followed:

- Use antennas designed by an antenna manufacturer, providing the best possible return loss (or VSWR).
- Provide a ground plane large enough according to the relative integrated antenna requirements. The ground plane of the application PCB can be reduced down to a minimum size that must be similar to one quarter of a wavelength of the minimum frequency that must be radiated. As a numerical example,
  Frequency = 750 MHz → Wavelength = 40 cm → Minimum GND plane size = 10 cm
- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, antennas may require a tuning to comply with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for the design-in guidelines for the antenna matching relative to the custom application.

Additionally, these recommendations regarding the antenna system placement must be followed:

- Do not place antennas within a closed metal case.
- Do not place the antennas in close vicinity to the end user since the emitted radiation in human tissue is limited by regulatory requirements.

- Place the antennas far from sensitive analog systems or employ countermeasures to reduce EMC issues.
- Take care of interaction between co-located RF systems since the LTE/3G/2G transmitted power may interact or disturb the performance of companion systems.
- Place the two LTE antennas providing low Envelope Correlation Coefficient (ECC) between the primary (**ANT1**) and secondary (**ANT2**) antenna: the antenna 3D radiation patterns should have lobes in different directions. The ECC between the primary and secondary antennas needs to be low enough to comply with the radiated performance requirements specified by related certification schemes, as indicated in Table 10.
- Place the two LTE antennas providing enough high isolation (see Table 10) between the primary (**ANT1**) and secondary (**ANT2**) antennas. The isolation depends on the distance between antennas (separation of at least a quarter wavelength required for good isolation), antenna type (using antennas with different polarization improves isolation), and the antenna 3D radiation patterns (uncorrelated patterns improve isolation).

Examples of antennas

Table 26 lists some examples of possible internal on-board surface-mount antennas.

Manufacturer	Part Number	Product Name	Description
Taoglas	PA.710.A	Warrior	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 40.0 x 6.0 x 5.0 mm
Taoglas	PA.711.A	Warrior II	GSM / WCDMA / LTE SMD Antenna Pairs with the Taoglas PA.710.A Warrior for LTE MIMO applications 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 40.0 x 6.0 x 5.0 mm
Antenova	SR4L002	Lucida	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 35.0 x 8.5 x 3.2 mm

Table 26: Examples of internal surface-mount antennas

Table 27 lists some examples of possible internal off-board PCB-type antennas with cable and connector.

Manufacturer	Part Number	Product Name	Description
Taoglas	FXUB63.07.0150C		GSM / WCDMA / LTE PCB Antenna with cable and U.FL 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2690 MHz 96.0 x 21.0 mm
Taoglas	FXUB66.07.0150C	Maximus	GSM / WCDMA / LTE PCB Antenna with cable and U.FL 698..960 MHz, 1390..1435 MHz, 1575.42 MHz, 1710..2170 MHz, 2300..2700 MHz, 3400..3600 MHz, 4800..6000 MHz

			120.2 x 50.4 mm
Taoglas	FXUB70.A.07.C.001		GSM / WCDMA / LTE PCB MIMO Antenna with cables and U.FL 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2690 MHz 182.2 x 21.2 mm
EAD	FSQS35241-UF-10	SQ7	GSM / WCDMA / LTE PCB Antenna with cable and U.FL 690..960 MHz, 1710..2170 MHz, 2500..2700 MHz 110.0 x 21.0 mm
Ethertronics	5001537	Prestta	GSM / WCDMA / LTE PCB Antenna with cable 704..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2500..2690 MHz 80.0 x 18.0 mm

Table 27: Examples of internal antennas with cable and connector

Table 28 lists some examples of possible external antennas.

Manufacturer	Part Number	Product Name	Description
Taoglas	GSA.8827.A.101111	Phoenix	GSM / WCDMA / LTE adhesive-mount antenna with cable and SMA(M) 698..960 MHz, 1575.42 MHz, 1710..2700 MHz 105 x 30 x 7.7 mm
Taoglas	MA241.BI.001	Genesis	GSM / WCDMA / LTE MIMO 2-in-1 adhesive-mount combination antenna waterproof IP67 rated with cable and SMA(M) 698..960 MHz, 1710..2690 MHz 205.8 x 58 x 12.4 mm
Laird Tech.	TRA6927M3PW-001		GSM / WCDMA / LTE screw-mount antenna with N-type(F) 698..960 MHz, 1710..2170 MHz, 2300..2700 MHz 83.8 x Ø 36.5 mm
Laird Tech.	OC69271-FNM		GSM / WCDMA / LTE pole-mount antenna with N-type(M) 698..960 MHz, 1710..2690 MHz 248 x Ø 24.5 mm
Laird Tech.	CMD69273-30NM		GSM / WCDMA / LTE ceiling-mount MIMO antenna with cables & N-type(M) 698..960 MHz, 1710..2700 MHz 43.5 x Ø 218.7 mm
Pulse Electronics	WA700/2700SMA		GSM / WCDMA / LTE clip-mount MIMO antenna with cables and SMA(M) 698..960 MHz,1710..2700 MHz 149 x 127 x 5.1 mm

Table 28: Examples of external antennas

2.4.2 Antenna detection interface (ANT_DET)

2.4.2.1 Guidelines for ANT_DET circuit design

Figure 35 and Table 29 describe the recommended schematic / components for the antennas detection circuit that must be provided on the application board and for the diagnostic circuit that must be provided on the antennas' assembly to achieve primary and secondary antenna detection functionality.

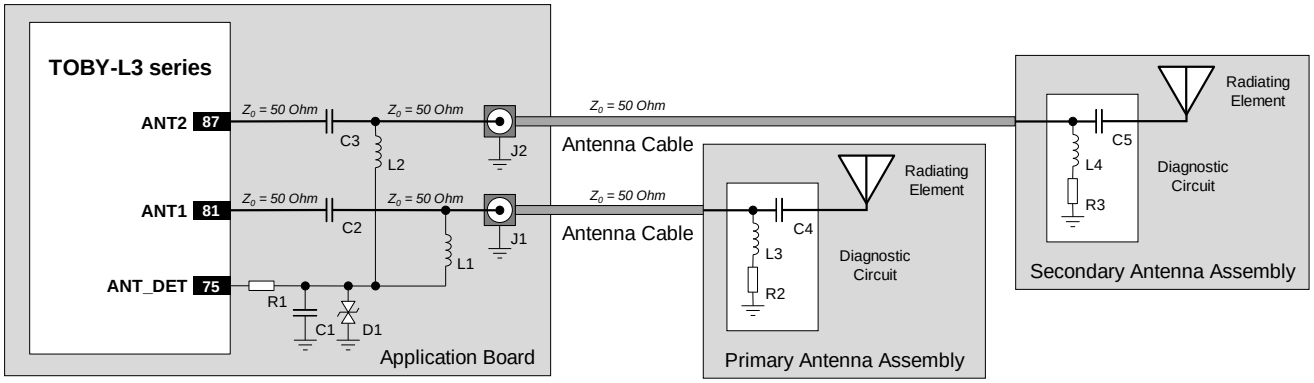

Figure 35: Schematic example for antenna detection circuit on application PCB and diagnostic circuit on antennas assembly

Reference	Description	Part Number - Manufacturer
C1	27 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H270J - Murata
C2, C3	33 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H330J - Murata
D1	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
L1, L2	68 nH Multilayer Inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R1	10 kΩ Resistor 0402 1% 0.063 W	RK73H1ETTP1002F - KOA Speer
J1, J2	SMA Connector 50 Ω Through Hole Jack	SMA6251A1-3GT50G-50 - Amphenol
C4, C5	22 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H220J - Murata
L3, L4	68 nH Multilayer Inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R2, R3	15 kΩ Resistor for Diagnostic	Various Manufacturers

Table 29: Example of parts for antenna detection circuit on application PCB and diagnostic circuit on antennas assembly

The antenna detection circuit and diagnostic circuit suggested in Figure 35 and Table 29 are explained here:

- When antenna detection is forced by the AT+UANTR command, **ANT_DET** generates a DC current measuring the resistance (R2 // R3) from the antenna connectors (J1, J2) provided on the application board to GND.
- DC blocking capacitors are needed at the **ANT1** / **ANT2** pins (C2, C3) and at the antenna radiating element (C4, C5) to decouple the DC current generated by the **ANT_DET** pin.
- Choke inductors with a Self-Resonance Frequency (SRF) in the range of 1 GHz are needed in series at the **ANT_DET** pin (L1, L2) and in series at the diagnostic resistor (L3, L4), to avoid a reduction of the RF performance of the system, improving the RF isolation of the load resistor.

- Additional components (R1, C1 and D1 in Figure 35) are needed at the **ANT_DET** pin as ESD protection.
- The **ANT1** / **ANT2** pins must be connected to the antenna connector by means of a transmission line with a nominal characteristic impedance as close as possible to 50 Ω.

The DC impedance at the RF port for some antennas may be a DC open (e.g. linear monopole) or a DC short to reference GND (e.g. PIFA antenna). For those antennas without the diagnostic circuit of Figure 35, the measured DC resistance is always at the limits of the measurement range (respectively open or short), and there is no means to distinguish between a defect on the antenna path with similar characteristics (respectively: removal of linear antenna or RF cable shorted to GND for a PIFA antenna).

Furthermore, any other DC signal injected to the RF connection from an ANT connector to a radiating element will alter the measurement and produce invalid results for antenna detection.

☞ It is recommended to use an antenna with a built-in diagnostic resistor in the range from 5 kΩ to 30 kΩ to assure good antenna detection functionality and avoid a reduction of module RF performance. The choke inductor should exhibit a parallel Self Resonance Frequency (SRF) in the range of 1 GHz to improve the RF isolation of the load resistor.

For example:

Consider an antenna with a built-in DC load resistor of 15 kΩ. Using the +UANTR AT command, the module reports the resistance value evaluated from the antenna connector provided on the application board to GND:

- Reported values close to the used diagnostic resistor nominal value (i.e. values from 13 kΩ to 17 kΩ if a 15 kΩ diagnostic resistor is used) indicate that the antenna is properly connected.
- Values close to the measurement range maximum limit (approximately 50 kΩ) or an open-circuit "over range" report (see the TOBY-L3 series AT Commands Manual [2]) means that that the antenna is not connected or the RF cable is broken.
- Reported values below the measurement range minimum limit (1 kΩ) indicate a short to GND at the antenna or along the RF cable.
- Measurement inside the valid measurement range and outside the expected range may indicate an incorrect connection, damaged antenna or wrong value of antenna load resistor for diagnostics.
- The reported value could differ from the real resistance value of the diagnostic resistor mounted inside the antenna assembly due to the antenna cable length, the antenna cable capacity or the measurement method used.

☞ If the primary / secondary antenna detection function is not required by the customer application, the **ANT_DET** pin can be left unconnected and the **ANT1** / **ANT2** pins can be directly connected to the related antenna connector by means of a 50 Ω transmission line as shown in Figure 34.

2.4.2.2 Guidelines for ANT_DET layout design

The recommended layout for the primary antenna detection circuit to be provided on the application board to achieve the primary antenna detection functionality, implementing the recommended schematic illustrated in Figure 35 and Table 29, is explained here:

- The **ANT1** / **ANT2** pins must be connected to the antenna connector by means of a 50 Ω transmission line, implementing the design guidelines described in section 2.4.1 and the recommendations of the SMA connector manufacturer.
- DC blocking capacitor at **ANT1** / **ANT2** pins (C2, C3) must be placed in series to the 50 Ω RF line.
- The **ANT_DET** pin must be connected to the 50 Ω transmission line by means of a sense line.
- Choke inductors in series at the **ANT_DET** pin (L1, L2) must be placed so that one pad is on the 50 Ω transmission line and the other pad represents the start of the sense line to the **ANT_DET** pin.
- The additional components (R1, C1 and D1) on the **ANT_DET** line must be placed as ESD protection.

2.5 SIM interfaces

2.5.1 Guidelines for SIM circuit design

TOBY-L3 series modules provide one SIM interface for the direct connection of external SIM cards/chips:

- SIM interface (**VSIM**, **SIM_IO**, **SIM_CLK**, **SIM_RST** pins)

The ISO/IEC 7816, the ETSI TS 102 221 and the ETSI TS 102 671 specifications define the physical, electrical and functional characteristics of Universal Integrated Circuit Cards (UICC), which contains the Subscriber Identification Module (SIM) integrated circuit that securely stores all the information needed to identify and authenticate subscribers over the LTE/3G/2G network.

Removable UICC / SIM card contact mapping is defined by ISO/IEC 7816 and ETSI TS 102 221:

- Contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Contact C4 = AUX1 (Auxiliary contact) → It must be left not connected
- Contact C5 = GND (Ground) → It must be connected to **GND**
- Contact C6 = VPP (Programming supply) → It can be left not connected
- Contact C7 = I/O (Data input/output) → It must be connected to **SIM_IO**
- Contact C8 = AUX2 (Auxiliary contact) → It must be left not connected

A removable SIM card can have 6 contacts (C1, C2, C3, C5, C6, C7) or 8 contacts, also including the auxiliary contacts C4 and C8. Only 5 contacts are required (C1, C2, C3, C5, C7) to be connected.

Removable SIM cards are suitable for applications requiring a change of SIM card during the product's lifetime.

A SIM card holder can have 6 or 8 positions if a mechanical card presence detector is not provided, or it can have 6+2 or 8+2 positions if two additional pins relative to the normally-open mechanical switch integrated in the SIM connector for the mechanical card presence detection are provided. Select a SIM connector providing 6+2 or 8+2 positions if the optional SIM detection feature is required by the custom application, otherwise a connector without an integrated mechanical presence switch can be selected.

Solderable UICC / SIM chip contact mapping (M2M UICC Form Factor) is defined by ETSI TS 102 671:

- Case Pin 8 = UICC Contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Case Pin 7 = UICC Contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Case Pin 6 = UICC Contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Case Pin 5 = UICC Contact C4 = AUX1 → It must be left not connected
- Case Pin 1 = UICC Contact C5 = GND (Ground) → It must be connected to **GND**
- Case Pin 2 = UICC Contact C6 = VPP → It can be left not connected
- Case Pin 3 = UICC Contact C7 = I/O (Data I/O) → It must be connected to **SIM_IO**
- Case Pin 4 = UICC Contact C8 = AUX2 → It must be left not connected

A solderable SIM chip has 8 contacts and can also include the auxiliary contacts C4 and C8 for other uses, but only 5 contacts are required (C1, C2, C3, C5, C7) to be connected as described above.

Solderable SIM chips are suitable for M2M applications where it is not required to change the SIM once installed.

Guidelines for single SIM card connection without detection

A removable SIM card placed in a SIM card holder must be connected to the SIM interface of TOBY-L3 series modules as shown in Figure 36, where the optional SIM detection feature is not implemented.

Follow these guidelines to connect the module to a SIM connector without SIM presence detection:

- Connect the UICC / SIM contact C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) on SIM supply line, close to the relative pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line, very close to each related pad of the SIM connector, to prevent RF coupling especially when the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.

- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco PESD0402-140) on each externally accessible SIM line, close to each relative pad of the SIM connector. The ESD sensitivity rating of the SIM interface pins is 1 kV (HBM). So that, according to EMC/ESD requirements of the custom application, a higher protection level can be required if the lines are externally accessible on the application device.
- Limit the capacitance and series resistance on each SIM signal to match the SIM requirements (23 ns is the maximum allowed rise time on the clock line, 1 µs is the maximum allowed rise time on the data and reset lines).

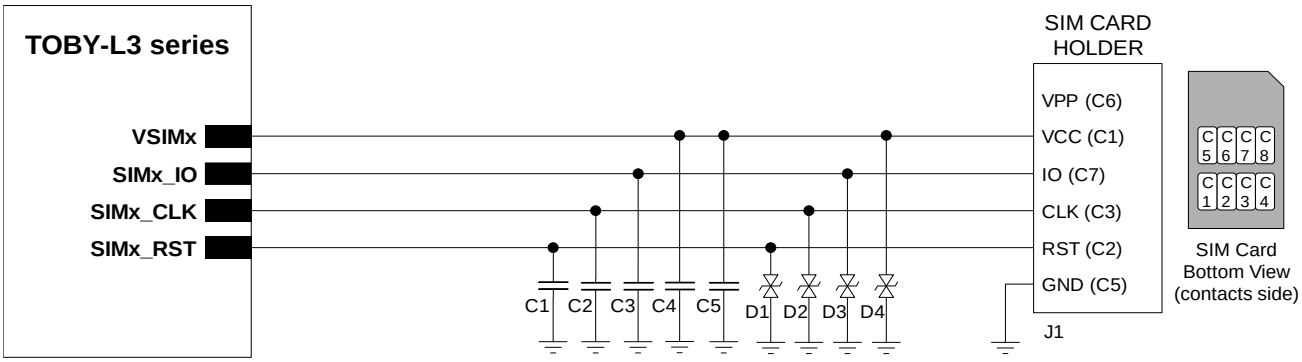

Figure 36: Application circuits for the connection to a single removable SIM card, with SIM detection not implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, D2, D3, D4	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
J1	SIM Card Holder, 6 p, without card presence switch	Various manufacturers, as C707 10M006 136 2 - Amphenol

Table 30: Example of components for the connection to a single removable SIM card, with SIM detection not implemented

Guidelines for single SIM chip connection

A solderable SIM chip (M2M UICC Form Factor) must be connected the SIM interface of the TOBY-L3 series modules as shown in Figure 37.

Follow these guidelines to connect the module to a solderable SIM chip without SIM presence detection:

- Connect the UICC / SIM contact C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.

- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line close to the relative pad of the SIM chip, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line, to prevent RF coupling especially when the RF antenna is placed closer than 10 - 30 cm from the SIM lines.
- Limit the capacitance and series resistance on each SIM signal to match the SIM requirements (23 ns is the max rise time on the clock line, 1 µs is the max rise time on the data and reset lines).

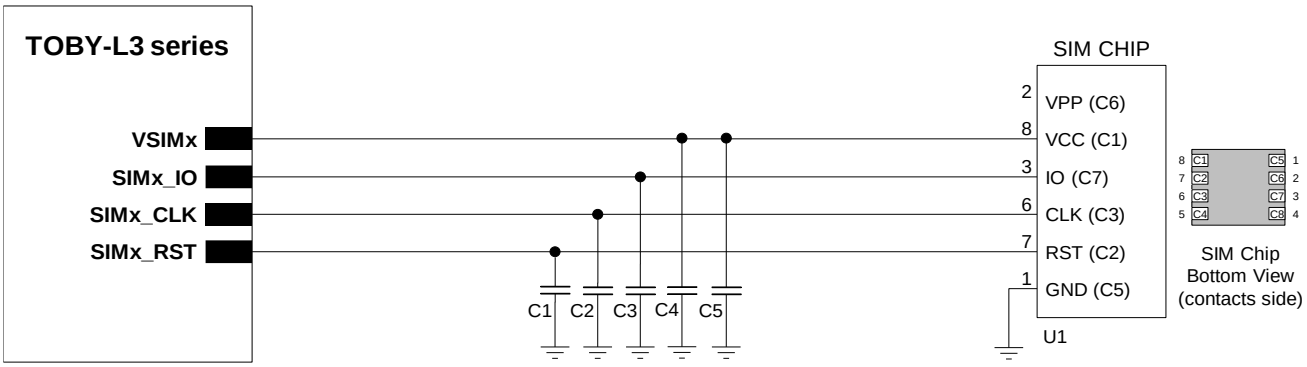

Figure 37: Application circuits for the connection to a single solderable SIM chip, with SIM detection not implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
U1	SIM chip (M2M UICC Form Factor)	Various Manufacturers

Table 31: Example of components for the connection to a single solderable SIM chip, with SIM detection not implemented

Guidelines for single SIM card connection with detection

If the optional SIM card detection feature is required by the application, then a removable SIM card placed in a SIM card holder must be connected to the SIM0 interface of TOBY-L3 series modules as shown in Figure 38:

Follow these guidelines to connect the module to a SIM connector implementing SIM detection:

- Connect the UICC / SIM contact C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Connect one pin of the normally-open mechanical switch integrated in the SIM connector (e.g. the SW2 pin as shown in Figure 38) to the **GPIO5** input pin of the module.
- Connect the other pin of the normally-open mechanical switch integrated in the SIM connector (e.g. the SW1 pin as shown in Figure 38) to the **V_INT** 1.8 V supply output of the module by means of a strong (e.g. 1 kΩ) pull-up resistor, as the R1 resistor in Figure 38.
- Provide a weak (e.g. 470 kΩ) pull-down at the SIM detection line, as the R2 resistor in Figure 38.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line, close to the related pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line, very close to each related pad of the SIM connector, to prevent RF coupling especially when the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco PESD0402-140) on each externally accessible SIM line, close to each related pad of the SIM connector: ESD sensitivity rating of the SIM interface pins is 1 kV (HBM), so that, according to the EMC/ESD requirements of the custom application, a higher protection level can be required if the lines are externally accessible on the application device.
- Limit the capacitance and series resistance on each SIM signal to match the SIM requirements (23 ns is the max rise time on the clock line, 1.0 µs is the max rise time on the data and reset lines).

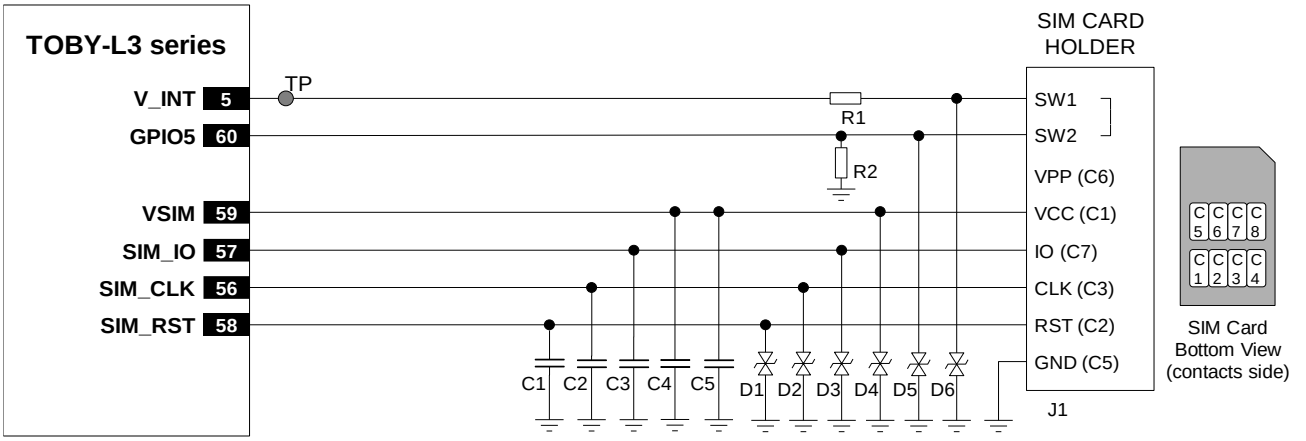

Figure 38: Application circuit for the connection to a single removable SIM card, with SIM detection implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, … , D6	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
R1	1 kΩ Resistor 0402 5% 0.1 W	RC0402JR-071KL - Yageo Phycomp
R2	470 kΩ Resistor 0402 5% 0.1 W	RC0402JR-07470KL- Yageo Phycomp
J1	SIM Card Holder, 6 + 2 p, with card presence switch	Various manufacturers, as CCM03-3013LFT R102 - C&K

Table 32: Example of components for the connection to a single removable SIM card, with SIM detection implemented

2.5.2 Guidelines for SIM layout design

The layout of the SIM card interfaces lines (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST** for the SIM interface) may be critical if the SIM card is placed far away from the TOBY-L3 series modules or in close proximity to the RF antenna: these two cases should be avoided or at least mitigated as described below.

In the first case, the long connection can cause the radiation of some harmonics of the digital data frequency as any other digital interface. It is recommended to keep the traces short and avoid coupling with the RF line or sensitive analog inputs.

In the second case, the same harmonics can be picked up and create self-interference that can reduce the sensitivity of LTE/3G/2G receiver channels whose carrier frequency is coincidental with the harmonic frequencies. It is strongly recommended to place the RF bypass capacitors suggested in Figure 36 near the SIM connector.

In addition, since the SIM card is typically accessed by the end user, it can be subjected to ESD discharges. Add adequate ESD protection as suggested to protect the module SIM pins near the SIM connector.

Limit the capacitance and series resistance on each SIM signal to match the SIM specifications. The connections should always be kept as short as possible.

Avoid coupling with any sensitive analog circuit, since the SIM signals can cause the radiation of some harmonics of the digital data frequency.

2.6 Data communication interfaces

2.6.1 USB interface

2.6.1.1 Guidelines for USB circuit design

- USB 2.0 interface, with the module acting as USB device, as shown in Figure 39 and Table 33
- USB 2.0 interface, with the module acting as USB host, as shown in Figure 40 and Table 34

USB pull-up or pull-down resistors and external series resistors on the **USB_D+** and **USB_D–** lines as required by the USB 2.0 specification [4] are part of the module USB pins driver and do not need to be externally provided.

Routing the USB pins to a connector, they will be externally accessible on the application device. According to the EMC/ESD requirements of the application, an additional ESD protection device with very low capacitance should be provided close to the accessible point on the line connected to this pin.

☞ ESD sensitivity rating of USB interface pins is 1 kV (HBM according to the JESD22-A114F). A higher protection level could be required if the lines are externally accessible and it can be achieved by mounting a very low capacitance (i.e. less or equal to 1 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on the lines connected to these pins, close to the accessible points.

The USB pins of the modules can be directly connected to the USB host processor without additional ESD protections if they are not externally accessible or according to EMC/ESD requirements.

☞ If the USB interface pins are not used, they must be all left unconnected on the application board.

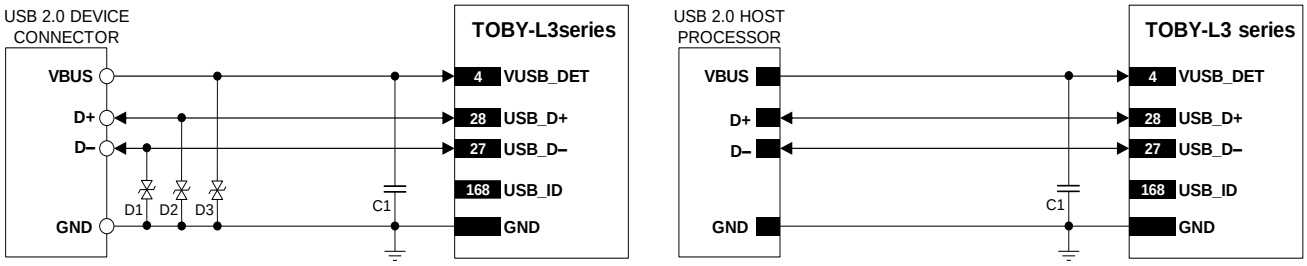

Figure 39: USB 2.0 interface application circuits, with TOBY-L3 series module acting as a USB device

Reference	Description	Part Number - Manufacturer
C1	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
D1, D2, D3	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics

Table 33: Component for USB 2.0 interface application circuits, with TOBY-L3 series module acting as a USB device

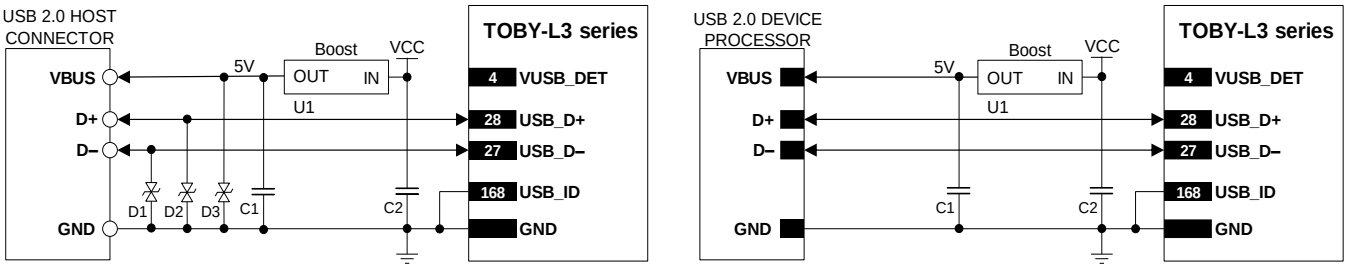

Figure 40: USB 2.0 interface application circuits, with TOBY-L3 series module acting as a USB host

Reference	Description	Part Number - Manufacturer
C1, C2	10 µF Capacitor Ceramic X7R 5750 15% 50 V	C5750X7R1H106MB - TDK
D1, D2, D3	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
U1	DC/DC Boost Regulator	Various Manufacturer

Table 34: Component for USB 2.0 interface application circuits, with TOBY-L3 series module acting as a USB host

2.6.1.2 Guidelines for USB layout design

The **USB_D+/USB_D–** lines require accurate layout design to achieve reliable signaling at the high speed data rates (up to 480 Mbit/s) supported by the USB 2.0 interface.

The nominal characteristic impedance of the **USB_D+/USB_D–** lines is specified by the USB 2.0 specification [4]. The most important parameter is the differential characteristic impedance applicable for the odd-mode electromagnetic field, which should be as close as possible to 90 Ω differential. Signal integrity may be degraded if the PCB layout is not optimal, especially when the USB signaling lines are very long.

Use the following general routing guidelines to minimize signal quality problems:

- Route the USB_D+ / USB_D– lines as a differential pair
- Route the USB_D+ / USB_D– lines as short as possible
- Ensure the differential characteristic impedance (Z_0) is as close as possible to 90 Ω
- Ensure the common mode characteristic impedance (Z_{CM}) is as close as possible to 30 Ω
- Consider design rules for the USB_D+ / USB_D– similar to RF transmission lines, these being coupled differential micro-strip or buried stripline: avoid any stubs, abrupt change of layout, and route on clear PCB area

Figure 41 and Figure 42 provide two examples of coplanar waveguide designs with differential characteristic impedance close to 90 Ω and common mode characteristic impedance close to 30 Ω. The first transmission line can be implemented for a 4-layer PCB stack-up herein illustrated; the second transmission line can be implemented for a 2-layer PCB stack-up herein illustrated.

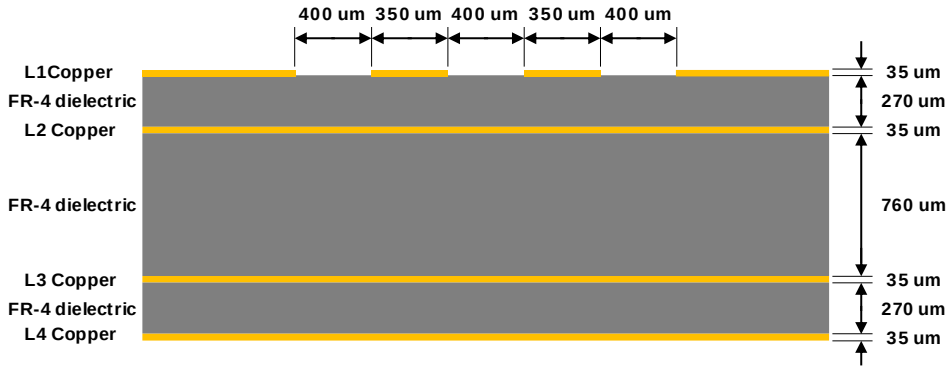

Figure 41: Example of USB line design, with Z_0 close to 90 Ω and Z_{CM} close to 30 Ω, for the described 4-layer board layup

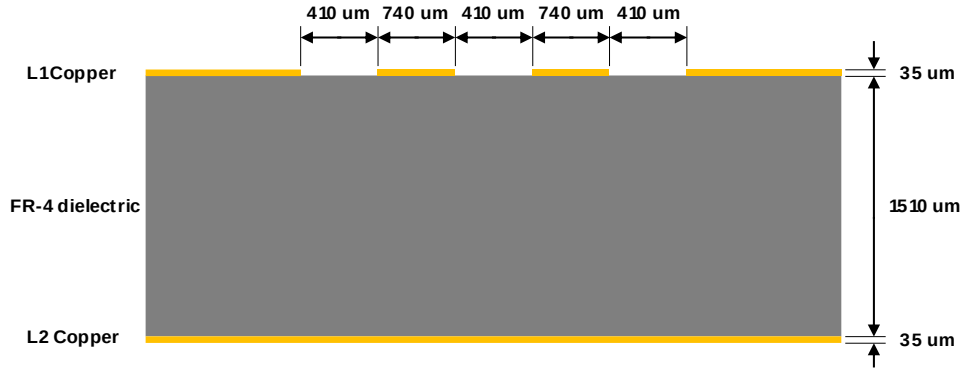

Figure 42: Example of USB line design, with Z_0 close to 90 Ω and Z_{CM} close to 30 Ω, for the described 2-layer board layup

2.6.2 UART interfaces

2.6.2.1 Guidelines for UART circuit design

4-wire UART

If RS-232 compatible signal levels are needed, the Maxim MAX13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V external Processor / Device is used, the circuit should be implemented as shown in Figure 43.

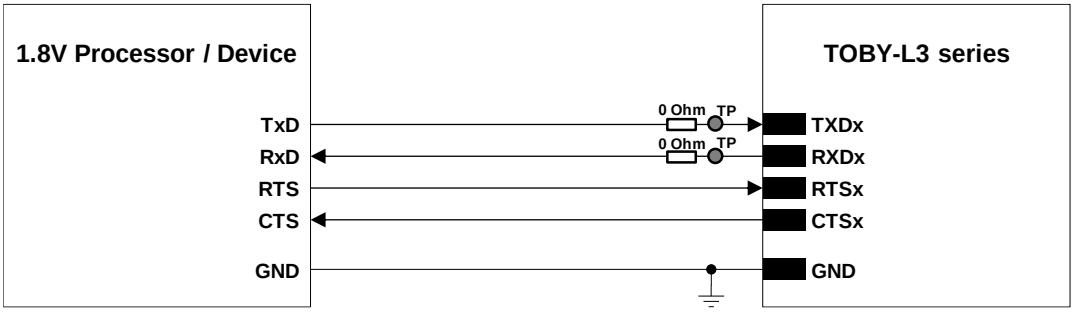

Figure 43: 4-wire UART interface application circuit to connect an external 1.8 V processor / device

If a 3.0 V external Processor / Device is used, then it is recommended to connect the 1.8 V UART interface of the module by means of appropriate unidirectional voltage translators using the module **V_INT** output as a 1.8 V supply for the voltage translators on the module side, as shown in Figure 44.

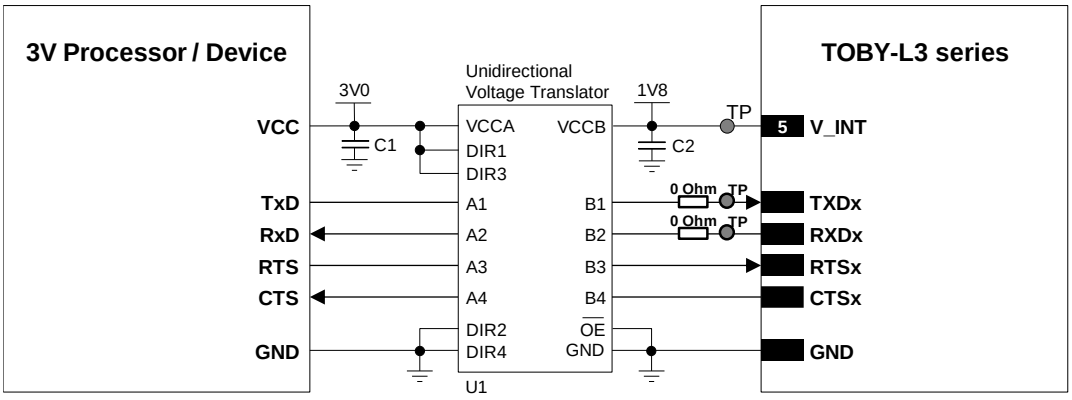

Figure 44: 4-wire UART interface application circuit to connect an external 3.0V processor / device

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC4T774[7] - Texas Instruments

Table 35: Component for 4-wire UART interface application circuit to connect an external 3.0V processor / device

☞ Test-Points for diagnostic access are recommended to be provided on the UART0 **TXD** and **RXD** lines. They are not required on other UART lines.

2-wire UART

If the functionality of the **CTSx** and **RTSx** are not required in the application, or the lines are not available, then:

- Consider to connect the module **RTSx** input line to GND or to the **CTSx** output line of the module, since the module requires **RTSx** active (low electrical level) if HW flow-control is enabled

If RS-232 compatible signal levels are needed, the Maxim MAX13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V external Processor / Device is used, the circuit should be implemented as shown in Figure 45.

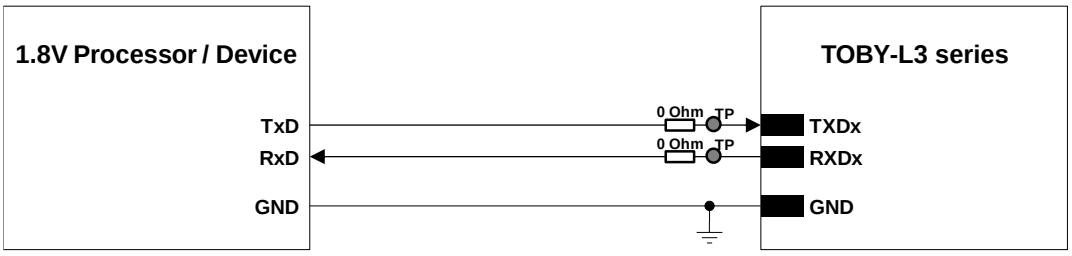

Figure 45: 2-wire UART interface application circuit to connect an external 1.8V processor / device

If a 3.0 V external Processor / Device is used, then it is recommended to connect the 1.8 V UART interface of the module by means of appropriate unidirectional voltage translators using the module **V_INT** output as a 1.8 V supply for the voltage translators on the module side, as shown in Figure 46.

[7] Voltage translator providing partial power down feature, thus the external 3.0 V rail can be ramped up before **V_INT** 1.8 V rail

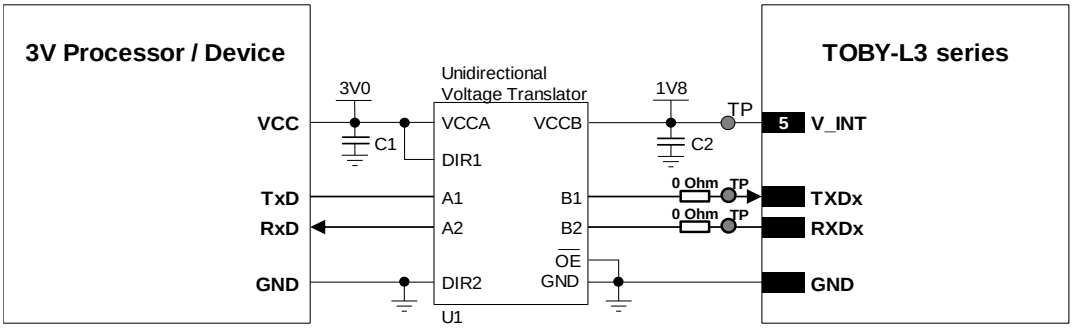

Figure 46: 2-wire UART interface application circuit to connect an external 3.0 V processor / device

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC2T245[8] - Texas Instruments

Table 36: Component for 2-wire UART interface application circuit to connect an external 3.0 V processor / device

☞ Test-Points for diagnostic access are recommended to be provided on the UART0 **TXD** and **RXD** lines for diagnostic purposes. Test-Points are not required on other UART lines.

Ring Indicator

If a 1.8 V external Processor / Device is used, the Ring Indicator circuit should be implemented as shown in Figure 47.

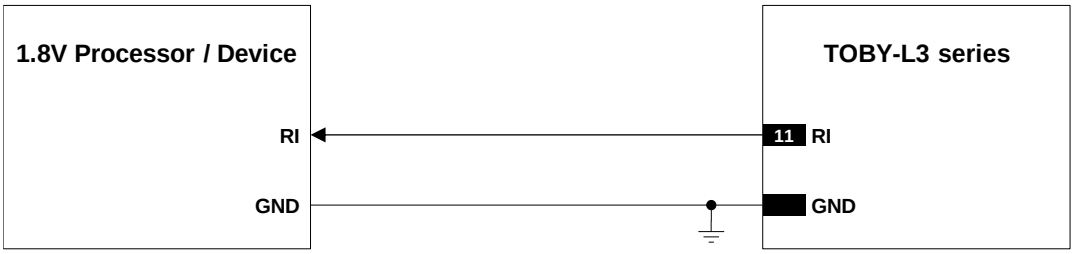

Figure 47: Ring Indicator application circuit to connect an external 1.8V processor / device

If a 3.0 V external Processor / Device is used, then it is recommended to connect the 1.8 V Ring Indicator output of the module by means of proper unidirectional voltage translators using the module **V_INT** output as a 1.8 V supply for the voltage translator on the module side, as shown in Figure 48.

[8] Voltage translator providing partial power down feature, thus the external 3.0 V rail can be ramped up before **V_INT** 1.8 V rail

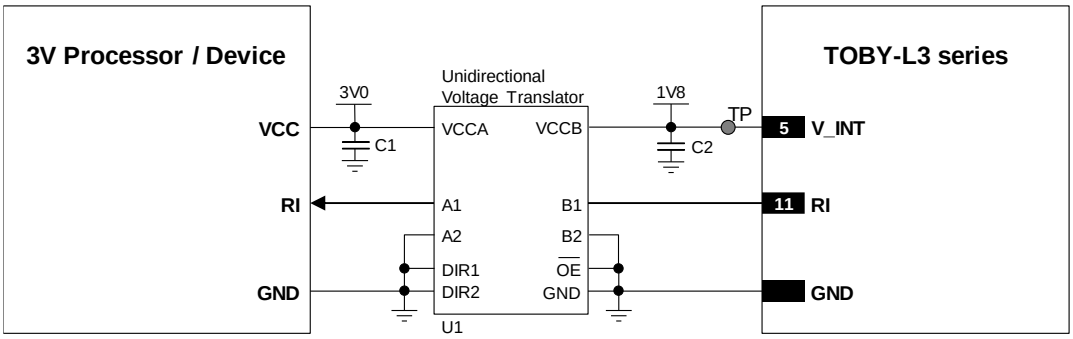

Figure 48: Ring Indicator(Configured by GPIO8) application circuit to connect an external 3.0V processor / device

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC2T245[9] - Texas Instruments

Table 37: Component for the Ring Indicator application circuit to connect an external 3.0V processor / device

☞ Do not apply voltage to any UART interfaces pin before the switch-on of the UART supply source (**V_INT**), to avoid latch-up of circuits and allow a clean boot of the module.

☞ The ESD sensitivity rating of UART pins is 1 kV (HBM according to JESD22-A114). A higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG) close to the accessible points.

☞ If the UART interfaces pins are not used, they can be left unconnected on the application board, but it is recommended to provide accessible test points directly connected to the UART0 **TXD** and **RXD** pins for diagnostic purposes.

2.6.2.2 Guidelines for UART layout design

The UART serial interface requires the same considerations regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.6.3 SPI interfaces

☞ SPI interfaces are not supported by the "0x" product feature versions.

2.6.3.1 Guidelines for SPI circuit design

TOBY-L3 series modules include up to two 1.8 V Serial Peripheral Interfaces to communicate with external SPI slave devices, with the module acting as SPI master, by means of the open CPU API.

[9] Voltage translator providing partial power down feature: the external 3.0 V supply can be ramped up before **V_INT** 1.8 V supply

Figure 49 describes a possible application circuit for the SPI0 interface, where two SPI slave devices are connected to the module using the two SPI0 Chip Select 0 (**SPI_CS** pin) to select the specific SPI slave device.

The external SPI slave device must provide compatible voltage levels (1.80 V typ.), otherwise it is recommended to connect the 1.8 V SPI interface of the module to the external 3.0 V (or similar) SPI device by means of appropriate unidirectional voltage translators (e.g. TI SN74AVC4T774 or SN74AVC2T245, providing partial power down feature so that the digital audio device 3.0 V supply can be also ramped up before **V_INT** 1.8 V supply), using the module's **V_INT** output as a 1.8 V supply for the voltage translators on the module side.

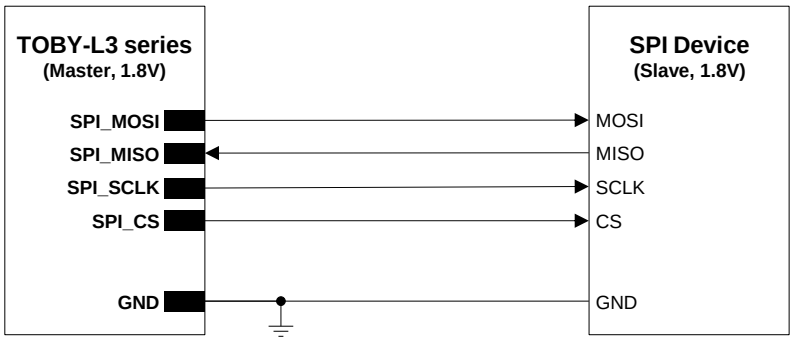

Figure 49: SPI interface application circuit for connecting external SPI slave devices

☞ Do not apply voltage to any SPI interface pins before the switch-on of the SPI supply source (**V_INT**), to avoid latch-up of circuits and allow a clean boot of the module.

☞ The ESD sensitivity rating of SPI pins is 1 kV (HBM according to JESD22-A114). A higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible points.

☞ If the SPI interfaces pins are not used, they can be left unconnected on the application board.

2.6.3.2 Guidelines for SPI layout design

The SPI serial interface requires the same considerations regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.6.4 DDC (I2C) interfaces

2.6.4.1 General guidelines for DDC (I2C) circuit design

The DDC I^2C-bus pins of the module are open drain outputs conforming to I^2C bus specifications [7]. External pull-up resistors to a suitable 1.8 V supply (e.g. **V_INT**) are required for operations: for example, 4.7 kΩ resistors can be commonly used.

☞ Connect the DDC (I²C) pull-ups to the **V_INT** 1.8 V supply source, or another 1.8 V supply source enabled after **V_INT** (e.g., as the GNSS 1.8 V supply present in Figure 51 application circuit), as any external signal connected to the DDC (I²C) interface must not be set high before the switch-on of the **V_INT** supply of DDC (I²C) pins, to avoid latch-up of circuits and allow a clean boot of the module.

The signal shape is defined by the values of the pull-up resistors and the bus capacitance. Long wires on the bus will increase the capacitance. If the bus capacitance is increased, use pull-up resistors with a nominal resistance value lower than 4.7 kΩ, to match the I²C bus specifications [7] regarding the rise and fall times of the signals.

Figure 50 and Table 38 describe typical application circuits for connecting TOBY-L3 series modules to 1.8 V I2C devices (see Figure 50 top side) or 3 V I2C devices (see Figure 50 bottom side).

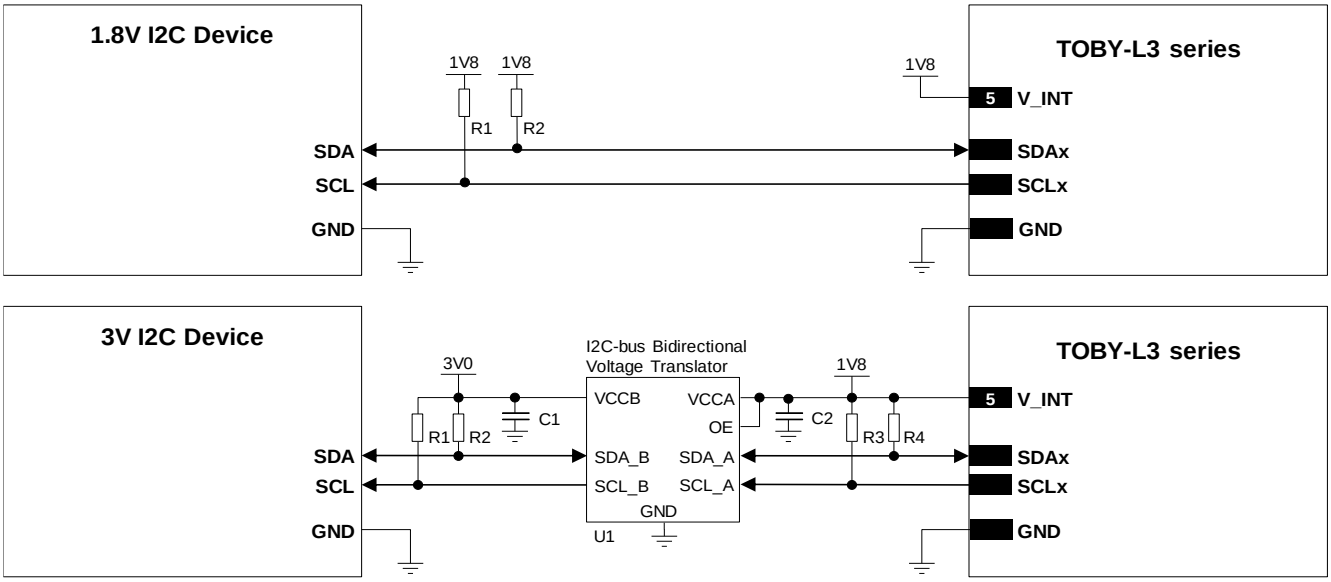

Figure 50: Application circuit for connecting TOBY-L3 series modules to 1.8 V or 3 V I2C devices

Reference	Description	Part Number - Manufacturer
R1, R2, R3, R4	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
U1	I2C-bus Bidirectional Voltage Translator	TCA9406DCUR[10] - Texas Instruments

Table 38: Components for connecting TOBY-L3 series modules to 1.8 V or 3 V I2C devices

☞ The ESD sensitivity rating of the DDC (I²C) pins is 1 kV (HBM according to JESD22-A114). A higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG) close to the accessible points.

[10] Voltage translator providing partial power down feature: the external 3 V supply can be ramped up before **V_INT** 1.8 V supply

☞ If the pins are not used as DDC (I^2C) bus interface, they can be left unconnected.

Connection with u-blox 1.8 V GNSS devices

Figure 51 shows an application circuit for connecting the cellular modules to a u-blox 1.8 V GNSS device.

- **SDA** / **SCL** pins of the cellular module are directly connected to the relative I^2C pins of the u-blox 1.8 V GNSS device, with appropriate pull-up resistors connected to the 1.8 V GNSS supply enabled after the **V_INT** supply of the I^2C pins of the cellular module.
- **GPIO2** pin is connected to the shutdown input pin (**SHDNn**) of the LDO regulators providing the 1.8 V supply rail for the u-blox 1.8 V GNSS device implementing the "GNSS supply enable" function, with an appropriate pull-down resistor mounted on the **GPIO2** line to avoid an improper switch-on of the u-blox GNSS device.
- **GPIO3** pin is directly connected to the **TXD1** pin of the u-blox 1.8 V GNSS device providing "GNSS Tx data ready" function.
- The **V_BCKP** backup supply input pin of the GNSS device is connected to the external battery to provide the supply for the GNSS real time clock and backup RAM when the **VCC** supply of the cellular module is within its operating range and the **VCC** supply of the GNSS device is disabled. This enables the u-blox GNSS device to recover from a power breakdown with either a hot start or a warm start (depending on the actual duration of the GNSS **VCC** outage) and to maintain the configuration settings saved in the backup RAM.

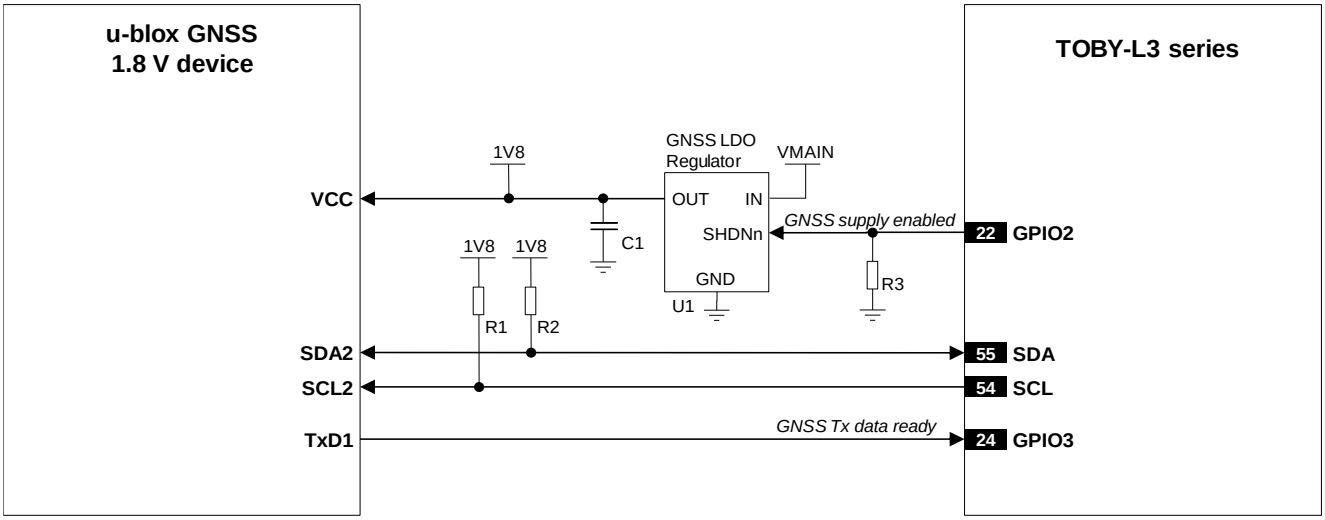

Figure 51: Application circuit for connecting TOBY-L3 series modules to u-blox 1.8 V GNSS devices

Reference	Description	Part Number - Manufacturer
R1, R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
U1, C1	Voltage Regulator for GNSS device and capacitor	See GNSS device Hardware Integration Manual

Table 39: Components for connecting TOBY-L3 series modules to u-blox 1.8 V GNSS devices

Figure 52 illustrates an alternative application circuit solution in which the cellular module supplies a u-blox 1.8 V GNSS device. The **V_INT** 1.8 V regulated supply output of the cellular module can be used as supply source for a u-blox 1.8 V GNSS device instead of using an external voltage regulator, as shown in Figure 51. The **V_INT** supply is able to support the maximum current consumption of these positioning devices.

The internal switching step-down regulator that generates the **V_INT** supply is set to 1.8 V (typical) when the cellular module is switched on and it is disabled when the module is switched off.

The supply of the u-blox 1.8 V GNSS device can be switched off using an external p-channel MOS controlled by the **GPIO2** pin of the cellular modules by means of a suitable inverting transistor as shown in Figure 52, implementing the "GNSS supply enable" function. If this feature is not required, the **V_INT** supply output can be directly connected to the u-blox 1.8 V GNSS device, so that it will switch on when **V_INT** output is enabled.

According to the **V_INT** supply output voltage ripple characteristic specified in the TOBY-L3 series Data Sheet [1], additional filtering may be needed to properly supply an external LNA, depending on the characteristics of the used LNA, adding a series ferrite bead and a bypass capacitor (e.g. the Murata BLM15HD182SN1 ferrite bead and the Murata GRM1555C1H220J 22 pF capacitor) at the input of the external LNA supply line.

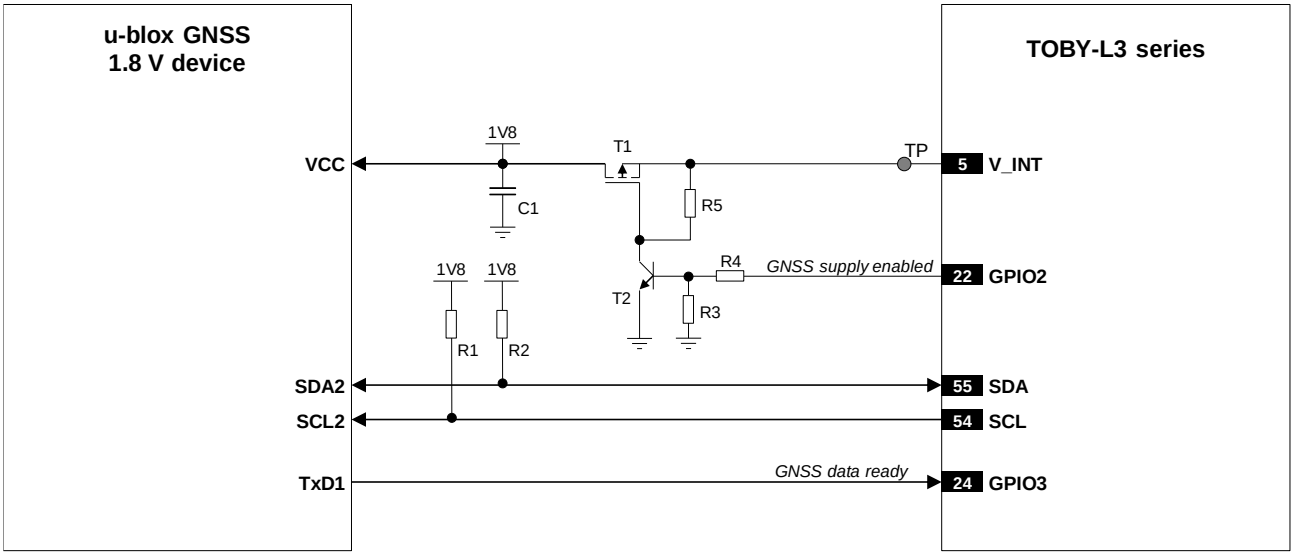

Figure 52: Application circuit for connecting TOBY-L3 series modules to u-blox 1.8 V GNSS devices using V_INT as supply

Reference	Description	Part Number - Manufacturer
R1, R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
R4	10 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0710KL - Yageo Phycomp

R5	100 kΩ Resistor 0402 5% 0.1 W	RC0402JR-07100KL - Yageo Phycomp
T1	P-Channel MOSFET Low On-Resistance	IRLML6401 - International Rectifier or NTZS3151P - ON Semi
T2	NPN BJT Transistor	BC847 - Infineon
C1	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata

Table 40: Components for connecting TOBY-L3 series modules to u-blox 1.8 V GNSS devices using V_INT as supply

Connection with u-blox 3.0 V GNSS devices

Figure 53 shows an application circuit for connecting the cellular modules to a u-blox 3.0 V GNSS device:

- As the **SDA** and **SCL** pins of the cellular module are not tolerant up to 3.0 V, the connection to the related I^2C pins of the u-blox 3.0 V GNSS device must be provided using a suitable I^2C-bus Bidirectional Voltage Translator with appropriate pull-up resistors (e.g. the TI TCA9406 additionally provides the partial power down feature so that the GNSS 3.0 V supply can be ramped up before the **V_INT** 1.8 V cellular supply).
- **GPIO2** pin is connected to the shutdown input pin (**SHDNn**) of the LDO regulators providing the 3.0 V supply rail for the u-blox 3.0 V GNSS device implementing the "GNSS enable" function, with an appropriate pull-down resistor mounted on the **GPIO2** line to avoid an improper switch-on of the u-blox GNSS device.
- As the **GPIO3** pin of the cellular module is not tolerant up to 3.0 V, the connection to the related pin of the u-blox 3.0 V GNSS device must be provided using a suitable Unidirectional General Purpose Voltage Translator (e.g. TI SN74LVC1T45, which additionally provides the partial power down feature so that the 3.0 V GNSS supply can be also ramped up before the **V_INT** 1.8 V rail).
- The **V_BCKP** backup supply input pin of the GNSS device is connected to the external battery as in the application circuit for a u-blox 1.8 V GNSS device.

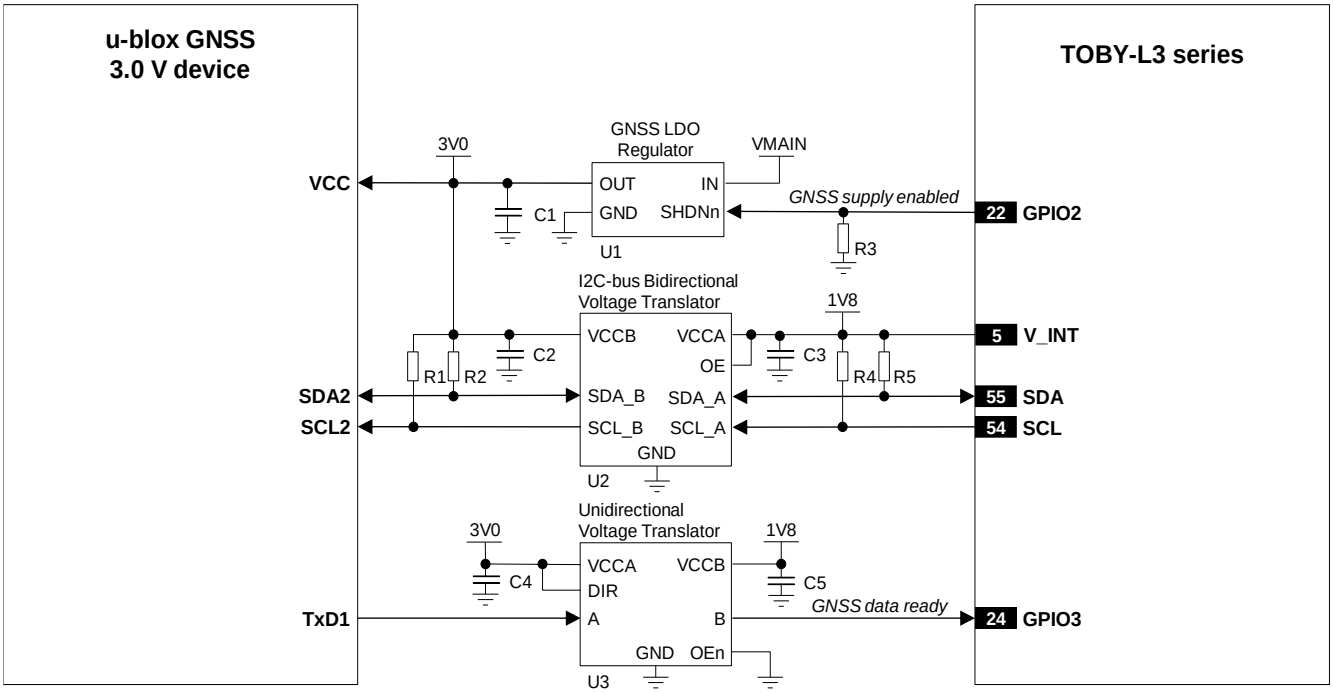

Figure 53: Application circuit for connecting TOBY-L3 series modules to u-blox 3.0 V GNSS devices

Reference	Description	Part Number - Manufacturer
R1, R2, R4, R5	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
C2, C3, C4, C5	100 nF Capacitor Ceramic X5R 0402 10% 10V	GRM155R71C104KA01 - Murata
U1, C1	Voltage Regulator for GNSS device and capacitor	See GNSS device Hardware Integration Manual
U2	I2C-bus Bidirectional Voltage Translator	TCA9406DCUR - Texas Instruments
U3	Generic Unidirectional Voltage Translator	SN74LVC1T45 - Texas Instruments

Table 41: Components for connecting TOBY-L3 series modules to u-blox 3.0 V GNSS devices

2.6.4.2 Guidelines for DDC (I2C) layout design

The DDC (I^2C) interface requires the same considerations regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.6.5 SDIO interface

2.6.5.1 Guidelines for SDIO circuit design

TOBY-L3 series modules include a 4-bit Secure Digital Input Output interface (**SDIO_D0**, **SDIO_D1**, **SDIO_D2**, **SDIO_D3**, **SDIO_CLK**, **SDIO_CMD**), where the module acts as an SDIO host controller designed to

- communicate with compatible u-blox short range radio communication modules by means of the open CPU API
- communicate with external SDIO devices by means of the open CPU API

Connection with u-blox short range radio communication modules

Figure 55 and Table 43 show an application circuit for connecting TOBY-L3 series cellular modules to u-blox JODY-W2 short range radio communication modules supporting IEEE 802.11a/b/g/n/ac 1x1 data rates for Wi-Fi:

- The SDIO pins of the TOBY-L3 series cellular module are connected to the related SDIO pins of the u-blox JODY-W2 short range radio communication module, with appropriate low value series damping resistors to avoid reflections and other losses in signal integrity, which may create ringing and loss of a square wave shape.
- The most appropriate value for the series damping resistors on the SDIO lines depends on the specific line lengths and layout implemented. In general, the SDIO series resistors are not strictly required, but it is recommended to slow the SDIO signal, for example with 22 Ω or 33 Ω resistors, and avoid any possible ringing problem without violating the rise / fall time requirements.
- The **V_INT** supply output pin of the TOBY-L3 series cellular module is connected to the shutdown input pin (**SHDNn**) of the LDO regulators providing the 1.8 V supply rails for the u-blox JODY-W2 module, with appropriate pull-down resistors to avoid an improper switch-on of the Wi-Fi module before the switch-on of the **V_INT** supply source of the cellular module SDIO interface pins.
- The **GPIO6** pin of the cellular module is connected to the active low full power down input pin (**PDN**) of the u-blox JODY-W2 module, and the **GPIO7** pin of the cellular module is connected to the **CORE_PDN** of the u-blox JODY-W2 module, implementing the Wi-Fi enable function.
- The **UART2** (**TXD2**, **RXD2**) pins of the cellular module are connected to the **LTE_COEXT** (**LTE_COEX_TX** and **LTE_COEX_RX**) pins of the u-blox JODY-W2 module, implementing the LTE-WIFI coexisting function.
- The **GPIO1** pin of the cellular module is connected to the **WL_DEV_WAKE** pin of the u-blox JODY-W2 module, implementing the waking up the JODY-W2 module by the cellular module.
- The configuration pin (**CFG**) of the u-blox JODY-W2 module is connected to ground by means of a proper pull-down resistor
- The WLAN antenna RF input/output (**ANT1**) of the u-blox JODY-W2 Wi-Fi module is directly connected to a Wi-Fi antenna considering that the u-blox JODY-W2 module integrates a 2.4 GHz BAW band pass filter that enables co-existence with LTE RF signals.

- All **GND** pins of the cellular module and the u-blox JODY-W2 Wi-Fi module are connected to ground.
- All the other pins of the u-blox JODY-W2 Wi-Fi module are intended to be not connected.

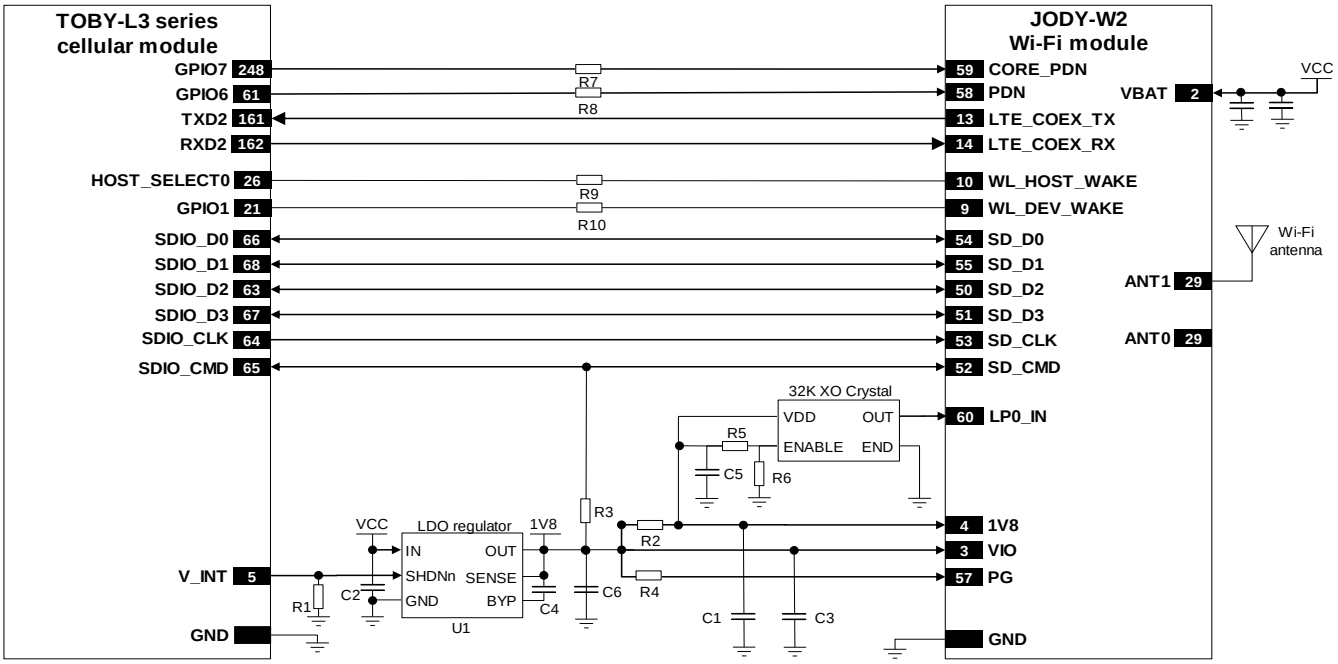

Figure 54: Application circuit for TOBY-L3 cellular module and u-blox JODY-W2 short range radio communication module

Reference	Description	Part Number - Manufacturer
C1, C3, C5	100 nF Capacitor Ceramic X5R 0402 10% 10V	GRM155R71C104KA01 – Murata
C2	1 µF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E105KA12 - Murata
C4	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C6	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
R1	470 kΩ Resistor 0402 5% 0.1 W	RK73B1ETTD474J - KOA
R2	22 Ω Resistor 0402 5% 0.1 W	RK73B1ETTP220J - KOA
R3, R5	10 kΩ Resistor 0402 5% 0.1 W	RK73B1ETTP103J - KOA
R4, R6	100 kΩ Resistor 0402 1% 0.1 W	RK73H1ETTP1003F - KOA
R7, R8, R9, R10	1 kΩ Resistor 0402 5% 0.1 W	RC0402JR-071KL - Yageo Phycomp
U1	LDO Linear Regulator 1.8 V 0.3 A	LT1962EMS8-1.8 - Linear Technology

Table 42: Parts for connecting TOBY-L3 cellular modules and u-blox EMMY-W161 short range communication modules

Connection with external SDIO devices

Figure 55 and Table 43 show an application circuit example for connecting the SDIO interface of the TOBY-L3 series modules to a 1.8 V SDIO device: the SDIO pins of the cellular module are connected to the related

SDIO pins of the SDIO device, with appropriate low value series damping resistors to avoid reflections and other losses in signal integrity, which may create ringing and loss of a square wave shape.

The most appropriate value for the series damping resistors on the SDIO lines depends on the specific line lengths and layout implemented. In general, the SDIO series resistors are not strictly required, but it is recommended to slow the SDIO signal, for example with 22 Ω or 33 Ω resistors, and avoid any possible ringing problem without violating the rise / fall time requirements.

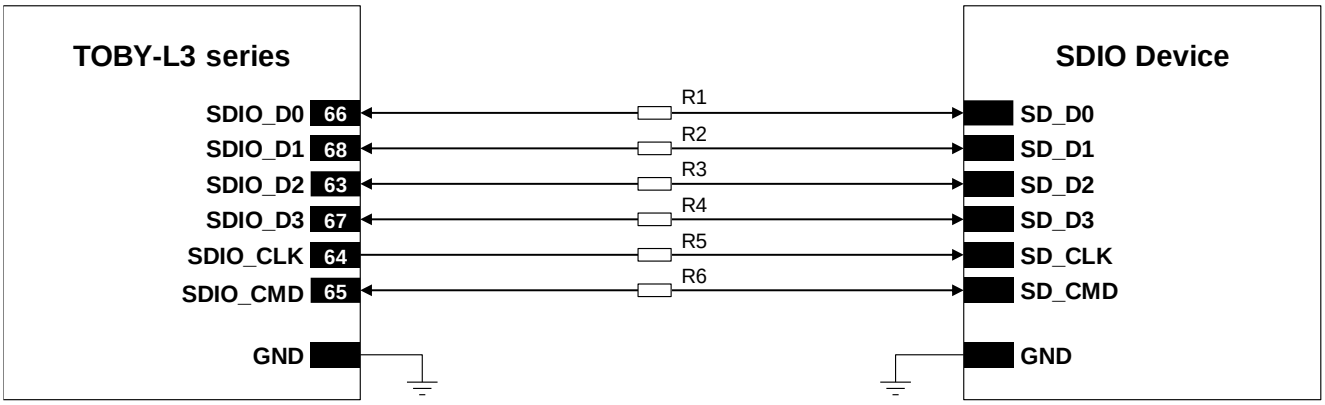

Figure 55: Application circuit for connecting TOBY-L3 series modules to a 1.8 V SDIO device

Reference	Description	Part Number - Manufacturer
R1, R2, R3, R4, R5, R6	22 Ω Resistor 0402 5% 0.1 W	RK73B1ETTP220J - KOA

Table 43: Components for connecting TOBY-L3 series modules to a 1.8 V SDIO device

☞ Do not apply voltage to any SDIO interface pin before the switch-on of SDIO interface supply source (**V_INT**), to avoid latch-up of circuits and allow a proper boot of the module.

☞ The ESD sensitivity rating of SDIO interface pins is 1 kV (HMB according to JESD22-A114). A higher protection level could be required if the lines are externally accessible and this can be achieved by mounting a very low capacitance ESD protection (e.g. Tyco Electronics PESD0402-140 ESD) close to the accessible points.

☞ If the SDIO interface pins are not used, they can be left unconnected on the application board.

2.6.5.2 Guidelines for SDIO layout design

The SDIO serial interface requires the same considerations regarding electro-magnetic interference as any other high speed digital interface.

Keep the traces short, avoid stubs and avoid coupling with RF lines / parts or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

Consider the usage of low value series damping resistors to avoid reflections and other losses in signal integrity, which may create ringing and loss of a square wave shape.

2.6.6 SGMII interface

2.6.6.1 Guidelines for SGMII circuit design

TOBY-L3 series modules include an Ethernet Media Access Control (MAC) block supporting up to 1 Gbit/s data rate via a Serial Gigabit Media-Independent Interface compliant with the SGMII Version 1.8 specification [8].

The module represents an Ethernet MAC controller, which can be connected to a compatible external Ethernet physical transceiver (PHY) chip to provide communication over Ethernet as illustrated in Figure 56.

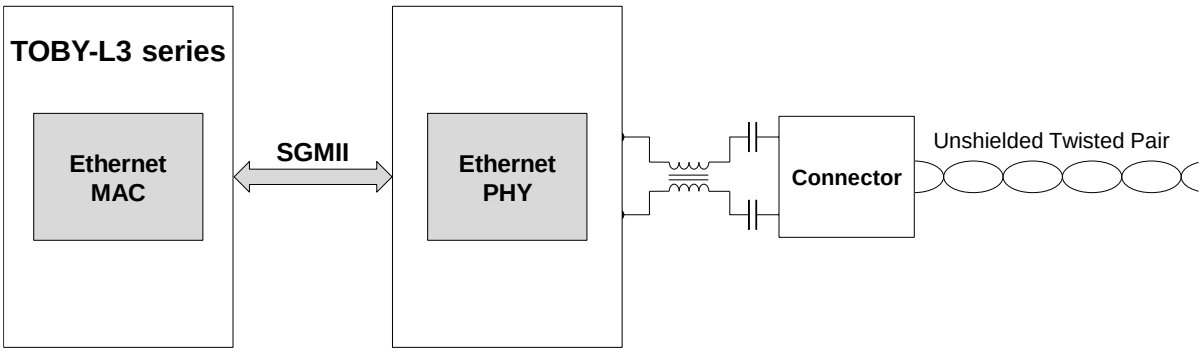

Figure 56: SGMII interface application circuit block diagram

- ☞ Do not apply loads which might exceed the limit for the maximum available current from **V_ETH** supply (see TOBY-L3 series Data Sheet [1]) as this can cause malfunctions in the internal circuitry.
- ☞ The ESD sensitivity rating of the SGMII pins is 1 kV (HMB according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting a very low capacitance ESD protection (e.g. Tyco Electronics PESD0402-140 ESD) close to the accessible points.
- ☞ If the SGMII interface pins are not used, they can be left unconnected on the application board.

2.6.6.2 Guidelines for SGMII layout design

The SGMII interface requires the same considerations regarding electro-magnetic interference as any other high speed digital interface.

Keep the traces short, avoid stubs and avoid coupling with RF lines / parts or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

Consider the usage of low value series damping resistors to avoid reflections and other losses in signal integrity, which may create ringing and loss of a square wave shape.

2.7 eMMC interface

☞ The eMMC interface is not supported by the "0x" product feature versions.

2.7.1 Guidelines for eMMC circuit design

TOBY-L3 series modules include a 4-bit embedded Multi-Media Card interface compliant with JESD84-B451 Embedded Multimedia Card (eMMC) Electrical Standard 4.51 [9], which can be handled by means of the open CPU API.

The eMMC interface can be connected to an external eMMC / SD memory as defined by the standard.

Pull-up resistors can be added on **MMC_D0**, **MMC_D1**, **MMC_D2** and **MMC_D3** data lines, the **MMC_CLK** clock line and the **MMC_CMD** command line, to increase the rise time on the signals so as to compensate for any capacitance on the board, even if not strictly required.

☞ Do not apply loads which might exceed the limit for the maximum available current from **V_MMC** supply (see TOBY-L3 series Data Sheet [1]) as this can cause malfunctions in the internal circuitry.

☞ The ESD sensitivity rating of eMMC interface pins is 1 kV (HMB according to JESD22-A114). A higher protection level could be required if the lines are externally accessible and it can be achieved by mounting a very low capacitance ESD protection (e.g. Tyco Electronics PESD0402-140 ESD) close to the accessible points.

☞ If the eMMC interface pins are not used, they can be left unconnected on the application board.

2.7.2 Guidelines for eMMC layout design

The eMMC interface requires the same considerations regarding electro-magnetic interference as any other high speed digital interface.

Keep the traces short, avoid stubs and avoid coupling with RF lines / parts or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

Consider the usage of low value series damping resistors to avoid reflections and other losses in signal integrity, which may create ringing and loss of a square wave shape.

2.8 Digital Audio interface

2.8.1 Guidelines for digital audio circuit design

I²S digital audio interfaces can be connected to external digital audio devices for voice applications.

Any external digital audio device compliant with the configuration of the digital audio interface of the TOBY-L3 series cellular module can be used, given that the external digital audio device must provide:

- The opposite role: slave or master role, as TOBY-L3 series modules may act as master or slave
- The same mode and frame format: PCM / short synch mode or Normal I²S / long synch mode with
  - data in 2's complement notation, linear
  - MSB transmitted first
  - data word length = 16-bit (16 clock cycles)
  - frame length = synch signal period:
    - 17-bit or 18-bit in PCM / short alignment mode (16 + 1 or 16 + 2 clock cycles, with the Word Alignment / Synchronization signal set high for 1 clock cycle or 2 clock cycles)
    - 32-bit in Normal I²S mode / long alignment mode (16 x 2 clock cycles)
- The same sample rate, i.e. synch signal frequency, <I2S_sample_rate> parameter:
  - 8 kHz, 16 kHz, 48 kHz
- The same serial clock frequency:
  - 17 x <I2S_sample_rate> or 18 x <I2S_sample_rate> in PCM / short alignment mode, or
  - 16 x 2 x <I2S_sample_rate> in Normal I²S mode / long alignment mode
- Compatible voltage levels (1.80 V typ.), otherwise it is recommended to connect the 1.8 V digital audio interface of the module to the external 3.0 V (or similar) digital audio device by means of appropriate unidirectional voltage translators (e.g. TI SN74AVC4T774 or SN74AVC2T245, providing a partial power down feature so that the digital audio device 3.0 V supply can be also ramped up before **V_INT** 1.8 V supply), using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side.

An appropriate specific application circuit must be implemented and configured according to the particular external digital audio device or codec used and according to the application requirements.

Examples of manufacturers offering compatible audio codec parts are the following:

- Maxim Integrated (as the MAX9860, MAX9867, MAX9880A audio codecs)
- Texas Instruments / National Semiconductor
- Cirrus Logic / Wolfson Microelectronics
- Nuvoton Technology
- Asahi Kasei Microdevices
- Realtek Semiconductor

Figure 57 and Table 44 describe circuits for the digital audio interfaces, considering these scenarios:

- 1.8 V audio device with slave role connected to a digital audio interface of the module set as master
- 1.8 V audio device with master role connected to a digital audio interface of the module set as slave
- 3.0 V audio device with slave role connected to a digital audio interface of the module set as master
- 3.0 V audio device with master role connected to a digital audio interface of the module set as slave

The same circuits can be implemented for both I2S0 and I2S1 digital audio interfaces of the module.

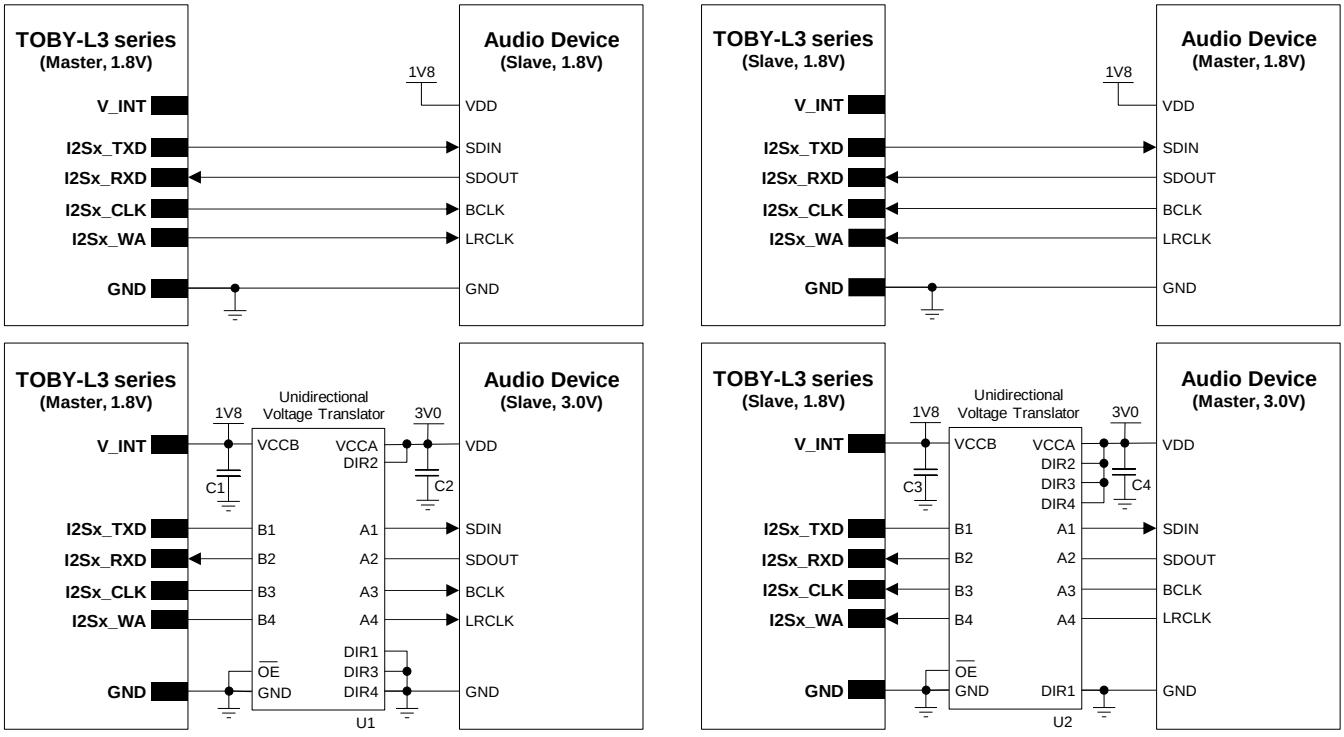

Figure 57: I²S interface application circuit with an external audio codec to provide voice capability

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	100 nF Capacitor Ceramic X5R 0402 10% 10V	GRM155R71C104KA01 – Murata
U1, U2	Unidirectional Voltage Translator	SN74AVC4T774[11] - Texas Instruments

Table 44: Example of components for an audio voice codec application circuit

Figure 58 and Table 45 describe an application circuit for the PCM digital audio interface providing basic voice capability using an external audio voice codec, in particular the Realtek ALC5660 audio codec.

- DAC and ADC integrated in the external audio codec respectively converts an incoming digital data stream to analog audio output through a mono amplifier and converts the microphone input signal to the digital bit stream over the digital audio interface.
- A digital side-tone mixer integrated in the external audio codec provides loopback of the microphones/ADC signal to the DAC/headphone output.

[11] Voltage translator providing partial power down feature, thus external 3 V rail can be also ramped up before **V_INT** 1.8 V rail

- The module's PCM interface (mast mode) is connected to the related pins of the external audio codec (slave mode).
- The external audio codec is controlled by the TOBY-L3 series module using the DDC (I2C) interfaces (**I2C_SDA**1, **I2C_SCL**1) which can be configured through AT command. For more details, see the TOBY-L3 series AT Commands Manual [2].
- The **VDD_INT** output supplies the external audio codec (**SPKVDD**, **MICVDD**, **DBVDD** and **AVDO1** pins), the **MICVDD** pin of the ALC5660 is supplied by the 3.3 V output through the LDO regulator, defining proper digital interfaces voltage level.
- Specific AT commands are available to configure the Realtek ALS5660 audio codec: for more details, see the TOBY-L3 series AT Commands Manual [2].

As various external audio codecs other than the one described in Figure 58 and Table 45 can be used to provide voice capability, the appropriate specific application circuit has to be implemented and configured according to the particular external digital audio device or audio codec used and according to the application requirements.

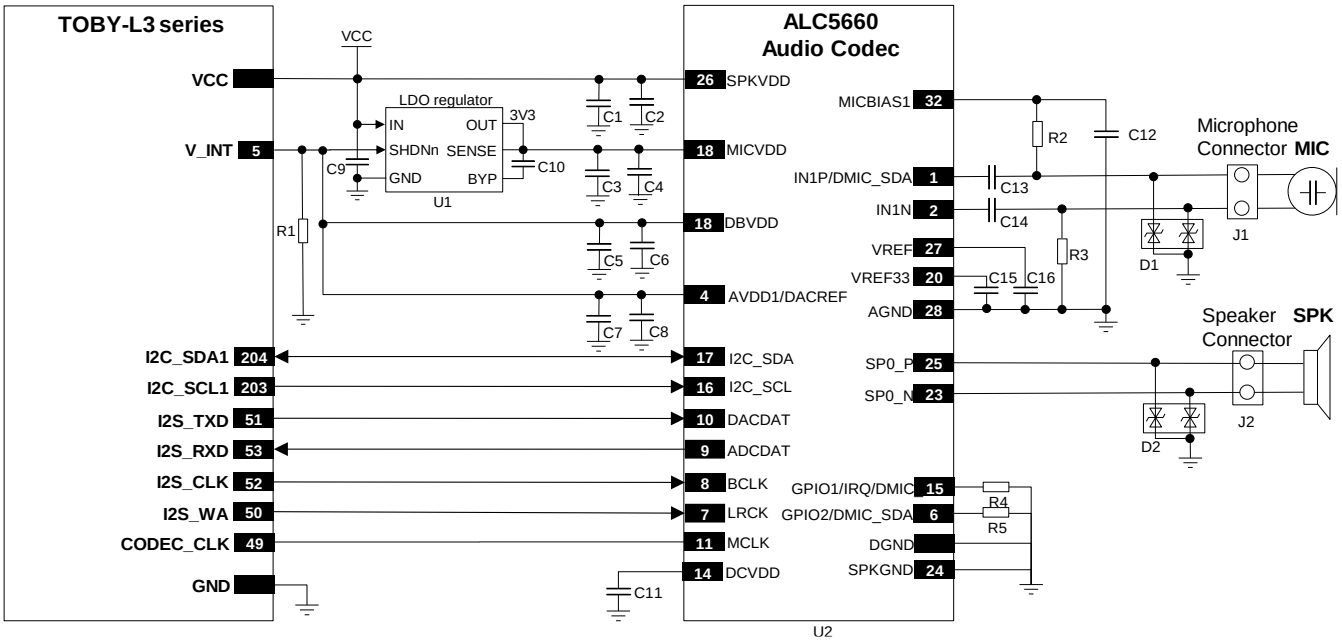

Figure 58: Digital audio interface application circuit with an external ACL5660 audio codec to provide voice capability

Reference	Description	Part Number - Manufacturer
C1,C3,C5,C6,C7	100 nF Capacitor Ceramic X5R 0402 10% 10V	GRM155R71C104KA01 – Murata
C2	47 µF Capacitor Ceramic X5R 0805 20% 6.3 V	GRT21BR60J476ME13L – Murata
C4,C8	2.2 µF Capacitor Ceramic X5R 0805 20% 16 V	GRT21BR61C226ME3L – Murata
C9,C11,C13,C14	1 µF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E105KA12 - Murata
C10	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C12,C15,C16	4.7 µF Capacitor Ceramic X5R 0805 10% 10V	GRT21BR61A475KE13L - Murata
R1	470 kΩ Resistor 0402 5% 0.1 W	RK73B1ETTD474J - KOA

R2,R3	2.2 kΩ Resistor 0402 0.1% 62.5 mW	RN73R1ETP2201B25 - KOA
D1,D2	Low Capacitance ESD Protection	USB0002RP or USB0002DP – AVX
U1	LDO Linear Regulator 1.8 V 0.3 A	LT1962EMS8-1.8 - Linear Technology
U2	Audio Voice Codec	ALC5660 - Realtek

Table 45: Example of components for an ACL5660 audio voice codec application circuit

☞ Do not apply voltage to any PCM digital audio interface pins before the switch-on of the supply source (**V_INT**), to avoid latch-up of circuits and allow a clean boot of the module.

☞ The ESD sensitivity rating of the I²S interface pins is 1 kV (Human Body Model according to JESD22-A114). A higher protection level could be required if the lines are externally accessible and it can be achieved by mounting a general purpose ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible points.

☞ If the PCM digital audio pins or the I2C pins (**I2C_SDA1**, **I2C_SCL1**) are not used, they can be left unconnected on the application board.

2.8.2 Guidelines for digital audio layout design

I²S interface and clock output lines require the same considerations regarding electromagnetic interference as any other high speed digital interface. Keep the traces short and avoid coupling with RF lines / parts or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.9 ADC interfaces

☞ The ADC pins are not supported by the "0x" product feature versions.

2.9.1 Guidelines for ADC circuit design

TOBY-L3 series modules include Analog to Digital Converter inputs (**ADC1**, **ADC2**), which can be handled by means of the dedicated open CPU API.

The ADC pins can be connected to external circuits for general purpose voltage measurements.

The voltage value at the ADC input must be within the range reported in the TOBY-L3 series Data Sheet [1].

If an external voltage divider is implemented to increase the measurement voltage range, check the input resistance of the ADC inputs reported in the TOBY-L3 series Data Sheet [1]: if the equivalent of the external circuit has a significant value as compared to the input resistance of the ADC inputs, this should be taken into account and corrected to properly associate the ADC response to the voltage source value, implementing an appropriate ADC calibration procedure.

☞ The ESD sensitivity rating of ADC pins is 1 kV (HBM according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible points.

☞ If the ADC pins are not used, they can be left unconnected on the application board.

2.9.2 Guidelines for ADC layout design

The Analog to Digital Converters (**ADC1**, **ADC2**) are high impedance analog inputs. The conversion accuracy will be degraded if noise is injected. Low-pass filter may be used to improve noise rejection; typically, L-C tuned for RF rejection gives better results.

2.10 General Purpose Input/Output

2.10.1 Guidelines for GPIO circuit design

A typical usage of TOBY-L3 series modules' GPIOs can be the following:

- Wi-Fi enable function provided by **GPIO6** (see Figure 55 in section 2.6.5)[12]
- GNSS supply enable function provided by **GPIO2** (see Figure 51, Figure 53 in section 2.6.4)[12]
- GNSS Tx data ready function provided by **GPIO3** (see Figure 51, Figure 53 in section 2.6.4)[12]
- SIM card detection provided by the **GPIO5** (see Figure 38 / Table 32 in section 2.5)

Other configurations of the TOBY-L3 series modules' GPIOs are possible, as shown in section 1.13.

☞ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series with the GPIO of TOBY-L3 series modules.

☞ Do not apply voltage to any GPIO of the module before the switch-on of the GPIOs supply (**V_INT**), to avoid latch-up of circuits and allow a clean module boot. If the external signals connected to the module cannot be tri-stated or set low, insert a multi-channel digital switch (e.g. TI SN74CB3Q16244, TS5A3159, TS5A63157) between the two-circuit connections and set to high impedance before **V_INT** switch-on.

☞ The ESD sensitivity rating of the GPIO pins is 1 kV (HBM according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG) close to the accessible points.

☞ If the GPIO pins are not used, they can be left unconnected on the application board.

[12] Not supported by "0x" product feature version

2.10.2 Guidelines for general purpose input/output layout design

The general purpose inputs / outputs pins are generally not critical for layout.

2.11 Reserved pins (RSVD)

TOBY-L3 series modules have pins reserved for future use, marked as **RSVD**. All the **RSVD** pins are to be left unconnected on the application board.

2.12 Module placement

An optimized placement allows a minimum RF line's length and a closer path from the DC source for **VCC**.

Make sure that the module, analog parts and RF circuits are clearly separated from any possible source of radiated energy. In particular, digital circuits can radiate digital frequency harmonics, which can produce electromagnetic interference that affects the module, analog parts and RF circuits' performance. Implement suitable countermeasures to avoid any possible electromagnetic compatibility issues.

Make sure that the module, RF and analog parts / circuits, and high speed digital circuits are clearly separated from any sensitive part / circuit which may be affected by electromagnetic interference, or employ countermeasures to avoid any possible electromagnetic compatibility issue.

Provide enough clearance between the module and any external part.

☞ The heat dissipation during continuous transmission at maximum power can significantly raise the temperature of the application base-board below the TOBY-L3 series modules: avoid placing temperature sensitive devices close to the module.

2.13 Module footprint and paste mask

Figure 59 and Table 46 describe the suggested footprint (i.e. copper mask) and the paste mask (i.e. stencil) layout for TOBY-L3 series modules, to be implemented on the application PCB.

The proposed land pattern layout (i.e. the footprint, the application board top-layer copper mask) reflects the modules' pads layout, with the pads on the application board designed as the LGA pads of the module.

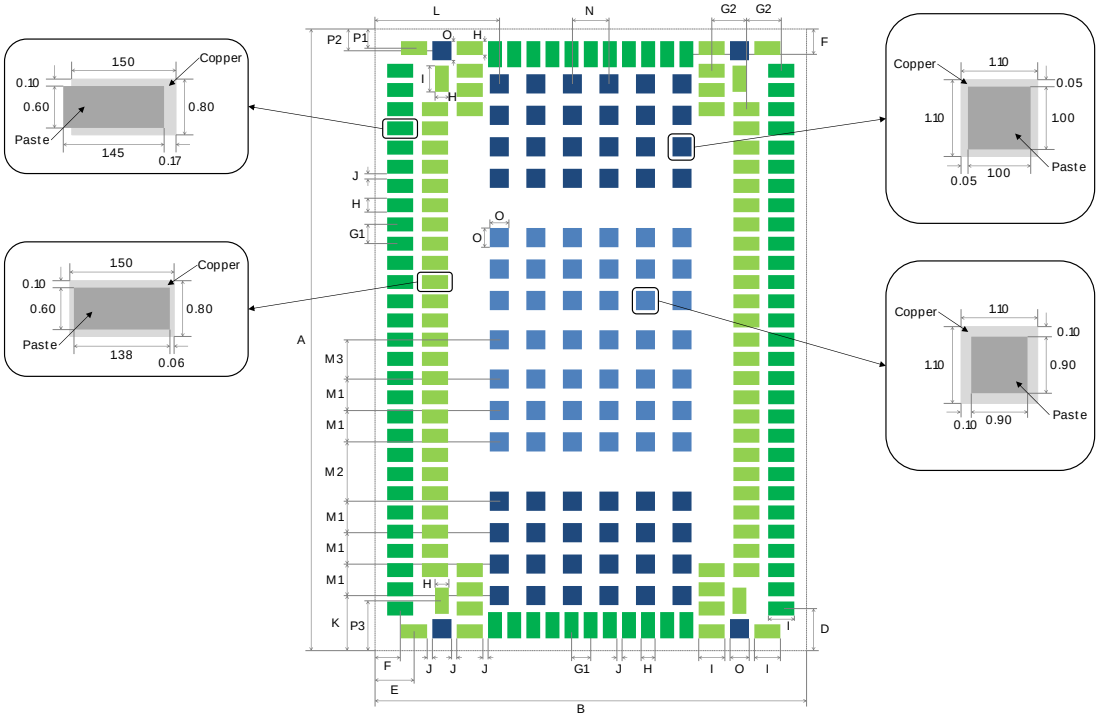

Figure 59: Suggested footprint and stencil design for TOBY-L3 modules, to be implemented on application PCB (top view)

Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value
A	35.6 mm	G1	1.10 mm	K	3.15 mm	N	2.10 mm
B	24.8 mm	G2	2.00 mm	L	7.15 mm	O	1.10 mm
D	2.40 mm	H	0.80 mm	M1	1.80 mm	P1	1.10 mm
E	2.25 mm	I	1.50 mm	M2	3.40 mm	P2	1.25 mm
F	1.45 mm	J	0.30 mm	M3	2.25 mm	P3	2.85 mm

Table 46: Suggested footprint design dimensions for TOBY-L3 series modules, to be implemented on application PCB

Non Solder resist Mask Defined pad type is recommended over Solder resist Mask Defined type, designing the solder resist mask opening 50 µm larger per side than the corresponding copper pad.

The suggested paste mask (i.e. stencil) layout to mount the modules on the application PCB is also illustrated in Figure 59. Different stencil apertures layout for any specific pad is recommended:

- Green marked pads: Paste layout enlarged on the lateral side and reduced on other sides
- Light-Green marked pads: Paste layout reduced circumferentially to Copper layout
- Blue marked pads: Paste layout reduced circumferentially 0.05 mm to Copper layout

- Light-Blue marked pads: Paste layout reduced circumferentially 0.1 mm to Copper layout

The recommended solder paste (i.e. stencil) thickness is 150 µm, according to application production process requirements.

☞ These are recommendations only and not specifications. The exact mask geometries, distances and stencil thicknesses must be adapted to the specific production processes of the customer.

2.14 Thermal guidelines

☞ Modules' temperature range and thermal parameters are specified in the TOBY-L3 series Data Sheet [1].

The most critical condition concerning module thermal performance is the uplink transmission at maximum power (data upload in connected mode), because when the baseband processor runs at full speed, radio circuits are all active and the RF power amplifier is driven to higher output RF power. This scenario is not often encountered in real networks (for example, see the Terminal Tx Power distribution for WCDMA, taken from operation on a live network, described in the GSMA TS.09 Battery Life Measurement and Current Consumption Technique [10]); however the application should be correctly designed to cope with it.

During transmission at maximum RF power, the TOBY-L3 series modules generate thermal power that may exceed 4 W in the worst case condition: this is an indicative value since the exact generated power strictly depends on operating conditions such as the actual antenna return loss, the number of allocated TX resource blocks, the transmitting frequency band, etc. The generated thermal power must be adequately dissipated through the thermal and mechanical design of the application.

The spreading of the actual Module-to-Ambient thermal resistance ($R_{th,M-A}$) depends on the module operating condition. The overall temperature distribution is influenced by the configuration of the active components during the specific mode of operation and their different thermal resistance toward the case interface.

☞ The actual Module-to-Ambient thermal resistance value and the relative increase of module temperature will differ according to the specific mechanical deployments of the module, e.g. application PCB with different dimensions and characteristics, mechanical shells enclosure, or forced air flow.

The increase of the thermal dissipation, i.e. the reduction of the actual Module-to-Ambient thermal resistance, will decrease the temperature of the modules' internal circuitry for a given operating ambient temperature. This improves the device long-term reliability in particular for applications operating at high ambient temperature.

Recommended hardware techniques to be used to improve heat dissipation in the application:

- Connect each **GND** pin with solid ground layer of the application board and connect each ground area of the multilayer application board with a complete thermal via stacked down to the main ground layer.
- Provide a ground plane as wide as possible on the application board.

- Optimize antenna return loss, to optimize overall electrical performance of the module including a decrease of module thermal power.
- Optimize the thermal design of any high-power components included in the application, such as linear regulators and amplifiers, to optimize overall temperature distribution in the application device.
- Select the material, the thickness and the surface of the box (i.e. the mechanical enclosure) of the application device that integrates the module so that it provides good thermal dissipation.

Further hardware techniques that may be considered to improve the heat dissipation in the application:

- Provide a heat sink component on the backside of the application board, below the cellular module, as a large part of the heat is transported through the GND pads of the TOBY-L3 series LGA modules and dissipated over the backside of the application board.
- Force ventilation air-flow within the mechanical enclosure.

Beside the reduction of the Module-to-Ambient thermal resistance implemented with the correct application hardware design, the increase of module temperature can be moderated by suitable application software implementation:

- Enable power saving configuration or the power state manager.
- Enable module connected mode for a given time period and then disable it for a time period long enough to properly mitigate temperature increase.

☞ TOBY-L3 series modules include a thermal daemon that monitors the internal temperatures by means of sensors integrated within the module, and it takes actions in order to reduce the module temperature, implementing a progressive reduction of the maximum Tx RF power, a progressive reduction of the maximum throughput, a progressive reduction of the processing cores clock frequency, a progressive shutdown of the processing cores, up to the shutdown of the module.

2.15 Design-in checklist

This section provides a design-in checklist.

2.15.1 Schematic checklist

The following are the most important points for a simple schematic check:

☑ DC supply must provide a nominal voltage at the **VCC** pin within the operating range limits.

☑ DC supply must be capable of supporting both the highest peak and the highest averaged current consumption values in connected mode, as specified in the TOBY-L3 series Data Sheet [1].

☑ **VCC** voltage supply should be clean, with very low ripple/noise: provide the suggested bypass capacitors, in particular if the application device integrates an internal antenna.

- ☑ Do not apply loads which might exceed the limit for the maximum available current from **V_INT** supply.
- ☑ Check that the voltage level of any connected pin does not exceed the relative operating range.
- ☑ Provide accessible test points directly connected to the following pins of the TOBY-L3 series modules: **V_INT**, **PWR_ON** and **RESET_N** for diagnostic purposes.
- ☑ Capacitance and series resistance must be limited on each SIM signal to match the SIM specifications.
- ☑ Insert the suggested pF capacitors on each SIM signal and low capacitance ESD protections if accessible.
- ☑ Check UART signals direction, as the modules' signal names follow the ITU-T V.24 Recommendation [6].
- ☑ Provide accessible test points directly connected to all the UART pins of the TOBY-L3 series modules (**TXD**, **RXD**) for diagnostic purposes.
- ☑ Provide accessible test points directly connected to all the UART3 pins of the TOBY-L3 series modules (**TXD3**, **RXD3**) for Linux debug console access.
- ☑ Capacitance and series resistance must be limited on each high speed line of the USB interface.
- ☑ Provide accessible test points directly connected to the USB 2.0 interface pins of the TOBY-L3 series modules (**VUSB_DET**, **USB_D+** and **USB_D–**) for diagnostic and FW update purposes.
- ☑ Consider providing appropriate low value series damping resistors on SDIO lines to avoid reflections.
- ☑ Add a suitable pull-up resistor (e.g. 4.7 kΩ) to **V_INT** or another suitable 1.8 V supply on each DDC (I^2C) interface line, if the interface is used.
- ☑ Check the digital audio interface specifications to connect a suitable external audio device.
- ☑ Capacitance and series resistance must be limited on master clock output line and each I^2S interface line
- ☑ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO when those are used to drive LEDs.
- ☑ Provide suitable precautions for EMC / ESD immunity as required on the application board.
- ☑ Do not apply voltage to any generic digital interface pin of TOBY-L3 series modules before the switch-on of the generic digital interface supply source (**V_INT**).
- ☑ All unused pins of TOBY-L3 series modules can be left unconnected, which must all be connected to GND.

2.15.2 Layout checklist

The following are the most important points for a simple layout check:

☑ Check 50 Ω nominal characteristic impedance of the RF transmission line connected to the **ANT1** and the **ANT2** ports (antenna RF interfaces).

☑ Ensure no coupling occurs between the RF interface and noisy or sensitive signals (SIM signals, high-speed digital lines such as the USB, SDIO, SGMII, eMMC, SPI and other data lines).

☑ Optimize placement for minimum length of the RF line.

☑ Check the footprint (copper mask), solder resist mask and stencil (paste mask) designed for TOBY-L3 series modules as shown in section 2.13.

☑ **VCC** line should be as wide and as short as possible.

☑ Route **VCC** supply line away from RF lines / parts and other sensitive analog lines / parts.

☑ The **VCC** bypass capacitors in the picoFarad range should be placed as close as possible to the **VCC** pins, in particular if the application device integrates an internal antenna.

☑ Ensure an optimal grounding connecting each **GND** pin with the application board solid ground layer.

☑ Use as many vias as possible to connect the ground planes on a multilayer application board, providing a dense line of vias at the edges of each ground area, in particular along the RF and high speed lines.

☑ Keep routing short and minimize parasitic capacitance on the SIM lines to preserve signal integrity.

☑ USB 2.0 data line traces must meet characteristic impedance requirements as per USB 2.0 specification [4], and should not be routed close to any RF line / part.

☑ Keep the SDIO traces short, avoid stubs, avoid coupling with any RF line / part and consider low value series damping resistors to avoid reflections and other losses in signal integrity.

☑ Ensure appropriate RF precautions for the Wi-Fi and Cellular technologies coexistence.

☑ Ensure appropriate RF precautions for the GNSS and Cellular technologies coexistence.

☑ Route digital audio signals away from noisy sources (primarily RF interface, **VCC**, switching supplies).

☑ The audio outputs lines on the application board must be wide enough to minimize series resistance.

2.15.3 Antenna checklist

☑ Antenna termination should provide a 50 Ω characteristic impedance with VSWR at least less than 3:1 (recommended 2:1) on operating bands in the deployment geographical area.

☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).

☑ Ensure compliance with any regulatory agency RF radiation requirement.

☑ Ensure high and similar efficiency for both the primary (**ANT1**) and the secondary (**ANT2**) antennas.

☑ Ensure high isolation between the primary (**ANT1**) and the secondary (**ANT2**) antennas.

☑ Ensure a low Envelope Correlation Coefficient between the primary (**ANT1**) and the secondary (**ANT2**) antennas: the 3D antenna radiation patterns should have radiation lobes in different directions.

☑ Ensure high isolation between the cellular antennas and any other antenna or transmitter.

3 Handling and soldering

☞ No natural rubbers, no hygroscopic materials or materials containing asbestos are employed.

3.1 Packaging, shipping, storage and moisture preconditioning

For information about the TOBY-L3 series reels / tapes, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning, see the TOBY-L3 series Data Sheet [1].

3.2 Handling

The TOBY-L3 series modules are Electro-Static Discharge (ESD) sensitive devices.

⚠ Ensure ESD precautions are implemented during handling of the module.

Electrostatic discharge (ESD) is the sudden and momentary electric current that flows between two objects at different electrical potentials caused by direct contact or induced by an electrostatic field. The term is usually used in the electronics and other industries to describe momentary unwanted currents that may cause damage to electronic equipment.

The ESD sensitivity for each pin of TOBY-L3 series modules (as Human Body Model according to JESD22-A114F) is specified in the TOBY-L3 series Data Sheet [1].

ESD prevention is based on establishing an Electrostatic Protective Area (EPA). The EPA can be a small working station or a large manufacturing area. The main principle of an EPA is that there are no highly charging materials near ESD sensitive electronics, all conductive materials are grounded, workers are grounded, and charge build-up on ESD sensitive electronics is prevented. International standards are used to define typical EPA and can be obtained for example from International Electrotechnical Commission (IEC) or American National Standards Institute (ANSI).

In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the TOBY-L3 series modules:

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect the ground of the device.
- When handling the module, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna, coax cable, soldering iron).

- To prevent electrostatic discharge through the RF pin, do not touch any exposed antenna area. If there is any risk that such an exposed antenna area is touched in a non-ESD protected work area, implement suitable ESD protection measures in the design.
- When soldering the module and patch antennas to the RF pin, make sure to use an ESD safe soldering iron.

3.3 Soldering

3.3.1 Soldering paste

"No Clean" soldering paste is strongly recommended for TOBY-L3 series modules, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering Paste: OM338 SAC405 / Nr.143714 (Cookson Electronics)
Alloy specification: 95.5% Sn / 3.9% Ag / 0.6% Cu (95.5% Tin / 3.9% Silver / 0.6% Copper)
95.5% Sn / 4.0% Ag / 0.5% Cu (95.5% Tin / 4.0% Silver / 0.5% Copper)
Melting Temperature: +217 °C
Stencil Thickness: 150 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.13.

☞ The quality of the solder joints should meet the appropriate IPC specification.

3.3.2 Reflow soldering

A convection type-soldering oven is strongly recommended for TOBY-L3 series modules over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Refer to the "IPC-7530A Guidelines for temperature profiling for mass soldering (reflow and wave) processes".

Reflow profiles are to be selected according to the following recommendations.

⚠ Failure to observe these recommendations can result in severe damage to the device!

Preheat phase

Initial heating of component leads and balls. Residual humidity will be dried out. Note that this preheat phase will not replace prior baking procedures.

- Temperature rise rate: max 3 °C/s — If the temperature rise is too rapid in the preheat phase, it may cause excessive slumping.
- Time: 60 – 120 s — If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End Temperature: 150 °C - 200 °C — If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ reflow phase

The temperature rises above the liquidus temperature of +217 °C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above +217 °C liquidus temperature: 40 - 60 s
- Peak reflow temperature: +245 °C

Cooling phase

A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 4 °C/s

☞ To avoid falling off, modules should be placed on the topside of the motherboard during soldering.

The soldering temperature profile chosen at the factory depends on additional external factors, such as the choice of soldering paste, size, thickness and properties of the base board, etc.

⚠ Exceeding the maximum soldering temperature and the maximum liquidus time limit in the recommended soldering profile may permanently damage the module.

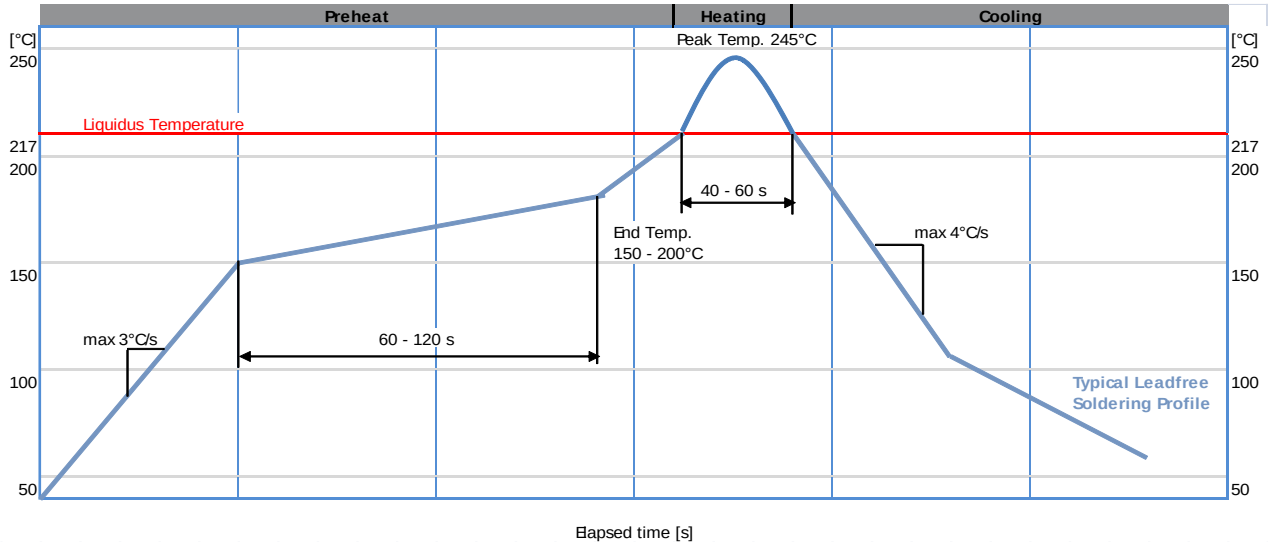

Figure 60: Recommended soldering profile

☞ The modules must not be soldered with a damp heat process.

3.3.3 Optical inspection

After soldering the module, inspect it optically to verify that it is properly aligned and centered.

3.3.4 Cleaning

Cleaning the modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

For best results, use a "no clean" soldering paste and eliminate the cleaning step after the soldering.

3.3.5 Repeated reflow soldering

Repeated reflow soldering processes and soldering the module upside down are not recommended.

Boards with components on both sides may require two reflow cycles. In this case, the module should always be placed on the side of the board that is submitted into the last reflow cycle. The reason for this

(besides others) is the risk of the module falling off due to the significantly higher weight in relation to other components.

☞ Tashang gives no warranty against damages to the TOBY-L3 series modules caused by performing more than a total of two reflow soldering processes (one reflow soldering process to mount the TOBY-L3 series module, plus one reflow soldering process to mount other parts).

3.3.6 Wave soldering

TOBY-L3 series LGA modules must not be soldered with a wave soldering process.

Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. No more than one wave soldering process is allowed for board with a TOBY-L3 series module already populated on it.

⚠ Performing a wave soldering process on the module can result in severe damage to the device!

☞ Tashang gives no warranty against damages to the TOBY-L3 series modules caused by performing more than a total of two soldering processes (one reflow soldering process to mount the module, plus one wave soldering process to mount other THT parts on the application board).

3.3.7 Hand soldering

Hand soldering is not recommended.

3.3.8 Rework

Rework is not recommended.

☞ Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.

3.3.9 Conformal coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products.

These materials affect the HF properties of the cellular modules and it is important to prevent them from flowing into the module.

The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, and therefore care is required in applying the coating.

☞ Conformal coating of the module will void the warranty.

3.3.10 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the cellular modules before implementing this in production.

☞ Casting will void the warranty.

3.3.11 Grounding metal covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interferences and noise.

☞ Tashang gives no warranty for damages to the TOBY-L3 series modules caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

3.3.12 Use of ultrasonic processes

The cellular modules contain components which are sensitive to ultrasonic waves. Use of any ultrasonic processes (cleaning, welding etc.) may cause damage to the module.

☞ Tashang gives no warranty against damages to TOBY-L3 series modules caused by any ultrasonic processes.

4 Approvals

☞ For the complete list and specific details regarding the certification schemes approvals, see the TOBY-L3 series Data Sheet [1], or contact the Tashang office or sales representative nearest you.

4.1 Product certification approval overview

Product certification approval is the process of certifying that a product has passed all tests and criteria required by specifications, typically called "certification schemes" that can be divided into three distinct categories:

- Regulatory certification
  - Country specific approval required by local government in most regions and countries, such as:
    - CE (Conformité Européenne) marking for the European Union
    - FCC (Federal Communications Commission) approval for the United States
- Conformance certification
  - Telecom industry specific approval verifying interoperability between devices and networks:
    - GCF (Global Certification Forum), a partnership between mainly European manufacturers and network operators to ensure and verify global devices and networks interoperability
    - PTCRB (PCS Type Certification Review Board), created by United States network operators to ensure and verify interoperability between devices and North America networks

Even using a module already approved under all major certification schemes, the application device integrating the module must be approved under all the certification schemes required by the specific application device to be deployed into the market. The required certification scheme approvals and relative testing specifications differ depending on the country or the region where the device integrating the module is intended to be deployed, on the relative vertical market of the device, on type, features and functionalities of the whole application device, and on the network operators where the device is intended to operate.

☞ Check the appropriate applicability of the TOBY-L3 series module's approvals while starting the certification process of the device integrating the module: the re-use of the Tashang cellular module's approval can significantly reduce the cost and time-to-market of the application device certification.

☞ The certification of the application device that integrates a TOBY-L3 series module and the compliance of the application device with all the applicable certification schemes, directives and standards are the sole responsibility of the application device manufacturer.

TOBY-L3 series modules are certified according to all the supported capabilities, functions and options stated in the Protocol Implementation Conformance Statement document (PICS) of the module. The PICS, according to 3GPP TS 51.010-2 [11], 3GPP TS 34.121-2 [12], 3GPP TS 36.521-2 [14] and 3GPP TS 36.523-2

[15] documents, is a statement of the implemented and supported capabilities, functions and options of a device.

☞ The PICS document of the application device integrating TOBY-L3 series modules must be updated from the module PICS statement if any feature stated as supported by the module in its PICS document is not implemented or disabled in the application device.

☞ Check the specific settings required for mobile network operator approvals as they may differ from the AT commands settings defined in the module as integrated in the application device.

5 Product testing

5.1 Product test

Tashang focuses on high quality for its products. All units produced are fully tested automatically in the production line. A stringent quality control process has been implemented in the production line. Defective units are analyzed in detail to improve production quality.

This is achieved with automatic test equipment (ATE) in the production line, which logs all production and measurement data. A detailed test report for each unit can be generated from the system.

- The following typical tests are among the production tests.
- Digital self-test (firmware download, Flash firmware verification, IMEI programming)
- Measurement of voltages and currents
- Functional tests (serial interface communication, SIM card communication)
- Digital tests (GPIOs and other interfaces)
- Measurement and calibration of RF characteristics in all supported bands (such as receiver S/N verification, frequency tuning of the reference clock, calibration of transmitter and receiver power levels, etc.)
- Verification of RF characteristics after calibration (i.e. modulation accuracy, power levels, spectrum, etc. are checked to ensure they are all within tolerances when calibration parameters are applied)

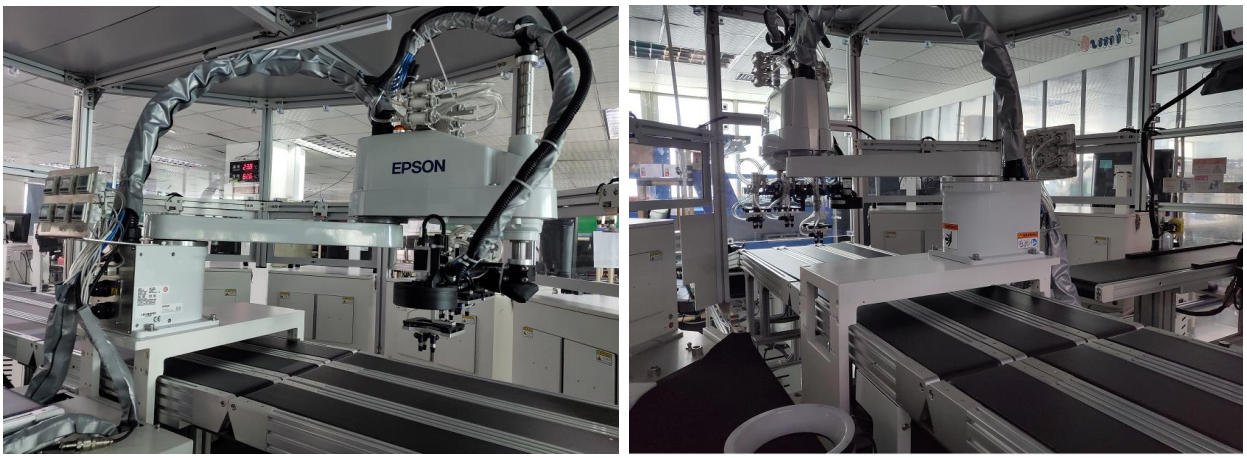

Figure 61: Automatic test equipment for module tests

5.2 Test parameters for OEM manufacturers

Because of the testing performed by Tashang (with 100% coverage), an OEM manufacturer does not need to repeat firmware tests or measurements of the module RF performance or tests over digital interface in their production test.

However, an OEM manufacturer should focus on:

- Module assembly on the device; it should be verified that:
  - Soldering and handling processes did not damage the module components
  - All module pins are well soldered on the device board
  - There are no short circuits between pins
- Component assembly on the device; it should be verified that:
  - Communications with the external host controller can be established
  - The interfaces between the module and external devices are working
  - Overall RF performance test of the device including the antenna

Dedicated tests can be implemented to check the device. For example, AT commands can be used to perform functional tests on the modules' interfaces (for more details see the TOBY-L3 series AT Commands Manual [2]), in details:

- Digital interfaces can be checked using the +UTEST=10 AT command
- RF interfaces can be checked using the +UTEST AT command (see the following section 5.2.1)

5.2.1 RF functional tests

The overall RF functional test of the OEM device integrating the cellular module, including the antenna(s), can be performed in the OEM production line with basic instruments such as a spectrum analyzer (or an RF power meter) and a signal generator with the assistance of the AT+UTEST command over the AT command user interface.

The +UTEST AT command provides a simple interface to set the module to Rx or Tx test modes ignoring the LTE/3G/2G signaling protocol (for more details see the TOBY-L3 series AT Commands Manual [2]). The command can set the module into:

- transmitting mode in a specified channel and power level
- receiving mode in a specified channel to returns the measured power level in all supported bands

This feature allows the measurement of the transmitter and receiver power levels to check component assembly related to the module antenna interface and to check other device interfaces on which RF performance depends.

⚠ To avoid module damage during the transmitter test, a suitable antenna according to module specifications or a 50 Ω termination must be connected to the **ANT1** port.

⚠ To avoid module damage during receiver, test the maximum power level received at the **ANT1** and **ANT2** ports which must meet the module specifications.

☞ The AT+UTEST command sets the module to emit RF power ignoring LTE/3G/2G signaling protocol. This emission can generate interference that can be prohibited by law in some countries. The use of this feature is intended for testing purposes in controlled environments by qualified users and must not be used during normal module operation. Follow the instructions suggested in the Tashang's documentation. Tashang assumes no responsibilities for the inappropriate use of this feature.

Figure 62 illustrates a typical test setup for such an RF functional test.

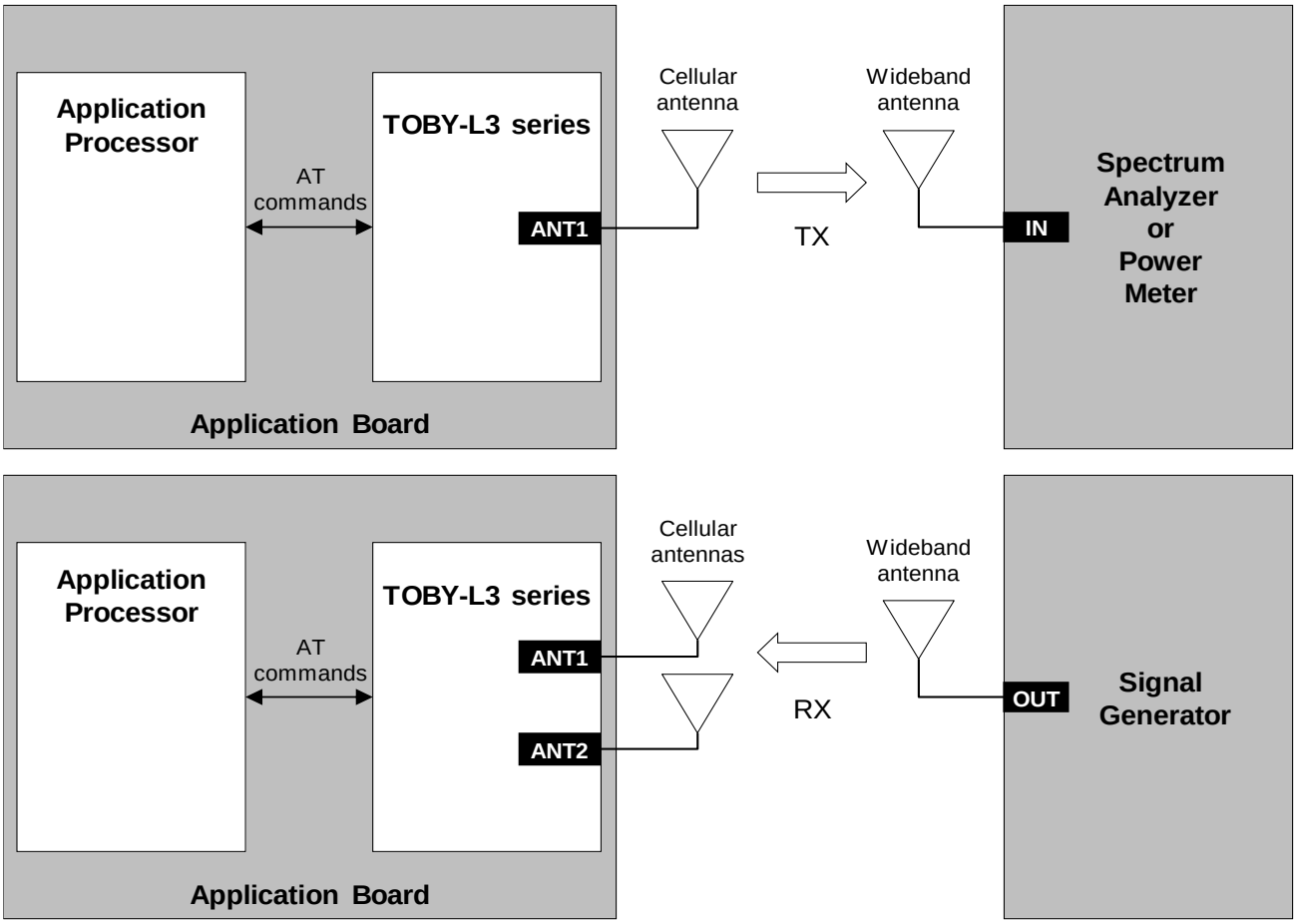

Figure 62: Setup with spectrum analyzer or power meter and signal generator for radiated measurements

6 FCC Notes

1. This module is limited to OEM installation ONLY.

2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).

3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations

4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

End Product labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text:

“Contains FCC ID: 2A3Z6TOBYL3404 ”

The FCC ID can be used only when all FCC compliance requirements are met.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are

designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment

off and on, the user is encouraged to try to correct the interference by one of the following measures:

-Reorient or relocate the receiving antenna.

-Increase the separation between the equipment and receiver.

-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Appendix

Glossary

Abbreviation	Definition
3GPP	3rd Generation Partnership Project
8-PSK	8 Phase-Shift Keying modulation
16QAM	16-state Quadrature Amplitude Modulation
64QAM	64-state Quadrature Amplitude Modulation
ACM	Abstract Control Model
ADC	Analog to Digital Converter
AP	Application Processor
API	Application Program Interface
ASIC	Application-Specific Integrated Circuit
AT	AT Command Interpreter Software Subsystem, or attention
BAW	Bulk Acoustic Wave
CSFB	Circuit Switched Fall-Back
DC	Direct Current
DCE	Data Communication Equipment
DDC	Display Data Channel interface
DL	Down-Link (Reception)
DRX	Discontinuous Reception
DSP	Digital Signal Processing
DTE	Data Terminal Equipment
EDGE	Enhanced Data rates for GSM Evolution
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
eMMC	Embedded Multi-Media Card
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
E-UTRA	Evolved Universal Terrestrial Radio Access
FDD	Frequency Division Duplex
FEM	Front End Module
FOAT	Firmware Over AT commands
FOTA	Firmware Over The Air

Abbreviation	Definition
FTP	File Transfer Protocol
FW	Firmware
GMSK	Gaussian Minimum-Shift Keying modulation
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
HBM	Human Body Model
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
HTTP	HyperText Transfer Protocol
HW	Hardware
I/Q	In phase and Quadrature
I^2C	Inter-Integrated Circuit interface
I^2S	Inter IC Sound interface
ISM	Industrial Scientific Medical
LDO	Low-Dropout
LGA	Land Grid Array
LNA	Low Noise Amplifier
LPDDR	Low Power Double Data Rate synchronous dynamic RAM memory
LTE	Long Term Evolution
M2M	Machine-to-Machine
MIMO	Multi-Input Multi-Output
N/A	Not Applicable
N.A.	Not Available
OEM	Original Equipment Manufacturer device
OTA	Over The Air
OTP	One Time Programmable
PA	Power Amplifier
PCM	Pulse Code Modulation
PCN	Product Change Notification / Information Note / Sample Delivery Note
PCS	Personal Communications Service
PFM	Pulse Frequency Modulation
PMU	Power Management Unit
PWM	Pulse Width Modulation

Abbreviation	Definition
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
RSE	Radiated Spurious Emission
RTC	Real Time Clock
SAW	Surface Acoustic Wave
SDIO	Secure Digital Input Output
SDN / PCN / IN	Sample Delivery Note / Product Change Notification / Information Note
SGMII	Serial Gigabit Media Independent Interface
SIM	Subscriber Identification Module
SMS	Short Message Service
SPI	Serial Peripheral Interface
SRF	Self Resonant Frequency
SSL	Secure Socket Layer
TBD	To Be Defined
TCP	Transmission Control Protocol
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
TIS	Total Isotropic Sensitivity
TP	Test-Point
TRP	Total Radiated Power
UART	Universal Asynchronous Receiver-Transmitter
UICC	Universal Integrated Circuit Card
UL	Up-Link (Transmission)
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
VoLTE	Voice over LTE
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access
Wi-Fi	Wireless Local Area Network (IEEE 802.11 short range radio technology)
WLAN	Wireless Local Area Network (IEEE 802.11 short range radio technology)
WWAN	Wireless Wide Area Network (GSM / UMTS / LTE cellular radio technology)

Related documents

[1] TOBY-L3 series Data Sheet, Doc. No. TSD-19081201

[2] TOBY-L3 series AT Commands Manual, Doc. No. TSD-19102501

[3] TOBY-L3 series Open CPU SDK User Manual. TSD-20080301

[4] Universal Serial Bus Rev. 2.0 specification, https://www.usb.org/

[5] Universal Serial Bus Rev. 3.0 specification, https://www.usb.org/

[6] ITU-T Recommendation V.24 - 02-2000 - List of definitions for interchange circuits between Data Terminal Equipment (DTE) and Data Circuit-terminating Equipment (DCE), http://www.itu.int/rec/T-REC-V.24-200002-I/en

[7] I^2C-bus specification and user manual - Rev. 5 - 9 October 2012 - NXP Semiconductors, https://www.nxp.com/docs/en/user-guide/UM10204.pdf

[8] Serial Gigabit Media-Independent Interface (SGMII) Version 1.8

[9] JESD84-B451 - Embedded Multimedia Card (eMMC), Electrical Standard 4.51

[10] GSM Association TS.09 - Battery Life Measurement and Current Consumption Technique https://www.gsma.com/newsroom/wp-content/uploads/TS.09-v10.2.pdf

[11] 3GPP TS 51.010-2 - Technical Specification Group GSM/EDGE Radio Access Network; Mobile Station (MS) conformance specification; Part 2: Protocol Implementation Conformance Statement (PICS)

[12] 3GPP TS 34.121-2 - Technical Specification Group Radio Access Network; User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 2: Implementation Conformance Statement (ICS)

[13] 3GPP TS 36.521-1 - Evolved Universal Terrestrial Radio Access; User Equipment conformance specification; Radio transmission and reception; Part 1: Conformance Testing

[14] 3GPP TS 36.521-2 - Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment conformance specification; Radio transmission and reception; Part 2: Implementation Conformance Statement (ICS)

[15] 3GPP TS 36.523-2 - Evolved Universal Terrestrial Radio Access (E-UTRA) and Evolved Packet Core (EPC); User Equipment conformance specification; Part 2: Implementation Conformance Statement (ICS)

Revision history

Revision	Date	Name	Comments
R01	06-Sep-2019	Herb	Initial release
R02	28-Feb-2020	Herb	Add the details of the software features Modify the circuit design of SDIO and I2S interface
R03	17-Mar-2020	Herb	Modify the default GPIO configuration
R04	05-Aug-2020	Herb	Add the PIN reuse of UART, SPI and I2S interfaces Add LTE B18 for Japan and India region in TOBY-L3904 series module.
R05	22-Aug-2020	Herb	Modify the SW functions of TOBY-L3
R06	24-Sep-2020	Herb	Adjust the family of TOBY-L3 series module
R07	12-Oct-2020	Herb	Update the product features of TOBY-L3 series modules.
R08	31-Oct-2020	Herb	Update the band information of TOBY-L3 series modules.
R09	09-Apr-2021	Herb	Update the TOBY-L3904 series module for China market
R10	18-May-2021	Herb	Update the product status of TOBY-L3904-50B-01 and TOBY-L3904-50A-01
R11	06-Dec-2021	Herb	Update the product code definition for TOBY-L3
R12	14-Dec-2021	Herb	Add the PCN TSD-21121301 and TSD-21121302 for TOBY-L3104 series product
R13	24-Jan-2022	Herb	Add FCC notes

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