

BLOCK DIAGRAM

LEGEND

Processor

Interface

RF/IF

Amplifier

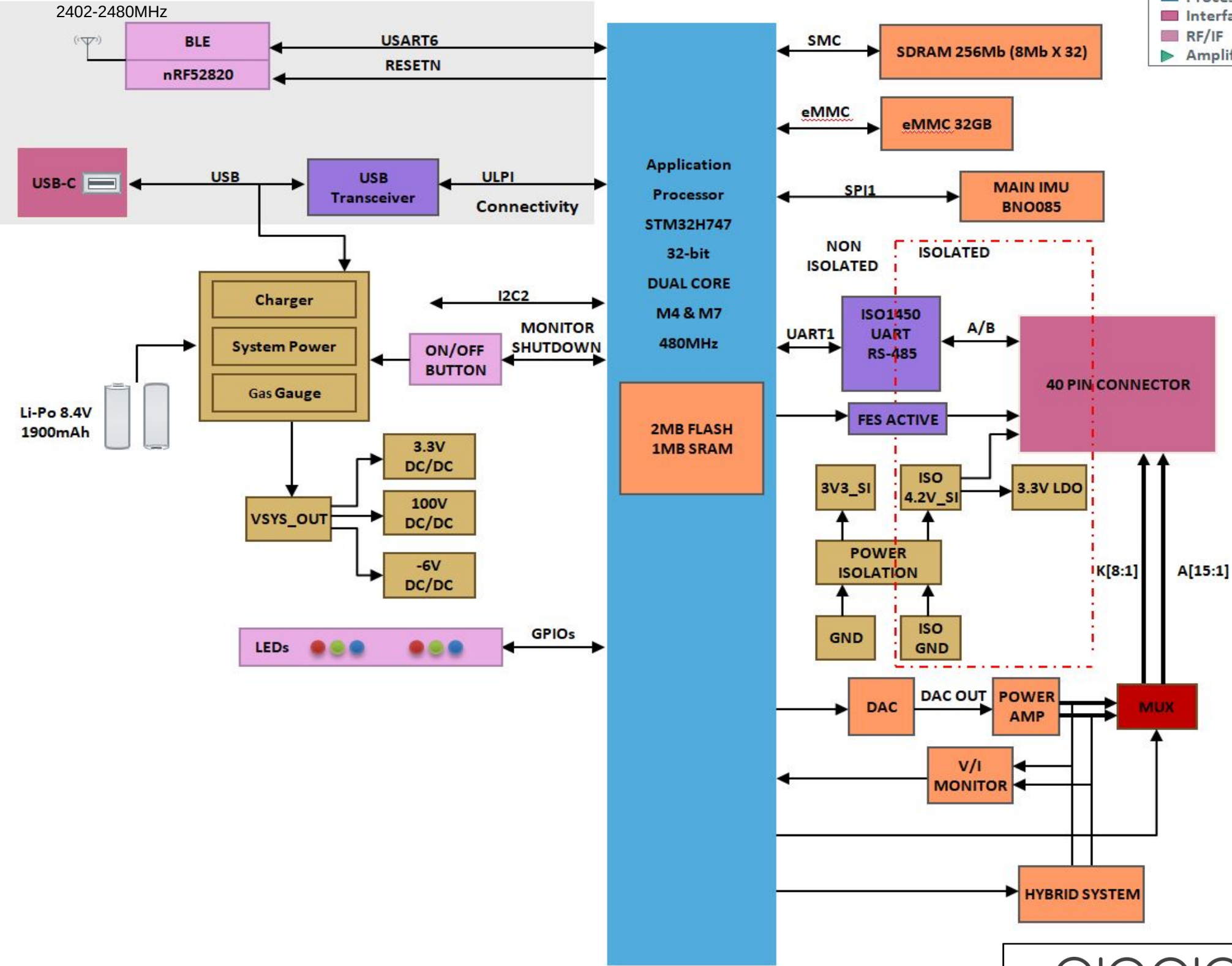
Logic

Power

ADC/DAC

Clocks

Other



CIONIC		CIONIC 1606 Stockton Street, Suite #1 San Francisco, CA 94133, USA		2024	
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO CIONIC USE OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN OFFICER OF CIONIC IS EXPRESSLY FORBIDDEN		BLOCK DIAGRAM			
		Size B		DWG NO 520 00027	
Sunday, September 01, 2024		Scale	DRAWN BY		Sheet 2 of 16