IEEE 802.11 1X1 a/b/g/n Wireless LAN+ Bluetooth 5.1 Combo Stamp Module

Datasheet

Version 1.7

LS001ONWAS Datasheet

Date	Revision Content	Revised By	Version
2020/8/18	Initial Release	EE	V1.0
2020/9/18	Modify Pin Map and PHY DMI	EE	V1.1
2020/11/6	Modify Pin Definition	EE	V1.2
2020/12/12	Updated 1. Pin Definition 2. Block Diagram 3. Specifications Table 4. Electrical Characteristics 5. Host Interface	RF	V1.3
2021/01/22	Updated 1. Package LGA change to Stamp 2. CON[0] and CON[1] 100k change to 51k 3. Dimension 4. Power up Timing Sequence	EE	V1.4
2021/01/31	Updated 1. Power up Timing Sequence	EE	V1.5
2021/05/23	Release 1. WLAN&BT Specification	RF	V1.6
2021/08/05	Modify 1. WLAN&BT Specification	RF	V1.7

Contents

1. Introduction

Product Overview and Functional Description

The LS001ONWAS is a highly integrated Wi-Fi 4 (2.4G/5G) and Bluetooth 5.1 Wi-Fi Module solution with a highly effective bill of material. The device has a power optimized architecture and features to save energy.

With the Bluetooth 5.1 direction-finding AoA/AoD and WLAN 11mc features, the Wi-Fi module improves the indoor location accuracy for asset management in warehouses or retail stores.

The support of WPA3 and high-performance 11i with various encryption mechanisms provide strong security foundation and immune the device from malicious attacks.

The module supports multiple interfaces:

WLAN: SDIO, USB; Bluetooth: SDIO, USB, UART.

Audio interface: I^2S and PCM for Bluetooth.

2. Features

2.1 Wi-Fi Features

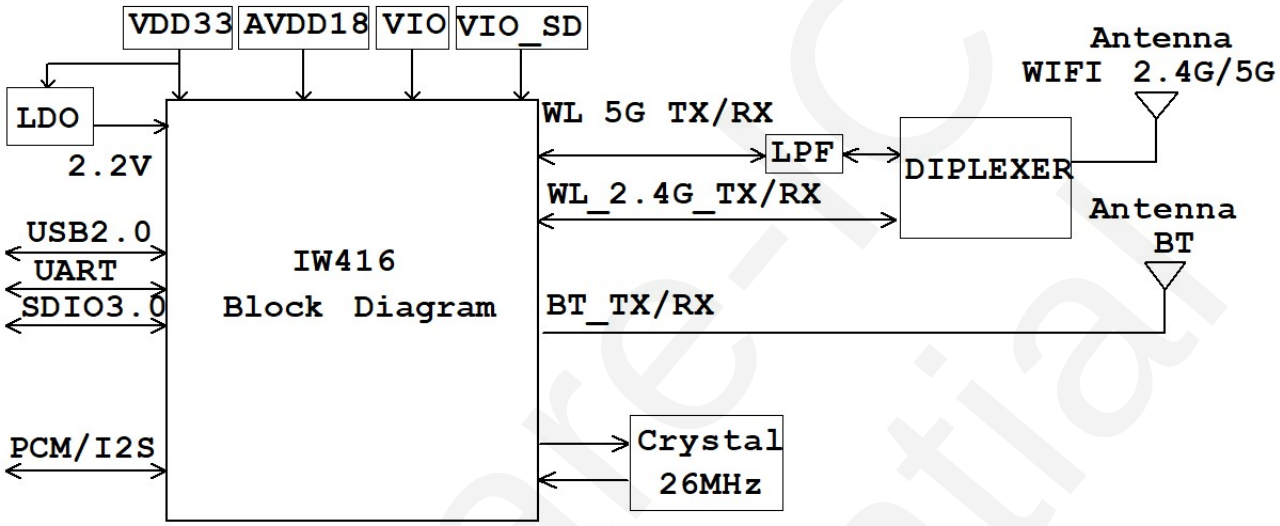
- Support 802.11 a/b/g/n
- Dual bands: 2.4 GHz and 5 GHz
- Single stream 802.11n with 20 MHz and 40 MHz channels
- Up to MCS7 data rates (150 Mbps)
- Support 802.11mc for location
- Dynamic Rapid Channel Switching (DRCS) for simultaneous and power efficient
- operation in 2.4 GHz and 5 GHz bands
- Security: WPA3 and WPA

2.2 Bluetooth Features

- Full Bluetooth 5.1 features
- Long range - 4x coverage
- 2 Mbps data rate - 2x faster
- Connection/connectionless AoA
- Connection/connectionless AoD
- Improved advertisement capacity- enables more IoT services
- Audio interface: I^2S and PCM
- Security: AES

3. Block Diagram

A simplified block diagram of the LS001ONWAS is depicted in the figure below.



4. Specifications Table

4.1 General Specification

Model Name	LS001ONWAS
Product Description	Support Wi-Fi 2.4G&5G/BT5.1 Functionalities
Dimension	L x W x H(Max)：15*15*2.55(Max)mm
Main Chip	IW416(NXP)
Standard	802.11a/b/g/n
Wi-Fi Encryption	WEP 64- and 128-bit encryption with hardware TKIP processing (WPA) AES/CCMP as part of the 802.11i security standard (WPA2 and WPA3) AES/CMAC as part of the 802.11w security standard WAPI
BT Encryption	AES
Wi-Fi Interface	SDIO3.0/USB2.0
BT Interface	SDIO3.0/USB2.0/UART
Package	Stamp
Audio interface	I^2S and PCM

4.2 WLAN&BT Specification

4.2.1 2.4G WLAN Specification

Features	Description
Operating Frequency	2.412GHz~2.472 GHz
Standards	IEEE 802.11b/g/n, Wi-Fi compliant
Modulation	802.11b: DQPSK, DBPSK, CCK 802.11g/n : OFDM
Data Rates	802.11b: 1, 2, 5.5, 11Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11n: Maximum data rates up to 150Mbps (40MHz channel)
Output Power	802.11b@11Mbps : 17dBm +/- 2dBm @ EVM≦35%
	802.11g@54Mbps : 16dBm +/- 2dBm @ EVM≦-27dB
	802.11n@ HT20 MCS 7 : 14dBm +/- 2dBm @ EVM≦-28dB
	802.11n@ HT40 MCS 7 : 14dBm +/- 2dBm @ EVM≦-28dB
Receiver Sensitivity	802.11b@11Mbps : -86dBm
	802.11g@54Mbps : -70dBm
	802.11n@ HT20 MCS 7 : -68dBm
	802.11n@ HT40 MCS 7 : -66dBm
Number of Channels	USA, North America, Canada and Taiwan: (Ch. 1-11) China, Australia, Most European Countries, Japan: (Ch. 1-13)

4.2.2 5G WLAN Specification

Features	Description
Operating Frequency	5.15GHz~5.825 GHz
Standards	IEEE 802.11a/n, Wi-Fi compliant
Modulation	802.11a/n : OFDM
Data Rates	802.11a: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11n: Maximum data rates up to 150Mbps (40MHz channel)
Output Power	802.11a@54Mbps : 16dBm +/- 2dBm @ EVM≦-27dB
	802.11n@ HT20 MCS 7 : 15dBm +/- 2dBm @ EVM≦-28dB
	802.11n@ HT40 MCS 7 : 14dBm +/- 2dBm @ EVM≦-28dB
Receiver Sensitivity	802.11a@54Mbps : -70dBm
	802.11n@ HT20 MCS 7 : -66dBm
	802.11n@ HT40 MCS 7 : -65dBm
Number of Channels	USA, Canada, Most European Countries - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,1 36,140,149,153,157,161,165 Japan - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140 China - 36,40,44,48,52,56,60,64, 149,153,157,161,165

4.2.3 BT Specification

Standard	Bluetooth 5.1
Modulation	GFSK, π/4-DQPSK, 8DPSK
Frequency Band	2402MHz~2483MHz
Output Power	BDR: 0~4dBm, typ:2dBm EDR: 0~4dBm, typ:2dBm LE: 0~4dBm, typ:2dBm
Sensitivity	BDR(DH5): -80dBm @ BER<0.1% EDR(2DH5): -85dBm @ BER<0.01% LE : -92dBm @ BER<30.8%
Number of Channels	79 Channels

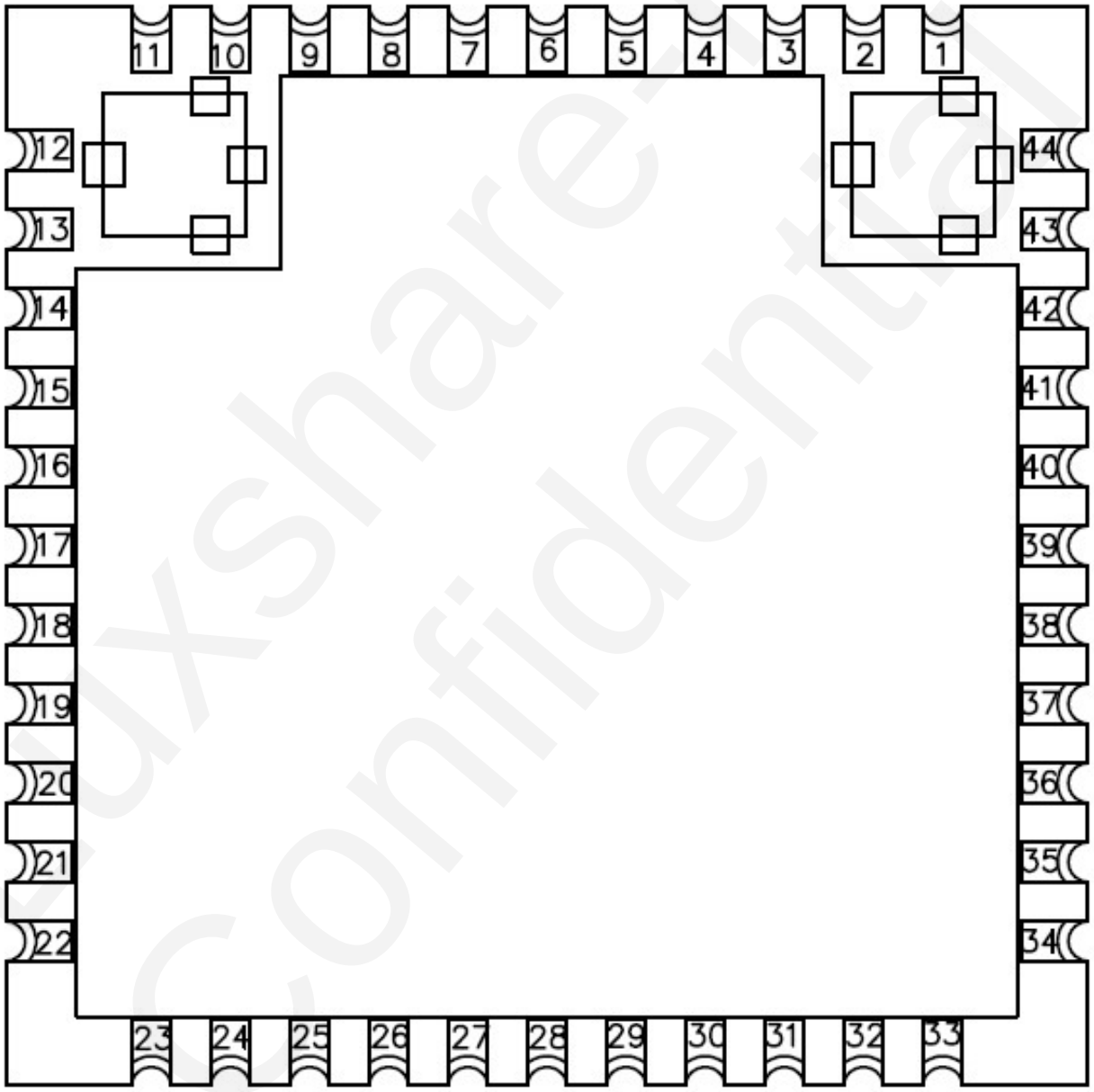
4.3 Operating Conditions

Operation Conditions	
Voltage	VDD33: 3.3V AVDD18: 1.8V VIO: 3.3V/1.8V VIO_SD: 3.3V/1.8V
Operating Temperature	0℃ to 70℃
Storage Temperature	-40℃ to 85℃
Humidity	Less than 95% (Non-Condensing)
ESD Protection	
Human Body Model	+-2KV
Changed Device Model	+-500V

5. Pin Assignments

5.1 Pin Map

LS001ONWAS Top View Pin Map



5.2 Pin Definition

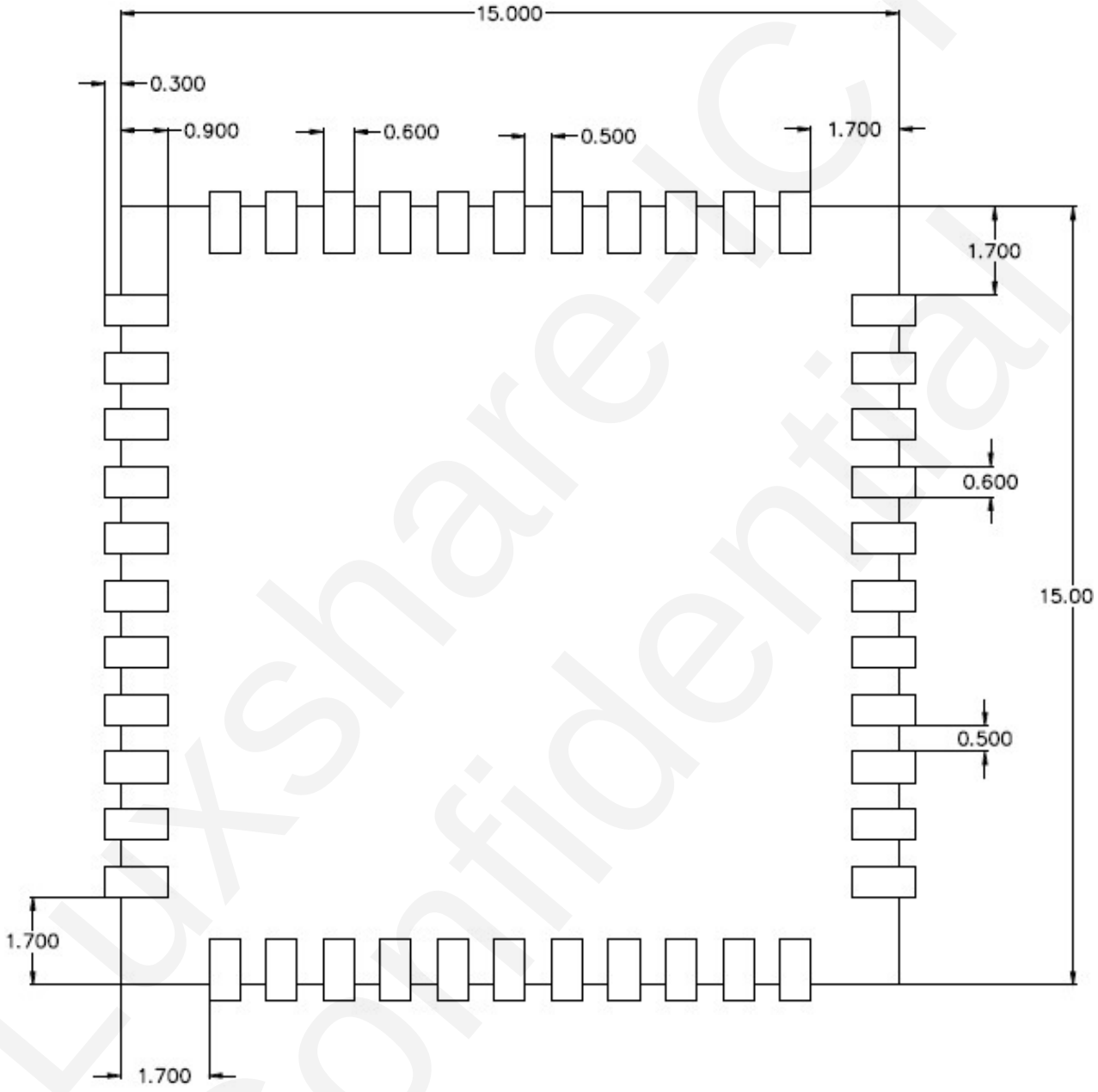
Pin No	Definition	Description	Voltage	Type
1	GND	Ground connections	---	---
2	GND	Ground connections	---	---
3	NC	No connect to anything	---	Floating
4	CON[0]	Firmware Boot Options [00] or [01]: USB[WLAN+BT] [10]: SDIO[WLAN]+UART[BT] [11]: SDIO[WLAN]+SDIO[BT]	VDD33	I
5	CON[1]	To set a configuration bit to 0, attach a 51k resistor from the pin to ground. No external circuitry is required to set a configuration bit to 1	VDD33	I
6	NC	No connect to anything	---	Floating
7	AVDD18	1.8V Analog Power Supply	1.8V	P
8	GND	Ground connections	---	---
9	GND	Ground connections	---	---
10	GND	Ground connections	---	---
11	GND	Ground connections	---	---
12	GND	Ground connections	---	---
13	GND	Ground connections	---	---
14	VDD33	3.3V Power Supply	3.3V	P
15	VDD33	3.3V Power Supply	3.3V	P
16	SLP_CLK	External Low Power Clock input(32.768KHz)	AVDD18	I
17	BT_RESET	BT reset pin	VIO	I
18	WL_RESET	WL reset pin	VIO	I
19	GPIO5	GPIO Mode: GPIO [5]	VIO	I/O

19	GPIO5	PCM_DOUT I2S_DOUT		O O
20	GPIO7	GPIO Mode: GPIO [7] PCM_SYNC I2S_LRCLK	VIO	I/O I/O I/O
21	System_PDn	Full Power-down input Low: Full power-down mode High: Normal mode Internal pull-up on this pin	AVDD18	I
22	WL_HOST_WAKE	WL device wake-up HOST	VIO	O
23	GPIO4	GPIO Mode: GPIO [4] PCM_DIN I2S_DIN	VIO	I/O I I
24	BT_HOST_WAKE	Bluetooth device to wake-up HOST	VIO	O
25	GPIO6	GPIO Mode: GPIO [6] PCM_CLK I2S_BCLK	VIO	I/O I/O I/O
26	GPIO3	GPIO Mode: GPIO [3] PCM_MCLK(optional) I2S_CCLK(optional)	VIO	I/O I/O I/O
27	SD_CMD	SDIO Command	VIO_SD	I/O
28	SD_CLK	SDIO Clock input	VIO_SD	I
29	SD_D0	SDIO Data line 0	VIO_SD	I
30	SD_D1	SDIO Data line 1	VIO_SD	I
31	SD_D2	SDIO Data line 2	VIO_SD	I
32	SD_D3	SDIO Data line 3	VIO_SD	I
33	GND	Ground connections	---	---
34	VIO_SD	1.8V/3.3V Digital I/O SDIO Power Supply	1.8/3.3V	P

35	USB_DP	USB 2.0 Serial Differential Data Positive	VDD33	I/O
36	USB_DN	USB 2.0 Serial Differential Data Negative	VDD33	I/O
37	GND	Ground connections	---	---
38	VIO	1.8V/3.3V Digital I/O Power Supply	1.8/3.3V	P
39	BT_UART_RXD	UART_RXD	VIO	I
40	BT_UART_TXD	UART_TXD	VIO	O
41	BT_UART_RTS	UART_RTS	VIO	O
42	BT_UART_CTS	UART_CTS	VIO	I
43	BT_WAKE	HOST wake-up Bluetooth device	VIO	I
44	WL_WAKE	HOST wake-up WL device	VIO	I

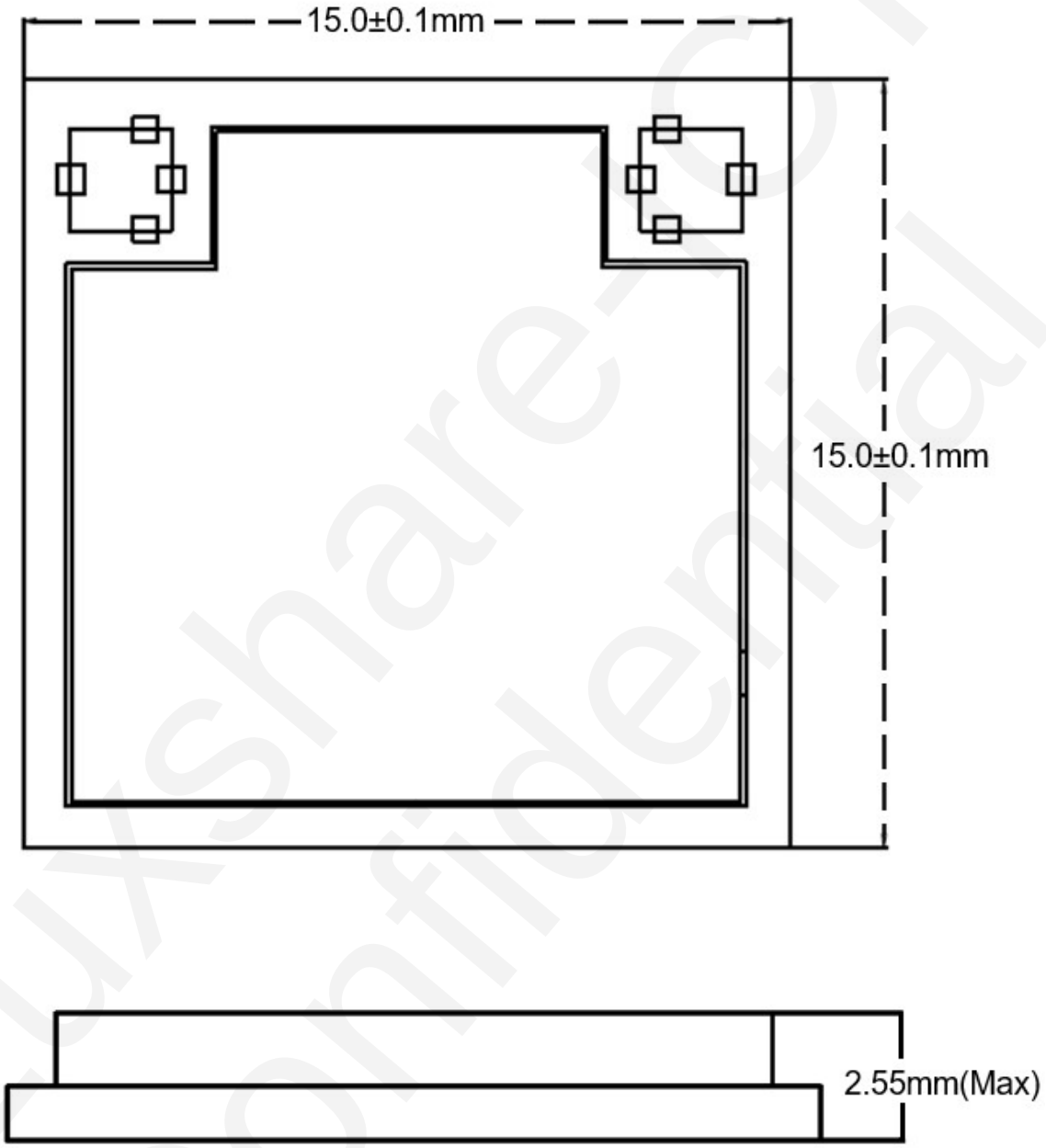
5.3 Layout Recommendation

Unit: mm



5.4 Physical Dimensions

Unit: mm



6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
VDD33	Power supply voltage with respect to VSS	--	3.3	3.96	V
AVDD18	Power supply voltage with respect to VSS	--	1.8	1.98	V
VIO	Power supply voltage with respect to VSS	--	1.8	2.2	V
		--	3.3	4.0	V
VIO_SD	Power supply voltage with respect to VSS	--	1.8	2.2	V
		--	3.3	4.0	V

6.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VDD33	3.3V power supply	3.14	3.3	3.46	V
AVDD18	1.8V Analog power supply	1.71	1.8	1.89	V
VIO	1.8V/3.3V digital I/O power supply	1.62	1.8	1.98	V
		2.97	3.3	3.47	V
VIO_SD	1.8V/3.3V digital SDIO I/O power supply	1.62	1.8	1.98	V
		2.97	3.3	3.47	V

6.3 DC Characteristics

6.3.1 VIO DC characteristics-3.3V/1.8V operation

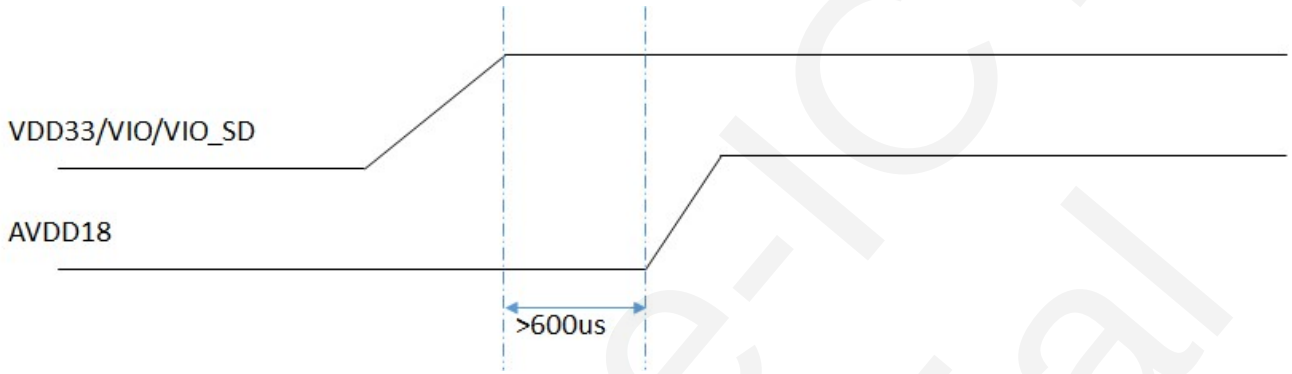
Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	--	0.7*VIO	--	VIO+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

6.3.2 VIO_SD DC characteristics-3.3V/1.8V operation

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	--	0.7*VIO_SD	--	VIO_SD+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO_SD	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO_SD-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

6.3.3 Power up Timing Sequence

A minimum time of 600us is required from VDD33/VIO/VIO_SD ready until AVDD18 ramp-up.



7. Host Interface

7.1 SDIO Host Interface

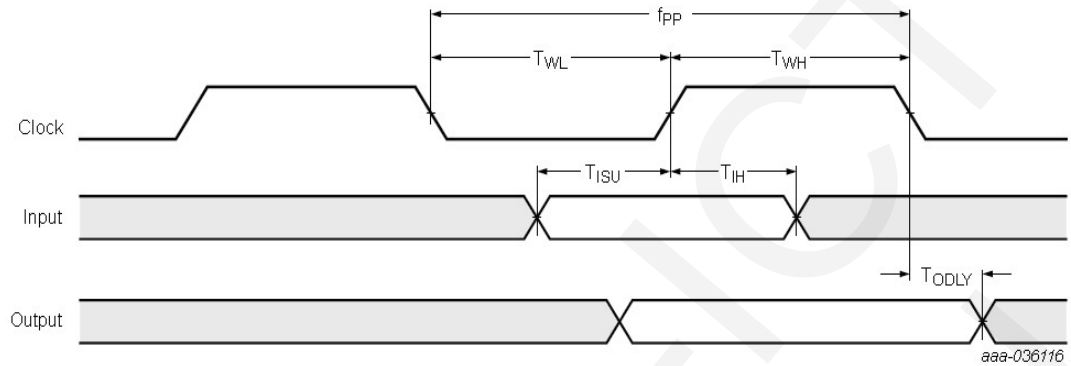
The SDIO host interface pins are powered by VIO_SD voltage supply.

The SDIO electrical specifications are identical for 4-bit SDIO and 1-bit SDIO (and SPI) transfer modes.

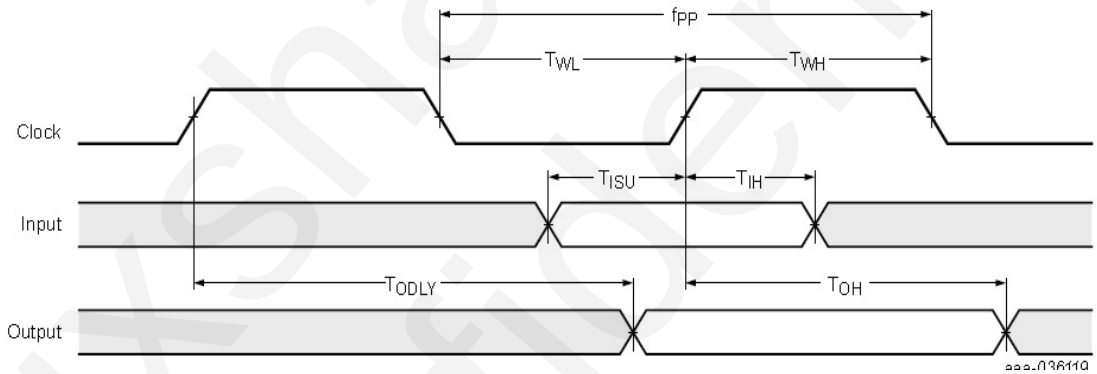
7.1.1 SDIO Interface Signals

Pin Name	Type	Description
SD_CLK	I	SDIO 4-bit Mode: Clock input SDIO 1-bit Mode: Clock input SDIO SPI Mode: Clock input
SD_CMD	I/O	SDIO 4-bit Mode: Command/response (input/output) SDIO 1-bit Mode: Command line SDIO SPI Mode: Data input
SD_D0	I/O	SDIO 4-bit Mode: Data line Bit[0] SDIO 1-bit Mode: Data line SDIO SPI Mode: Data output
SD_D1	I/O	SDIO 4-bit Mode: Data line Bit[1] SDIO 1-bit Mode: Interrupt SDIO SPI Mode: Interrupt
SD_D2	I/O	SDIO 4-bit Mode: Data line Bit[2] or read wait(optional) SDIO 1-bit Mode: Read wait (optional) SDIO SPI Mode: Reserved
SD_D3	I/O	SDIO 4-bit Mode: Data line Bit[3] SDIO 1-bit Mode: Reserved SDIO SPI Mode: Card select (active low)
VIO_SD	P	1.8V/3.3V Digital SDIO I/O Power Supply For SDIO 2.0 running at 25/50 MHz clock frequency, VIO_SD must be 3.3V

7.1.2 SDIO Timing Diagram—Default-Speed/High-Speed Modes



SDIO Timing Diagram—Default Speed Mode

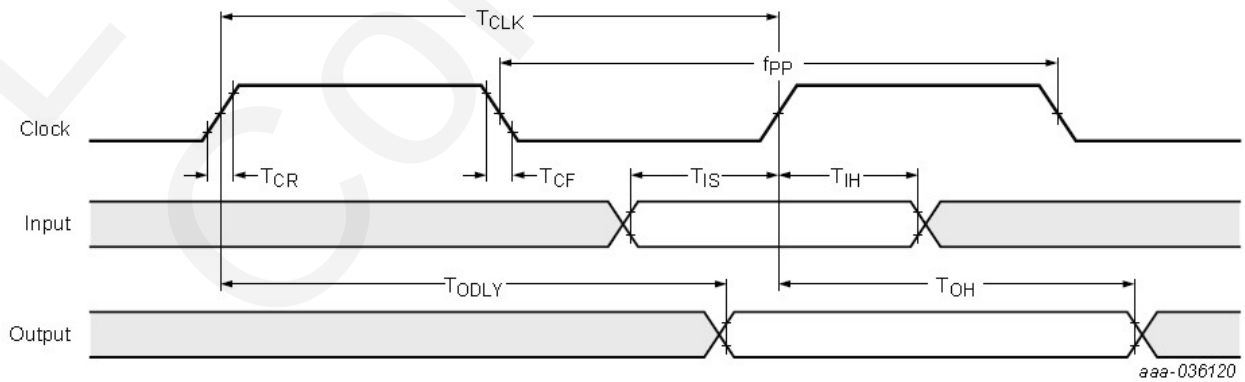


SDIO Timing Diagram—High-Speed Mode

7.1.3 SDIO Timing Data—Default-Speed/High-Speed Modes

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{pp}	Clock frequency	Default-speed	0	--	25	MHz
		High-speed	0	--	50	MHz
T_{WL}	Clock low time	Default-speed	10	--	--	ns
		High-speed	7	--	--	ns
T_{WH}	Clock high time	Default-speed	10	--	--	ns
		High-speed	7	--	--	ns
T_{ISU}	Input setup time	Default-speed	5	--	--	ns
		High-speed	6	--	--	ns
T_{IH}	Input hold time	Default-speed	5	--	--	ns
		High-speed	2	--	--	ns
T_{ODLY}	Output delay time CL ≤ 40 pF (1 card)	Default-speed	--	--	14	ns
		High-speed	--	--	14	ns
T_{OH}	Output hold time	High-speed	2.5	--	--	ns

7.1.4 SDIO Timing Diagram—SDR12/SDR25/SDR50 Modes (up to 100 MHz) (1.8V)



SDIO Timing Diagram—SDR12, SDR25, SDR50 Modes (up to 100 MHz) (1.8V)

7.1.5 SDIO Timing Data—SDR12/SDR25/SDR50 Modes (up to 100 MHz) (1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock frequency	SDR12/25/50	25	--	100	MHz
T_{IS}	Input setup time	SDR12/25/50	3	--	--	ns
T_{IH}	Input hold time	SDR12/25/50	0.8	--	--	ns
T_{CLK}	Clock time	SDR12/25/50	10	--	40	ns
T_{CR},T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR12/25/50	--	--	0.2*T_{CLK}	ns
T_{ODLY}	Output delay time CL ≤ 30 pF	SDR12/25/50	--	--	7.5	ns
T_{OH}	Output hold time CL = 15 pF	SDR12/25/50	1.5	--	--	ns

7.2 USB2.0 Host Interface

7.2.1 USB2.0 Interface Signals

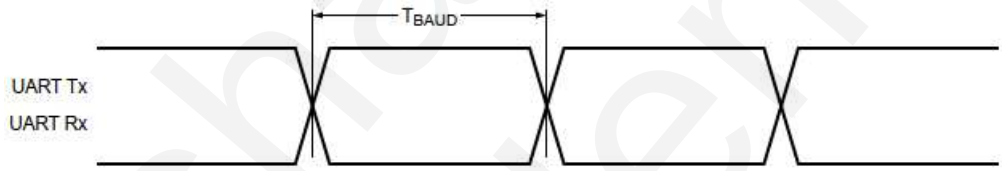
Pin Name	Type	Description
USB_DN	I/O	USB Serial Differential Data Negative
USB_DP	I/O	USB Serial Differential Data Positive
VDD33	P	USB power

7.3 UART Host Interface

7.3.1 UART Interface Signals

Pin Name	Type	Description
BT_UART_RXD	I	UART serial input signal
BT_UART_TXD	O	UART serial output signal
BT_UART_RTS	O	UART request-to-send output signal. Active low
BT_UART_CTS	I	UART clear-to-send input signal. Active low

7.3.2 UART Timing Diagram



UART Timing Diagram

7.3.3 UART Timing Data

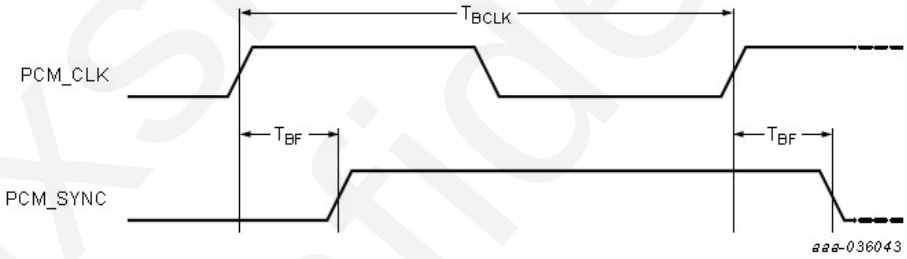
Symbol	Parameter	Condition	Min	Typ	Max	Units
TBAUD	Baud rate	26MHz input clock	250	--	--	ns

7.4 PCM Interface

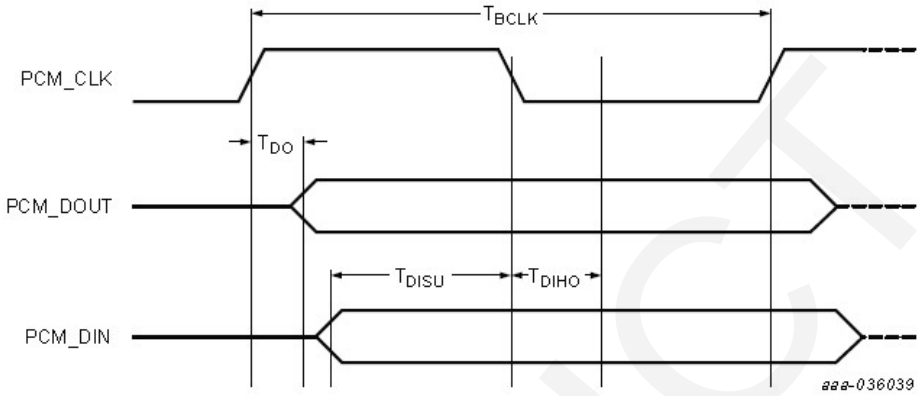
7.4.1 PCM Interface Signals

Pin Name	Type	Description
GPIO3	O	PCM_MCLK(optional)
GPIO4	I	PCM_DIN
GPIO5	O	PCM_DOUT
GPIO6	I/O	PCM_CLK
GPIO7	I/O	PCM_SYNC

7.4.2 PCM Timing Diagram—Master Mode



PCM Timing Diagram for PCM_SYNC Signal—Master Mode

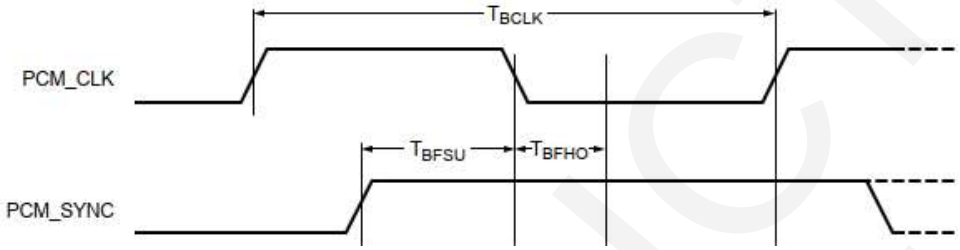


PCM Timing Diagram for Data Signals—Master Mode

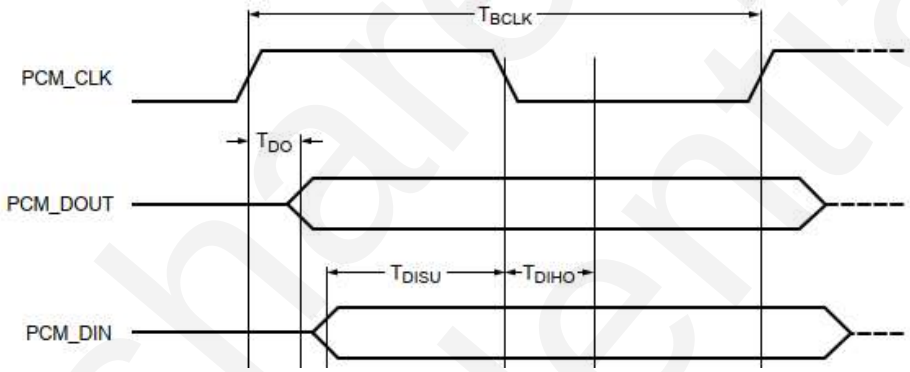
7.4.3 PCM Timing Data—Master Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	Bit clock frequency	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle	--	0.4	0.5	0.6	--
T_{BCLK} rise/fall	PCM_CLK rise/fall time	--	--	3	--	ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	--	--	--	15	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge	--	20	--	--	ns
T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge	--	15	--	--	ns
T_{BF}	Delay from PCM_CLK rising edge to PCM_SYNC rising edge	--	--	--	15	ns

7.4.4 PCM Timing Diagram—Slave Mode



PCM Timing Diagram for PCM_SYNC Signal—Slave Mode



PCM Timing Diagram for Data Signals—Slave Mode

7.4.5 PCM Timing Data—Slave Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	Bit clock frequency	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle	--	0.4	0.5	0.6	--
T_{BCLK} rise/fall	PCM_CLK rise/fall time	--	--	3	--	ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	--	--	--	30	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge	--	15	--	--	ns
T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge	--	10	--	--	ns
T_{BFSU}	Setup time for PCM_SYNC before PCM_CLK falling edge	--	15	--	--	ns
T_{BFHO}	Hold time for PCM_SYNC after PCM_CLK falling edge	--	10	--	--	ns

8. FCC Warning Statement

This equipment has been tested and found to comply with the limits for Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

• Reorient or relocate the receiving antenna.
• Increase the separation between the equipment and receiver.
• Connect the equipment to an outlet on a circuit different from that to which the receiver is connected.
• Consult the dealer or an experienced radio/TV technician for help.

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:
(1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

9. RF Exposure Warning

This equipment must be installed and operated in accordance with provided instructions and the antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. End-users and installers must be provide with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance.

10. User manual Warning

Please take attention that changes or modification not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1) This device may not cause harmful interference, and
(2) This device must accept any interference received, including interference that may cause undesired operation.
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

The module is limited to OEM installation ONLY
The OEM integrator is responsible for ensuring that the end-user has no manual instruction to remove or install module.
When the FCC identification number or ISED certification number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module.
This exterior label can use wording such as the following: "Contains FCC ID: 2A2EX-LS001" and the information should be also contained in the devices' user manual.