Exhibit 1
FCC Form 442, line 7

Single-Input Single-Output (SISO) Indoor Wireless OFDM links

a. This proposal is in connection with a state-sponsored research project called the Yamacraw Wireless Prototype, funded by the State of Georgia. The goal of this research includes the design and development radio prototypes to demonstrate a high data-rate air interface for indoor wireless communications. More specifically we hope to implement appropriate technologies to achieve high spectral efficiencies, with a goal of developing algorithms and architectures that can be extended to data rates approaching 1 Gb/s with spectral occupancies near 100 MHz. For the experimental system associated with this submission, however, the proposed spectral footprints will range between 6 MHz and 40 MHz due to equipment limitations. The waveforms to be employed by the radios will be based on orthogonal frequency division multiplexing (OFDM) modulations in a TDMA/TDD system. Various antenna architectures are anticipated as the research progresses, including single-input single-output (SISO), single input, multi-output (SIMO), multi-input single-output (MISO), and multi-input multi-output (MIMO) architectures. Attempts to maximize the spectral efficiencies and the data throughput associated with the experimental system will be optimized through use of smart antennas, space-time coding, low density parity check (LDPC) or similar coding, OFDM, and associated processing algorithms.

The radios will be configured with the equipment indicated in Exhibit #2, with likely upgrades as new boards become available. Anticipated upgrade boards for the next year are included in the list. The radios are comprised of a number of VME-based subsystem components that include single- or multi-channel RF receive front end configurations, single- or multi-channel RF transmit front end configurations, wideband A/D and digital downconversion boards, multiple quad DSP boards for IF and/or baseband processing, and D/A and I/Q upconversion boards. The programmable nature of many of the subsystems makes it very flexible in defining waveforms and processing algorithms for leading edge research in communications.

The experimental set-up will be utilized for testing and demonstrations of the indoor wireless air interface and associated prototcols between as many as four modems in an indoor multiple access environment

b. The specific objectives of the program are to integrate technologies associated with smart antennas, space-time coding, LDPC codes, OFDM, MAC protocols, automatic speech recognition, and system-on-a-chip design technologies to advance the state-of-the art associated with the design of a fixed-wireless radio system having high spectral efficiencies (e.g., 6 to 10 bits/s/Hz) that can potentially lead to data rates approaching 1 Gb/s (assuming an eventual 100 MHz footprint). While the prototype radios will only be able to achieve a fraction of the desired rates, algorithms employed in the testbed will be

investigated in a system-on-a-chip architecture study to identify SOC architecture yielding improved processing efficiency and performance.

c. OFDM-based waveforms have either been adopted or are under consideration for a number of standards, including IEEE 802.11a, ASTM DSRC, IEEE 802.16a, etc. This research, which will combine the collective efforts of approximately 20 faculty and 30 PhD students at Georgia Tech, has already resulted in contributions into the standards development of 802.16a (submission of a preamble design proposal). The goal of high spectral efficiencies (e.g., > 6 bits/s/Hz) is one that, if achieved, would help utilize scarce spectrum resources in an efficient manner. Moreover, since the collective goal of Yamacraw is to stimulate collaboration with industry, technologies developed from the research would have a means for transfer to the commercial sector. Wireless testing and demonstrations are key components in the development cycle and in soliciting commercial interest in developed technologies.

Exhibit 2
Equipment Description

The configuration of the Georgia Tech Software Radio Laboratory for the proposed experimental set-up is illustrated in Figure 2.1. The relevant systems in the lab associated with this application include software radio platforms, associated antenna subsystems, software radio host/control PCs, and MAC application layer host PCs.

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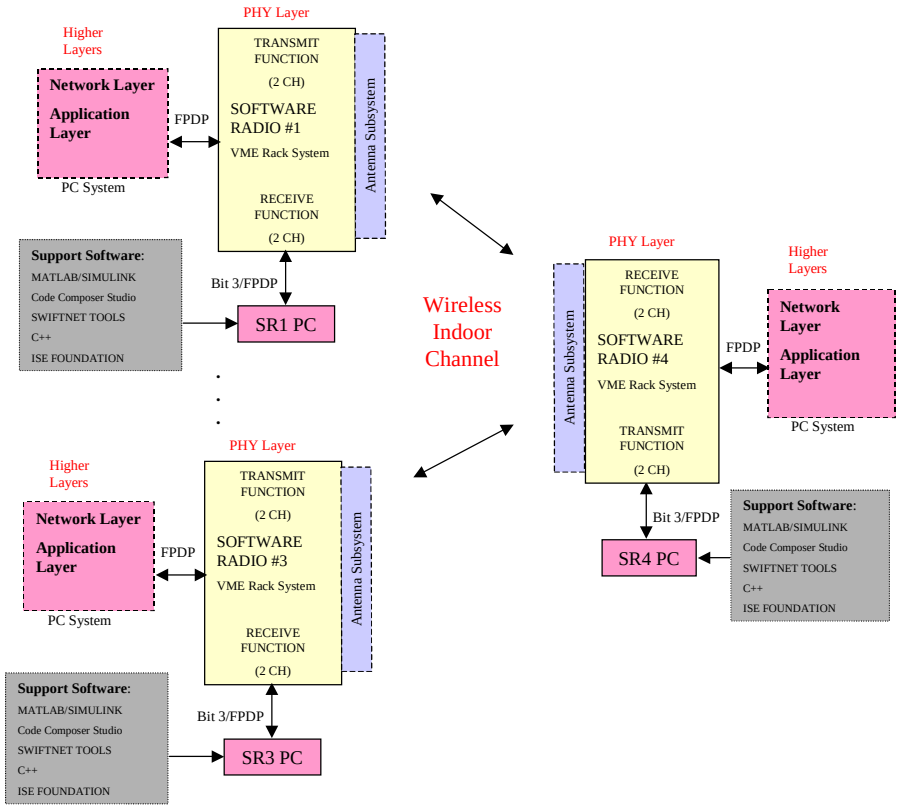


Figure 2.1. Software Radio Laboratory Configuration

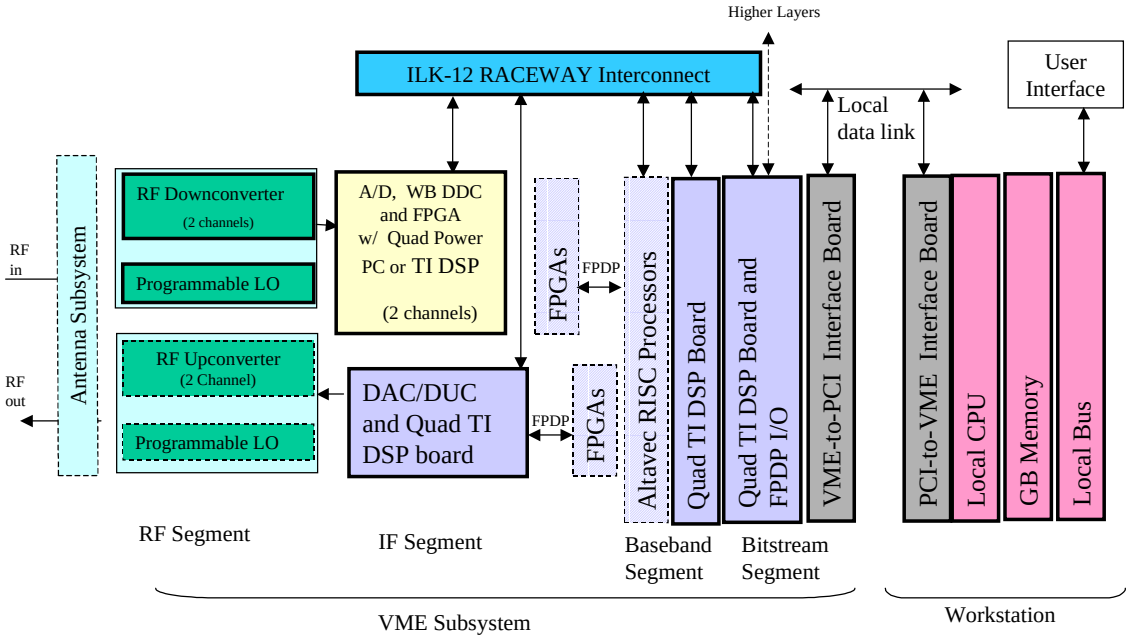
Table 2.1 provides a list of the key components comprising the wireless radios for which the license application is being made.

Table 2.1
Key Components (including anticipated future components) Comprising the Experimental Wireless Radios

Sub System	Component	Manufacturer	Model Numbers	Comments
RF RX	Two-channel RF to baseband converter	APCOM	1610 RB28 and 1610 RBC40 (upgrade)	Receive-only 28 MHz and 40 MHz (upgrade)
	Synthesizer for Receive Channels	APCOM	1610-SYN-140C	Provides tunable LO for RF downconverters
RF Tx (Option 1)	Two-channel baseband to RF converter	APCOM	1610 BRC40	Transmit only; 40 MHz max BW
	Synthesizer for Transmit Channels	APCOM	1610 SYN-140C	Provides tunable LO for IF to RF upconversion
RF Tx (Option 2)	Signal Generators	Agilent	Model 4433B ESG-D Model E4438C (upgrade)	IF to RF upconversion (<20 MHz) IF to RF upconversion (>20 MHz)
Antenna (Configuration 1)	Straight 3 dBi stub Antenna	unknown	unknown	Handset antenna
Antenna (Configuration 2)	Beam-switched antenna array	Custom GT design (See exhibit 4)	N/A	Provides beam selection capability
IF Rx	Wideband Digital Receiver	Pentek	Model 1616 (26 MHz max BW) and Model 6235 (50MHz max BW) upgrade	Provides A/D conversion and digital downconversion to complex baseband; The model 6235 has an embedded FPGA
IF/ Baseband Processing	Quad Processor boards	Pentek	Models 4291, and 4291-330, and 4294	Quad processing boards based on the TI C6701 and also Motorola's Altivec G4 Power PC processors; For IF and Baseband processing
	FPGA boards	Pentek	Model 6250	
IF Tx	D/A Conversion boards	Pentek	Model 6229	Digital to analog conversion and I/Q upconversion to IF frequency; Max BW per DAC channel is 12 .5 MHz
I/O	VME-based FPDP I/O boards	Pentek	Model 6226	FPDP I/O channel (via parallel cable) from software radio to application PC
	PC-based FPDP I/O boards	VMETRO	DPIO	Provides FPDP I/O link to the PCI bus in the application PC
	PCI-to-VME I/O boards	Pentek	Model 4229	VME-to-PCI interface data link with host PC
	Raceway Interconnect boards	Pentek	Model 6219	Provides high-rate data path across multiple quad DSP boards
Data Collection	1GB and 2 GB buffer	Communication Automation Corporation	6VDL2A	High data rate buffers
Computers	Host Computers	Dell Computers	Dell WorkStations	Host development tools and control/programming of software radio

	Application PCs	Dell Computers	Dell WorkStations	Hosts the MAC and other higher layers in the system

As shown in Figure 2.2, the GT software radio is configured for both receive and transmit processing functions. Each software radio is implemented as a VME rack system populated with COTS equipment to provide functions associated with RF down- and up-conversion, analog-to-digital conversion, digital-to-analog conversion, IF processing, baseband processing, and bitstream processing. A high data rate bus, called RACEWAY, is shared between processing boards to facilitate data transfers at rates up to 160 Mb/s. Each software radio is to be connected via an FPDP I/O link to a dedicated PC for the MAC and/or application layers associated with the modem. A photo of a software radio platform is shown in Figure 2.3.



*Note: Design based partly on architecture proposed by Joe Mitola

Figure 2.2. Software Radio Platform Configuration

Receive Chain

The receive RF front-end in each software radio platform includes a synthesizer board and two downconversion channels. These RF boards, obtained from APCOM Inc., include capability to synchronously downconvert input RF frequencies up to 3 GHz. The synthesizer board generates a programmable LO signal that is shared by the down-conversion boards for synchronous operation. The down-conversion boards each represent a separate physical receive channel with down-conversion circuitry, including image rejection filters, low noise amplifiers (LNAs), filters, amplifiers, and mixers. RF signals may be input to the receiver boards via cable connections from the outputs of the RF channel emulators or other sources. The input signals are filtered in the receiver to a spectral footprint of 28 MHz (40 MHz upgrade is pending), and are then down-converted to a low IF frequency for analog to digital conversion. The selection of the IF is driven by the A/D sampling rate associated with the A/D converters in the digital receiver boards that follow the RF down-conversion boards. C-based programs were developed to control the boards from the software radio (SR) host computers.

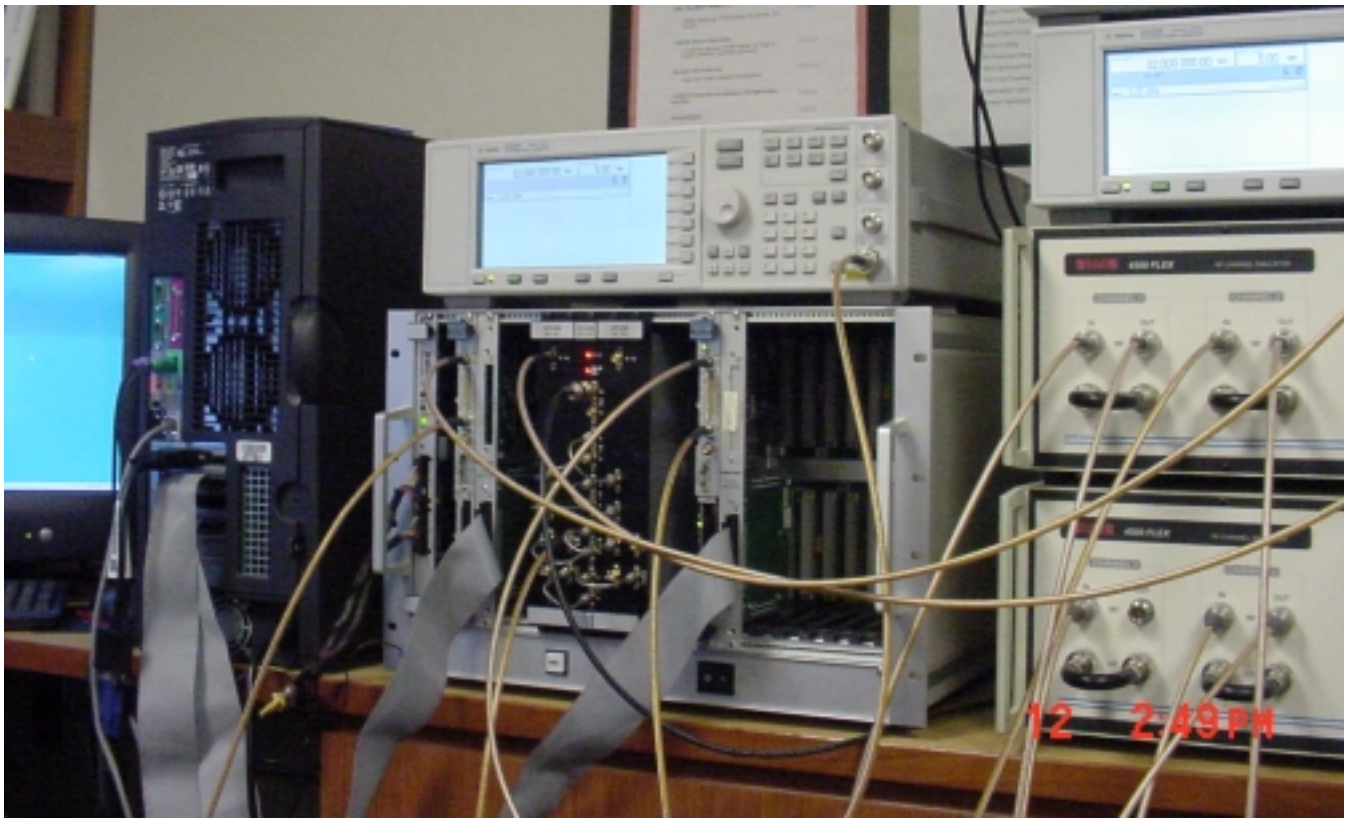


Figure 2.3. Photo of the Software Radio Platform with a VME/PCI controller, a two-channel Wideband Receiver Module and a dual FPDP module mounted on a Quad TI

C6701 DSP board, two phase-coherent RF downconversion channels with a shared synthesizer board, and a DAC/DUC board and dual FPDP board mounted on a Quad TI C6701 DSP board. The signal generator is used for IF to RF conversion.

The resulting IF signals are applied to the inputs of the digital receiver boards, where the signals are prefiltered with anti-aliasing filters and are sampled with A/D converters at a rates up to 105 Msamples/s. Signal bandwidths in excess of the desired 40 MHz signal bandwidth can be sampled without aliasing. Following the sampling operation, the signals are converted to complex baseband with digital receiver chips. The wideband down-converters support output bandwidths up to 40 MHz. The digital receiver chips have numerically controlled oscillators (NCOs), filters, and decimators for the down-conversion process. Synchronous demodulation across as many as eight channels is possible. If intermediate frequency (IF) processing is desired, such as for despreading or digital downconversion, the digital down-converters can be bypassed and the sampled signals output directly to an FPGA (on –board) or to a Pentek quad processing board.

Following down-conversion to baseband, the sampled signals are buffered to a quad DSP boards for baseband and bitstream processing, which could include baseband demodulation, decoding, and other processing functions. A RACEWAY interconnect is available to support high data-rate transfers between quad processor boards. The anticipated configuration will include four quad DSP boards and two quad Power PC boards all connected to a RACEWAY crossbar switch. An FPGA board will be acquired to support FPGA-based baseband processing. Following signal processing, the demodulated data is passed through an FPDP I/O link to a dedicated host platform for higher layer functions, or alternatively to a large (i.e., 2 Gbyte) memory buffer via FPDP for signal storage and post collection processing.

Transmit Chain

The transmit chain is projected to include data framing, data transfer from the application PC to the software radio platform, interleaving, FEC coding, space-time coding, symbol formation, OFDM modulation, guard insertion, digital to analog conversion, and IF-to-RF frequency conversion. Data from the application PC is streamed to a quad processing board in the software radio via an FPDP I/O link. Baseband modulation processing can be accomplished with the processing board and optionally with support from an FPGA board. The resulting baseband real and complex samples are buffered to a DAC/DUC, which performs digital to analog conversion, I/Q modulation, and upconversion to IF. The resulting analog IF signal is input to an IF to RF converter. A signal generator or dedicated VME-based transmit boards will be utilized for this function for the frequency conversion and transmit functions. The RF transmit front end is to provide 2-channel operation.

The specific operating characteristics of the prototype radios for the proposed experimental license are indicated in Exhibit 3. Note that the experimental set-up

includes single and multiple antenna configurations with straight 3 dBi antenna elements and a multiple antenna configuration with higher-gain beams derived from the Georgia Tech beamswitch antenna array.

Exhibit 3
Wireless System Attributes

Frequency Band: 2.4 GHz to 2.4835 GHz

Emission Type: (See Section 2.201)
OFDM

Modulation parameters
Block FFT size: 16 to 256
Max number of non-zero subcarriers: 208
OFDM Symbol duration: 0.32 us to 32 us (without guard interval)
Guard Interval: 0.08 us to 8 us.
Symbol levels: BPSK, 4-, 8-, 16-, 32-, 64-, 128-, and 256-QAM
Signaling Bandwidth (i.e., 3 dB Spectral Occupancy): ranges from 6.5 to 40.6 MHz

Antenna configuration:
SISO: single antenna at tx, single antenna at receiver
SIMO: single antenna at tx, multiple antennas at receiver
MISO: multiple antennas at tx, single antenna at receiver
MIMO: multiple antennas at tx, multiple antennas at receiver
Max number of antenna elements in array: 4
Antenna element types: 1) Straight "Rubber Duck" antenna
2) Beams from beamswitch matrix

2.4 GHz straight Rubber Duck antenna

Max RF Output power at Tx terminals:
10 dBm (single antenna configuration)
10 dBm combined power (assuming an array of omnidirectional antennas)

Max ERP from Antenna:
Max Antenna Gain: 2.2 dBi
Orientation: Vertically Polarized
Width of beam at 3dB points: Omnidirectional
Mean EIRP: 0.0166 W (0.235 V/m @ 3m)

Peak EIRP: 3.4 W [Based on PAP Ratio: < 23.2 dB (with ≤ 208 non-zero subcarriers]

2.4 GHz Beamswitched Antenna:

Max RF Output power at Tx terminals: 7 dBm per beam

Max ERP from Array:

Max Array Gain: 5 dBi
Orientation: Vertically Polarized
Width of beam at 3dB points: 13 degrees
Mean EIRP per beam: 0.0158 W (0.229 V/m @ 3m)
Peak EIRP: 3.3W [Based on PAP Ratio: < 23.2 dB (with ≤ 208 non-zero subcarriers]

Note 1: The maximum bandwidth may be achieved either through utilization of upgrade equipment that can support a 40 MHz signaling bandwidth, or alternatively employing up to four contiguous DAC subbands (see Table 2.1), each with maximum signaling bandwidths of 10 MHz.

Note 2: The bandwidth determination is based on the OFDM symbol rate and the number of non-zero subcarriers. Zero padding of approximately 20 to 25% of the subcarriers will normally be applied.

Location of transmitter and receiver: The prototype radios will be used in the Georgia Center for Advanced Telecommunications Technologies building, located on 14th street near the campus of Georgia Tech. Testing will normally be conducted in room 543. Demonstrations will also be conducted in the GCATT building but will not necessarily be confined to room 543. Other more open spaces (e.g., auditorium, conference rooms, etc) may be employed to accommodate crowds. In all cases, deployed antennas will be less than 2 meters above the floor.

Exhibit 4
Description of the Multibeam Antenna Setup

We consider an arrangement of four linear arrays in the horizontal plane, as shown in Fig. 4.1, where each linear array is represented by a dashed line and serves a 90 degree sector. Each array will have 8 elements. The beam mainlobes are shown in polar format for the array on the right.

The array weights are controlled by the Butler matrix, switch matrix and micro-controller boards, which are under construction. Their diagrams are shown in Fig. 4.2.

The half-power beamwidth (HPBW) for a phased array is found by taking the difference in the half power points. The equation for the half-power points is:

$$\theta_h = \cos^{-1}\left[\frac{\lambda}{2\pi d}\left(-\beta \pm \frac{2.782}{N}\right)\right]$$

Calculating the upper and lower half-power angles and finding the difference gives a HPBW of approx. 12.91^o.

The antenna elements are patch antennas, vertically polarized, with directivity in the elevation plane of 4 dBi and directivity in the azimuth plane of 0 dBi. They have an efficiency factor of -4 dB, so the peak element gain is 0 dBi.

The directivity of the array factor is 8, or 9 dB, because there are 8 elements. The beamformer and switch matrix are expected to have an insertion loss of about 4 dB. Therefore the overall maximum gain of the array in dB is the peak element gain plus the array factor minus the insertion loss, yielding about 5 dBi.

We would like to apply up to 7dBm of power to each of two selected beamports simultaneously to achieve transmit diversity through space-time block coding. The EIRP for one beam, therefore, is 22dBm (0.229V/m @ 3m).

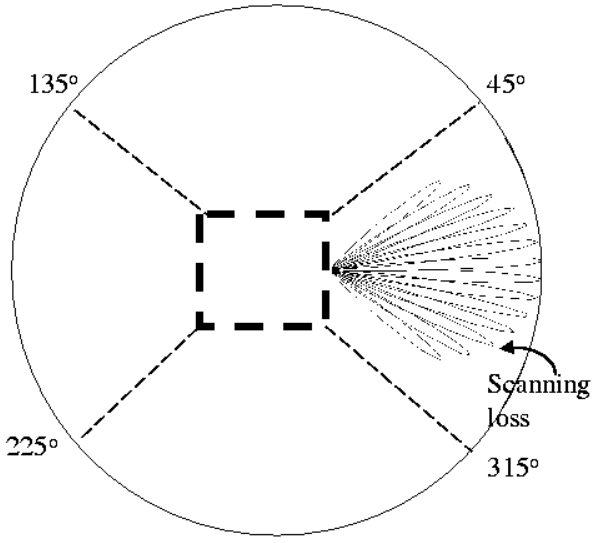


Figure 4.1. Illustration of the mainlobes of the different beams formed by one of the four RF beamformers.

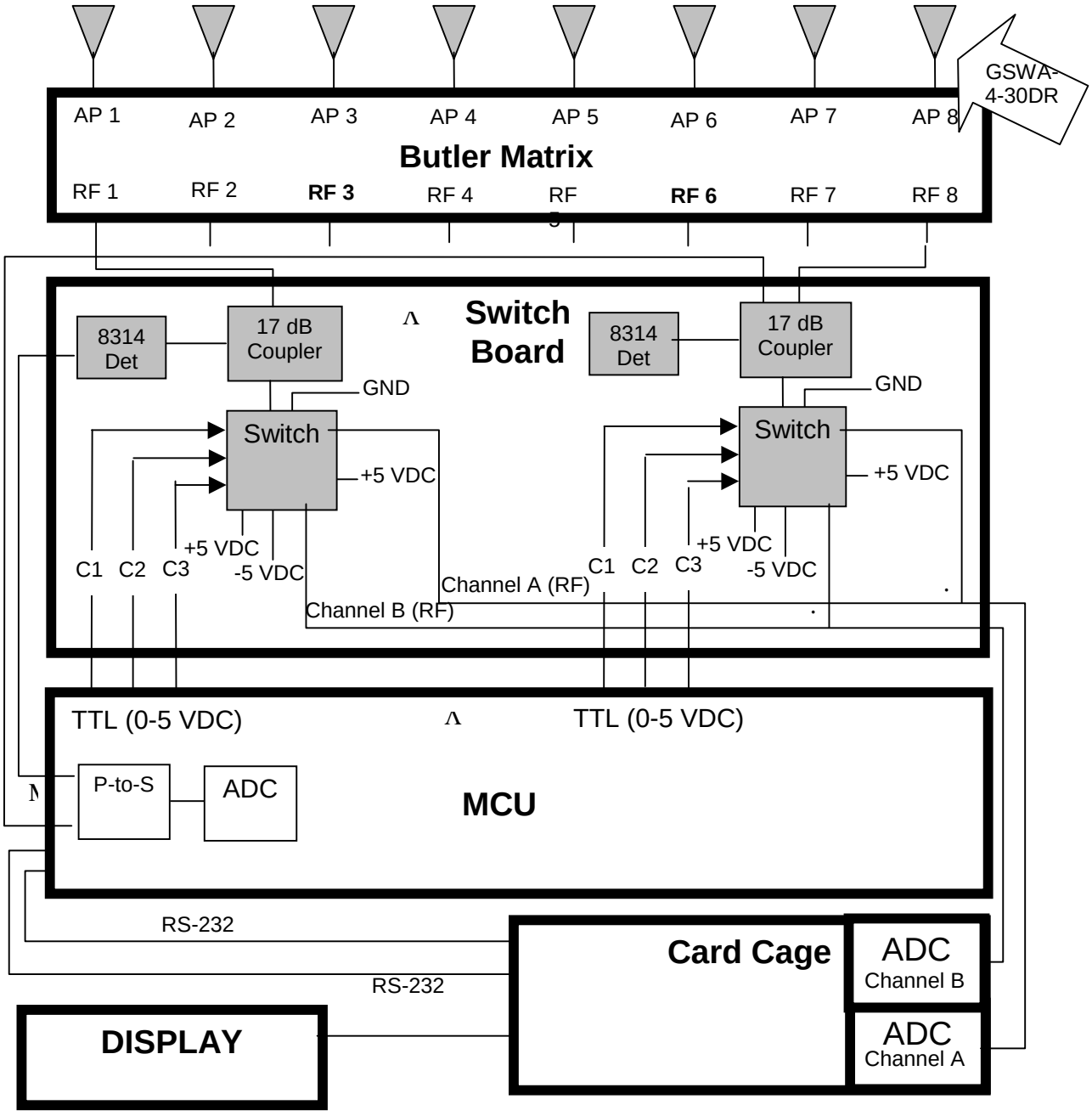


Figure 4.2. Block diagram of a RF multibeam beamformer and its associated controller. The beamformer comprises a Butler matrix board, a switch matrix board, and a microcontroller. The microcontroller interfaces both the switch board and the DSPs in the card cage.