Exhibit 2
Equipment Description

The configuration of the Georgia Tech Software Radio Laboratory for the proposed experimental set-up is illustrated in Figure 2.1. The relevant systems in the lab associated with this application include software radio platforms, associated antenna subsystems, software radio host/control PCs, and MAC application layer host PCs.

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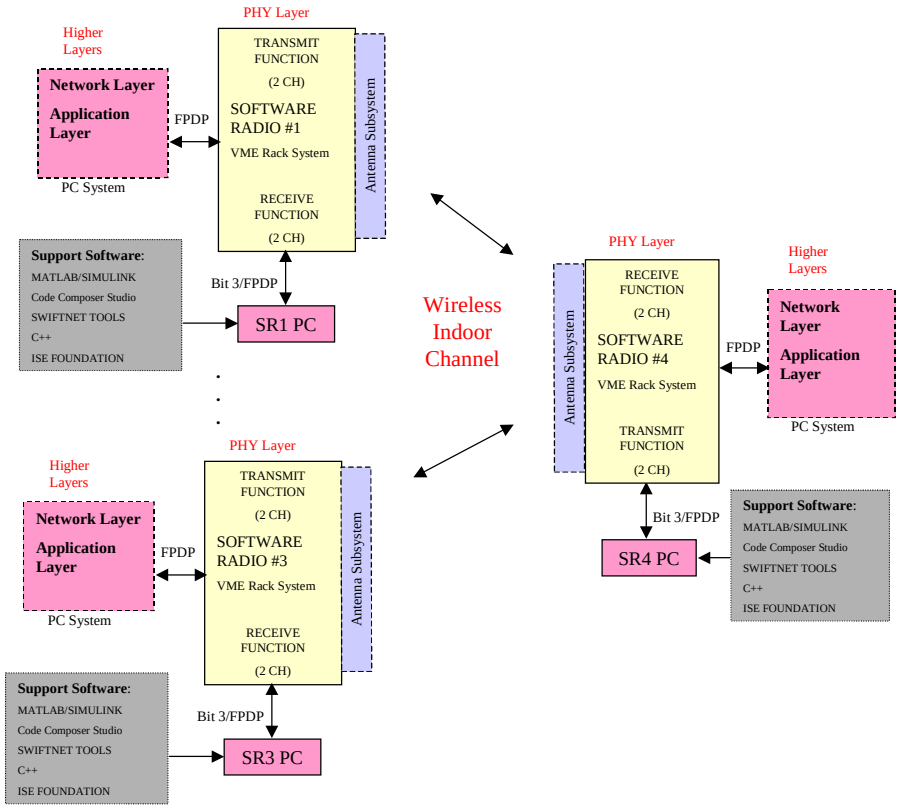


Figure 2.1. Software Radio Laboratory Configuration

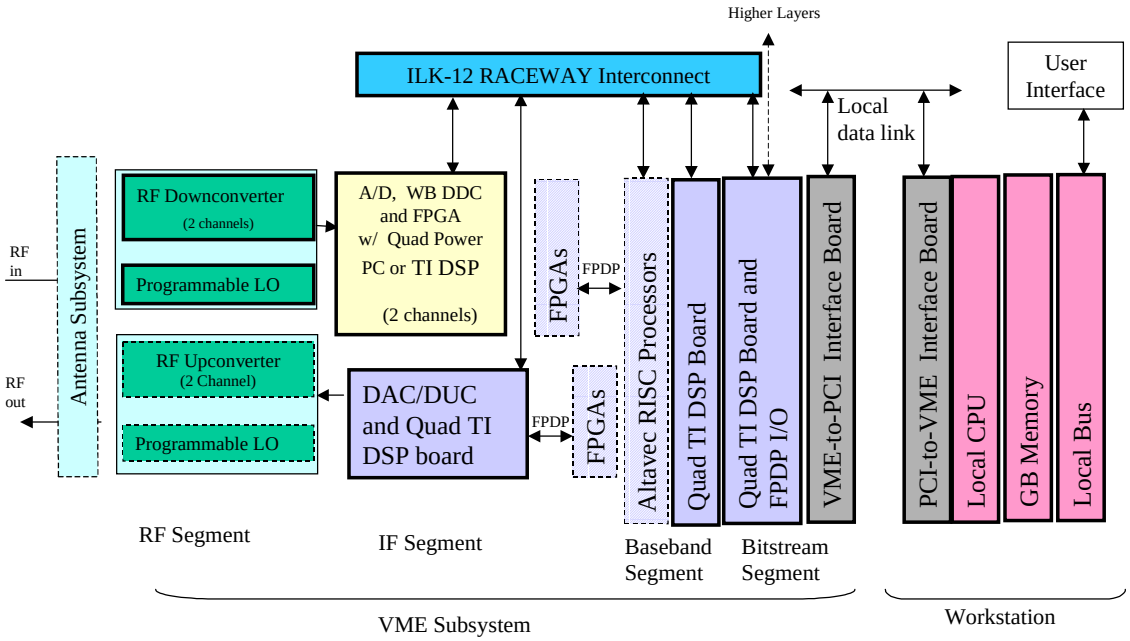
Table 2.1 provides a list of the key components comprising the wireless radios for which the license application is being made.

Table 2.1
Key Components (including anticipated future components) Comprising the Experimental Wireless Radios

Sub System	Component	Manufacturer	Model Numbers	Comments
RF RX	Two-channel RF to baseband converter	APCOM	1610 RB28 and 1610 RBC40 (upgrade)	Receive-only 28 MHz and 40 MHz (upgrade)
	Synthesizer for Receive Channels	APCOM	1610-SYN-140C	Provides tunable LO for RF downconverters
RF Tx (Option 1)	Two-channel baseband to RF converter	APCOM	1610 BRC40	Transmit only; 40 MHz max BW
	Synthesizer for Transmit Channels	APCOM	1610 SYN-140C	Provides tunable LO for IF to RF upconversion
RF Tx (Option 2)	Signal Generators	Agilent	Model 4433B ESG-D Model E4438C (upgrade)	IF to RF upconversion (<20 MHz) IF to RF upconversion (>20 MHz)
Antenna (Configuration 1)	Straight 3 dBi stub Antenna	unknown	unknown	Handset antenna
Antenna (Configuration 2)	Beam-switched antenna array	Custom GT design (See exhibit 4)	N/A	Provides beam selection capability
IF Rx	Wideband Digital Receiver	Pentek	Model 1616 (26 MHz max BW) and Model 6235 (50MHz max BW) upgrade	Provides A/D conversion and digital downconversion to complex baseband; The model 6235 has an embedded FPGA
IF/ Baseband Processing	Quad Processor boards	Pentek	Models 4291, and 4291-330, and 4294	Quad processing boards based on the TI C6701 and also Motorola's Altivec G4 Power PC processors; For IF and Baseband processing
	FPGA boards	Pentek	Model 6250	
IF Tx	D/A Conversion boards	Pentek	Model 6229	Digital to analog conversion and I/Q upconversion to IF frequency; Max BW per DAC channel is 12 .5 MHz
I/O	VME-based FPDP I/O boards	Pentek	Model 6226	FPDP I/O channel (via parallel cable) from software radio to application PC
	PC-based FPDP I/O boards	VMETRO	DPIO	Provides FPDP I/O link to the PCI bus in the application PC
	PCI-to-VME I/O boards	Pentek	Model 4229	VME-to-PCI interface data link with host PC
	Raceway Interconnect boards	Pentek	Model 6219	Provides high-rate data path across multiple quad DSP boards
Data Collection	1GB and 2 GB buffer	Communication Automation Corporation	6VDL2A	High data rate buffers
Computers	Host Computers	Dell Computers	Dell WorkStations	Host development tools and control/programming of software radio

	Application PCs	Dell Computers	Dell WorkStations	Hosts the MAC and other higher layers in the system

As shown in Figure 2.2, the GT software radio is configured for both receive and transmit processing functions. Each software radio is implemented as a VME rack system populated with COTS equipment to provide functions associated with RF down- and up-conversion, analog-to-digital conversion, digital-to-analog conversion, IF processing, baseband processing, and bitstream processing. A high data rate bus, called RACEWAY, is shared between processing boards to facilitate data transfers at rates up to 160 Mb/s. Each software radio is to be connected via an FPDP I/O link to a dedicated PC for the MAC and/or application layers associated with the modem. A photo of a software radio platform is shown in Figure 2.3.



*Note: Design based partly on architecture proposed by Joe Mitola

Figure 2.2. Software Radio Platform Configuration

Receive Chain

The receive RF front-end in each software radio platform includes a synthesizer board and two downconversion channels. These RF boards, obtained from APCOM Inc., include capability to synchronously downconvert input RF frequencies up to 3 GHz. The synthesizer board generates a programmable LO signal that is shared by the down-conversion boards for synchronous operation. The down-conversion boards each

represent a separate physical receive channel with down-conversion circuitry, including image rejection filters, low noise amplifiers (LNAs), filters, amplifiers, and mixers. RF signals may be input to the receiver boards via cable connections from the outputs of the RF channel emulators or other sources. The input signals are filtered in the receiver to a spectral footprint of 28 MHz (40 MHz upgrade is pending), and are then down-converted to a low IF frequency for analog to digital conversion. The selection of the IF is driven by the A/D sampling rate associated with the A/D converters in the digital receiver boards that follow the RF down-conversion boards. C-based programs were developed to control the boards from the software radio (SR) host computers.

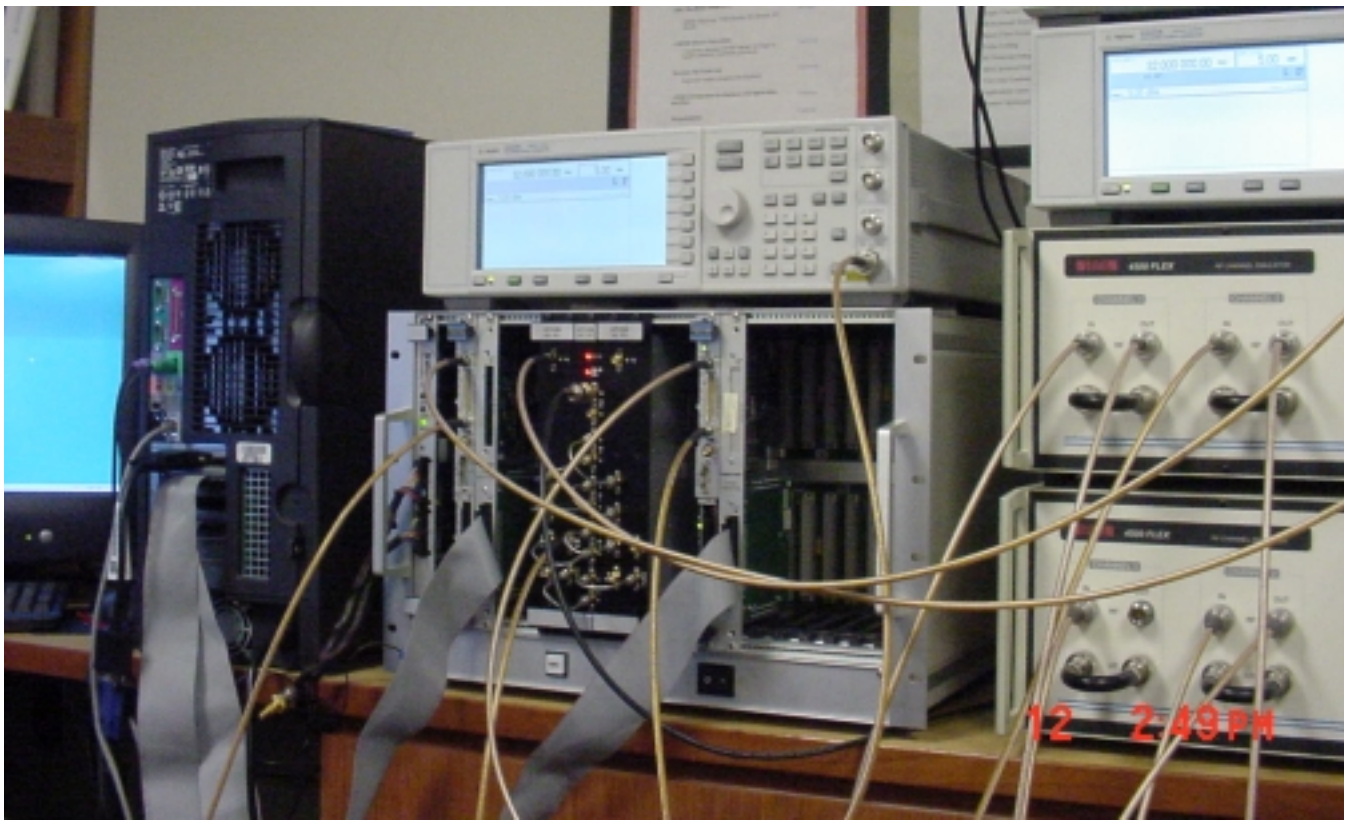


Figure 2.3. Photo of the Software Radio Platform with a VME/PCI controller, a two-channel Wideband Receiver Module and a dual FPDP module mounted on a Quad TI C6701 DSP board, two phase-coherent RF downconversion channels with a shared synthesizer board, and a DAC/DUC board and dual FPDP board mounted on a Quad TI C6701 DSP board. The signal generator is used for IF to RF conversion.

The resulting IF signals are applied to the inputs of the digital receiver boards, where the signals are prefiltered with anti-aliasing filters and are sampled with A/D converters at a rates up to 105 Msamples/s. Signal bandwidths in excess of the desired 40 MHz signal bandwidth can be sampled without aliasing. Following the sampling operation, the signals are converted to complex baseband with digital receiver chips. The wideband down-converters support output bandwidths up to 40 MHz. The digital receiver chips have numerically controlled oscillators (NCOs), filters, and decimators for the down-

conversion process. Synchronous demodulation across as many as eight channels is possible. If intermediate frequency (IF) processing is desired, such as for despreading or digital downconversion, the digital down-converters can be bypassed and the sampled signals output directly to an FPGA (on –board) or to a Pentek quad processing board.

Following down-conversion to baseband, the sampled signals are buffered to a quad DSP boards for baseband and bitstream processing, which could include baseband demodulation, decoding, and other processing functions. A RACEWAY interconnect is available to support high data-rate transfers between quad processor boards. The anticipated configuration will include four quad DSP boards and two quad Power PC boards all connected to a RACEWAY crossbar switch. An FPGA board will be acquired to support FPGA-based baseband processing. Following signal processing, the demodulated data is passed through an FPDP I/O link to a dedicated host platform for higher layer functions, or alternatively to a large (i.e., 2 Gbyte) memory buffer via FPDP for signal storage and post collection processing.

Transmit Chain

The transmit chain is projected to include data framing, data transfer from the application PC to the software radio platform, interleaving, FEC coding, space-time coding, symbol formation, OFDM modulation, guard insertion, digital to analog conversion, and IF-to-RF frequency conversion. Data from the application PC is streamed to a quad processing board in the software radio via an FPDP I/O link. Baseband modulation processing can be accomplished with the processing board and optionally with support from an FPGA board. The resulting baseband real and complex samples are buffered to a DAC/DUC, which performs digital to analog conversion, I/Q modulation, and upconversion to IF. The resulting analog IF signal is input to an IF to RF converter. A signal generator or dedicated VME-based transmit boards will be utilized for this function for the frequency conversion and transmit functions. The RF transmit front end is to provide 2-channel operation.

The specific operating characteristics of the prototype radios for the proposed experimental license are indicated in Exhibit 3. Note that the experimental set-up includes single and multiple antenna configurations with straight 3 dBi antenna elements and a multiple antenna configuration with higher-gain beams derived from the Georgia Tech beamswitch antenna array.